Pipelining Examples and Back-Pressure

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Outline

- Throughput Handling
- Why do we need rate control
- Types of control
  - Global stall signal
  - Registered stage-by-stage stall

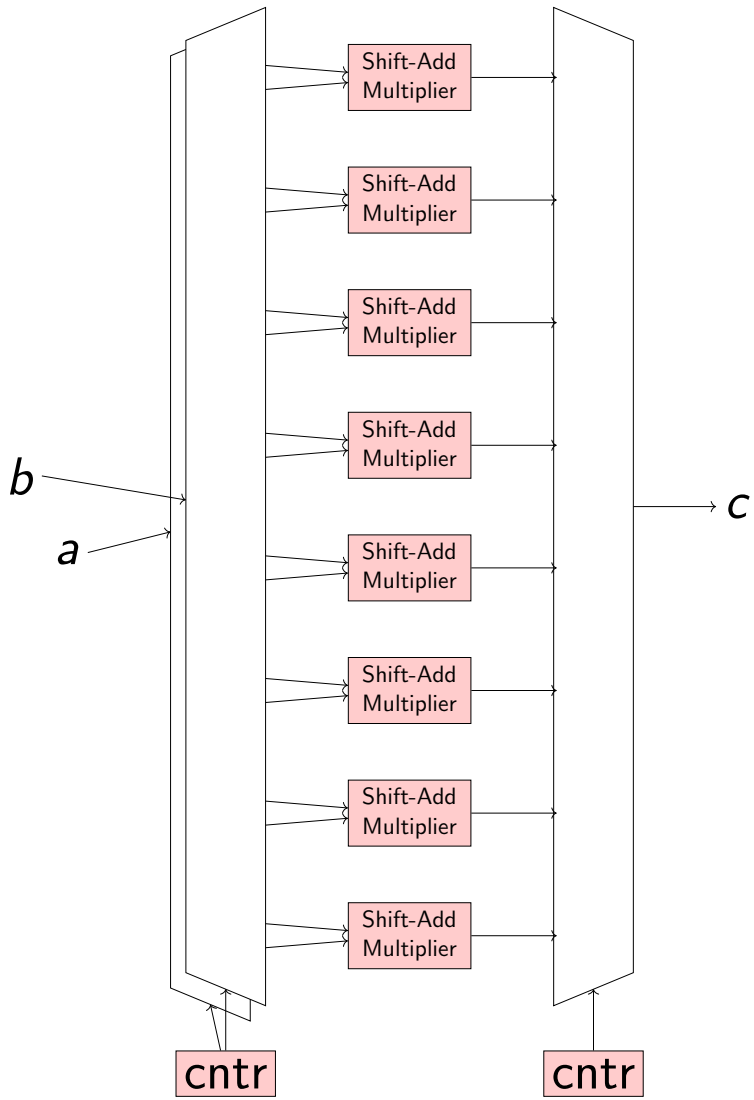
Pipelining with low-throughput components

- Not always possible to *fully pipeline* the datapath for high throughput
  - Some components naturally take multiple cycles to complete $\rightarrow$ shift-add multiplier
  - Sometimes you run out of resources
- For these components, computation is sequential $\rightarrow$ Throughput T is inverse of Latency L.
  - Range of throughputs possible $\frac{1}{L} \leq T \leq 1$
  - Even lower throughputs possible if some internal state clearing logic is activated
- **Q** Can we check if our design is balanced? Are we over or under pipelining our hardware?
  - It is all about equalizing throughput!

Throughput Balancing through Replication

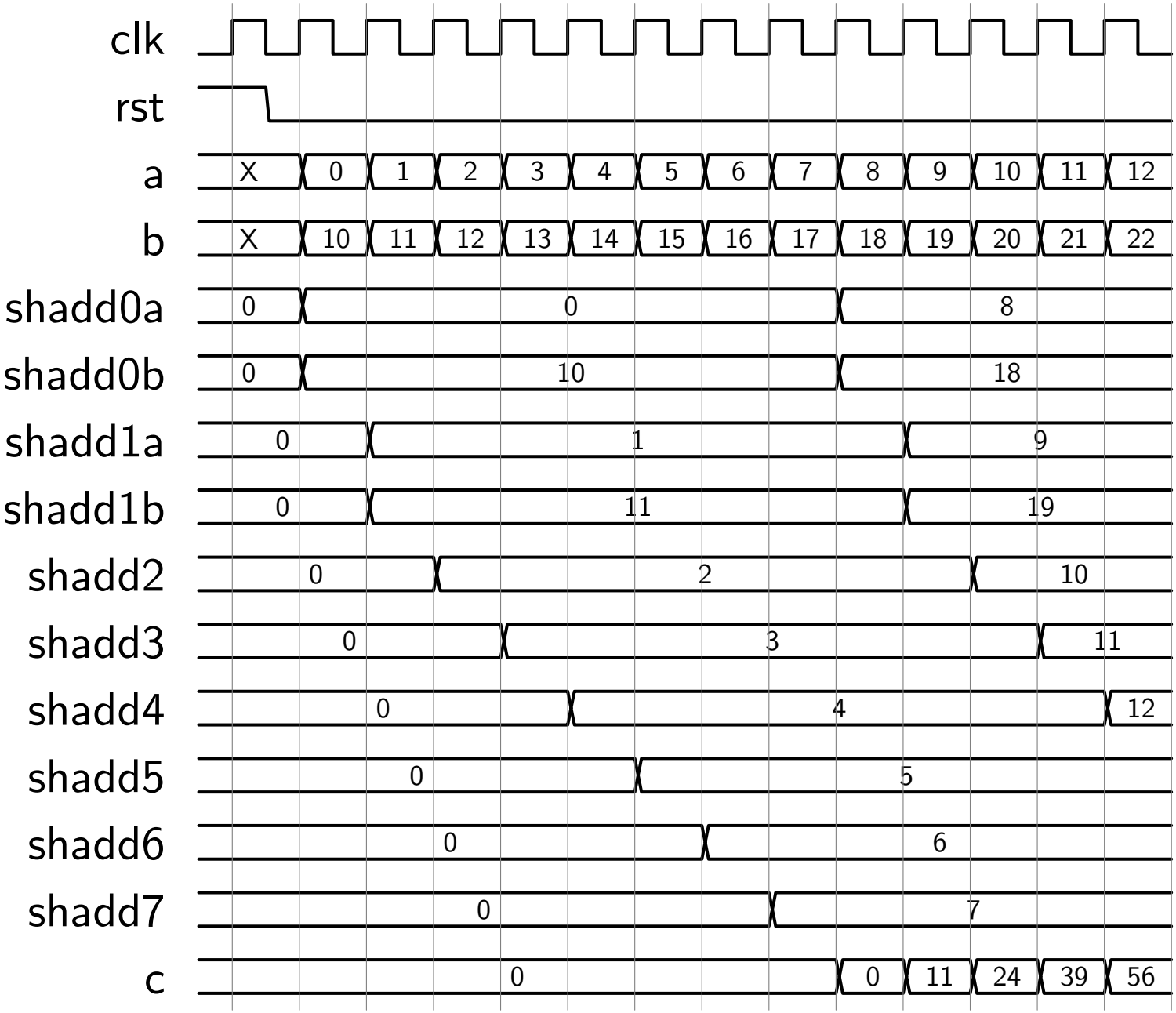
- Shift-add multiplier takes 8 cycles to perform an 8×8 multiplication → each cycle is a shift-and-add operation
- Throughput=$\frac{1}{8}$, Latency=8
- You are required to boost throughput of the design but do not have manpower to rewrite RTL for a new multiplier architecture

Throughput Balancing through Replication

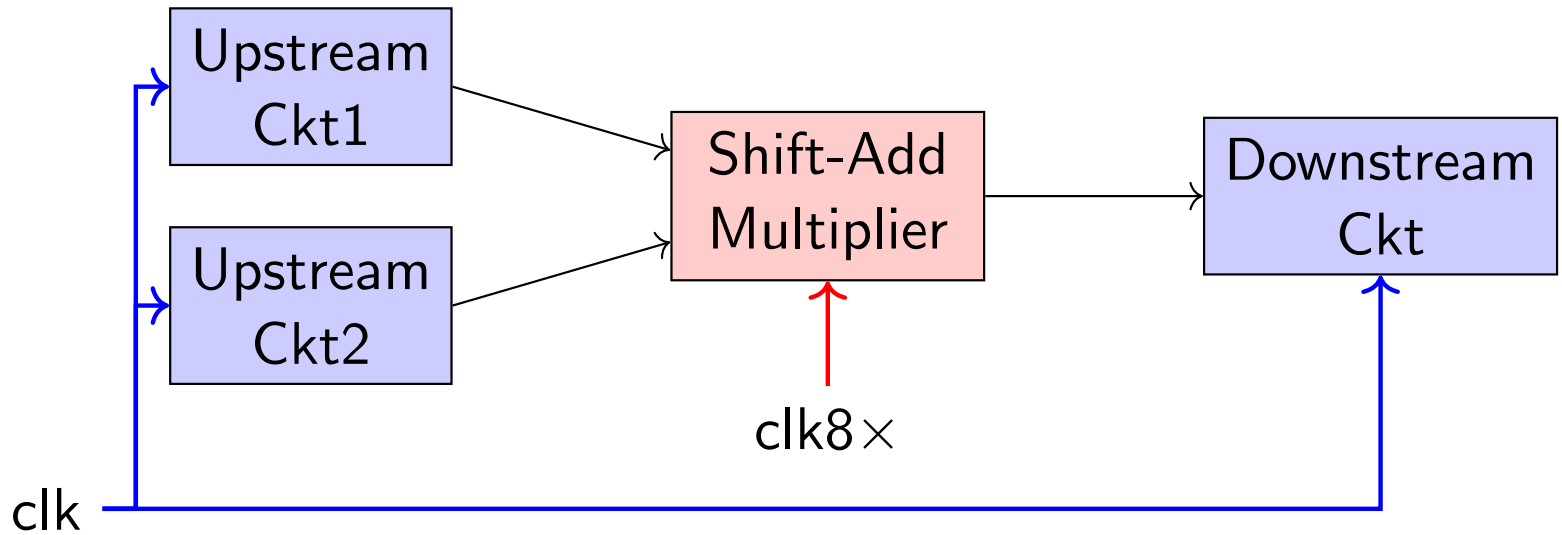


- Perform $a \times b = c$ on inputs arriving each cycle
- Replicate the shift-and-add multiplier $8\times$ to boost throughput.
- Add 1:8 demultiplexer at input to distribute inputs to the eight components
  - A demux is often just a wire with valid signals
- An 8:1 multiplexer at the output collects results from each block
- A 3-bit counter drives the select lines of mux and demux structures

Replication Waveforms



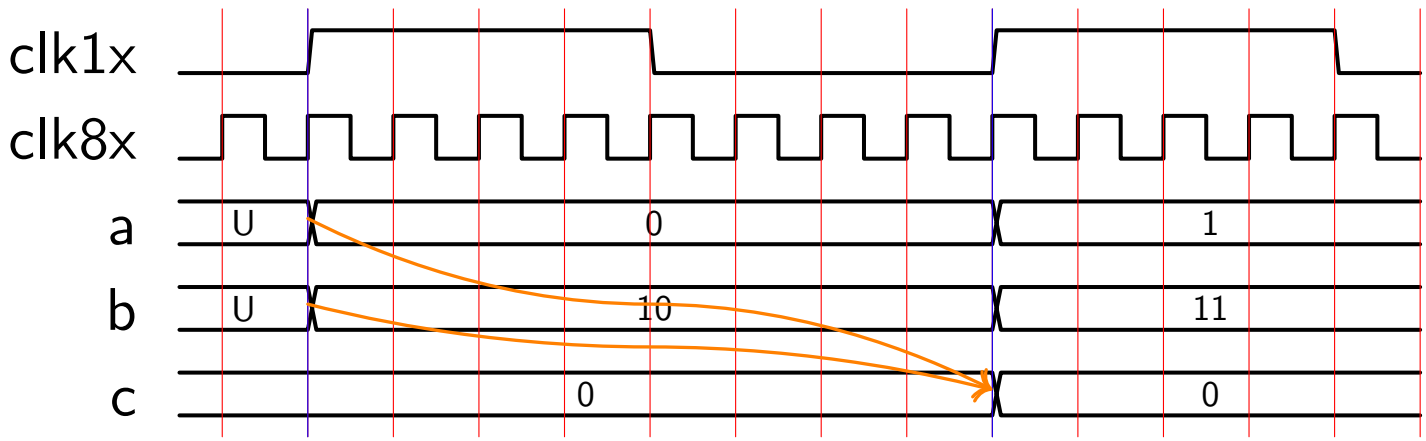
Throughput Balancing through Clock Domains



- Supply two different clocks (phase aligned, integer multiples)
- Shift-Add runs at fast 8× clock → one cycle for the upstream/downstream circuits is 8 cycles for a shift add!
- In general, crossing clock domains is like crossing countries → you need a passport, visas, ... Here, we need synchronizers or asynchronous FIFOs (out of scope of 627)


EIGHT CYCLES OF SHIFT-ADD (CLK8X)
ARE WORTH ONE CYLE OF IO (CLK1X)
imgflip.com

Clock Domain Crossing Waveforms



Controlling data transfers

- Valid signaling is useful for one-way communication of information
- Most hardware designs use standard handshake protocols requiring bidirectional dataflow
  - Valid bit from sender to receiver
  - Ready bit from receiver to sender
- Standard bus interfaces such as AXI (Advanced Extensible Interface) part of AMBA (ARM Advanced Microcontroller Bus Architecture) support valid + ready handshake