ARM926EJ-S

- 32-bit Harvard architecture (2001)

Capacitance (nF)				Power (mW)	
C_{ca}	C_{cs}	C_{ma}	C_{ms}	I	R
0.505	0.224	0.540	0.210	6.570	67.434

CPU clock	20 - 200 MHz (2 MHz step)
Bus clock	20 - 100 MHz (f_c/n)
Voltage	1.504 - 1.824 V (0.32 V step)
L1 cache	8 KiB I, 8 KiB D

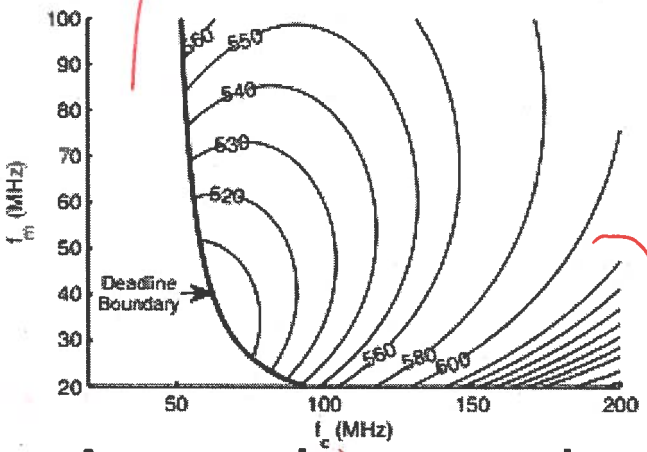
and memory

91 steps

11 steps

0.032 V step

E vs f_c and f_m



energy

$K = 1.4 \times 10^8$, $M = 3.0 \times 10^7$, $T = 3$ s

* for a set of tasks, T = LCM of periods

- Assuming continuous – use continuous optimization
- Assuming discrete – perform exhaustive search

Yun, et al System-wide Energy Optimization for Multiple DVS Components and Real-time Tasks, 2010