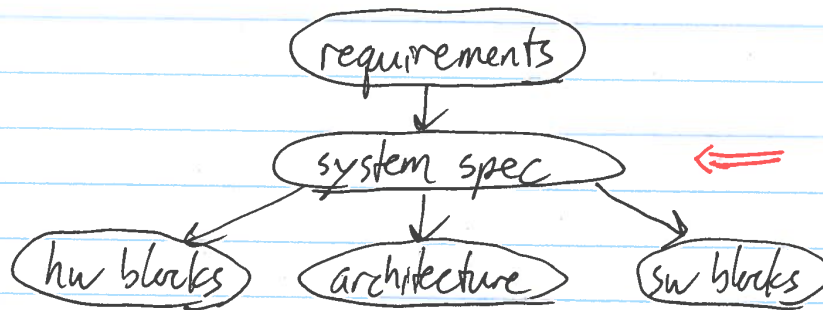


Models of Computation

①

- recall:



- the high-level system specification:
 - needs to express parallelism
 - is used for:
 - ① ~~simulatable~~ simulation (if its executable)
 - ② formal verification: proving properties mathematically
 - ③ partitioning & scheduling - map blocks to processing elements
determining temporal schedule
 - ④ code generation - automatically generate hw & sw (e.g. HLS)

- what about C/C++?

Problem #1: hard to express parallelism correctly

- threading model is fundamentally non-deterministic
- any interleaving of operations is possible by default
- race conditions occur by default and programmer must restrict parallelism to ensure correctness (mutex, semaphores, cond. vars., ...)
- however \uparrow synchronization $\Rightarrow \downarrow$ parallelism $\Rightarrow \downarrow$ performance
- bugs are hard to find (e.g. Mars Pathfinder priority inversion)
- it would be safer to have a deterministic model where the programmer specifies which parallelism to allow: trades safety for performance

(2)

Problem #2: there is no explicit concept of time

- must use (system) libraries for timing
- compiler can't check timing correctness
e.g. pthread library does have timed waits but it's not part of the language standard

High-Level Specification Language Requirements:

① Hierarchical

- we're not good at managing or reasoning systems of >5 objects
- types of hierarchy: behavioural (states, processes)
structural (processor, PCB, node)

② Compositional Behaviour

- we can derive system properties/behaviours from those of the sub-systems

③ Have Intrinsic Representation of Time

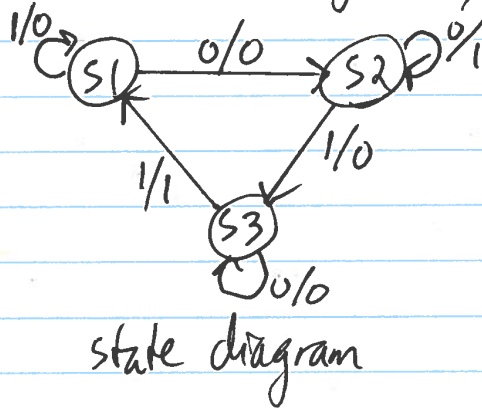
- support delays, timeouts, deadlines

④ Efficient Implementation

Model Classification:

- control-oriented: e.g. state machines (good for reactive systems)
- data-oriented: e.g. dataflow (good for signal processing)

State Machines e.g. Mealy machines



input	curr state	next state	output
0	S1	S2	0
1	S1	S1	0
0	S2	S2	1
1	S2	S3	0
0	S3	S3	0
1	S3	S1	1

state transition table

- can produce the output stream given initial state and input stream

e.g.

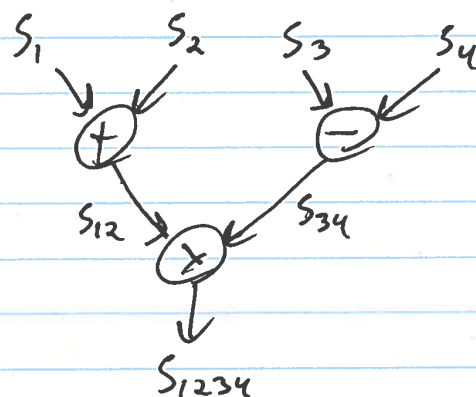
state	S1	S1	S2	S2	S3	S1
input	0	0	0	1	1	...
output	0	0	1	0	1	

- problems: no parallelism, state explosion
- solution: hierarchical composition of state machines (e.g. Statecharts)

(4)

Simple Dataflow Graph

- nodes: data operations
- edges: data dependencies
- a stream is associated with each edge (FIFO)
- timing is based on the arrival of input tokens
- Node Firing Rule: execution consumes one ~~symbol~~ token on each incoming edge and produces one ~~token~~ token on each outgoing edge



S_1	2	4	-2	...
S_2	1	-3	4	...
S_3	0	5	8	...
S_4	3	9	2	...
S_{12}	3	1	2	...
S_{34}	-3	-4	6	...
S_{1234}	-9	-4	12	...

Limitations

- no conditional execution
- no loops

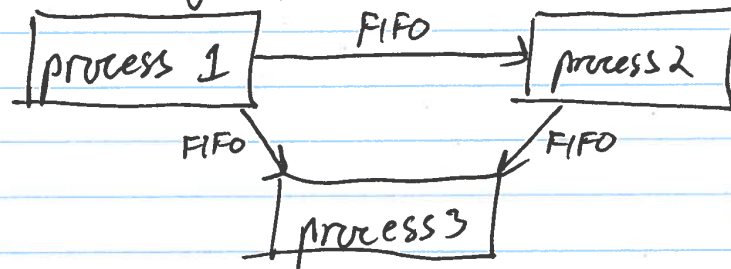
Solution

- more expressive dataflow model (e.g. Kahn Process Networks)

5

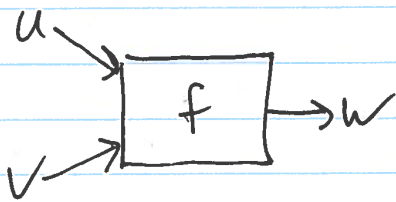
Kahn Process Networks (KPN)

- dataflow language



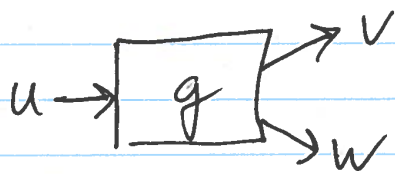
- a KPN is a set of processes that communicate over unidirectional communication channels
- channels: 1 reader, 1 writer, infinite FIFO of tokens
- tokens can be any data structure e.g. image
- processes execute concurrently
- each process can be described by imperative code (e.g. C)
- the language is augmented with a blocking wait() and a non-blocking send

- example:

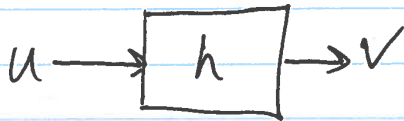


```
process f(in int u, in int v, out int w) {  
    bool b = true;  
    for(;;) {  
        int i = b ? wait(u) : wait(v);  
        printf("%d ", i);  
        send(i, w);  
        b = !b;  
    }  
}
```

6



```
process g(in int u, out int v, out int w) {  
    bool b = true;  
    for(;;) {  
        int i = wait(u);  
        if(b) send(i, v);  
        else send(i, w);  
        b != b;  
    }  
}
```



initialization process:
sends initial value, then
passes through values

```
process h(in int u, out int v, int init) {  
    int i = init;  
    send(i, v);  
    for(;;) {  
        i = wait(u);  
        send(i, v);  
    }  
}
```


8

- questions of termination and boundedness are undecidable

all processes are blocked on wait()

finite length queues

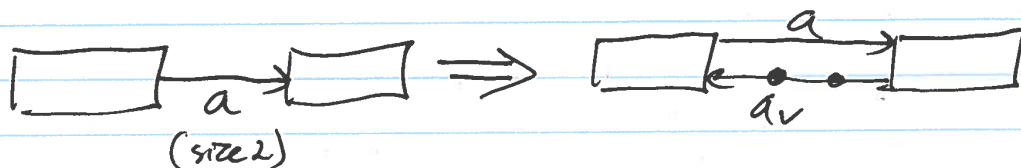
- if a KPN has a bounded implementation, then it can be transformed into a strictly bounded network without losing its determinism

Tom Park's Algorithm

- simulation based
- schedules a KPN in bounded memory if possible
- starts with all buffers with size=1 and blocking sends
- use any working-conserving scheduling technique (run something if at least 1 process can run)
- if the system deadlocks due to blocking sends, increase the size of the smallest buffer and continue
- there is no stopping condition: ~~etc~~ just run for a "long" time and if buffers keep growing then probably a bounded implementation isn't possible

How to simulate finite buffers with a KPN simulation:

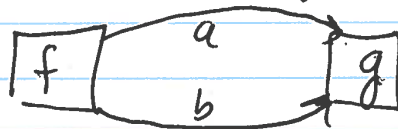
- every channel, a , add a virtual channel, a_v , in the opposite direction
- each virtual channel is initialized with n tokens where n is the buffer size



(9)

- $\text{send}(a) \Rightarrow \text{wait}(a_v); \text{send}(a_v);$
- $\text{wait}(a) \Rightarrow \text{wait}(a); \text{send}(a_v);$

- example of simulating a bounded buffer in a KPN simulation (which doesn't have blocking sends)



$\text{size}(a) = 1$

$\text{size}(b) = 1$

```

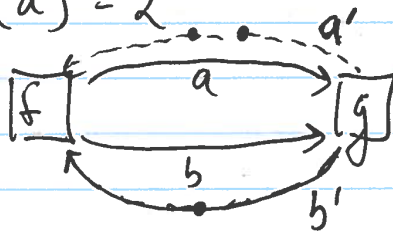
process f(out int a, out int b) {
  for(j;j) {
    send(1, a);
    send(1, a);
    send(1, b)
  }
}
  
```

```

process g(in int a, in int b) {
  for(j;j) {
    wait(b);
    wait(a);
    wait(a);
  }
}
  
```

- this will deadlock on a blocking send

- set $\text{size}(a) = 2$



```

process f(out int a, out int a', in int b) {
  for(j;j) {
    wait(a'); send(1, a);
    wait(a'); send(1, a);
    wait(b'); send(1, b);
  }
}

process g(in int a, out int a', in int b) {
  send(1, a'); send(1, a'); send(1, b');
  for(j;j) {
    wait(b); send(1, b');
    wait(a); send(1, a');
    wait(a); send(1, a');
  }
}
  
```

- won't deadlock with $\text{size}(a) = 2$

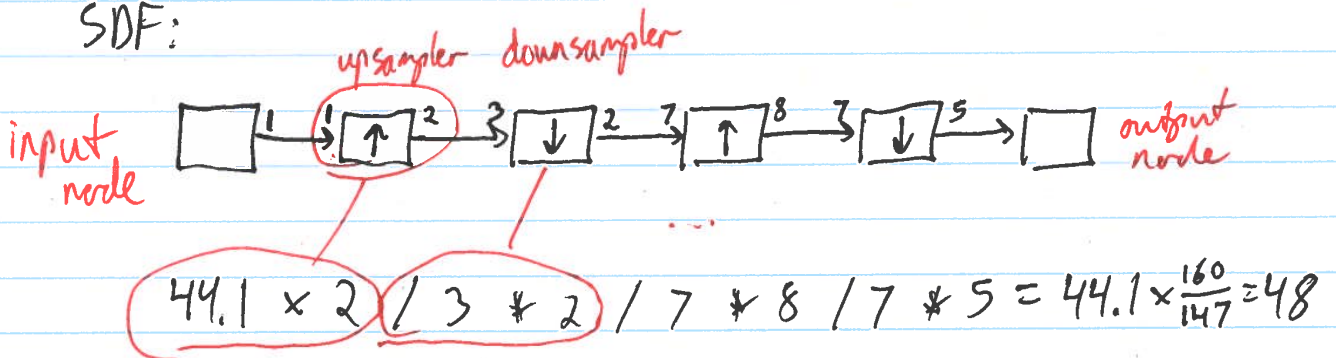
Synchronous Dataflow (SDF)

- Lee & Messerschmitt 1987
- KPN is very flexible but a schedule can't be produced deterministically
- SDF adds restrictions to KPN to enable deterministic compile-time scheduling
- each node (process) has fixed production/consumption of tokens every time it fires
- node firing is atomic: it reads all input buffers at the same time
 - doesn't fire until the required # of tokens is available on each input
- the model ignores node execution time
- the system is described solely by the # of tokens read and written when each node fires

e.g. DAT-to-CD ~~audio~~ converter

DAT = digital audio tape samples at 44.1 kHz
 CD = compact disc samples at 48 kHz

SDF:

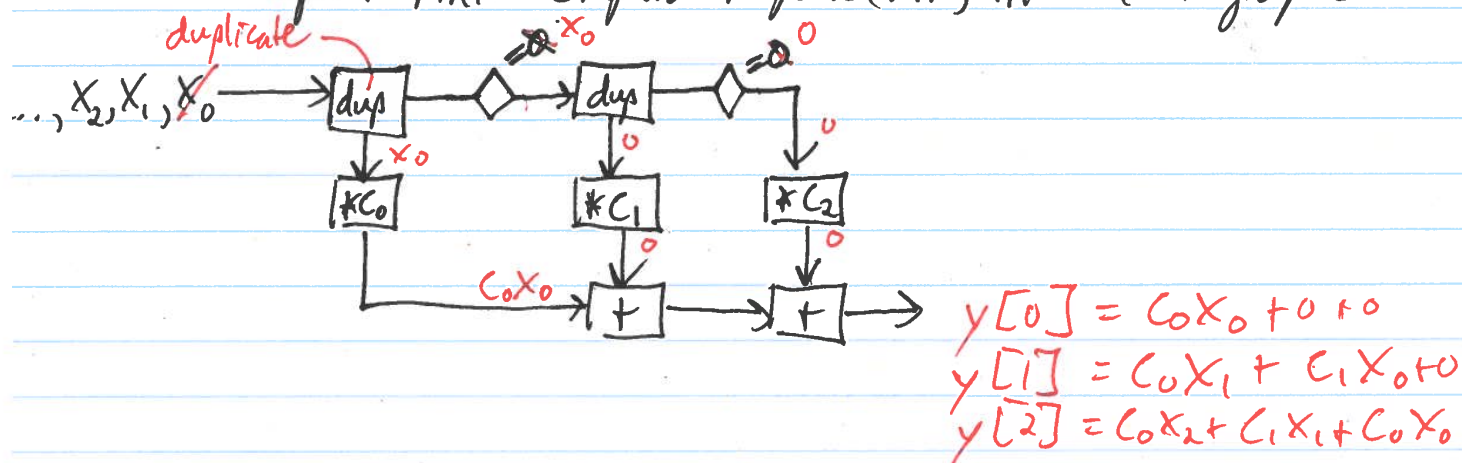


- can determine the relative firing rates of each node which leads to a periodic schedule

11

- unlike KPN, SDF doesn't permit initialization phases in nodes since input and output rates are fixed
- instead the SDF can start with initial tokens in buffers
 - these may be needed to avoid deadlock

- example: Finite Impulse Response (FIR) filter (SDF graph)



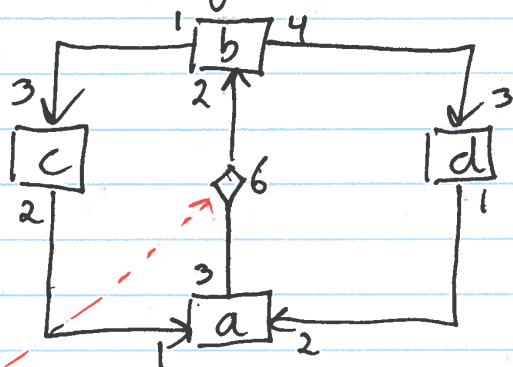
SDF scheduling algorithm

- ① establish node firing rates (per iteration of the periodic schedule) using balancing equations
- ② determine periodic schedule by simulating for 1 iteration (done when # tokens in each channel/buffer returns to its initial count)

- the resulting schedule will have bounded buffer size i.e. tokens will not accumulate

(12)

① balancing equations



this channel/buffer has 6 initial tokens

- channel balancing equations

#output tokens firing rates

$$3a - 2b = 0 \quad (\text{no token accumulation})$$

#input tokens

$$4b - 3d = 0$$

$$b - 3c = 0$$

$$2c - a = 0$$

$$d - 2a = 0$$

$$\begin{matrix} & a & b & c & d \\ \begin{bmatrix} 3 & -2 & 0 & 0 \\ 0 & 4 & 0 & -3 \\ 0 & 1 & -3 & 0 \\ -1 & 0 & 2 & 0 \\ -2 & 0 & 0 & 1 \end{bmatrix} & \begin{bmatrix} a \\ b \\ c \\ d \end{bmatrix} & = & 0 \end{matrix}$$

$$\begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix}$$

M q
topology matrix node firing rates (per schedule iteration)

SDF Scheduling Theorem

- an SDF with n nodes has a periodic schedule iff $\text{rank}(M) = n-1$
- if $\text{rank}(M) = n-1 \exists$ a smallest positive integer solution to $Mq = 0$

(13)

- determine q without finding rank(M):

i) take one node and run once e.g. $a=1$

ii) iteratively determine rates of connected nodes

e.g. $3(1) - 2b = 0; \quad b = \frac{3}{2}$
 $-1(1) + 2c = 0; \quad c = \frac{1}{2}$
 $-2(1) + d = 0; \quad d = 2$

$$x = \begin{bmatrix} 1 \\ \frac{3}{2} \\ \frac{1}{2} \\ 2 \end{bmatrix}$$

iii) verify $M \cdot x = 0$ (it won't for an SDF that can't be scheduled periodically)

iv) compute LCM of denominators e.g. 2
 (Least Common Multiple: $LCM(a,b) = \frac{a \cdot b}{GCD(a,b)}$)

$$LCM(a,b,c) = LCM(a, LCM(b,c))$$

or multiply prime factors of highest power)

v) $q = LCM \cdot x$

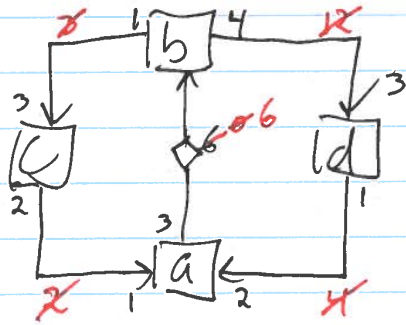
e.g. $\begin{bmatrix} 2 \\ 3 \\ 1 \\ 4 \end{bmatrix} \begin{matrix} a \\ b \\ c \\ d \end{matrix}$

14

② determine periodic schedule

- done by simulation
- any schedule that doesn't cause buffer underflow works
- there may be multiple solutions

P.S.



$$a = 2^0$$

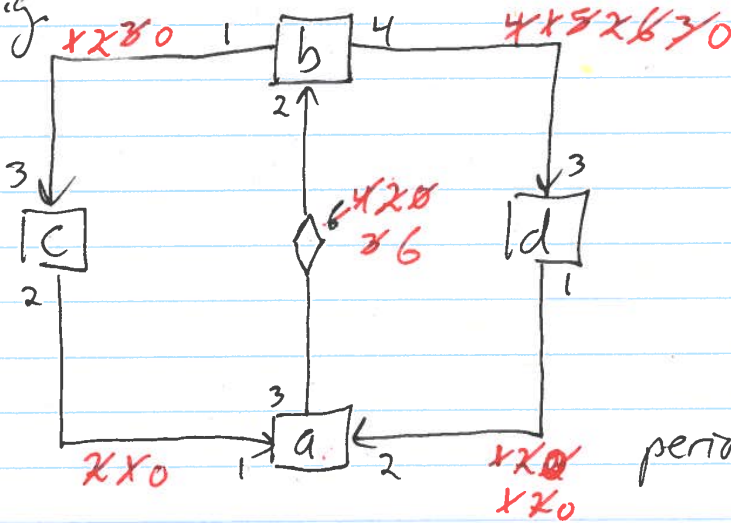
$$b = 3^0$$

$$C = X^0$$

$$d = 4^0$$

\checkmark schedule = bbb c dddd aa
periodic

e.g.



$$a = 2 \neq 0$$

$$b = 3^2 \times 10$$

$C \neq 0$

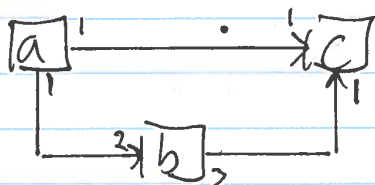
$$d = 43210$$

periodic schedule = b d b d b c a d d a

- this schedule requires smaller buffers

- special SDF cases

1) Inconsistent System, $\text{rank}(M) = n$



$$a - c = 0$$

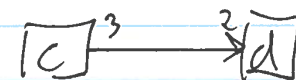
$$a - 2b = 0$$

$$3b - c = 0$$

$$\left. \begin{matrix} a - c = 0 \\ a - 2b = 0 \\ 3b - c = 0 \end{matrix} \right\} \text{subst} \Rightarrow a - 2c = 0 \quad \leftarrow \text{---} \neq$$

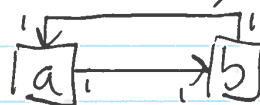
- the only solution is $q = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix}$ (never fire the nodes)

2) Underconstrained, $\text{rank}(M) < n-1$



- unconnected graphs; the firing rates of a/b and c/d are unrelated

3) Consistent System, No Schedule



$$q = \begin{bmatrix} 1 \\ 1 \end{bmatrix} \quad \text{- no initial inputs; can't run}$$

- solution: need to add initial tokens

- can often know the initial tokens needed based on the application

- otherwise, can do a modified Park's algorithm

- run simulation

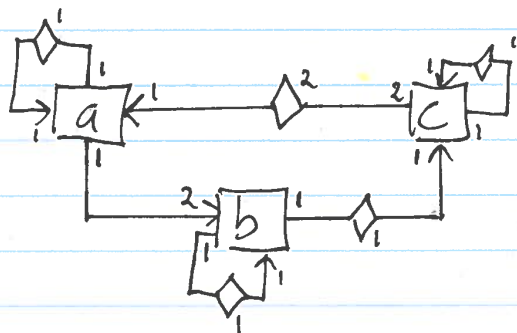
- if all nodes block on missing tokens, add tokens and continue

Multiprocessor SDF Scheduling

- need to know node execution times on each PE (processing element)
- compute q
- pick $j \geq 1$ (# of periodic repetitions)
- create a DAG (directed acyclic graph of precedence relations between instances of node executions for $p = jq$
- if a node should not fire in parallel on different PEs (e.g. due to internal state), add a self-loop ρ

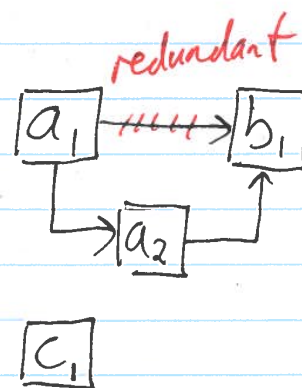


- example:

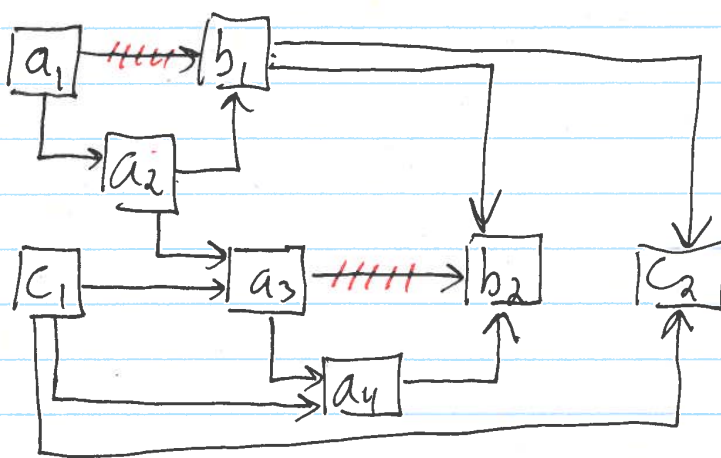


$$q = \begin{bmatrix} 2 \\ 1 \\ 1 \end{bmatrix}$$

$$j=1$$

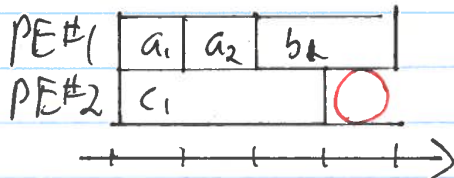


$$j=2, \rho = \begin{bmatrix} 4 \\ 2 \\ 2 \end{bmatrix}$$

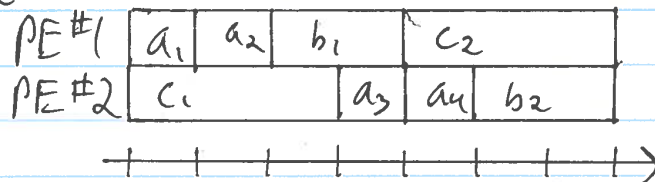


(17)

- scheduled on 2 homogeneous PEs
 $t_a=1$, $t_b=2$, $t_c=3$

 $j=1$ 

$$\text{throughput} = \frac{1 \text{ period}}{4}$$

 $j=2$ 

$$\text{throughput} = \frac{2}{7}$$

- no idle time \Rightarrow
 optimal

- to determine j , can increment j and schedule until throughput doesn't improve

Task Graph Scheduling

- a task graph is DAG of tasks (nodes) and precedence relations
- task latencies are known
- objective: schedule tasks on PEs to minimize makespan (time to execute the graph)

List Scheduling

- it is a metaheuristic (doesn't specify how priorities are assigned)
 - 1) assign task priorities
 - 2) create list of active tasks (those not blocked by precedence constraints, in priority order)
 - 3) schedule first task from list on the PE where it can run earliest (obeying precedence constraints)
 - 4) remove this task from list and add any tasks it enables
 - 5) goto 3) until the list is empty

Priority Assignment

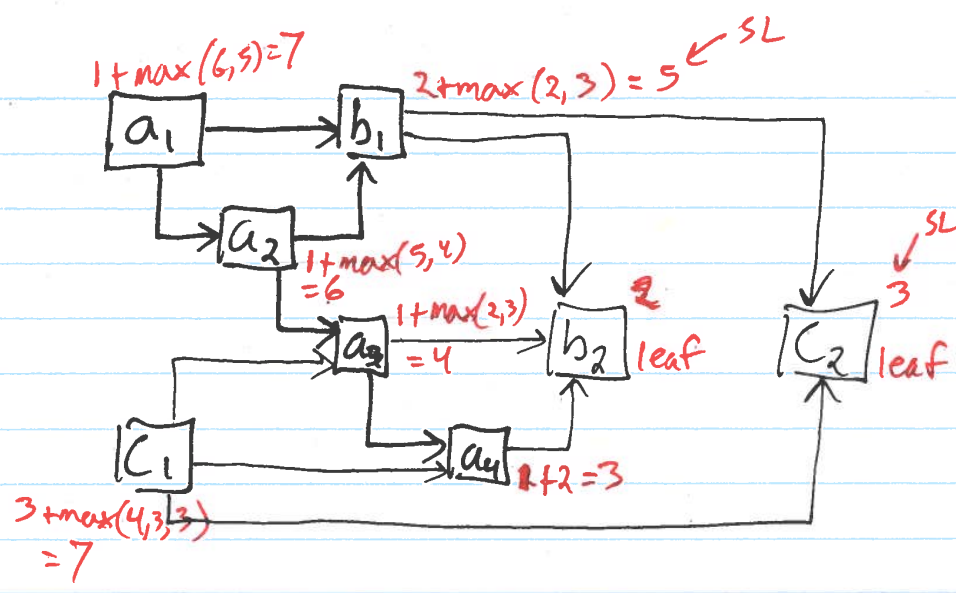
- use static level (SL) - the longest path to any leaf node

$$SL(x) = \max \left(\forall e \in \text{leaves} \quad \forall p \in \text{paths}(x \dots e) \sum_{p_i=x}^e \text{latency}(p_i) \right)$$

- to determine SL:

- 1) for each leaf node (no successors), $SL = \text{node latency}$
- 2) recursively set $SL(x) = \text{latency}(x) + \max_{p_i \in \text{succ}(x)} (SL(p_i))$

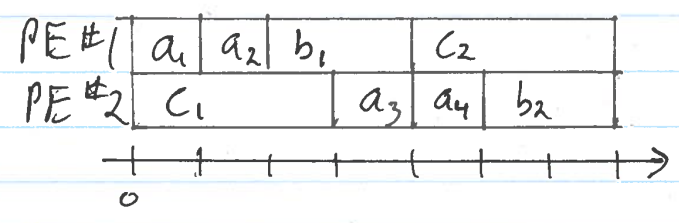
(19)



$t_a = 1$
 $t_b = 2$
 $t_c = 3$

list

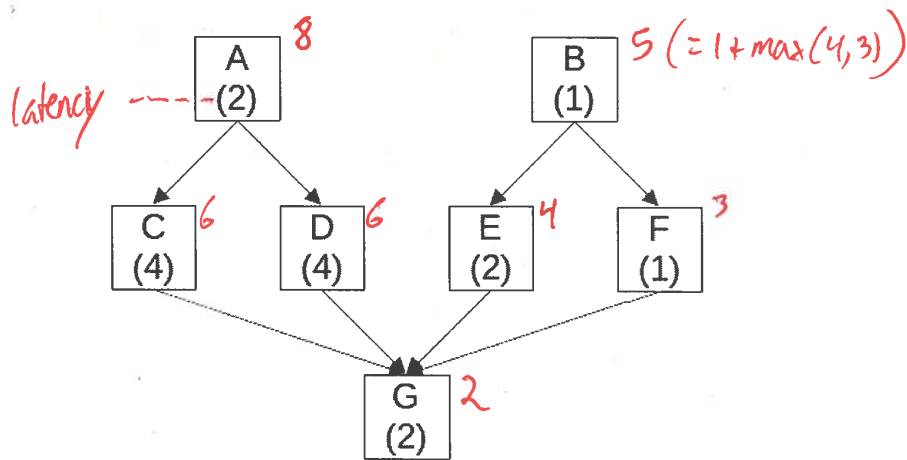
- {~~a1~~, c1}
- {~~a1~~, a2}
- {~~a2~~}
- {~~b1~~, a3}
- {~~a3~~, c2}
- {~~a4~~, c2}
- {~~a2~~, b2}
- {~~b2~~}
- { }



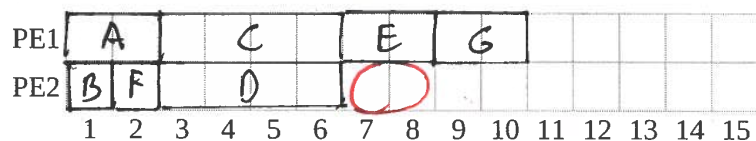
"forward list scheduling"
- schedule from $t=0$

Alternatives

- backward list scheduling: SL longest path to any root (no pred)
- schedule from end
- dynamic list scheduling: if a lower priority task on the list can start earlier, then schedule it first
 - might reduce idle time
 - might penalize tasks on the critical path



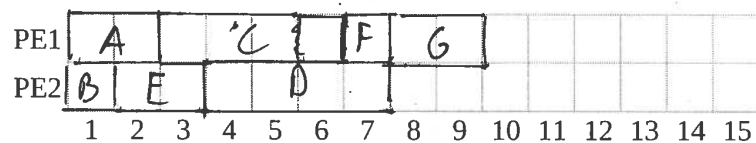
forward list scheduling



— 2 units of idle time before G runs

list
~~{A, B}~~
~~{C, D, B}~~
~~{D, B}~~
~~{B}~~
~~{E, F}~~
~~{F}~~
~~{G}~~
~~{}~~

dynamic list scheduling



— no idle time before G runs
 (optimal)

list
~~{A, B}~~
~~{C, D, B}~~
~~{C, D, E, F}~~
~~{C, D, F}~~
~~{D, F}~~
~~{F}~~
~~{G}~~
~~{}~~

(21)

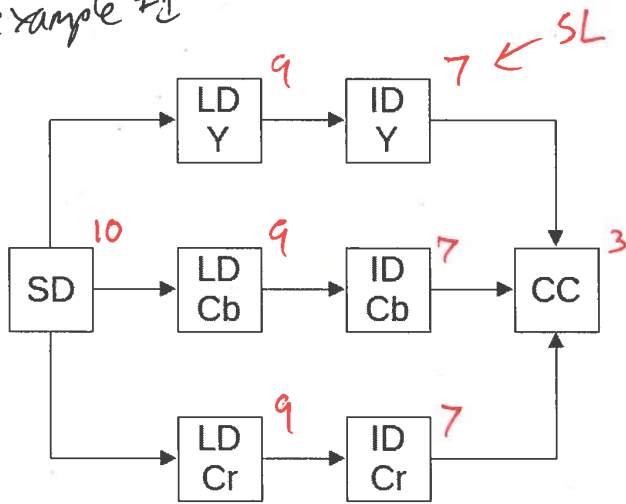
MJPEG423 decoder task graph

- assumptions: - 1 block per frame
- lossless decode time is same for Y' , Cb , Cr

- tasks: read SD card (SD)
- lossless decode (LD)
- idct (ID)
- colour conversion (CC)

- page 22 {
- handout: 1st example (2 homogeneous PEs)
 - handout: 2nd example (PE#2 - IDCT implemented in hardware)
(limit ID tasks to PE#2)

example #1

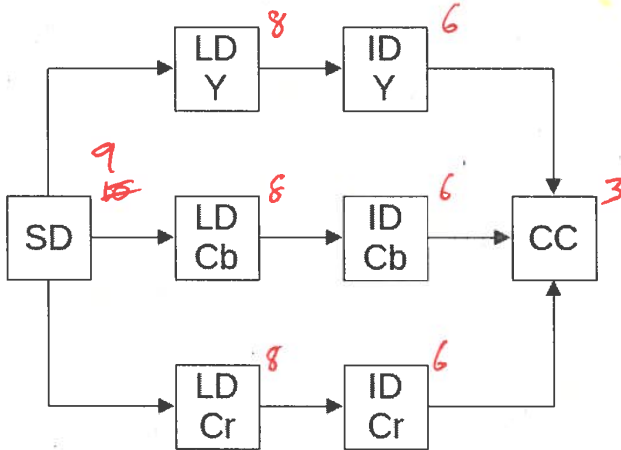


	PE #1	PE #2
SD	1	1
LD	2	2
ID	4	4
CC	3	3

PE1	SD	LD Y	LD Cr												
PE2		LD Cb	ID Y					ID Cb	ID Cr						
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

makespan = 14

example #2: PE #2: FPGA



	PE #1	PE #2
SD	1	∞
LD	2	∞
ID	∞	3
CC	3	∞

PE1	SD	LD Y	LD Cb	LD Cr											
PE2				ID Y				ID Cb	ID Cr						
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

makespan = 15

Periodic Task Graphs

- repeated execution of the task graph
- max period = makespan of a single iteration
- min period = $\lceil \text{workload} / \#PE \rceil$, where workload is the sum of task latencies

page 24 (2 periods)
 - example #3: max = 14, min $\lceil 22/2 \rceil = 11$
 (homogeneous PEs)

- ~~period~~ - period = 11, latency = 23
- extra buffers for $IDY \rightarrow CC$, $IDCb \rightarrow CC$ (, $IDCr \rightarrow CC$)

- example #4: max = 15, min $\lceil 19/2 \rceil = 10$ ← from pg 22

- period = 10, latency = 20
- extra buffers for $IDY \rightarrow CC$ (, $IDCb \rightarrow CC$)

- extra buffer factor

- regular load (repeating period): latency
 $\text{factor} \leq \lceil \text{makespan} / \text{period} \rceil$

eg. example 3: factor = $\lceil 23/11 \rceil = 3$
 example 4: factor = $\lceil 20/10 \rceil = 2$

- if ~~for~~ iterations vary: eg. frame
 for each iteration i :

factor _{i} = 1

s_i = start time, f_i = finish time

for each other iteration j :

factor _{i} += $(s_j \leq s_i < f_j) \text{ or } (s_j < f_i \leq f_j)$

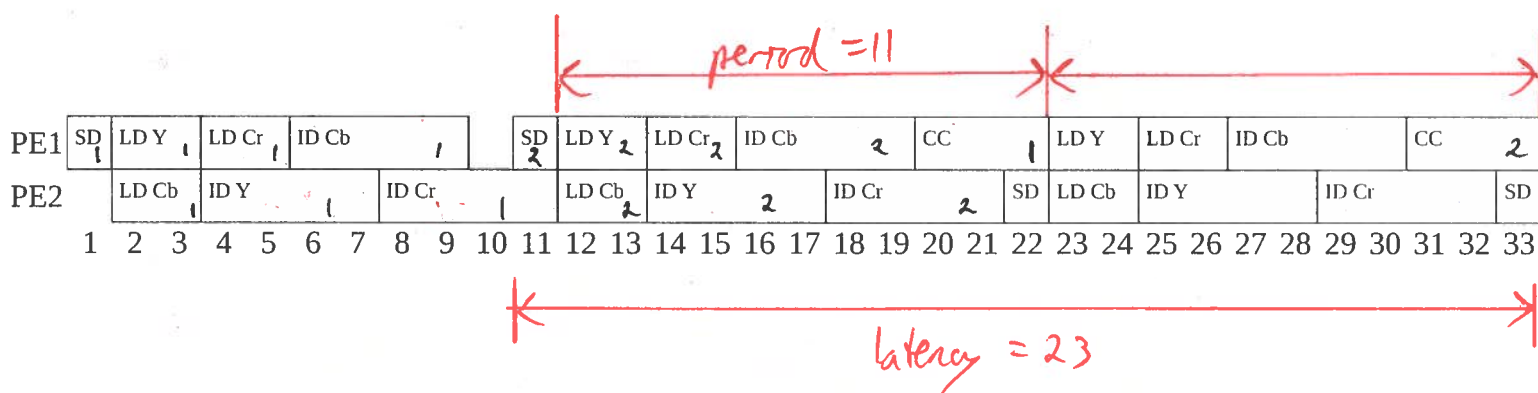
buffer factor = max(factor _{i})

example #3

	PE #1	PE #2
SD	1	1
LD	2	2
ID	4	4
CC	3	3

- assume sequential buffer fill

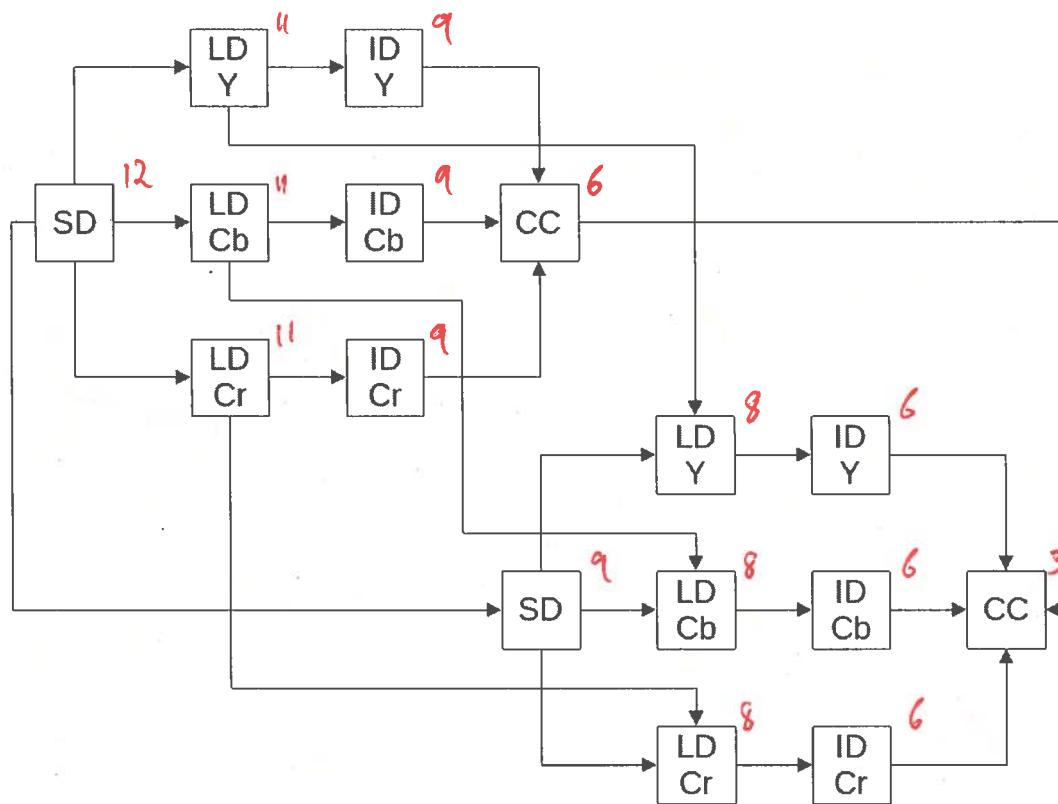
sequential SD card reads

p-frame: decode is based on Δ with previous frame

example #4

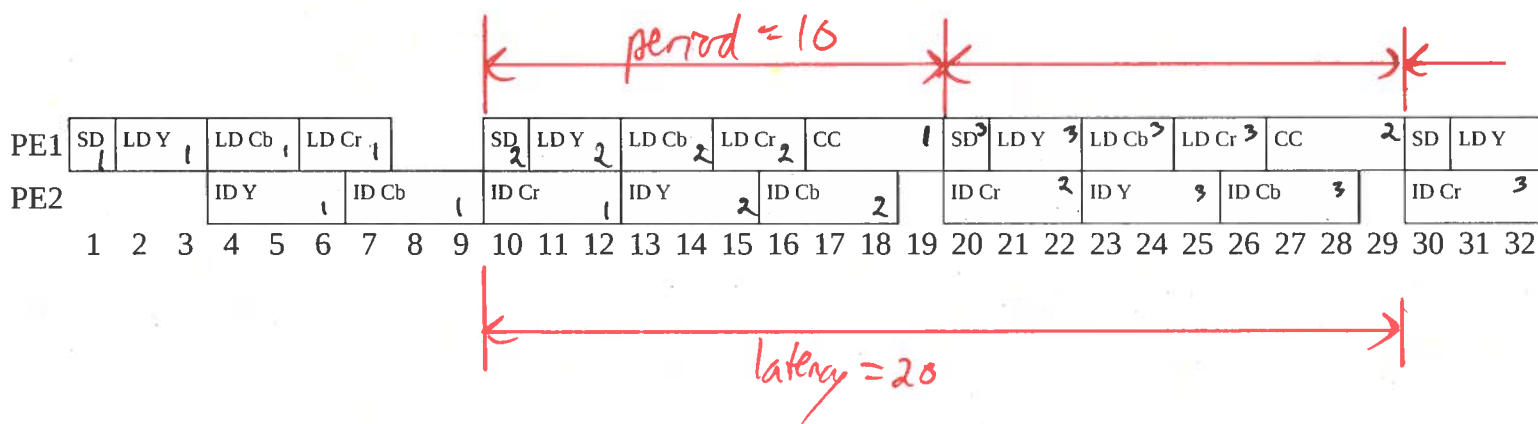
(25)

(24)



	PE #1	PE #2
SD	1	∞
LD	2	∞
ID	∞	3
CC	3	∞

↑
hw INCT



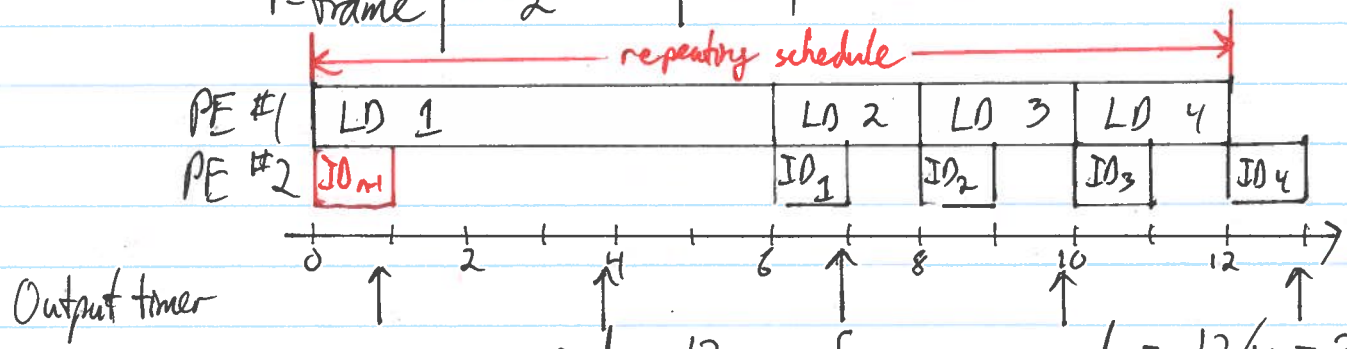
Periodic Output with Variable Load

e.g. I-frames and P-frames

sequence I P P P
 1 2 3 4

(only have LD and IDCT tasks)

	LD (PE#1)	ID (PE#2)
I-frame	6	1
P-frame	2	1



- sequence period = 12, frame period = $12/4 = 3$
- use a timer to perform output every 3 units (ISR vdma_out())
- worst-case: timer interrupt at $t = 7 - \epsilon$
 \Rightarrow output frame 1 at $t = 10 - \epsilon$

Frame	1	2	3	4
s_i	0	6	8	10
f_i	10	12	14	16
$delay_i$	3	2	2	2
f_i^*	12	15	18	21

$delay_i = \lceil f_i / period \rceil - i$ (# missed output IRAs)
 e.g. $delay_1 = \lceil 10/3 \rceil - 1 = 3$, $delay_2 = \lceil 12/3 \rceil - 2 = 2$

- when starting the sequence, skip $\max(delay_i)$ outputs
 e.g. count = 3 ISR: if (count > 0) count--; else vdma_out()

- $f_i^* = (\text{delay} + i) \times \text{output period}$
- use s_i, f_i^* to compute buffer factor

adjusted finish time

- ~~ff~~

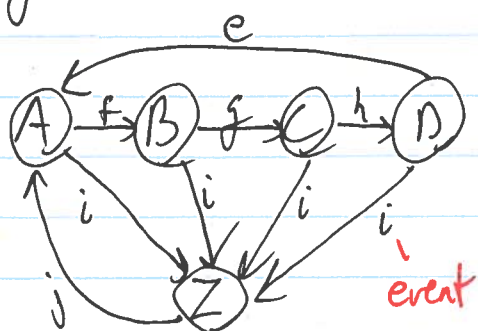
Executing a Task Graph

- 1) determine sequence on each PE
- 2) use a timer on each PE to start entry tasks
- 3) use synchronization primitives (e.g. semaphores) to block tasks until their predecessors have finished

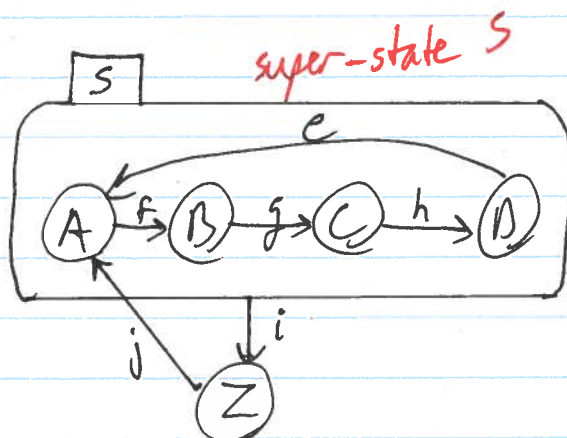
State Charts

- hierarchical state machine
- tools exist to convert them to SW & HW

e.g. FSM



⇒



- definitions:

active state = current state

basic state has no sub-states

super-states have sub-states

ancestor states = containing cases

OR-super-state = in exactly 1 sub-state when it's active
(models sequential execution)

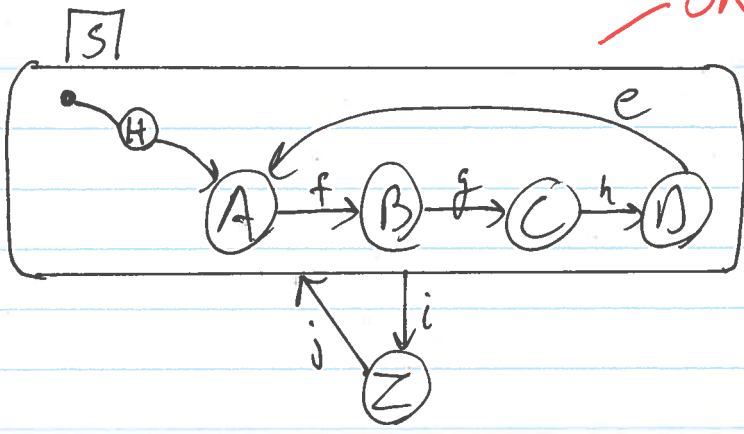
AND-super-state = in all sub-states when it's active
(models concurrent execution)

↑
OR-super-state

- default state:

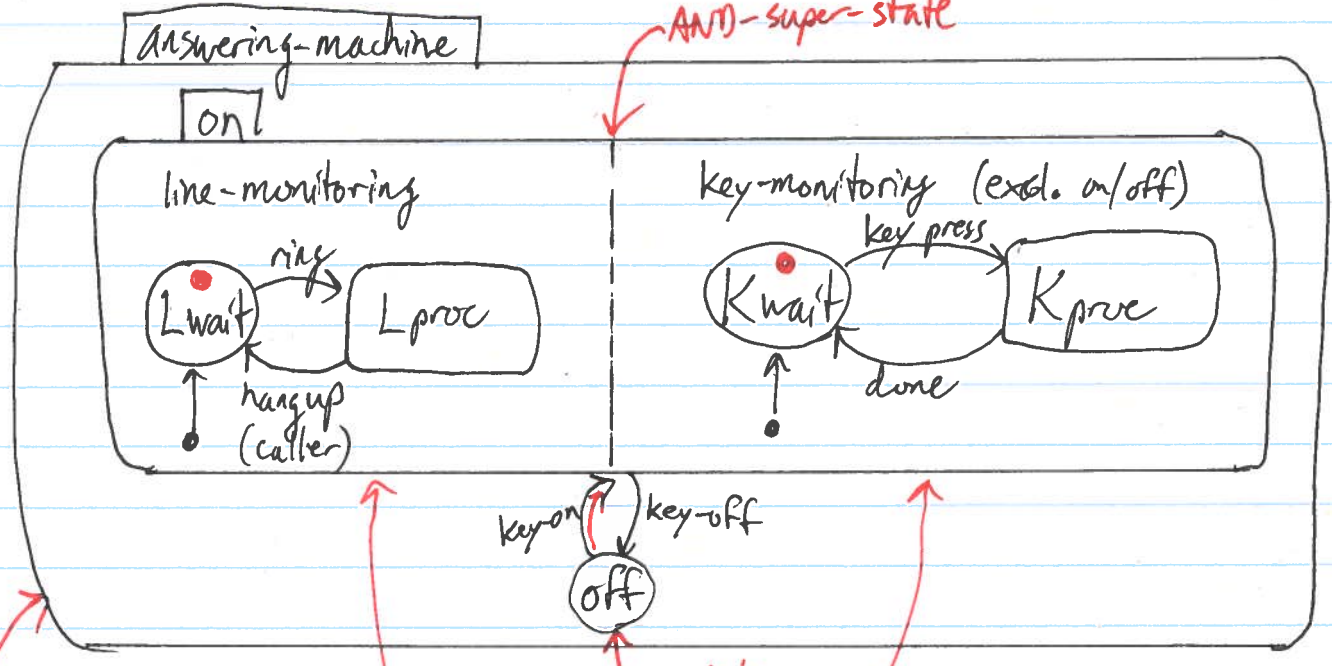
- history

OR-super-state



- enters (A) first time
- remembers last sub-state if next time S is active

AND-super-state

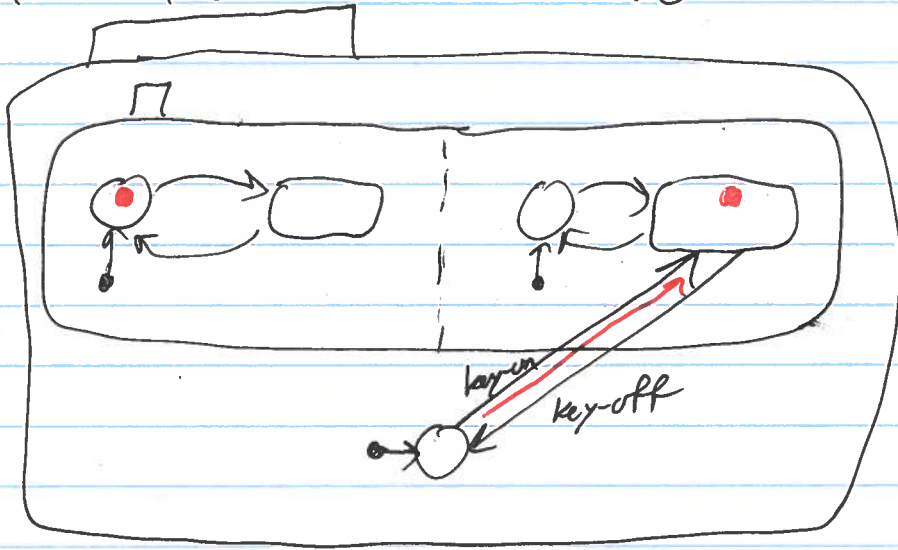


OR-super-state

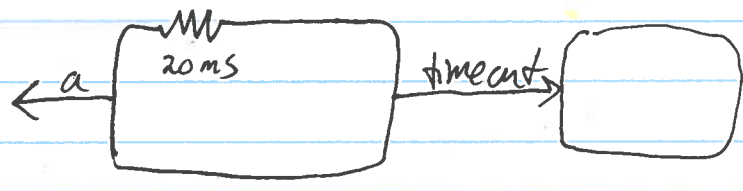
basic state
OR-super-states

active states: Lwait, line-monitoring, Kwait, key-monitoring, on, answering-machine

- entering AND-super-state means entering all sub-states
- leaving " " " " " "
- can transition into a sub-state of the AND-superstate

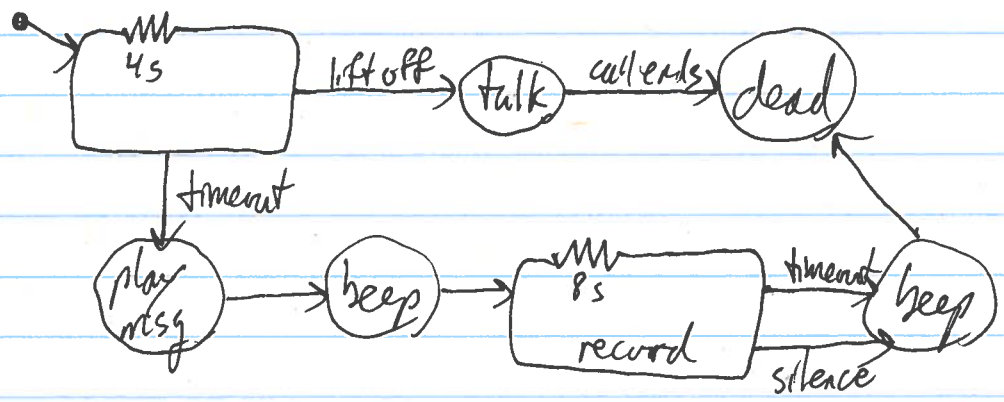


- Timers



- stays in the state for at most the stated time
- must have a timeout edge

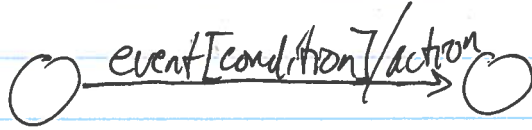
e.g.



Variables

- used to encode states with large numbers of values
e.g. to model queuing system
 - use states to encode actions such as service
 - # of clients encoded as a variable

Transitions



- condition: based on variable values
- action: assignment to a variable or generate event

e.g.

service-off [$C=7$] / $e:=0$
 (# clients

State Chart Semantics

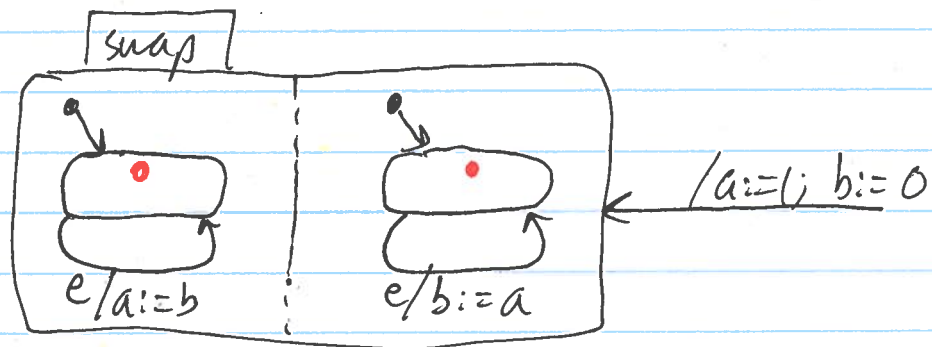
- models synchronous behaviour: all transitions fire at once

- ① evaluate events and conditions
- ② determine transitions^{which} happen
- ③ fire all transitions and apply any actions

- time semantics

- ① evaluate all internally generated events
- ② apply transitions and repeat until stable
- ③ advance simulation time to next external event (or timeout)

- example:



- when event e arrives, left state assigns 0 to a , right state assigns 1 to b

- translates well to hardware

- can produce inefficient software implementations