**Towards Sentient Chips: Self-Awareness through On-Chip Sensemaking - by Nikhil Dutt**

**Cyberphysical-Systems-on-Chip (CPSoC)**

a new class of sensor-actuator-rich, many-core computing platforms that intrinsically couple on-chip and cross-layer sensing and actuation to enable self-awareness.

Unlike traditional Multiprocessor Systems-on-Chip (MPSoCs), CPSoC is distinguished by an intelligent co-design of the control, communication, and computing (C3) system that interacts with the physical environment in real time in order to modify the system's behavior so as to adaptively achieve desired objectives and Quality-of-Service (QoS).

The CPSoC design paradigm enables self-awareness (i.e., the ability of the system to observe its own internal and external behaviors such that it is capable of making judicious decision) and (opportunistic) adaptation using the concept of cross-layer physical and virtual sensing and actuations applied across different layers of the hardware/software system stack. The closed loop control used for adaptation to dynamic variation—commonly known as the observe-decide-act (ODA) loop—is implemented using an adaptive, reflexive middleware layer. The learning abilities of CPSoC provide a unified interface API for sensor and actuator fusion along with the ability to improve autonomy in system management. The CPSoC paradigm is the first step towards a holistic software/hardware effort to make complex chips "sentient."

Introducing the combined application of artificial intelligence and machine learning where hardware is introduced with advanced features to enhance the smart devices. This hardware possesses properties like self-awareness , context awareness

Self-awareness – like living mechanisms becoming aware of the system states and behaviors

Context awareness - Becoming aware of not just the system itself but also the surroundings and understanding it. Tuning system settings and features to optimize the performance of hardware and resultantly the software.

For example - Self-awareness and adaptation in biology.

More concepts related to self-awareness and context awareness like self-configuring, self-healing, self-optimizing, self-protecting to create self-dependent hardware to share the task of performance optimization among both hardware and software.

Sensemaking : Process that let’s one give meaning to experience. The ability to perceive things and recognize it.

For example : self-assembling robots. The robots who are aware of their surroundings and themselves (their system) and are programmed to the assemble. The rule of assembly involve rules that require self-awareness and context-awareness.

Sentient Chips:

– Construct model of behaviors and environment using sensor data

– Achieve self-awareness through on-chip sensors and monitors

• Experience phenomena

• Aware of state and behavior

– The ability to introspect

– Adapt behavior based on model of external and internal environment

Chips must adapt to Dynamic Performance, Power, Resilience, Security,….

Cyber-Physical System-On-Chip (CPSoC)

Sensor-actuator rich adaptive SoC platform

* Self-awareness
* Predictive modeling and learning
* Combine hardware and software sensors

Cross-Layer Physical/Virtual Sensing & Actuation

* On-chip sensing and actuation unit
* NoC overlay
* SW enable sensors and actuators
* Adaptive control of platform resources

Cross-Layer Physical/Virtual Sensing

• Many restrictions in physical deployment of sensors and test structures in MPSoCs:

– Resource constraints

• e.g., Area, Power

– Limited number, resolution, accuracy, range

– Placement Restrictions

– Complexity of sensing and observation structures

– Inaccessibility or inability of direct measurement

– Prohibitive cost Virtual Sensing is a Indirect Computa3onal Approach to overcome several sensing limita3ons

For example virtual power sensing with few thermal sensors (results achieved were very close to expected )

Sample Application and Use cases

• Energy Efficiency (Throughput/Power) – Dynamic Workloads – Opportunistic Load balancing – Adaptive Scheduler – Evolutionary Approach

• Thermal-Aware Performance – Dynamic/Adaptive Parallelization – Heterogeneous Architecture – Adaptive Scheduling

• Aging and Resilience – Opportunistic Allocation – Duty cycling of Active and Resting periods **Towards Sentient Chips: Self-Awareness through On-Chip Sensemaking - by Nikhil Dutt**

Introducing smartness in hardware as well software to enhance the efficiency and performance of computing to a whole new level. A new class of sensor-actuator-rich, many-core computing platforms that intrinsically couple on-chip and cross-layer sensing and actuation to enable self-awareness.Cyberphysical-Systems-on-Chip (CPSoC) includes Self-awareness, predictive modeling and learning, combine hardware and software sensors which makes the performance of the hardware very efficient and resultantly enhanced software. The self-awareness and context-awareness provides the hardware ability to moderate the temperature and other factors of hardware to maintain the performance.

Question: Are we making our hardware overly complex by providing them sensors and giving them ability to govern themselves and giving less and less control to human?