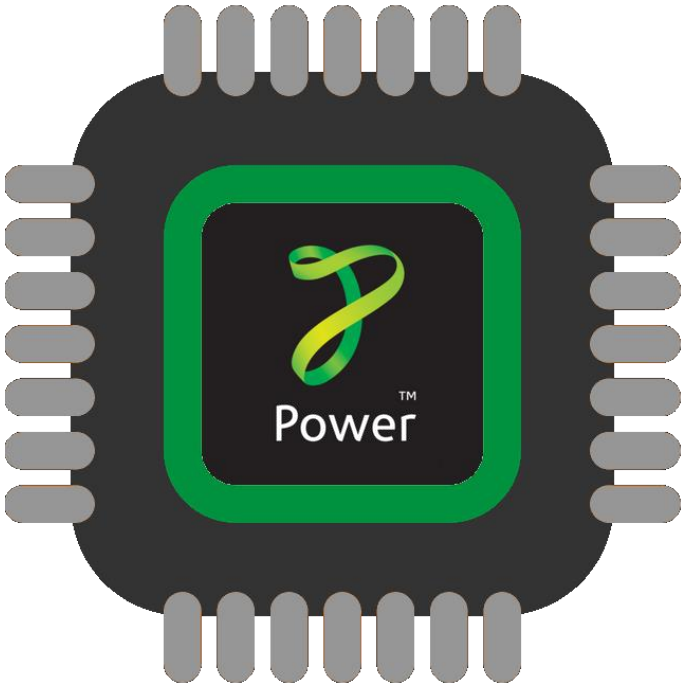
IBM – POWER8

Processor Architecture



COMBE Pierre, DESPLANCHES Cédric, HISSELLI Alexandre and RAJFURA Tristan
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UNIVERSITÉ Grenoble Alpes

POLYTECH GRENOBLE

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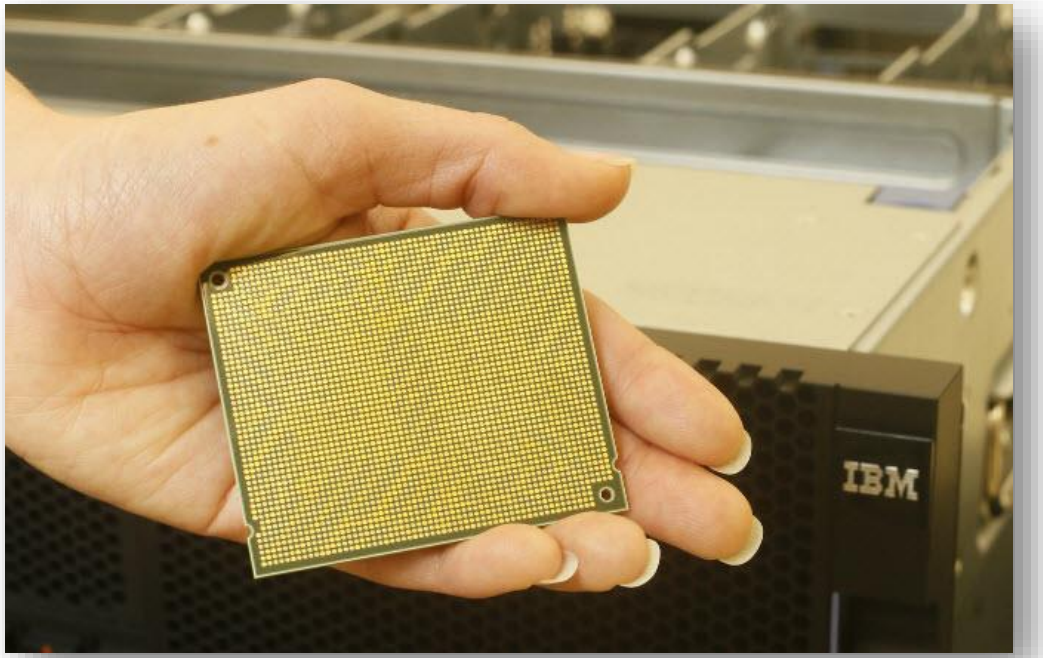


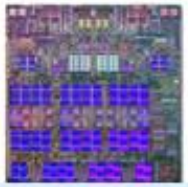
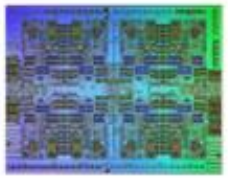
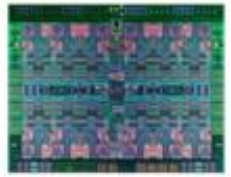
SOME FIGURES…

Produced	2013
Manufacturer	IBM (Computer Hardware Company)
Clock Frequency	2,5 GHz to 5 GHz
Technology	22 nm
Instruction Set	Power Architecture (Power ISA v2.07)
Cores	4, 6, 8, 10 or 12
Cache L1	64 + 32 KB per core
Cache L2	512 KB per core
Cache L3	8 MB per chipset
Cache L4	16 MB per Centaur
Predecessor	POWER7
Successor	POWER9

POWER BACKGROUND

- **What is the POWER architecture ?**
  - RISC architecture developed by IBM
  - Acronym for Performance Optimization with Enhanced RISC
  - Open for licensing
- **Goals of POWER8**
  - Compete with x86 Architecture
  - Focus on support for Linux machines
  - Create an open-source processor, with the OpenPOWER Consortium
  - Scalability
  - Target servers / large systems, IBMi OS's, Linux
- **Implementations**
  - IBM's Watson (POWER7-8)
  - Mars rovers (POWER1)
  - Servers
  - PowerPC (modified version of POWER architecture)

POWER BACKGROUND

	POWER5 2004	POWER6 2007	POWER7 2010	POWER7+ 2012	POWER8
					
Technology	130nm SOI	65nm SOI	45nm SOI eDRAM	32nm SOI eDRAM	22nm SOI eDRAM
Compute					
Cores	2	2	8	8	12
Threads	SMT2	SMT2	SMT4	SMT4	SMT8
Caching					
On-chip	1.9MB	8MB	2 + 32MB	2 + 80MB	6 + 96MB
Off-chip	36MB	32MB	None	None	128MB
Bandwidth					
Sust. Mem.	15GB/s	30GB/s	100GB/s	100GB/s	230GB/s
Peak I/O	6GB/s	20GB/s	40GB/s	40GB/s	96GB/s

POWER8 VISION

Leadership Performance

- Increase core throughput at single thread, SMT2, SMT4, SMT8 level
- Large step in per socket performance
- Enable more robust multi-socket scaling

System Innovation

- Higher capacity cache hierarchy and highly threaded processor
- Enhanced memory bandwith, capacity, and expansion
- Dynamic code optimization
- Hardware-accelerate virtual memory management

Open System Innovation

- Coherent Accelerator Processor Interface (CAPI)
- Open system software

Optimize Analytics & Big Data

Enhance Cloud Efficiency

Enable Open Innovation on POWER

POWER8 PROCESSOR

Energy Management

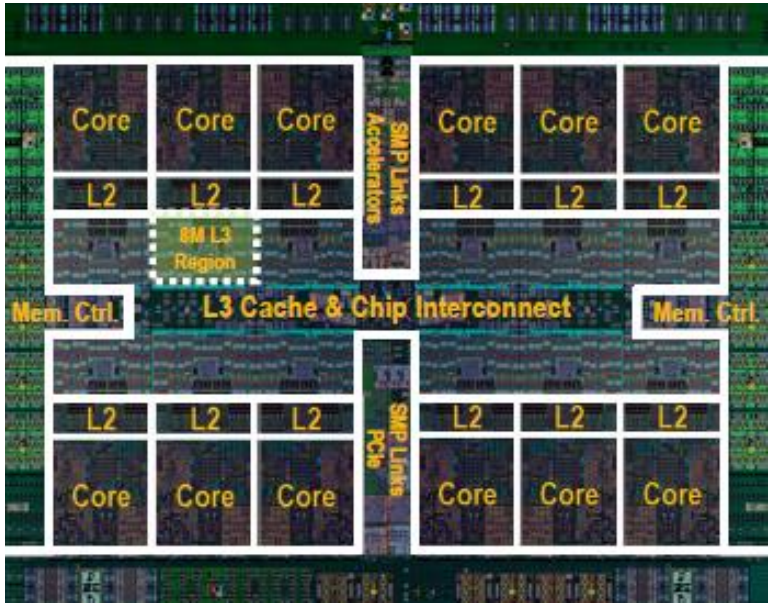
- On-chip Power Management Micro-controller
- Integrated Per-core VRM (Voltage Regulator)

Cores

- 12 cores (SMT8)
- 8dispatch, 10 issue, 16 exec pipe
- 2X internal data flows/queues
- Enhanced prefetching
- 64K data cache, 32K instruction

Accelerators

- Crypto & memory expansion
- Transactionnal Memory
- Virtual Machine Monitor assist
- Data Move / VM mobility



Technology

- 22nm SOI, eDRAM, 15 ML 650 mm²

Caches

- 512KB SRAM L2 / core
- 96 MB eDRAM shared L3
- Up to 128 MB eDRAM L4 (off-chip)

Memory

- Up to 230 GB/s sustained bandwith

Bus interface

- Durable open memory attach interface
- Integrated PCIe Gen3
- Synchr. Multi-Proc. Interconnect
- CAPI (Coherent Accelerator Processor Interface)

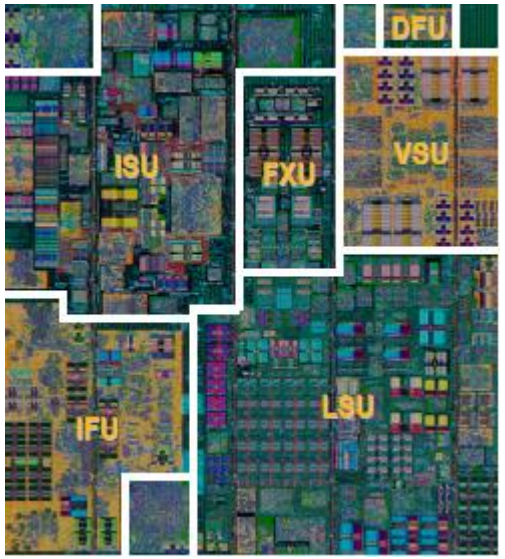
POWER8 CORE

Execution Improvement vs POWER7

- SMT4 → SMT8
- 6 dispatch → 8
- 8 issue →10
- 12 execution pipes →16
- 2*24 Issue queues → 4*16-entry
- Larger global completion, Load/Store reorder
- Improved branch prediction
- Improved unaligned storage access

Core Performance vs POWER7

- 1,6x Thread
- 2x Max SMT



Larger Caching Structures vs POWER7

- 32KB → 2x L1 data cache (64 KB)
- 2x outstanding data cache misses
- 4x translation cache

Wider Load/Store

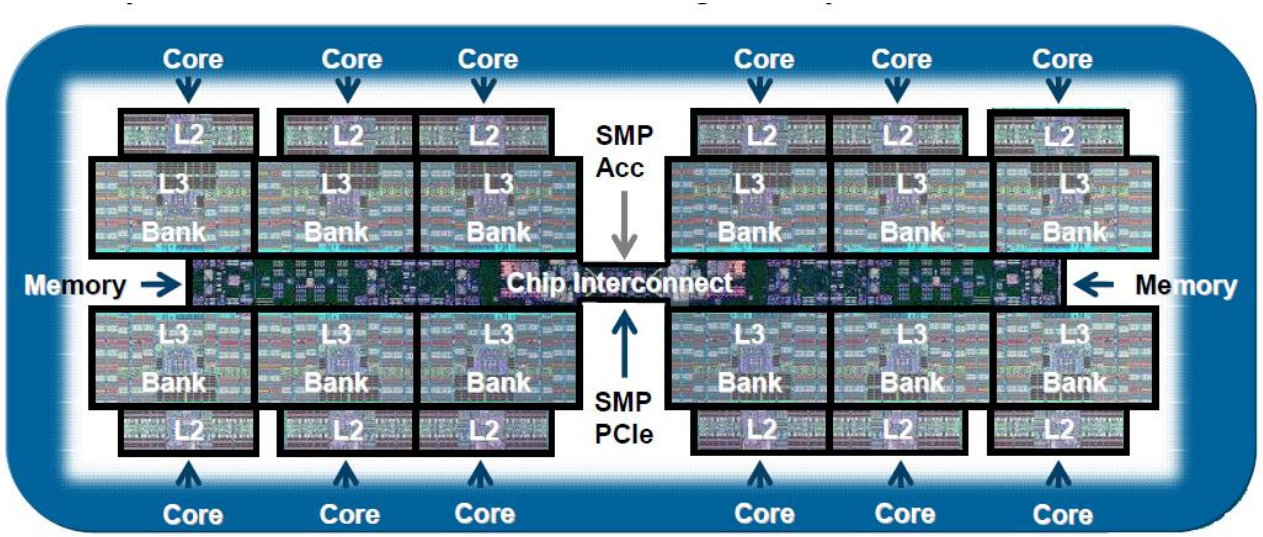
- 32 B → 64 B L2 to L1 data bus
- 2x data cache to execution dataflow

Enhanced Prefetch

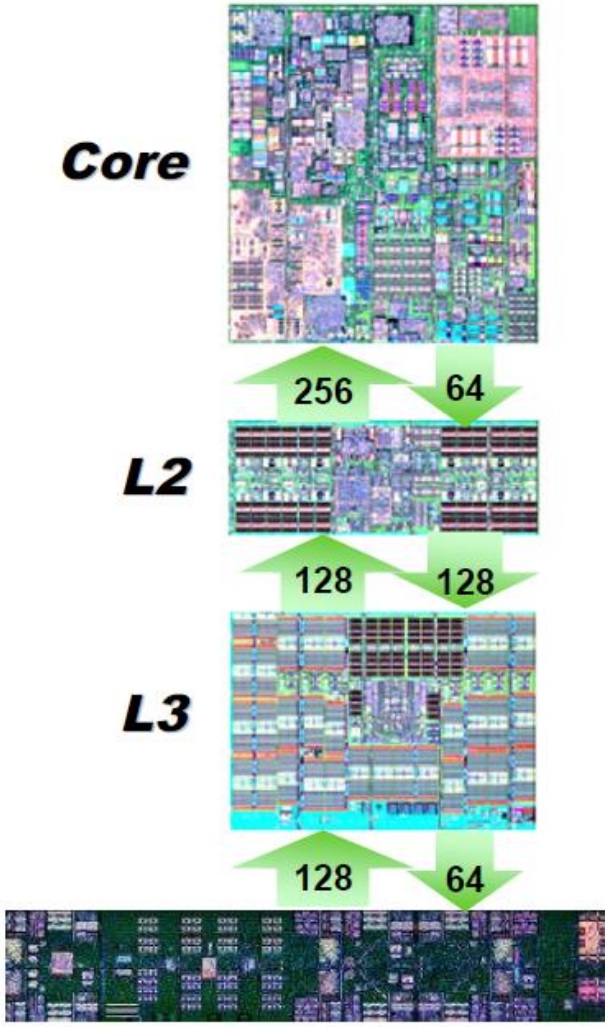
- Instruction Speculation awareness
- Data prefetch depth awareness
- Adaptative bandwith awareness
- Topology awareness

POWER8 ON-CHIP CACHES

- L2 : 512 KB 8 way per core
- L3 : 96 MB (12*8 MB 8 way bank)
- Chip Interconnect: 150 GB/sec * 12 segments per direction = 3,6 TB/ sec
- « NUCA » cache policy (Non-Uniform Cache Architecture)
  - Scalable bandwith and latency
  - Migrate « hot » lines to local L2, then local L3 (replicate L2 contained footprint)



CACHE BANDWITHS



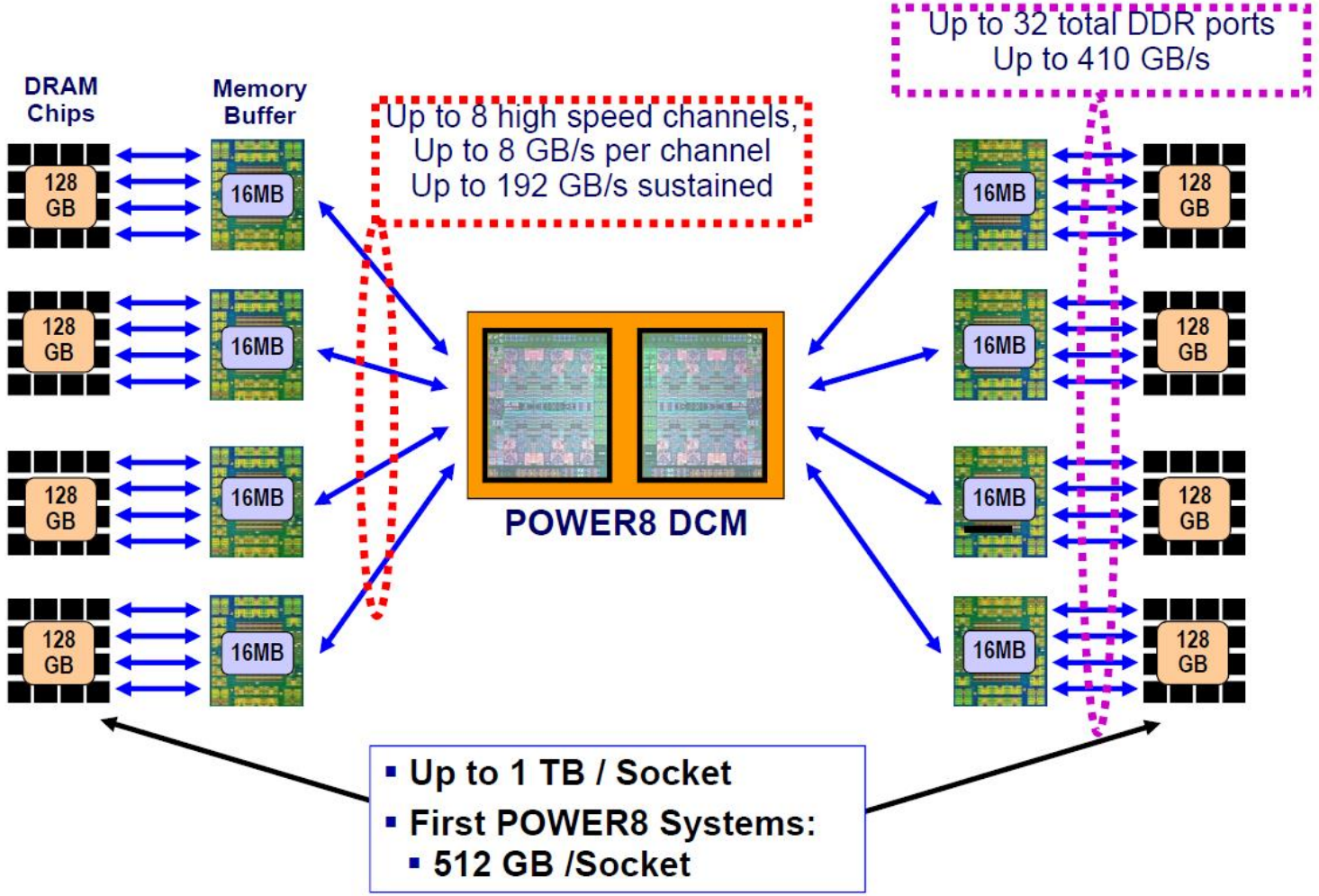
GB/sec shown assuming 4 GHz

- Product frequency will vary based on model type

Accross 12 core chip

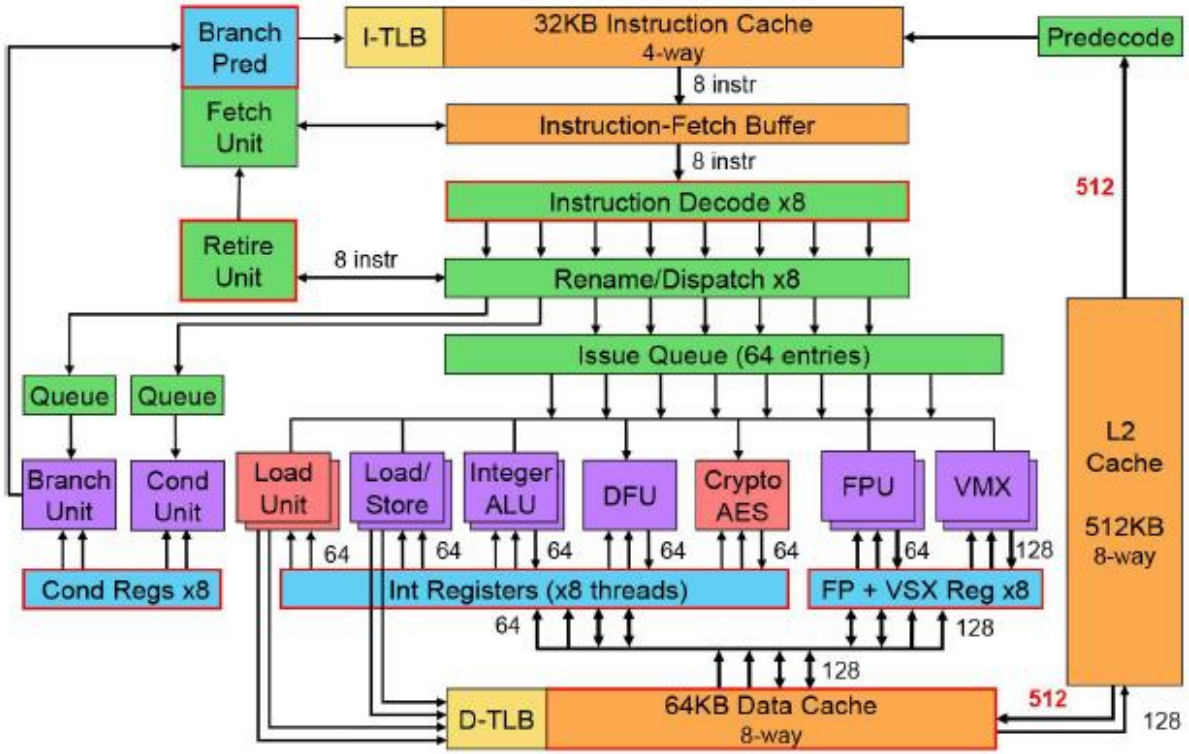
- 4 TB/sec L2 BW
- 3 TB/sec L3 BW

POWER8 MEMORY ORGANIZATION

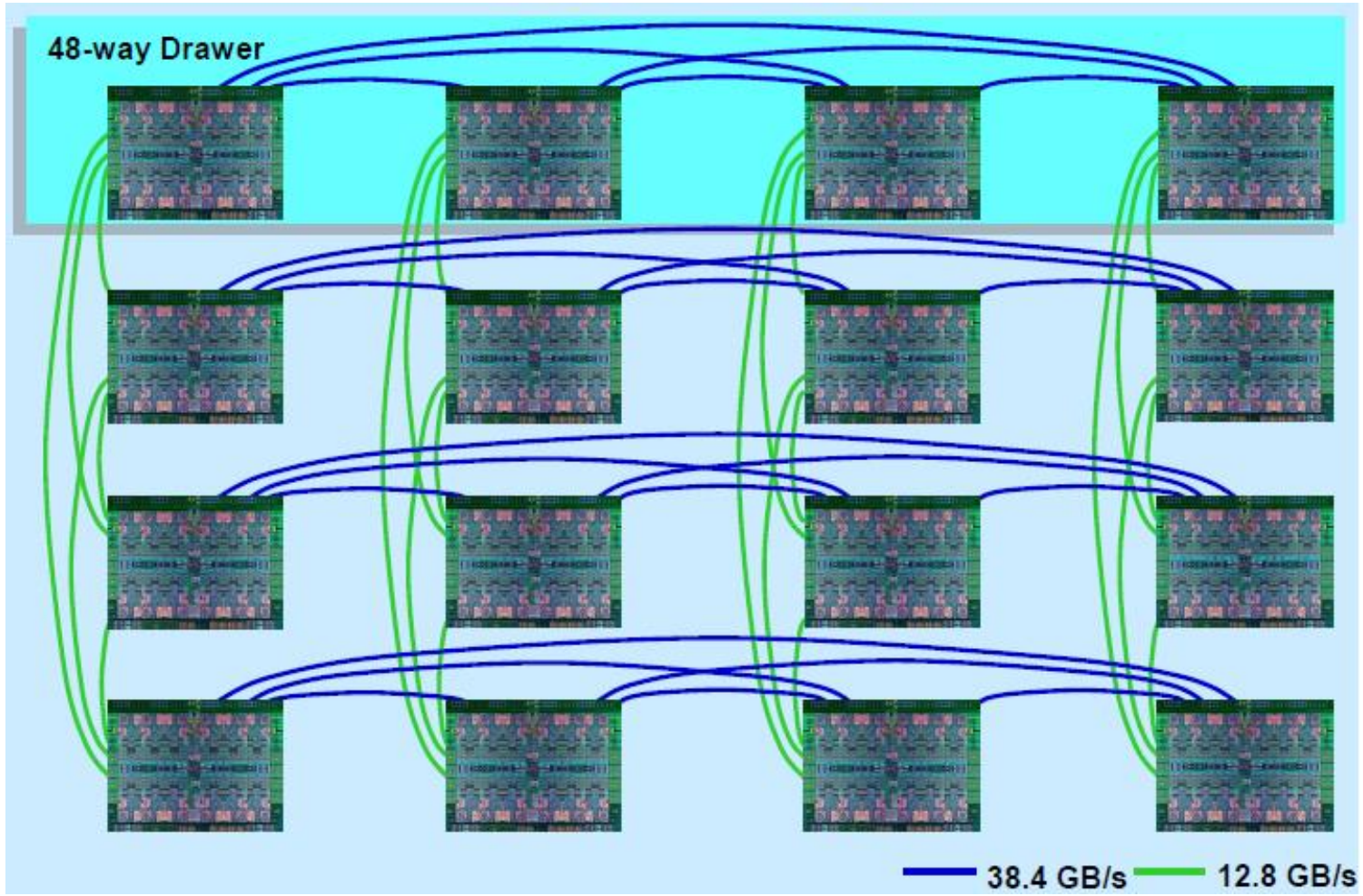


PIPELINE

- 16 execution pipes :
  - 2 FXU : Fixed-Point Units
  - 2 LSU : Load Store Units
  - 2 LU : Load Units
  - 4 FPU : (Double precision) Fixed Point Units
  - 2 VMX : Vector Math Units
  - 1 Crypto
  - 1 DFU : Decimal Floating Unit
  - 1 CRU : Condition Register Unit
  - 1 BRU : Branch Register Unit



INTERCONNECTION SMP



CAPI – COHERENT ACCELERATOR PROCESSOR INTERFACE

- Allows direct communication between CPU and PCIe connected devices
- Removes OS and Driver overhead
- More coherent memory addressing
- Follows more natural programming model
- Accomplished by circumventing I/O bridge used in processor

CAPI – COHERENT ACCELERATOR PROCESSOR INTERFACE

Virtual Addressing

- Accelerator can work with same memory addresses that the processors use
- Pointers dereferenced same as the host application
- Removes OS & device driver overhead

Hardware Managed Cache Coherence

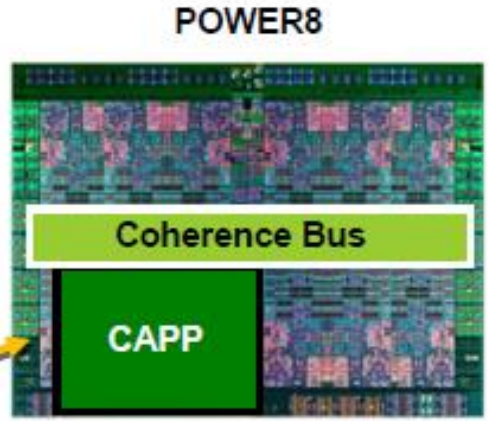
- Enables the accelerator to participate in « Locks » as a normal thread lowers latency over IO communication model

Customizable Hardware Application Accelerator

- Specific system SW, middleware, or user application
- Written to durable interface provided by PSL

PCIe Gen 3

Transport for encapsulated messages



Processor Service Layer (PSL)

- Present Robust, durable interfaces to applications
- Offload complexity / content from CAPP

CAPI – COHERENT ACCELERATOR PROCESSOR INTERFACE

https://www.youtube.com/watch?v=4ZyXc12J6FA

Morceau choisi : 1’30 → 2’48

SOFTWARE TOOLS AVAILABLE

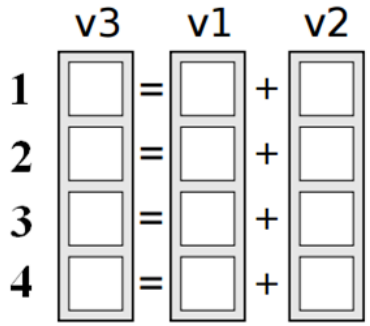
IBM i	Linux on Power	AIX
IBM Rational Developer	IBM Software Development Kit	PowerSC PowerHA
PowerVM : Server Virtualization		
XL C/C++ Compiler		
XL Fortran Compiler		

INSTRUCTION SET

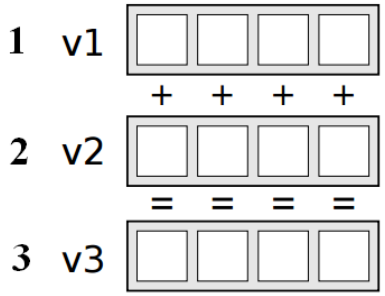
- Reduced Instruction Set Computer
- Power I.S.A. v2.07

```
int *x, *y, *z;
x = (int*) malloc(n * sizeof(int));
y = (int*) malloc(n * sizeof(int));
z = (int*) malloc(n * sizeof(int));

#pragma omp simd
for(i = 0; i < N; ++i)
  z[i] = a * x[i] + y[i];
```



Scalar Calculus



Vector Calculus

INSTRUCTION SET

```
.L7:
lwz 9,124(31)
extsw 9,9
std 9,104(31)
lfd 0,104(31)
stfd 0,104(31)
ld 8,104(31)
sldi 9,8,2
ld 10,152(31)
add 9,10,9
lwz 10,124(31)
extsw 10,10
std 10,104(31)
lfd 0,104(31)
stfd 0,104(31)
ld 7,104(31)
sldi 10,7,2
ld 8,136(31)
add 10,8,10
```

```
lwz 10,0(10)
extsw 10,10
lwz 8,132(31)
mullw 10,8,10
extsw 8,10
lwz 10,124(31)
extsw 10,10
std 10,104(31)
lfd 0,104(31)
stfd 0,104(31)
ld 7,104(31)
sldi 10,7,2
ld 7,144(31)
add 10,7,10
lwz 10,0(10)
extsw 10,10
add 10,8,10
extsw 10,10
stw 10,0(9)
```

GCC with -01 –fopenmp -simd

Load VSX vector 4 words
Vector shift left word

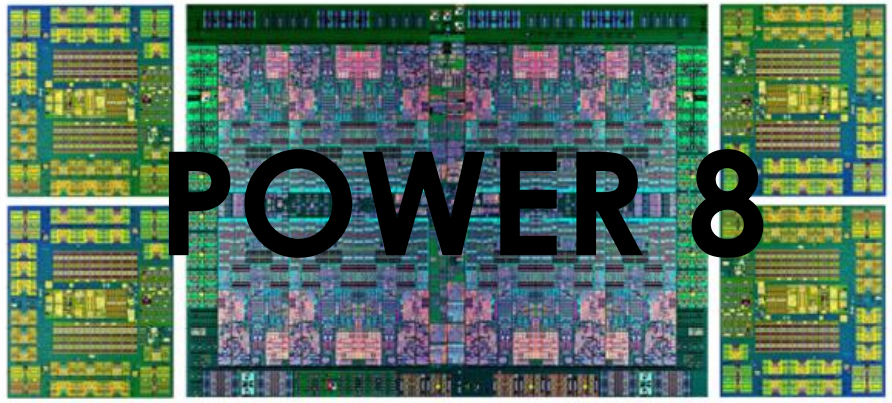
Vector add unsigned half
Vector add unsigned word
Store VSX vector 4 words

```
lxvw4x  vs36,0,r5
vslw    v5,v6,v1
addi    r7,r7,16
addi    r5,r5,16
vadduhm v3,v3,v5
vadduwm v3,v3,v4
stxvw4x vs35,r6,r9
beq     cr1,3b8 <foo+0x3b8>
li      r9,16
lxvw4x  vs41,r7,r9
lxvw4x  vs37,0,r7
```

XL C/C++ Compiler with :
-O3 -qhot -qarch=pwr8 -qtune=pwr8

CONCLUSION

- Significant Performance at Thread, Core and System
- Strong Enablement of Autonomic System Optimization
- Excellent Big Data Analytics Capability
- Virtualization of data
- Secure data
- Making resource groups highly available
- Vector and Parallel Computing



THANK YOU FOR YOUR ATTENTION!

SOURCES

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