self_balancing_robot Design Description Horia

self_balancing_robot: Design Description Horia

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Chapter 1. Model Version

Version: 1.9

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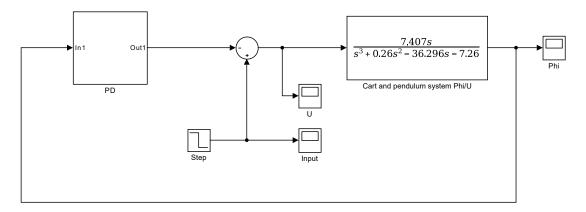
Checksum: 1197441069 524376390 3545489264 441486458

Chapter 2. Root System

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Figure 2.1. self_balancing_robot



2.1. Blocks

2.1.1. Parameters

2.1.1.1. "Cart and pendulum system Phi/U" (TransferFcn)

Table 2.1. "Cart and pendulum system Phi/U" Parameters

Parameter	Value
Numerator coefficients	[7.407 0]
Denominator coefficients	[1 0.26 -36.296 -7.26]
State Name (e.g., 'position')	

2.1.1.2. "Step" (Step)

Table 2.2. "Step" Parameters

Parameter	Value
Step time	0.2

Parameter	Value
Initial value	1
Final value	0
Sample time	0
Interpret vector parameters as 1-D	on
Enable zero-crossing detection	on

2.1.1.3. "Sum" (Sum)

Table 2.3. "Sum" Parameters

Parameter	Value
Icon shape	round
List of signs	-+
Sum over	All dimensions
Dimension	1
Require all inputs to have the same data type	off
Accumulator data type	Inherit: Inherit via internal rule
Output minimum	
Output maximum	
Output data type	Inherit: Inherit via internal rule
Lock data type settings against changes by the fixed-point tools	off
Integer rounding mode	Floor
Saturate on integer overflow	off
Sample time (-1 for inherited)	-1

2.1.2. Block Execution Order

- Step [2] (Step)
 Input [2] (Scope)
 Cart and pendulum system Phi/U [2] (TransferFcn)
- 4. Phi [2] (Scope)

- Kp [7] (Gain)
 Integrator [6] (Integrator)
 Kd [6] (Gain)
 Derivative [5] (Derivative)
 Sum [9] (Sum)
 Sum [3] (Sum)
 U [3] (Scope)
 Ki [7] (Gain)

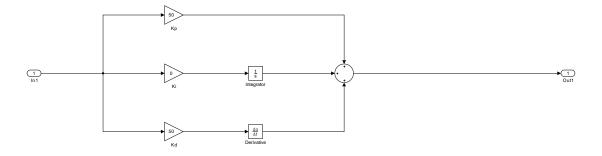
Chapter 3. Subsystems

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3.1. PD

Figure 3.1. self_balancing_robot/PD



3.1.1. Blocks

3.1.1.1. Parameters

3.1.1.1. "Derivative" (Derivative)

Table 3.1. "Derivative" Parameters

Parameter	Value
Coefficient c in the tr- ansfer function appr- oximation s/(c*s + 1) used for linearization	

3.1.1.1.2. "In1" (Inport)

Table 3.2. "In1" Parameters

Parameter	Value
Port number	1
Port dimensions (-1 for inherited)	-1

Parameter	Value
Sample time (-1 for inherited)	-1
Minimum	
Maximum	
Data type	Inherit: auto

3.1.1.3. "Integrator" (Integrator)

Table 3.3. "Integrator" Parameters

Parameter	Value
External reset	none
Initial condition sou- rce	internal
Initial condition	0
Limit output	off
Upper saturation limit	inf
Lower saturation li- mit	-inf
Wrap state	off
Wrapped state upper value	pi
Wrapped state lower value	-pi
Show saturation port	off
Show state port	off
Ignore limit and reset when linearizing	off
Enable zero-crossing detection	on
State Name (e.g., 'position')	

3.1.1.1.4. "Kd" (Gain)

Table 3.4. "Kd" Parameters

Parameter	Value
Gain	50
Multiplication	Element-wise(K.*u)

Parameter	Value
Parameter minimum	
Parameter maximum	
Parameter data type	Inherit: Inherit via internal rule
Output minimum	
Output maximum	
Output data type	Inherit: Inherit via internal rule
Lock output data ty- pe setting against changes by the fixe- d-point tools	off
Integer rounding mo- de	Floor
Saturate on integer overflow	off
Sample time (-1 for inherited)	-1

3.1.1.1.5. "Ki" (Gain)

Table 3.5. "Ki" Parameters

Parameter	Value
Gain	0
Multiplication	Element-wise(K.*u)
Parameter minimum	
Parameter maximum	
Parameter data type	Inherit: Inherit via internal rule
Output minimum	
Output maximum	
Output data type	Inherit: Inherit via internal rule
Lock output data ty- pe setting against changes by the fixe- d-point tools	off
Integer rounding mode	Floor
Saturate on integer overflow	off
Sample time (-1 for inherited)	-1

3.1.1.1.6. "Kp" (Gain)

Table 3.6. "Kp" Parameters

Parameter	Value
Gain	50
Multiplication	Element-wise(K.*u)
Parameter minimum	
Parameter maximum	
Parameter data type	Inherit: Inherit via internal rule
Output minimum	
Output maximum	
Output data type	Inherit: Inherit via internal rule
Lock output data ty- pe setting against changes by the fixe- d-point tools	off
Integer rounding mo- de	Floor
Saturate on integer overflow	off
Sample time (-1 for inherited)	-1

3.1.1.7. "Out1" (Outport)

Table 3.7. "Out1" Parameters

Parameter	Value
Port number	1
Icon display	Port number
Minimum	
Maximum	
Data type	Inherit: auto
Lock output data ty- pe setting against changes by the fixe- d-point tools	off
Output as nonvirtual bus in parent model	off
Unit (e.g., m, m/s^2, N*m)	inherit
Port dimensions (-1 for inherited)	-1

Parameter	Value
Variable-size signal	Inherit
Sample time (-1 for inherited)	-1
Ensure outport is virtual	off
Source of initial output value	Dialog
Output when disabled	held
Initial output	
MustResolveToSigna- lObject	off

3.1.1.1.8. "Sum" (Sum)

Table 3.8. "Sum" Parameters

Parameter	Value
Icon shape	round
List of signs	+++
Sum over	All dimensions
Dimension	1
Require all inputs to have the same data type	off
Accumulator data ty- pe	Inherit: Inherit via internal rule
Output minimum	
Output maximum	
Output data type	Inherit: Inherit via internal rule
Lock data type settings against changes by the fixed-point tools	off
Integer rounding mode	Floor
Saturate on integer overflow	off
Sample time (-1 for inherited)	-1

Chapter 4. System Design Variables

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4.1. Design Variable Summary

Table 4.1. Functions used in Design Variable Expressions

Function Name	Parent Blocks	Calling character vector
pi	Integrator [6] Integrator [6]	pi -pi

Chapter 5. Requirements Traceability

self_balancing_robot does not contain requirements traceability links.

Chapter 6. System Model Configuration

Source: Model

Source Name: self_balancing_robot

Table 6.1. self_balancing_robot Configuration Set

Property	Value
Description	
Components	[self_balancing_robot Configuration Set.Components(1) [12], self_balancing_robot Configuration Set.Components(2) [13], self_balancing_robot Configuration Set.Components(3) [14], self_balancing_robot Configuration Set.Components(4) [15], self_balancing_robot Configuration Set.Components(5) [18], self_balancing_robot Configuration Set.Components(6) [20], self_balancing_robot Configuration Set.Components(7) [20], self_balancing_robot Configuration Set.Components(8) [21], self_balancing_robot Configuration Set.Components(9) [23], self_balancing_robot Configuration Set.Components(10) [24]]
Name	Configuration
SimulationMode	normal
ConfigType	Model

Table 6.2. self_balancing_robot Configuration Set.Components [12](1)

Property	Value
Name	Solver
Description	
Components	
StartTime	0.0
StopTime	10
AbsTol	auto
FixedStep	auto
InitialStep	auto
MaxNumMinSteps	-1
MaxOrder	5
ZcThreshold	auto

ConsecutiveZCsStepRelTol	10*128*eps
MaxConsecutiveZCs	1000
ExtrapolationOrder	4
NumberNewtonIterations	1
MaxStep	auto
MinStep	auto
MaxConsecutiveMinStep	1
RelTol	1e-3
SolverMode	SingleTasking
EnableMultiTasking	off
EnableConcurrentExecution	off
ConcurrentTasks	off
Solver	VariableStepAuto
SolverName	VariableStepAuto
SolverType	Variable-step
SolverJacobianMethodControl	auto
ShapePreserveControl	DisableAll
ZeroCrossControl	UseLocalSettings
ZeroCrossAlgorithm	Nonadaptive
SolverResetMethod	Fast
PositivePriorityOrder	off
AutoInsertRateTranBlk	off
SampleTimeConstraint	Unconstrained
InsertRTBMode	Whenever possible
SampleTimeProperty	

Table 6.3. self_balancing_robot Configuration Set.Components [12](2)

Property	Value
Name	Data Import/Export
Description	
Components	
Decimation	1
ExternalInput	[t, u]
FinalStateName	xFinal
InitialState	xInitial
LimitDataPoints	off
MaxDataPoints	1000
LoadExternalInput	off

LoadInitialState	off
SaveFinalState	off
SaveCompleteFinalSimState	off
SaveFormat	Dataset
SaveOutput	on
SaveState	off
SignalLogging	on
DSMLogging	on
InspectSignalLogs	off
SaveTime	on
ReturnWorkspaceOutputs	off
StateSaveName	xout
TimeSaveName	tout
OutputSaveName	yout
SignalLoggingName	logsout
DSMLoggingName	dsmout
OutputOption	RefineOutputTimes
OutputTimes	0
ReturnWorkspaceOutputsName	out
Refine	1
LoggingToFile	off
DatasetSignalFormat	timeseries
LoggingFileName	out.mat
LoggingIntervals	[-inf, inf]

Table6.4.self_balancing_robotConfigurationSet.Components [12](3)

Property	Value
Name	Optimization
Description	
Components	
BlockReduction	on
BooleanDataType	on
ConditionallyExecuteInputs	on
DefaultParameterBehavior	Tunable
InlineParams	off
UseDivisionForNetSlopeComputation	off
UseFloatMulNetSlope	off
DefaultUnderspecifiedDataType	double

UseSpecifiedMinMax	off
InlineInvariantSignals	off
OptimizeBlockIOStorage	on
BufferReuse	on
GlobalBufferReuse	on
GlobalVariableUsage	None
StrengthReduction	off
AdvancedOptControl	
EnforceIntegerDowncast	on
ExpressionFolding	on
BooleansAsBitfields	off
BitfieldContainerType	uint_T
EnableMemcpy	on
MemcpyThreshold	64
PassReuseOutputArgsAs	Structure reference
PassReuseOutputArgsThreshold	12
FoldNonRolledExpr	on
LocalBlockOutputs	on
RollThreshold	5
StateBitsets	off
DataBitsets	off
ActiveStateOutputEnumStorageType	Native Integer
UseTempVars	off
ZeroExternalMemoryAtStartup	on
ZeroInternalMemoryAtStartup	on
InitFltsAndDblsToZero	off
NoFixptDivByZeroProtection	off
EfficientFloat2IntCast	off
EfficientMapNaN2IntZero	on
LifeSpan	auto
EvaledLifeSpan	Inf
MaxStackSize	Inherit from target
BufferReusableBoundary	on
SimCompilerOptimization	off
AccelVerboseBuild	off
OptimizeBlockOrder	off
OptimizeDataStoreBuffers	on
BusAssignmentInplaceUpdate	on

Table 6.5. self_balancing_robot Configuration Set.Components [12](4)

Property	Value
Name	Diagnostics
Description	
Components	
RTPrefix	error
ConsistencyChecking	none
ArrayBoundsChecking	none
SignalInfNanChecking	none
SignalRangeChecking	none
ReadBeforeWriteMsg	UseLocalSettings
WriteAfterWriteMsg	UseLocalSettings
WriteAfterReadMsg	UseLocalSettings
AlgebraicLoopMsg	warning
ArtificialAlgebraicLoopMsg	warning
SaveWithDisabledLinksMsg	warning
SaveWithParameterizedLinksMsg	warning
CheckSSInitialOutputMsg	on
UnderspecifiedInitializationDetection	Simplified
MergeDetectMultiDrivingBlocksExec	error
CheckExecutionContextRuntimeOutputM-sg	off
SignalResolutionControl	UseLocalSettings
BlockPriorityViolationMsg	warning
MinStepSizeMsg	warning
TimeAdjustmentMsg	none
MaxConsecutiveZCsMsg	error
MaskedZcDiagnostic	warning
IgnoredZcDiagnostic	warning
SolverPrmCheckMsg	none
InheritedTsInSrcMsg	warning
MultiTaskDSMMsg	error
MultiTaskCondExecSysMsg	error
MultiTaskRateTransMsg	error
SingleTaskRateTransMsg	none
TasksWithSamePriorityMsg	warning
SigSpecEnsureSampleTimeMsg	warning
CheckMatrixSingularityMsg	none

IntegerOverflowMsg	warning
Int32ToFloatConvMsg	warning
ParameterDowncastMsg	error
ParameterOverflowMsg	error
ParameterUnderflowMsg	none
ParameterPrecisionLossMsg	warning
ParameterTunabilityLossMsg	warning
FixptConstUnderflowMsg	none
FixptConstOverflowMsg	none
FixptConstPrecisionLossMsg	none
UnderSpecifiedDataTypeMsg	none
UnnecessaryDatatypeConvMsg	none
VectorMatrixConversionMsg	none
InvalidFcnCallConnMsg	error
FcnCallInpInsideContextMsg	error
SignalLabelMismatchMsg	none
UnconnectedInputMsg	warning
UnconnectedOutputMsg	warning
UnconnectedLineMsg	warning
UseOnlyExistingSharedCode	error
SFcnCompatibilityMsg	none
FrameProcessingCompatibilityMsg	error
UniqueDataStoreMsg	none
BusObjectLabelMismatch	warning
RootOutportRequireBusObject	warning
AssertControl	UseLocalSettings
Echo	
EnableOverflowDetection	off
AllowSymbolicDim	on
ModelReferenceIOMsg	none
Model Reference Version Mismatch Message	none
ModelReferenceIOMismatchMessage	none
ModelReferenceCSMismatchMessage	none
ModelReferenceSimTargetVerbose	off
UnknownTsInhSupMsg	warning
ModelReferenceDataLoggingMessage	warning
ModelReferenceSymbolNameMessage	warning
ModelReferenceExtraNoncontSigs	error
StateNameClashWarn	none

$\Big SimStateInterfaceChecksumMismatchMsg$	warning
SimStateOlderReleaseMsg	error
InitInArrayFormatMsg	warning
StrictBusMsg	ErrorLevel1
BusNameAdapt	WarnAndRepair
NonBusSignalsTreatedAsBus	none
SFUnusedDataAndEventsDiag	warning
SFUnexpectedBacktrackingDiag	error
SFInvalidInputDataAccessInChartInitDiag	warning
SFNoUnconditionalDefaultTransitionDiag	error
SFTransitionOutsideNaturalParentDiag	warning
SFUnconditionalTransitionShadowingDiag	warning
SFUnreachableExecutionPathDiag	warning
SFUndirectedBroadcastEventsDiag	warning
SFTransitionActionBeforeConditionDiag	warning
SFOutputUsedAsStateInMooreChartDiag	error
SFTemporalDelaySmallerThanSampleTimeDiag	warning
SFUnconditionalPathOutOfParentDiag	warning
SFSelfTransitionDiag	warning
SFExecutionAtInitializationDiag	warning
SFMachineParentedDataDiag	warning
SFUnreachableStateOrJunctionDiag	warning
SFDanglingTransitionDiag	warning
IntegerSaturationMsg	warning
AllowedUnitSystems	all
UnitsInconsistencyMsg	warning
AllowAutomaticUnitConversions	on

Table 6.6. self_balancing_robot Configuration Set.Components [12](5)

Property	Value
Name	Hardware Implementation
Description	
Components	
ProdBitPerChar	8
ProdBitPerShort	16
ProdBitPerInt	32
ProdBitPerLong	32

ProdBitPerLongLong	64
ProdBitPerFloat	32
ProdBitPerDouble	64
ProdBitPerPointer	64
ProdBitPerSizeT	64
ProdBitPerPtrDiffT	64
ProdLargestAtomicInteger	Char
ProdLargestAtomicFloat	Float
ProdIntDivRoundTo	Zero
ProdEndianess	LittleEndian
ProdWordSize	64
ProdShiftRightIntArith	on
ProdLongLongMode	off
ProdHWDeviceType	Intel->x86-64 (Windows64)
TargetBitPerChar	8
TargetBitPerShort	16
TargetBitPerInt	32
TargetBitPerLong	32
TargetBitPerLongLong	64
TargetBitPerFloat	32
TargetBitPerDouble	64
TargetBitPerPointer	32
TargetBitPerSizeT	32
TargetBitPerPtrDiffT	32
TargetLargestAtomicInteger	Char
TargetLargestAtomicFloat	None
TargetShiftRightIntArith	on
TargetLongLongMode	off
TargetIntDivRoundTo	Undefined
TargetEndianess	Unspecified
TargetWordSize	32
TargetTypeEmulationWarnSuppressLevel	0
TargetPreprocMaxBitsSint	32
TargetPreprocMaxBitsUint	32
TargetHWDeviceType	Specified
TargetUnknown	off
ProdEqTarget	on
UseEmbeddedCoderFeatures	on
UseSimulinkCoderFeatures	on

Table 6.7. self_balancing_robot Configuration Set.Components [12](6)

Property	Value
Name	Model Referencing
Description	
Components	
UpdateModelReferenceTargets	IfOutOfDateOrStructuralChange
SkipRefExpFcnMdlSchedulingOrderCheck	off
EnableRefExpFcnMdlSchedulingChecks	on
CheckModelReferenceTargetMessage	error
EnableParallelModelReferenceBuilds	off
ParallelModelReferenceErrorOnInvalidPool	on
ParallelModelReferenceMATLABWorkerI- nit	None
ModelReferenceNumInstancesAllowed	Multi
PropagateVarSize	Infer from blocks in model
ModelDependencies	
Model Reference Pass Root Inputs By Reference	on
ModelReferenceMinAlgLoopOccurrences	off
PropagateSignalLabelsOutOfModel	on
SupportModelReferenceSimTargetCustom-Code	off

Table 6.8. self_balancing_robot Configuration Set.Components [12](7)

Property	Value
Name	Simulation Target
Description	
Components	
SimCustomSourceCode	
SimCustomHeaderCode	
SimCustomInitializer	
SimCustomTerminator	
SimReservedNameArray	
SimUserSources	
SimUserIncludeDirs	
SimUserLibraries	

SimUserDefines	
SFSimEnableDebug	off
SFSimOverflowDetection	on
SFSimEcho	on
SimBlas	on
SimCtrlC	on
SimExtrinsic	on
SimIntegrity	on
SimUseLocalCustomCode	off
SimParseCustomCode	on
SimBuildMode	sf_incremental_build
SimDataInitializer	
SimGenImportedTypeDefs	off
CompileTimeRecursionLimit	50
EnableRuntimeRecursion	on
MATLABDynamicMemAlloc	on
MATLABDynamicMemAllocThreshold	65536
CustomSymbolStrEMXArray	nothing
CustomSymbolStrEMXArrayFcn	nothing

Table 6.9. self_balancing_robot Configuration Set.Components [12](8)

Property	Value
Name	Code Generation
SystemTargetFile	grt.tlc
HardwareBoard	None
TLCOptions	
CodeGenDirectory	
GenCodeOnly	off
MakeCommand	make_rtw
GenerateMakefile	on
PackageGeneratedCodeAndArtifacts	off
PackageName	
TemplateMakefile	grt_default_tmf
PostCodeGenCommand	
Description	
GenerateReport	off
SaveLog	off
RTWVerbose	on

RetainRTWFile	off
ProfileTLC	off
TLCDebug	off
TLCCoverage	off
TLCAssert	off
ProcessScriptMode	Default
ConfigurationMode	Optimized
ProcessScript	
ConfigurationScript	
ConfigAtBuild	off
RTWUseLocalCustomCode	off
RTWUseSimCustomCode	off
CustomSourceCode	
CustomHeaderCode	
CustomInclude	
CustomSource	
CustomLibrary	
CustomDefine	
CustomLAPACKCallback	
CustomInitializer	
CustomTerminator	
Toolchain	Automatically locate an installed toolchain
BuildConfiguration	Faster Builds
CustomToolchainOptions	
IncludeHyperlinkInReport	off
LaunchReport	off
RecursionLimit	50
PortableWordSizes	off
GenerateErtSFunction	off
CreateSILPILBlock	None
CodeExecutionProfiling	off
CodeExecutionProfileVariable	executionProfile
CodeProfilingSaveOptions	SummaryOnly
CodeProfilingInstrumentation	off
CodeCoverageSettings	self_balancing_robot Configuration Set.Components(8).CodeCoverageSettings [24]
SILDebugging	off
TargetLang	С
IncludeERTFirstTime	off

GenerateTraceInfo	off
GenerateTraceReport	off
GenerateTraceReportSl	off
GenerateTraceReportSf	off
GenerateTraceReportEml	off
GenerateCodeInfo	off
GenerateWebview	off
GenerateCodeMetricsReport	off
GenerateCodeReplacementReport	off
RTWCompilerOptimization	off
ObjectivePriorities	
RTWCustomCompilerOptimizations	
CheckMdlBeforeBuild	Off
CustomRebuildMode	OnUpdate
DataInitializer	
Components	[self_balancing_robot Configuration Set.Components(8).Components(1) [25], selfbalancing_robot Configuration Set.Components(8).Components(2) [26]]

Table 6.10. self_balancing_robot Configuration Set.Components [12](9)

Property	Value
Description	Simulink Coverage Configuration Component
Components	
Name	Simulink Coverage
CovEnable	off
CovScope	EntireSystem
CovIncludeTopModel	on
RecordCoverage	off
CovPath	/
CovSaveName	covdata
CovCompData	
CovMetricSettings	dwe
CovFilter	
CovHTMLOptions	
CovNameIncrementing	off
CovHtmlReporting	off
CovForceBlockReductionOff	on

CovSaveCumulativeToWorkspaceVar off CovSaveSingleToWorkspaceVar off CovCumulativeVarName covCumulativeData CovCumulativeReport off CovSaveOutputData on CovOutputDir slcov_output/\$ModelName\$ CovDataFileName \$ModelName\$_cvdata CovShowResultsExplorer on CovReportOnPause on CovModelRefEnable off CovModelRefExcluded CovExternalEMLEnable on CovSFonEnable on CovSoundaryAbsTol 1.0000e-05 CovBoundaryRelTol 0.0100 CovUseTimeInterval off CovStoyTime 0 CovStoyTime CovMotricStructuralLevel Decision CovMetricSignalRange off CovMetricSignalRange off CovMetricSignalSize off CovMetricSignalSize off CovMetricSqualSize off CovMetricSaturateOnIntegerOverflow off CovLogicBlockShortCircuit off CovUsignipInteResults off CovMetchOde Masking	CovEnableCumulative	on
CovCumulativeVarName covCumulativeData CovCumulativeReport off CovSaveOutputData on CovOutputDir slcov_output/\$ModelName\$ CovDataFileName \$ModelName\$_cvdata CovShowResultsExplorer on CovReportOnPause on CovModelRefEnable off CovModelRefExcluded CovExternalEMLEnable on CovSFonEnable on CovSopondaryAbsTol 1.0000e-05 CovBoundaryRelTol 0.0100 CovUseTimeInterval off CovStopTime 0 CovStopTime 0 CovMetricStructuralLevel Decision CovMetricSignalRange off CovMetricSignalRange off CovMetricSignalSize off CovMetricSaturateOnIntegerOverflow off CovMetricRelationalBoundary off CovLogicBlockShortCircuit off CovUnsupportedBlockWarning on CovHighlightResults off	CovSaveCumulativeToWorkspaceVar	off
CovCumulativeReport off CovSaveOutputData on CovOutputDir slcov_output/\$ModelName\$ CovDataFileName \$ModelName\$_cvdata CovShowResultsExplorer on CovReportOnPause on CovModelRefEnable off CovModelRefExcluded CovExternalEMLEnable on CovSFonEnable on CovSFonEnable on CovBoundaryAbsTol 1.0000e-05 CovBoundaryRelTol 0.0100 CovUseTimeInterval off CovStartTime 0 CovStopTime 0 CovStopTime 0 CovMetricStructuralLevel Decision CovMetricSignalRange off CovMetricSignalRange off CovMetricSignalSize off CovMetricSaturateOnIntegerOverflow off CovMetricRelationalBoundary off CovLogicBlockShortCircuit off CovUnsupportedBlockWarning on CovHighlightResults off	CovSaveSingleToWorkspaceVar	off
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CovReportOnPause on CovModelRefEnable off CovModelRefExcluded CovExternalEMLEnable on CovSFcnEnable on CovBoundaryAbsTol 1.0000e-05 CovBoundaryRelTol 0.0100 CovUseTimeInterval off CovStartTime 0 CovStopTime 0 CovMetricStructuralLevel Decision CovMetricSignalRange off CovMetricSignalRange off CovMetricSignalSize off CovMetricObjectiveConstraint off CovMetricRelationalBoundary off CovUosuspportedBlockWarning on CovHighlightResults	CovDataFileName	\$ModelName\$_cvdata
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CovUseTimeInterval off CovStartTime 0 CovStopTime 0 CovMetricStructuralLevel Decision CovMetricLookupTable off CovMetricSignalRange off CovMetricSignalSize off CovMetricObjectiveConstraint off CovMetricSaturateOnIntegerOverflow off CovMetricRelationalBoundary off CovLogicBlockShortCircuit off CovUnsupportedBlockWarning on CovHighlightResults off	CovBoundaryAbsTol	1.0000e-05
CovStartTime 0 CovStopTime 0 CovMetricStructuralLevel Decision CovMetricLookupTable off CovMetricSignalRange off CovMetricSignalSize off CovMetricObjectiveConstraint off CovMetricSaturateOnIntegerOverflow off CovMetricRelationalBoundary off CovLogicBlockShortCircuit off CovUnsupportedBlockWarning on CovHighlightResults off	CovBoundaryRelTol	0.0100
CovStopTime 0 CovMetricStructuralLevel Decision CovMetricLookupTable off CovMetricSignalRange off CovMetricSignalSize off CovMetricObjectiveConstraint off CovMetricSaturateOnIntegerOverflow off CovMetricRelationalBoundary off CovLogicBlockShortCircuit off CovUnsupportedBlockWarning on CovHighlightResults off	CovUseTimeInterval	off
CovMetricStructuralLevel Decision CovMetricLookupTable off CovMetricSignalRange off CovMetricSignalSize off CovMetricObjectiveConstraint off CovMetricSaturateOnIntegerOverflow off CovMetricRelationalBoundary off CovLogicBlockShortCircuit off CovUnsupportedBlockWarning on CovHighlightResults off	CovStartTime	0
CovMetricLookupTable off CovMetricSignalRange off CovMetricSignalSize off CovMetricObjectiveConstraint off CovMetricSaturateOnIntegerOverflow off CovMetricRelationalBoundary off CovLogicBlockShortCircuit off CovUnsupportedBlockWarning on CovHighlightResults off	CovStopTime	0
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CovMetricSignalSize off CovMetricObjectiveConstraint off CovMetricSaturateOnIntegerOverflow off CovMetricRelationalBoundary off CovLogicBlockShortCircuit off CovUnsupportedBlockWarning on CovHighlightResults off	CovMetricLookupTable	off
CovMetricObjectiveConstraint off CovMetricSaturateOnIntegerOverflow off CovMetricRelationalBoundary off CovLogicBlockShortCircuit off CovUnsupportedBlockWarning on CovHighlightResults off	CovMetricSignalRange	off
CovMetricSaturateOnIntegerOverflow off CovMetricRelationalBoundary off CovLogicBlockShortCircuit off CovUnsupportedBlockWarning on CovHighlightResults off	CovMetricSignalSize	off
CovMetricRelationalBoundary off CovLogicBlockShortCircuit off CovUnsupportedBlockWarning on CovHighlightResults off	CovMetricObjectiveConstraint	off
CovLogicBlockShortCircuit off CovUnsupportedBlockWarning on CovHighlightResults off	CovMetricSaturateOnIntegerOverflow	off
CovUnsupportedBlockWarning on CovHighlightResults off	CovMetricRelationalBoundary	off
CovHighlightResults off	CovLogicBlockShortCircuit	off
	CovUnsupportedBlockWarning	on
CovMcdcMode Masking	CovHighlightResults	off
	CovMcdcMode	Masking

Table 6.11. self_balancing_robot Configuration Set.Components [12](10)

Property	Value
Description	HDL Coder custom configuration component
Components	
Name	HDL Coder

Table 6.12. self_balancing_robot Configuration Set.Components(8) [21].CodeCoverageSettings

Property	Value
TopModelCoverage	off
ReferencedModelCoverage	off
CoverageTool	None

Table 6.13. self_balancing_robot Configuration Set.Components(8).Components [23](1)

Property	Value
Name	Code Appearance
Description	
Components	
ForceParamTrailComments	off
GenerateComments	on
CommentStyle	Auto
IgnoreCustomStorageClasses	on
IgnoreTestpoints	off
IncHierarchyInIds	off
MaxIdLength	31
PreserveName	off
PreserveNameWithParent	off
ShowEliminatedStatement	off
OperatorAnnotations	off
IncAutoGenComments	off
SimulinkDataObjDesc	off
SFDataObjDesc	off
MATLABFcnDesc	off
IncDataTypeInIds	off
PrefixModelToSubsysFcnNames	on
MangleLength	1
CustomSymbolStr	\$R\$N\$M
CustomSymbolStrGlobalVar	\$R\$N\$M
CustomSymbolStrType	\$N\$R\$M_T
CustomSymbolStrField	\$N\$M
CustomSymbolStrFcn	\$R\$N\$M\$F
CustomSymbolStrSimulinkFcn	\$R\$N
CustomSymbolStrFcnArg	rt\$I\$N\$M
CustomSymbolStrBlkIO	rtb_\$N\$M

CustomSymbolStrTmpVar	\$N\$M
CustomSymbolStrMacro	\$R\$N\$M
CustomSymbolStrUtil	\$N\$C
CustomSymbolStrEmxType	emxArray_\$M\$N
CustomSymbolStrEmxFcn	emx\$M\$N
CustomUserTokenString	
CustomCommentsFcn	
DefineNamingRule	None
DefineNamingFcn	
ParamNamingRule	None
ParamNamingFcn	
SignalNamingRule	None
SignalNamingFcn	
InsertBlockDesc	off
InsertPolySpaceComments	off
SimulinkBlockComments	on
MATLABSourceComments	off
EnableCustomComments	off
InternalIdentifier	Shortened
InlinedPrmAccess	Literals
ReqsInCode	off
UseSimReservedNames	off
ReservedNameArray	

Table 6.14. self_balancing_robot Configuration Set.Components(8).Components [23](2)

Property	Value
Name	Target
Description	
Components	
IsERTTarget	off
TargetFcnLib	ansi_tfl_table_tmw.mat
TargetLibSuffix	
TargetPreCompLibLocation	
GenFloatMathFcnCalls	NOT IN USE
TargetLangStandard	C99 (ISO)
TargetFunctionLibrary	NOT IN USE
CodeReplacementLibrary	None
UtilityFuncGeneration	Auto

ERTMultiwordTypeDef	System defined
MultiwordTypeDef	System defined
ERTMultiwordLength	2048
MultiwordLength	2048
GenerateFullHeader	on
InferredTypesCompatibility	off
ExistingSharedCode	
GenerateSampleERTMain	off
GenerateTestInterfaces	off
ModelReferenceCompliant	on
ParMdlRefBuildCompliant	on
CompOptLevelCompliant	on
ConcurrentExecutionCompliant	on
IncludeMdlTerminateFcn	on
CombineOutputUpdateFcns	on
CombineSignalStateStructs	off
SuppressErrorStatus	off
ERTFirstTimeCompliant	off
IncludeFileDelimiter	Auto
ERTCustomFileBanners	off
SupportAbsoluteTime	on
LogVarNameModifier	rt_
MatFileLogging	on
MultiInstanceERTCode	off
CodeInterfacePackaging	Nonreusable function
SupportNonFinite	on
SupportComplex	on
PurelyIntegerCode	off
SupportContinuousTime	on
SupportNonInlinedSFcns	on
RemoveDisableFunc	off
RemoveResetFunc	off
SupportVariableSizeSignals	off
ParenthesesLevel	Nominal
CastingMode	Nominal
GenerateClassInterface	off
ModelStepFunctionPrototypeControlCompliant	off
CPPClassGenCompliant	on

GRTInterface	off
GenerateAllocFcn	off
UseToolchainInfoCompliant	on
GenerateSharedConstants	on
ExtMode	off
ExtModeStaticAlloc	off
ExtModeTesting	off
ExtModeStaticAllocSize	1000000
ExtModeTransport	0
ExtModeMexFile	ext_comm
ExtModeMexArgs	
ExtModeIntrfLevel	Level1
RTWCAPISignals	off
RTWCAPIParams	off
RTWCAPIStates	off
RTWCAPIRootIO	off
GenerateASAP2	off
MultiInstanceErrorCode	Error

Table 6.15. HDL Coder

Property	Value
HDLSubsystem	self_balancing_robot
Workflow	Generic ASIC/FPGA
TargetPlatform	
ReferenceDesign	
ReferenceDesignPath	
CoeffPrefix	coeff
InputType	std_logic_vector
OutputType	Same as input type
ScalarizePorts	off
CoeffMultipliers	Multiplier
ResetType	Asynchronous
FIRAdderStyle	linear
MultiplierInputPipeline	0
MultiplierOutputPipeline	0
FoldingFactor	1
NumMultipliers	-1
OptimizeForHDL	off
TimingControllerPostfix	_tc

TimingControllerArch CastBeforeSum On CheckHDL Off EnablePrefix enb ClockEnableInputPort ClockEnableOutputPort ClockEnableOutputPort ClockEnableOutputPort ClockEdge Rising ResetInputPort reset SimulatorFlags HDLCompileFilePostfix HDLCompileTerm HDLCompileVerilogCmd HDLCompileVHDLCmd EnableForGenerateLoops HDLMapFilePostfix Lmap.txt HDLMapSeparator HDLSimCmd HDLSimProjectFilePostfix Jinit.do HDLSimProjectCmd HDL
CheckHDL off EnablePrefix enb ClockEnableInputPort clk_enable ClockEnableOutputPort ce_out ClockInputPort clk ClockEdge Rising ResetInputPort reset SimulatorFlags HDLCompileFilePostfixcompile.do HDLCompileInit vlib %s\n HDLCompileVerilogCmd vlog %s %s\n HDLCompileVerilogCmd vcom %s %s\n EnableForGenerateLoops on HDLMapFilePostfixmap.txt HDLMapSeparator HDLSimCmd vsim -novopt %s.%s\n HDLSimProjectFilePostfixinit.do HDLSimProjectCmd project addfile %s\n HDLSimProjectTerm project new . %s work\n HDLSimProjectInit project new . %s work\n HDLSimProlieNewWaveCmd add wave sim:%s\n HDLSimViewWaveCmd add wave sim:%s\n HDLSimViewWaveCmd HDLSimViewWaveCmd HDLSimViewWaveCmd Idk enable Ce_out Clk_enable Clk_enable Ce_out Clk_enable Clk_enable Clk_enable Clk_enable Ce_out Clk_enable ClockEde Clk_enable Clk_enable Clk_enable Clk_enable Clk_enable Clk Clk_enable C
EnablePrefix ClockEnableInputPort ClockEnableOutputPort ClockInputPort ClockInputPort ClockInputPort ClockInputPort ClockInputPort ClockEdge Rising ResetInputPort reset SimulatorFlags HDLCompileFilePostfix Loompile.do HDLCompileInit Vlib %s\n HDLCompileTerm HDLCompileVerilogCmd Vlog %s %s\n HDLCompileVerllogCmd Vcom %s %s\n EnableForGenerateLoops On HDLMapFilePostfix Lmap.txt HDLMapSeparator HDLSimCmd HDLSimProjectFilePostfix Linit.do HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectTerm HDLSimProjectInit
ClockEnableInputPort ClockEnableOutputPort ClockInputPort ClockInputPort ClockEdge Rising ResetInputPort reset SimulatorFlags HDLCompileFilePostfix HDLCompileInit HDLCompileTerm HDLCompileVerilogCmd HDLCompileVerilogCmd HDLCompileVerilogCmd HDLMapFilePostfix Jmap.txt HDLMapSeparator HDLSimCmd HDLSimFilePostfix Jsim.do HDLSimProjectFilePostfix Jinit.do HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectTerm HDLSimProjectTerm HDLSimProjectTerm HDLSimProjectTerm HDLSimProjectTerm HDLSimProjectInit HDLSimProjectInit HDLSimTerm HDLSimTerm In Jallyn HDLSimViewWaveCmd HDLSimViewWaveCmd HDLSimViewWaveCmd HDLSimViewWaveCmd HDLSimViewWaveCmd HDLSynthTool None
ClockEnableOutputPort ce_out ClockInputPort clk ClockEdge Rising ResetInputPort reset SimulatorFlags HDLCompileFilePostfixcompile.do HDLCompileInit vlib %s\n HDLCompileVerilogCmd vlog %s %s\n HDLCompileVerilogCmd vcom %s %s\n HDLCompileVHDLCmd vcom %s %s\n HDLMapFilePostfixmap.txt HDLMapFilePostfixmap.txt HDLMapSeparator HDLSimCmd vsim -novopt %s.%s\n HDLSimFilePostfixsim.do HDLSimProjectFilePostfixinit.do HDLSimProjectCmd project addfile %s\n HDLSimProjectTerm project compileall\n HDLSimProjectInit project new . %s work\n HDLSimTerm run -all\n HDLSimViewWaveCmd add wave sim:%s\n HDLSynthTool
ClockInputPort ClockEdge Rising ResetInputPort reset SimulatorFlags HDLCompileFilePostfix Lcompile.do HDLCompileInit HDLCompileTerm HDLCompileVerilogCmd HDLCompileVerilogCmd HDLCompileVerilogCmd HDLCompileVerilogCmd HDLMapFilePostfix Lmap.txt HDLMapFilePostfix HDLMapSeparator HDLSimCmd HDLSimFilePostfix Lsim.do HDLSimProjectFilePostfix HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectTerm HDLSimProjectInit HDLSimProjectInit HDLSimProjectInit HDLSimProjectInit HDLSimProjectInit HDLSimViewWaveCmd HDLSimViewWaveCmd HDLSimViewWaveCmd HDLSynthTool None
ClockEdge Rising ResetInputPort reset SimulatorFlags HDLCompileFilePostfixcompile.do HDLCompileInit vlib %s\n HDLCompileVerilogCmd vlog %s %s\n HDLCompileVHDLCmd vcom %s %s\n EnableForGenerateLoops on HDLMapFilePostfixmap.txt HDLMapSeparator HDLSimCmd vsim -novopt %s.%s\n HDLSimFilePostfixinit.do HDLSimProjectFilePostfixinit.do HDLSimProjectCmd project addfile %s\n HDLSimProjectTerm project compileall\n HDLSimProjectInit project new . %s work\n HDLSimTerm run -all\n HDLSimViewWaveCmd add wave sim:%s\n HDLSynthTool None
ResetInputPort SimulatorFlags HDLCompileFilePostfix Lcompile.do HDLCompileInit HDLCompileTerm HDLCompileVerilogCmd HDLCompileVHDLCmd EnableForGenerateLoops HDLMapFilePostfix Lmap.txt HDLMapSeparator HDLSimCmd HDLSimFilePostfix Lsim.do HDLSimProjectFilePostfix HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectTerm HDLSimProjectInit HDLSimViewWaveCmd HDLSimViewWaveCmd HDLSynthTool
SimulatorFlags HDLCompileFilePostfix compile.do HDLCompileInit HDLCompileTerm HDLCompileVerilogCmd HDLCompileVHDLCmd EnableForGenerateLoops HDLMapFilePostfix HDLMapSeparator HDLSimCmd HDLSimFilePostfix sim.do HDLSimFilePostfix init.do HDLSimProjectFilePostfix HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectTerm HDLSimProjectInit HDLSimProjectInit HDLSimProjectInit HDLSimViewWaveCmd HDLSimViewWaveCmd HDLSynthTool None
HDLCompileFilePostfix
HDLCompileInit HDLCompileVerilogCmd HDLCompileVerilogCmd HDLCompileVHDLCmd vcom %s %s\n EnableForGenerateLoops HDLMapFilePostfix HDLSimCmd HDLSimFilePostfix Lsim.do HDLSimProjectFilePostfix HDLSimInit HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectTerm HDLSimProjectInit HDLSimProjectInit HDLSimTerm HDLSimViewWaveCmd HDLSimViewWaveCmd HDLSynthTool voom %s %s\n Lmap.txt Lmap.txt Lmap.txt Linit.do vsim -novopt %s.%s\n Lsim.do project %s.%s\n project addfile %s\n project addfile %s\n project compileall\n Project new . %s work\n HDLSimProjectInit HDLSimViewWaveCmd HDLSimViewWaveCmd HDLSynthTool None
HDLCompileTerm HDLCompileVerilogCmd Vlog %s %s\n HDLCompileVHDLCmd vcom %s %s\n EnableForGenerateLoops on HDLMapFilePostfix _map.txt HDLSimCmd HDLSimFilePostfix _sim.do HDLSimProjectFilePostfix _init.do HDLSimInit HDLSimProjectCmd HDLSimProjectCmd HDLSimProjectTerm HDLSimProjectTerm HDLSimProjectInit HDLSimProjectInit HDLSimTerm run -all\n HDLSimViewWaveCmd HDLSynthTool None
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HDLCompileVHDLCmd vcom %s %s\n EnableForGenerateLoops on HDLMapFilePostfix _map.txt HDLMapSeparator HDLSimCmd vsim -novopt %s.%s\n HDLSimFilePostfix _sim.do HDLSimProjectFilePostfix _init.do HDLSimInit onbreak resume\nonerror resume\n HDLSimProjectCmd project addfile %s\n HDLSimProjectTerm project compileall\n HDLSimProjectInit project new . %s work\n HDLSimTerm run -all\n HDLSimViewWaveCmd add wave sim:%s\n HDLSynthTool None
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HDLMapFilePostfixmap.txt HDLMapSeparator HDLSimCmd
HDLSimCmd vsim -novopt %s.%s\n HDLSimFilePostfix _sim.do HDLSimProjectFilePostfix _init.do HDLSimInit onbreak resume\nonerror resume\n HDLSimProjectCmd project addfile %s\n HDLSimProjectTerm project compileall\n HDLSimProjectInit project new . %s work\n HDLSimTerm run -all\n HDLSimViewWaveCmd add wave sim:%s\n HDLSynthTool None
HDLSimCmd vsim -novopt %s.%s\n HDLSimFilePostfix _sim.do HDLSimProjectFilePostfix _init.do HDLSimInit onbreak resume\nonerror resume\n HDLSimProjectCmd project addfile %s\n HDLSimProjectTerm project compileall\n HDLSimProjectInit project new . %s work\n HDLSimTerm run -all\n HDLSimViewWaveCmd add wave sim:%s\n HDLSynthTool None
HDLSimFilePostfix _sim.do HDLSimProjectFilePostfix _init.do HDLSimInit onbreak resume\nonerror resume\n HDLSimProjectCmd project addfile %s\n HDLSimProjectTerm project compileall\n HDLSimProjectInit project new . %s work\n HDLSimTerm run -all\n HDLSimViewWaveCmd add wave sim:%s\n HDLSynthTool None
HDLSimProjectFilePostfixinit.do HDLSimInit onbreak resume\nonerror resume\n HDLSimProjectCmd project addfile %s\n HDLSimProjectTerm project compileall\n HDLSimProjectInit project new . %s work\n HDLSimTerm run -all\n HDLSimViewWaveCmd add wave sim:%s\n HDLSynthTool None
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HDLSimProjectCmd project addfile %s\n HDLSimProjectTerm project compileall\n HDLSimProjectInit project new . %s work\n HDLSimTerm run -all\n HDLSimViewWaveCmd add wave sim:%s\n HDLSynthTool None
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HDLSynthFilePostfix
HDLSynthInit
HDLSynthLibCmd
HDLSynthLibSpec
HDLSynthTerm
ReservedWordPostfix _rsvd
BlockGenerateLabel _gen
VHDLLibraryName work
UseSingleLibrary off

VHDLArchitectureName	rtl
ClockProcessPostfix	_process
ComplexImagPostfix	_im
ComplexRealPostfix	_re
EntityConflictPostfix	_block
InstancePrefix	u_
InstancePostfix	
InstanceGenerateLabel	_gen
OutputGenerateLabel	outputgen
PackagePostfix	_pkg
SplitEntityArch	off
SplitEntityFilePostfix	_entity
SplitArchFilePostfix	_arch
VectorPrefix	vector_of_
ClockInputs	Single
TriggerAsClock	off
ConditionalizePipeline	off
InferControlPorts	off
UseRisingEdge	off
TargetDirectory	hdlsrc
TargetSubdirectory	Model
EDAScriptGeneration	on
HDLControlFiles	
AddInputRegister	on
AddOutputRegister	on
AddPipelineRegisters	off
PipelinePostfix	_pipe
InputPort	filter_in
OutputPort	filter_out
FracDelayPort	filter_fd
Name	filter
RemoveResetFrom	None
ResetAssertedLevel	Active-high
ReuseAccum	off
ScaleWarnBits	3
SerialPartition	-1
DALUTPartition	-1
DARadix	2
CoefficientSource	Internal

InputComplex AddRatePort off AddRatePort off InputDataType GenerateHDLCode on GenerateModel on GenerateTB off GenerateCEGenModel off Traceability off ResourceReport off OptimizationReport off IPCoreReport off IPCoreReport off Recommendations off RequirementComments on Backannotation off HierarchicalDistPipelining off PreserveDesignDelays off ClockRatePipelining off IncreaseCRPBudget off AdaptivePipelining on ClockRatePipelining off Optimizeserializer on shareequalwl on shareequalwl on shareequalwl on shareetmusetimated off NumCriticalPathEstimated 1 CriticalPathEstimated 1 CriticalPathEstimation File highlightFeedbackLoop HighlightFeedbackLoops on HighlightFeedbackLoops on HighlightClockRatePipeliningPile highlightClockRatePipeliningDiagnostic HighlightClockRatePipeliningCharatriers on HighlightClockRatePipeliningDiagnostic HighlightClockRatePipeliningDiagnostic HighlightClockRatePipeliningFile highlightClockRatePipeliningDistributedPipeliningDiagnostic	CoefficientMemory	Registers
InputDataType GenerateHDLCode GenerateModel GenerateTB Off GenerateCEGenModel Traceability Off Traceability Off OptimizationReport OptimizationReport Off ErrorCheckReport Off IPCoreReport Off IPCoreReport Off Recommendations Off RequirementComments On Backannotation Off HierarchicalDistPipelining Off ClockRatePipelining Off IncreaseCRPBudget AdaptivePipelining Off CriticalPathestimation Off Optimizeserializer On Shareequalwl On Shareequalwl On Sharedmulsign On Signed MultiplierPromotionThreshold OrbiticalPathestimated IncreaseCRPBudingCharacterizationFile HighlightFeedbackLoops HighlightFeedbackLoops HighlightClockRatePipeliningCharacteripelining On HighlightClockRatePipelining On On HighlightFeedbackLoops HighlightClockRatePipeliningCharacteripelining On HighlightClockRatePipeliningCharacteripeliningDiagnostic HighlightClockRatePipeliningDiagnostic HighlightClockRatePipeliningDiagnostic HighlightClockRatePipeliningDiagnostic HighlightClockRatePipeliningFile highlightClockRatePipeliningFile	InputComplex	off
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GenerateCEGenModel Traceability Off ResourceReport Off OptimizationReport Off ErrorCheckReport On HDLGenerateWebview Off Recommendations Off RequirementComments On Backannotation Off HierarchicalDistPipelining Off PreserveDesignDelays Off ClockRatePipelining Off IncreaseCRPBudget AdaptivePipelining Off CriticalPathEstimation Off Optimizeserializer Shareequalwl Shareequalwl Shareequalwl Shareedmulsign MultiplierPromotionThreshold RoutingFudgeFactor OptimizationCompatibilityCheck Off NumCriticalPathEstimated 1 CriticalPathEstimated HardwarePipeliningCharacterizationFile HighlightFeedbackLoops On HighlightFeedbackLoops HighlightFeedbackLoop HighlightFeedbackLoop HighlightClockRatePipeliningFile highlightClockRatePipeliningFile highlightClockRatePipeliningFile	GenerateModel	on
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SynthesisToolSpeedValue	SynthesisToolDeviceName	
	SynthesisToolPackageName	
SynthesisTool	SynthesisToolSpeedValue	
	SynthesisTool	

SynthesisProjectAdditionalFiles	
SimulationLibPath	
XilinxSimulatorLibPath	
AdderSharingMinimumBitwidth	0
MultiplierSharingMinimumBitwidth	0
MultiplyAddSharingMinimumBitwidth	0
ShareAdders	off
ShareMultipliers	on
ShareMultiplyAdds	on
ShareMATLABBlocks	on
ShareAtomicSubsystems	on
ShareFloatingPointIPs	on
PipelinedSharing	on
OptimizeCRPSharingRegisters	off
ClockRatePipeliningBudgetCheck	off
EnableFPGAWorkflow	off
FPGAWorkflowParameters	
GainMultipliers	Multiplier
ProductOfElementsStyle	linear
UserComment	
DateComment	on
SafeZeroConcat	on
SumOfElementsStyle	linear
TargetLanguage	VHDL
Oversampling	1
ClockRatePipeliningFraction	1
Verbosity	1
TestBenchName	filter_tb
MultifileTestBench	off
IgnoreDataChecking	0
TestBenchPostfix	_tb
TestBenchDataPostfix	_data
TestBenchStimulus	
TestBenchUserStimulus	
TestBenchFracDelayStimulus	
TestBenchCoeffStimulus	
TestBenchRateStimulus	
ForceClockEnable	on
MinimizeClockEnables	off

NoResetInitializationMode Script NoResetInitScript noresetinitScript.cl ComplexMulElaboration MultiplyAddBlock FlattenBus off TestBenchClockEnableDelay 1 ForceClock on ClockHighTime 5 ClockLowTime 5 HoldTime 2 InputDataInterval 0 ForceReset on ErrorMargin 4 HoldInputDataBetweenSamples on InitializeTestBenchInputs off ResetLength 2 TestBencReferencePostFix _ref GenerateValidationModel off RAMMappingThreshold 256 MapPipelineDelaysToRAM off RemoveRedundantCounters on ReplaceUnitDelayWithIntegerDelay on ConcatenateDelays on MergeDelaysToConstant on RAMArchitecture WithClockEnable InlineHDLCode off MaskParameterAsGeneric off BalanceDelays <th>MinimizeGlobalResets</th> <th>off</th>	MinimizeGlobalResets	off
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ExtraEffortMargin 1 MaxOversampling Inf MaxComputationLatency 1 MultiplierPartitioningThreshold Inf TreatDelayBalancingFailureAs Error TransformNonZeroInitValDelay on DelayElaborationLimit 20	BalanceDelays	on
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TransformNonZeroInitValDelay on DelayElaborationLimit 20	MultiplierPartitioningThreshold	Inf
DelayElaborationLimit 20	TreatDelayBalancingFailureAs	Error
	TransformNonZeroInitValDelay	on
GenerateCoSimBlock off	DelayElaborationLimit	20
	GenerateCoSimBlock	off

HDLCodeCoverage	off
GenerateHDLTestBench	on
GenerateCoSimModel	None
GenerateSVDPITestBench	None
SimulationTool	Mentor Graphics Modelsim
CoSimModelSetup	CosimBlockAndDut
SynthesisOnDirective	
SynthesisOffDirective	
LoopUnrolling	off
InlineConfigurations	on
UseAggregatesForConst	off
UseVerilogTimescale	on
VerilogFileExtension	.v
SystemVerilogFileExtension	.sv
VHDLFileExtension	.vhd
CodeGenerationOutput	GenerateHDLCode
GeneratedModelName	
GeneratedModelNamePrefix	gm_
UseDotLayout	off
ShowCodeGenPIR	off
SerializeModel	0
SerializeIO	0
UseSLAutoRoute	on
UseAutoPlace	on
HighlightAncestors	on
HighlightColor	cyan
InitializeBlockRAM	on
InitializeRealPort	off
MapVectorPortToStream	off
UseFileIOInTestBench	on
TurnkeyWorkflow	off
AlteraWorkflow	off
GenerateFILBlock	off
CoSimLibPostfix	_cosim
TestBenchInitializeInputs	off
MinimizeIntermediateSignals	off
GenerateCodeInfo	off
GatewayoutWithDTC	off
IncrementalCodeGenForTopModel	off

System Model Configuration

HDLWFSmartbuild	on
HDLCodingStandard	None
HDLCodingStandardCustomizations	
ReferenceDesignParameter	
HDLLintTool	None
HDLLintInit	
HDLLintTerm	
HDLLintCmd	
ModulePrefix	
DetectBlackBoxNameCollision	Warning
PIRTB	on
PIRTC	off
EmitNetlist	off
UsePipelinedToolboxFunctions	on
savepirtoscript	off
ConcatenateHDLModules	off
AMS	off

Chapter 7. Glossary

Atomic Subsystem. A subsystem treated as a unit by an implementation of the design documented in this report. The implementation computes the outputs of all the blocks in the atomic subsystem before computing the next block in the parent system's block execution order (sorted list).

Block Diagram. A Simulink block diagram represents a set of simultaneous equations that relate a system or subsystem's inputs to its outputs as a function of time. Each block in the diagram represents an equation of the form y = f(t, x, u) where t is the current time, u is a block input, y is a block output, and x is a system state (see the Simulink documentation for information on the functions represented by the various types of blocks that make up the diagram). Lines connecting the blocks represent dependencies among the blocks, i.e., inputs whose current values are the outputs of other blocks. An implementation of a design described in this document computes a root or atomic system's outputs at each time step by computing the outputs of the blocks in an order determined by block input/output dependencies.

Block Parameter. A variable that determines the output of a block along with its inputs, for example, the gain parameter of a Gain block.

Block Execution Order. The order in which Simulink evaluates blocks during simulation of a model. The block execution order determined by Simulink ensures that a block executes only after all blocks on whose outputs it depends are executed.

Checksum. A number that indicates whether different versions of a model or atomic subsystem differ functionally or only cosmetically. Different checksums for different versions of the same model or subsystem indicate that the versions differ functionally.

Design Variable. A symbolic (MATLAB) variable or expression used as the value of a block parameter. Design variables allow the behavior of the model to be altered by altering the value of the design variable.

Signal. A block output, so-called because block outputs typically vary with time.

Virtual Subsystem. A subsystem that is purely graphical, i.e., is intended to reduce the visual complexity of the block diagram of which it is a subsystem. An implementation of the design treats the blocks in the subsystem as part of the first nonvirtual ancestor of the virtual subsystem (see Atomic Subsystem).

Chapter 8. About this Report

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8.1. Report Overview

This report describes the design of the self_balancing_robot system. The report was generated automatically from a Simulink model used to validate the design. It contains the following sections:

Model Version. Specifies information about the version of the model from which this design description was generated. Includes the model checksum, a number that indicates whether different versions of the model differ functionally or only cosmetically. Different checksums for different versions indicate that the versions differ functionally.

Root System. Describes the design's root system.

Subsystems. Describes each of the design's subsystems.

Design Variables. Describes system design variables, i.e., MATLAB variables and expressions used as block parameter values.

System Model Configuration. Lists the configuration parameters, e.g., start and stop time, of the model used to simulate the system described by this report.

Requirements Traceability. Shows design requirements associated with elements of the design model. This section appears only if the design model contains requirements links.

Glossary. Defines Simulink terms used in this report.

8.2. Root System Description

This section describes a design's root system. It contains the following sections:

Diagram. Simulink block diagram that represents the algorithm used to compute the root system's outputs.

Description. Description of the root system. This section appears only if the model's root system has a Documentation property or a Doc block.

Interface. Name, data type, width, and other properties of the root system's input and output signals. The number of the block port that outputs the signal appears in angle brackets appended to the signal name. This section appears only if the root system has input or output ports.

Blocks. This section has two subsections:

- **Parameters.** Describes key parameters of blocks in the root system. This section also includes graphical and/or tabular representations of lookup table data used by lookup table blocks, i.e., blocks that use lookup tables to compute their outputs.
- **Block Execution Order.** Order in which blocks must be executed at each time step in order to ensure that each block's inputs are available when it executes.

State Charts. Describes state charts used in the root system. This section appears only if the root system contains Stateflow blocks.

8.3. Subsystem Descriptions

This section describes a design's subsystems. Each subsystem description contains the following sections:

Checksum. This section appears only if the subsystem is an atomic subsystem. The checksum indicates whether the version of the model subsystem used to generate this report differs functionally from other versions of the model subsystem. If two model checksums differ, the corresponding versions of the model differ functionally.

Diagram. Simulink block diagram that graphically represents the algorithm used to compute the subsystem's outputs.

Description. Description of the subsystem. This section appears only if the subsystem has a Documentation property or contains a Doc block.

Interface. Name, data type, width, and other properties of the subsystem's input and output signals. The number of the block port that outputs the signal appears in angle brackets appended to the signal name. This section appears only if the subsystem is atomic and has input or output ports.

Blocks. Blocks that this subsystem contains. This section has two subsections:

- Parameters. Key parameters of blocks in the subsystem. This section also includes graphical and/or tabular representations of lookup table data used by lookup table blocks, blocks that use lookup tables to compute their outputs.
- **Block Execution Order.** Order in which the subsystem's blocks must be executed at each time step in order to ensure that each block's inputs are available when the block executes .This section appears only if the subsystem is atomic. Note: in Acrobat(PDF) reports, the number in square brackets next to the block name is a hyperlink to the block parameter table. The number has no model significance.

State Charts. Describes state charts used in the subsystem. This section appears only if the root system contains Stateflow blocks.

8.4. State Chart Descriptions

This section describes the state machines used by Stateflow blocks to compute their outputs, i.e., Stateflow blocks. Each state machine description contains the following sections:

Chart. Diagram representing the state machine.

States. Describes the state machine's states. Each state description includes the state's diagram and diagrams and/or descriptions of graphical functions, Simulink functions, truth tables, and MATLAB functions parented by the state.

Transitions. Transitions between the state machine's states. Each transition description specifies the values of key transition properties. Appears only if a transition has properties that do not appear on the chart.

Junctions. Transition junctions. Each junction description specifies the values of key junction properties. Appears only if a junction has properties that do not appear on the chart.

Events. Events that trigger state transitions. Each event description specifies the values of key event properties.

Data. Data types and other properties of the Stateflow block's inputs, outputs, and other state machine data.

Targets. Executable implementations of the state machine used to compute the outputs of the corresponding Stateflow block.

MATLAB Supporting Functions. List of functions invoked by MATLAB functions defined in the chart.