Drive for better vision

PERC Standard Rule List

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Himax Technologies, Inc.
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PERC INFO Rule List (1/2)

No.	PERC Rule Name	Description
A	INFO.Pwr.Pad	Display user-defined power pads
B	INFO.Gnd.Pad	Display user-defined ground pads
C	INFO.Sig.Pad	Display user-defined signal pads
D	INFO.Int.Port	Display internal ports
E	INFO.APR.Pwr.Pad	Display user-defined APR power pads
F	INFO.APR.Gnd.Pad	Display user-defined APR ground pads
G	INFO.LDO.Pwr.Port	Display user-defined LDO power ports
H	INFO.MOS.Subtype	Display undefined subtypes of MOS, and should be 0 error count
I	INFO.Dio.Subtype	Display undefined subtypes of diode, and should be 0 error count
J	INFO.Cross.Ground	Display cross ground net

PERC INFO Rule List (2/2)

No.	PERC Rule Name	Description
K	INFO.PG.Junct	Collect all power and ground junction pairs
L	INFO.Subckt	The defined third-party sub-circuit are shown in this rule

PERC Chip Level Specifications (1/4)

No.	PERC Rule Name	ASIC	ASIC_LL	TCON	CAD
1	ESD.Rule.1.a	IP only	IP only	IP only	NA
2	ESD.Rule.1.b	IP only	NA	IP only	NA
3	ESD.Rule.1.c	IP only	NA	IP only	NA
4	ESD.Rule.1.c.OU3	NA	NA	NA	NA
5	ESD.R.Btwn.PG.MOS	IP only	IP only	All	NA
6	ESD.R.GGMOS.Gate	IP only	IP only	IP only	NA
7	ESD.Rule.1.2.a	IP only	IP only	IP only	NA
8	ESD.Rule.1.2.b	IP only	IP only	IP only	NA
9	ESD.Rule.1.2.c	NA	NA	NA	NA
10	EOS.LV.Gate.PG	All	All	All	All
11	EOS.MVHV.Gate.PG	All	All	All	NA
12	ESD.Cross.PG.1	IP only	IP only	IP only	NA
13	ESD.Cross.PG.2	IP only	IP only	IP only	NA
14	ESD.Cross.PG.3	NA	NA	NA	NA
15	ESD.Pwr.Cut.Dio	All	NA	NA	NA
16	ESD.Pwr.Clamp	All	All	All	NA
17	ERC.Floating.Gate	All	All	All	All
18	ERC.Floating.Power	All	All	All	NA
19	ERC.Floating.Ground	All	All	All	NA
20	ERC.Bulk.Connect	All	All	All	NA

PERC Chip Level Specifications (2/4)

No.	PERC Rule Name	ASIC	ASIC_LL	TCON	CAD
21	ERC.Cap.Voltage	NA	NA	NA	NA
22	ERC.LVMOS.To.MVHVMOS	All	All	All	NA
23	ERC.MVMOS.To.LVHVMOS	All	All	All	NA
24	ERC.HVMOS.To.LVMVMOS	NA	NA	NA	NA
25	ESD.Decap.Protect	IP only	IP only	IP only	NA
26	ESD.Decap.Connect	IP only	IP only	IP only	NA
27	ESD.Int.GGMOS	IP only	IP only	IP only	NA
28	ERC.Forward.Diode	All	All	All	NA
29	ERC.Forward.PMOS	All	All	All	NA
30	ERC.Forward.NMOS	All	All	All	NA
31	ESD.GGMOS.Width	IP only	IP only	IP only	NA
32	ESD.Cross.PG.APR.1	Chip only	Chip only	Chip only	All
33	ESD.Cross.PG.APR.2	Chip only	Chip only	Chip only	All
34	ESD.Cross.PG.APR.3	NA	NA	NA	All
35	ESD.LV.Decap	All	All	All	NA
36	ESD.LV.Decap.MV.Pwr	All	All	All	NA
37	ESD.Cross.PG.Wo.R	IP only	IP only	IP only	NA
38	ERC.Floating.Port	All	All	All	NA
39	ESD.GGP.LDO	All	All	All	NA
40	ERC.Content	IP only	IP only	IP only	NA

PERC Chip Level Specifications (3/4)

No.	PERC Rule Name	ASIC	ASIC_LL	TCON	CAD
41	ESD.B2B.Diode	All	All	All	NA
42	ESD.R.Sig.200	IP only	IP only	IP only	NA
43	ESD.Cross.PG.UPF	All	All	All	NA
44	ESD.Int.CDM	NA	NA	NA	IP only
45	ESD.Int.CDM.PG	IP only	IP only	IP only	IP only
46	ESD.Int.CDM.Spc	NA	NA	NA	IP only
47	ESD.Int.APR.PG	IP only	IP only	IP only	NA
48	ERC.Subckt.Pin	Chip only	Chip only	Chip only	Chip only
49	ESD.IO.Subtype	IP only	IP only	IP only	NA
50	ESD.IO.PG	All	All	IP only	NA
51	ESD.Cross.PG.LV.1	NA	IP only	NA	NA
52	ESD.Cross.PG.MV.1	NA	IP only	NA	NA
53	ESD.Cross.PG.LV.2	NA	IP only	NA	NA
54	ESD.Cross.PG.MV.2	NA	IP only	NA	NA
55	ESD.CrossPG.LV.3	NA	IP only	NA	NA
56	ESD.Cross.PG.MV.3	NA	IP only	NA	NA
57	ESD.CDM.LV	NA	IP only	NA	NA
58	ESD.CDM.MV	NA	IP only	NA	NA
59	ESD.CDM.LV.PG	NA	IP only	NA	NA
60	ESD.CDM.MV.PG	NA	IP only	NA	NA

PERC Chip Level Specifications (4/4)

No.	PERC Rule Name	ASIC	ASIC_LL	TCON	CAD
61	ESD.CDM.LV.Spc	NA	IP only	NA	NA
62	ESD.CDM.MV.Spc	NA	IP only	NA	NA
63	ESD.Sig.IO	NA	IP only	NA	NA

PERC Rule List (1/6)

No.	PERC Rule Name	Description
1	ESD.Rule.1.a	Check W and L of MOS and follow 1st ESD rule
2	ESD.Rule.1.b	Check W and L of MOS and follow 2nd ESD rule
3	ESD.Rule.1.c	Check W and L of MOS through resistors from signal pad, follow 1st and 2nd ESD rules
4	ESD.Rule.1.c.OU3	Check W and L of MOS through resistors from signal pad, follow 2nd ESD rules
5	ESD.R.Btwn.PG.MOS	Check the existence and value of resistance from power/ground pad to MOS S/D
6	ESD.R.GGMOS.Gate	Check the resistance between gate of ggmos and power/ground net > 1k ohm
7	ESD.Rule.1.2.a	Check self-domain ESD resistance, IO and CDM protection circuit
8	ESD.Rule.1.2.b	Check voltage source of CDM device and receiver MOS are identical
9	ESD.Rule.1.2.c	Check distance between CDM device and receiver MOS
10	EOS.LV.Gate.PG	Check LV MOS gate connected to P/G, but voltage of S/D is different from gate
11	EOS.MVHV.Gate.PG	Check MV/HV MOS gate connected to P/G, but voltage of S/D is different from gate
12	ESD.Cross.PG.1	Check cross domain net without complete CDM protection

PERC Rule List (2/6)

No.	PERC Rule Name	Description
13	ESD.Cross.PG.2	Check voltage source of CDM device and receiver MOS are identical
14	ESD.Cross.PG.3	Check distance between CDM device and receiver MOS on cross domain net
15	ESD.Pwr.Cut.Dio	Check discharging path with two power-cut diodes
16	ESD.Pwr.Clamp	Check power clamping circuit
17	ERC.Floating.Gate	Check floating gate
18	ERC.Floating.Power	Check floating power nets
19	ERC.Floating.Ground	Check floating ground nets
20	ERC.Bulk.Connect	Check that the bulk biasing of MOS device are applied correctly
21	ERC.Cap.Voltage	Check the voltage gap between P and N of capacitance
22	ERC.LVMOS.To.MVHVMOS	Check case that S/D of LV MOS is connected to gate of MV or HV MOS
23	ERC.MVMOS.To.LVHVMOS	Check case that S/D of MV MOS is connected to gate of LV or HV MOS
24	ERC.HVMOS.To.LVMVMOS	Check case that S/D of HV MOS is connected to gate of LV or MV MOS

PERC Rule List (3/6)

No.	PERC Rule Name	Description
25	ESD.Decap.Protect	Check CDM protection circuit for decouple capacitor
26	ESD.Decap.Connect	Check the gate of decap is not connected to signal pads or internal ports
27	ESD.Int.GGMOS	Check GGMOS protection circuit for receiver MOS on internal signal nets
28	ERC.Forward.Diode	Check that there are no forward-bias diode between power and ground nets
29	ERC.Forward.PMOS	Check PMOS which voltage of S/D is larger than bulk
30	ERC.Forward.NMOS	Check NMOS which voltage of S/D is smaller than bulk
31	ESD.GGMOS.Width	Check width of GGMOS is not smaller than finger width of receiver MOS
32	ESD.Cross.PG.APR.1	Check cross domain net without CDM protection
33	ESD.Cross.PG.APR.2	Check cross domain net without voltage-equivalence CDM circuit
34	ESD.Cross.PG.APR.3	Check cross domain net without CDM device in the range
35	ESD.LV.Decap	Check the LV decap
36	ESD.LV.Decap.MV.Pwr	Check the LV decap connected to MV power

PERC Rule List (4/6)

No.	PERC Rule Name	Description
37	ESD.Cross.PG.Wo.R	Check the cross domain net without resistance
38	ERC.Floating.Port	Check the port is not floating
39	ESD.GGP.LDO	Check the GGPMOS is not connected to real power
40	ERC.Content	Check the latch circuit with contention issue
41	ESD.B2B.Diode	Back-to-back diodes should be inserted into each separate ground net
42	ESD.R.Sig.200	Resistor between the gate oxide and Signal Pad >= 200 ohm
43	ESD.Cross.PG.UPF	Check cross domain net without complete CDM protection for UPF flow
44	ESD.Int.CDM	Find gate connected to internal port without CDM protection
45	ESD.Int.CDM.PG	Check voltage source of CDM device and receiver MOS are identical
46	ESD.Int.CDM.Spc	Check distance between CDM device and receiver MOS on internal port path
47	ESD.Int.APR.PG	Find S/D of MOS on internal port connected to non-APR P/G
48	ERC.Subckt.Pin	The subtypes of each selected pin and devices on the pin must be the same

PERC Rule List (5/6)

No.	PERC Rule Name	Description
49	ESD.IO.Subtype	Check the subtypes of devices on self domain net
50	ESD.IO.PG	Check the voltages of IO devices and receiver MOS on self domain net
51	ESD.Cross.PG.LV.1	Check cross domain net without cascade GGNMOS protection
52	ESD.Cross.PG.MV.1	Check cross domain net without complete CDM protection
53	ESD.Cross.PG.LV.2	Check voltage source of CDM device and receiver MOS are identical
54	ESD.Cross.PG.MV.2	Check voltage source of CDM device and receiver MOS are identical
55	ESD.Cross.PG.LV.3	Check distance between CDM device and receiver MOS on cross domain net
56	ESD.Cross.PG.MV.3	Check distance between CDM device and receiver MOS on cross domain net
57	ESD.CDM.LV	Find LV gate tied to internal/Signal port without cascoded GGNMOS protection
58	ESD.CDM.MV	Find MV gate tied to internal/Signal port without GGMOS protection
59	ESD.CDM.LV.PG	Check voltage source of CDM device and LV receiver MOS are identical
60	ESD.CDM.MV.PG	Check voltage source of CDM device and MV receiver MOS are identical

PERC Rule List (6/6)

No.	PERC Rule Name	Description
61	ESD.CDM.LV.Spc	Check distance between CDM device and LV receiver on internal/signal port
62	ESD.CDM.MV.Spc	Check distance between CDM device and MV receiver on internal/signal port
63	ESD.Sig.IO	Check resistor and IO protection circuit from signal pad

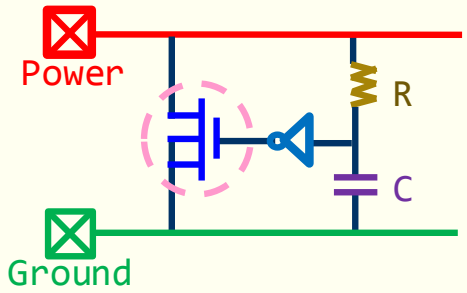
Rule 1: ESD.Rule.1.a

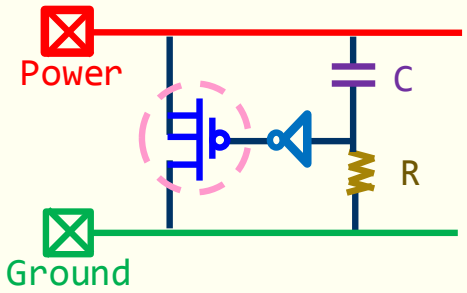
Return to rule list

- Description
  - The MOS connected to pad should follow BTG 1st ESD rule
  - Check width, length and total width of MOS
- Constraints
  - MOS is directly connected to power/ground/signal pad
  - Filter out the case that S/D and bulk of MOS are tied to the same pad

Passed

Check





RC-inv clamping circuit is filtered out.

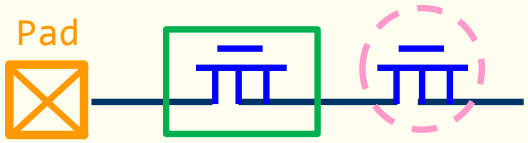
Rule 2: ESD.Rule.1.b

Return to rule list

- Description
  - The MOS connected to the first ESD MOS should follow BTG 2nd ESD rule
  - Check width, length and total width of MOS
- Constraints
  - MOS is connected to the first ESD MOS
  - Filter out the case that S/D and bulk of MOS are tied to the same pad
  - Skip 2nd total width check in U65, U40, GF55, T40 process

Passed

Check



Rule 3: ESD.Rule.1.c

Return to rule list

- Description
  - Check MOS connected through resistor(s) to signal pad
  - Check width, length and total width of MOS
- Constraints
  - Follow 1st and 2nd ESD rule according to the resistance value
  - Skip 2nd total width check in U65, U40, GF55, T40 process

Passed

Check

R < 1kΩ
Follow 1st ESD rule

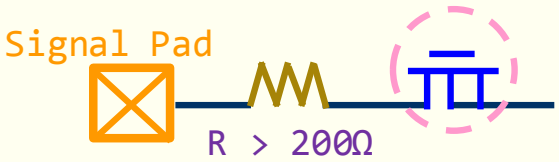
R > 1kΩ
Follow 2nd ESD rule

Rule 4: ESD.Rule.1.c.OU3

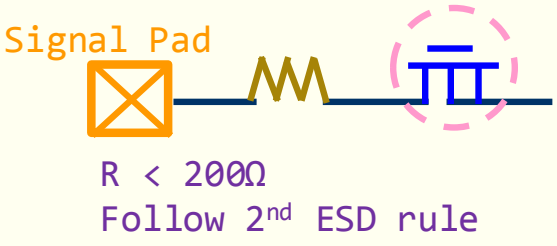
Return to rule list

- Description
  - Check MOS connected through resistor(s) to signal pad
  - Check width, length and total width of MOS
- Constraints
  - Follow 2nd ESD rule according to the resistance value

Passed



Check

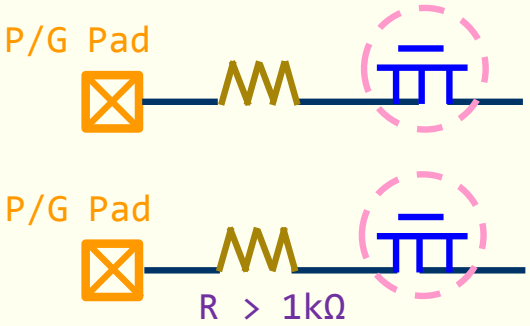


Rule 5: ESD.R.Btwn.PG.MOS

Return to rule list

- Description
  - Check MOS connected through resistor(s) to power/ground pad
  - Highlight the case that resistance value < 1k ohm
- Constraints
  - MOS is connected through the resistors to power/ground pad

Passed



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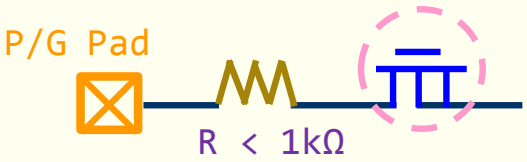
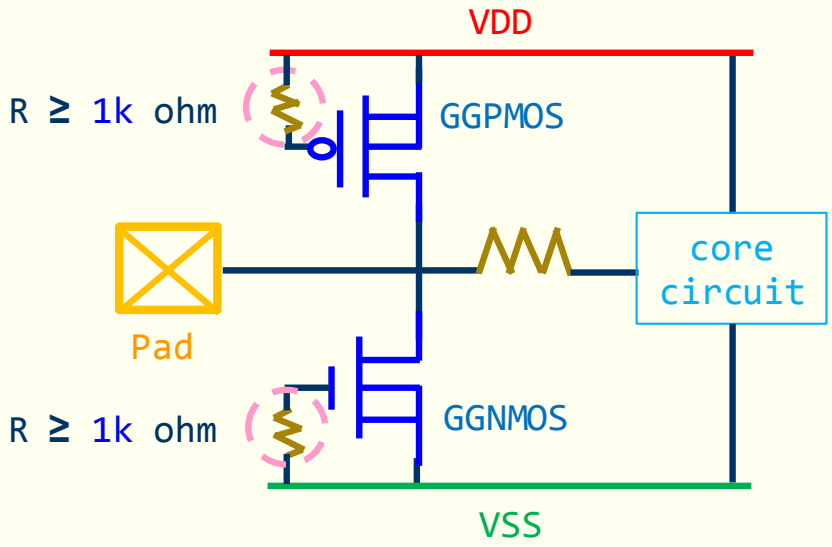


Rule 6: ESD.R.GGMOS.Gate

Return to rule list

- Description
  - Check the resistance connected to the gate of IO protection ggmos
- Constraints
  - The resistance between gate of ggmos and power/ground net must be ≥ 1k ohm
  - Filter out the RC-inv-clamp structure

Check

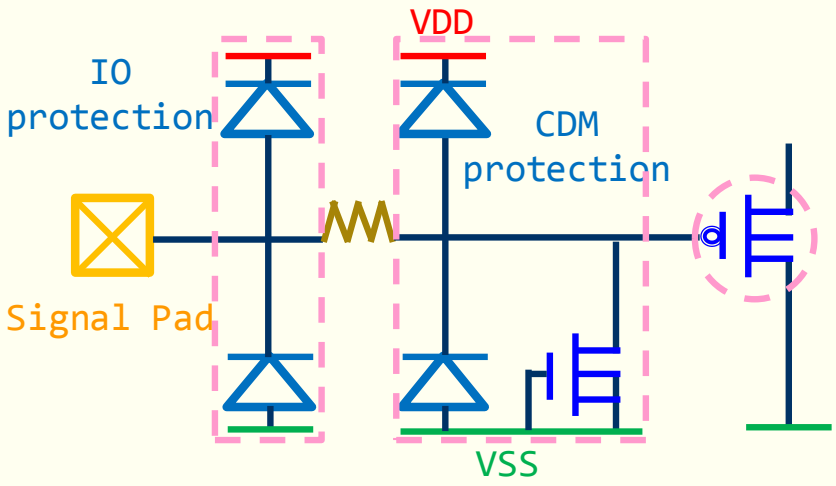


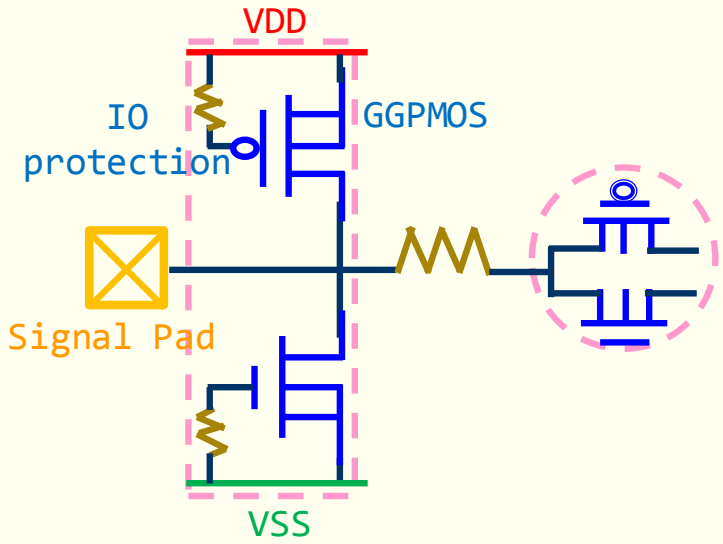
Rule 7: ESD.Rule.1.2.a

Return to rule list

- Description
  - Check self-domain IO protection circuit (diode or ggmos)
  - The internal gate connected to signal pad requires ESD resistor(s) and CDM protection (diode or ggmos)
- Constraints
  - The IO and CDM protection must contain both p-type and n-type devices

Passed



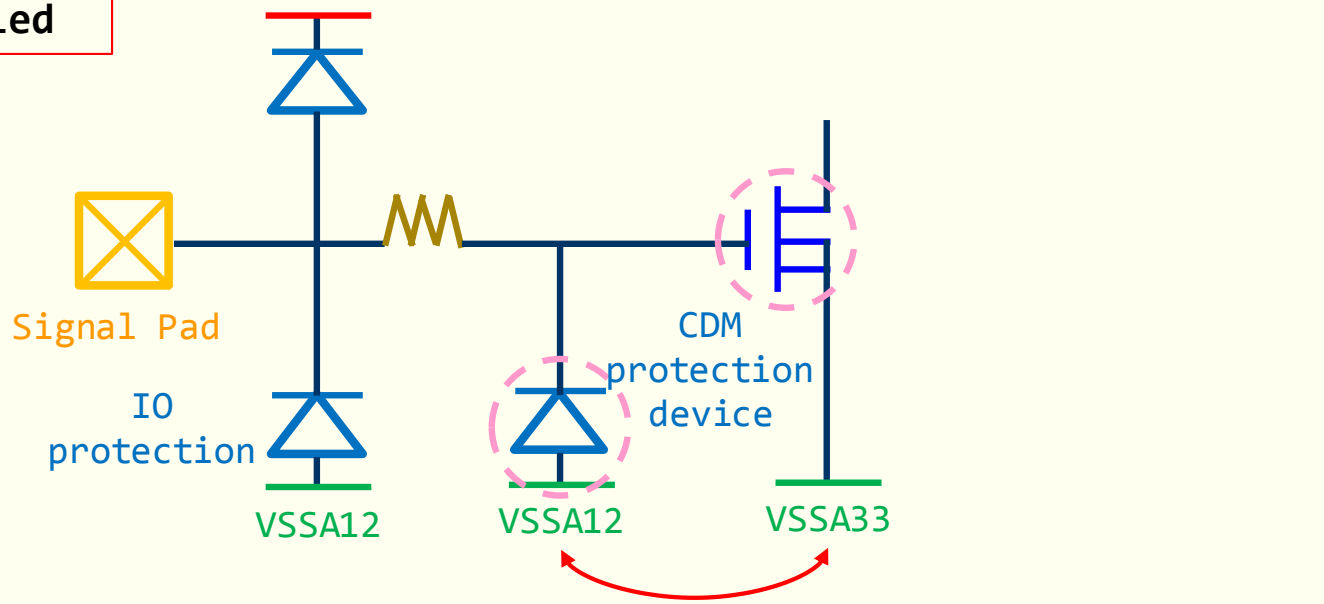


Rule 8: ESD.Rule.1.2.b

Return to rule list

- Description
  - Check the voltage source of receiver MOS and CDM devices are identical
- Constraints
  - Only check the case that MOS with CDM protection devices

Failed

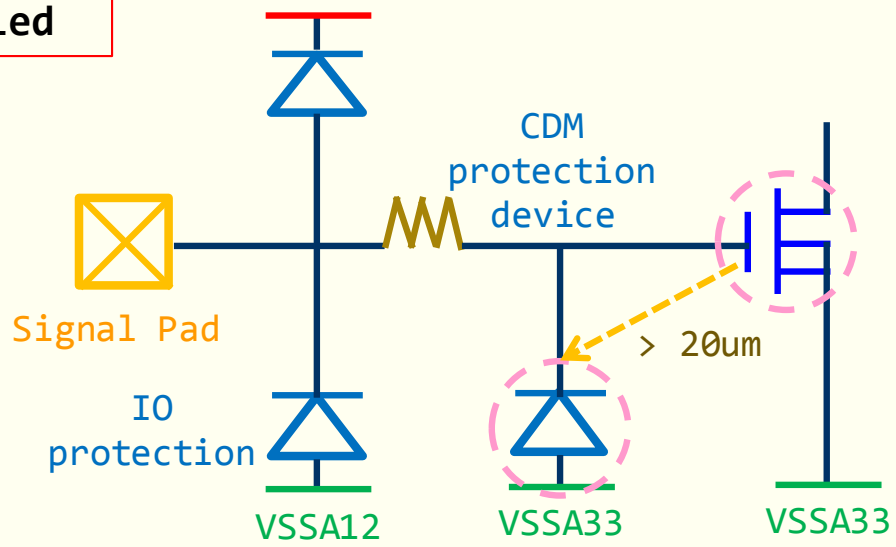


Rule 9: ESD.Rule.1.2.c

Return to rule list

- Description
  - Check the distance between CDM device and receiver MOS on self domain net
- Constraints
  - Only check CDM devices with identical voltage source
  - The distance between CDM device and receiver MOS should be < 20 um

Failed

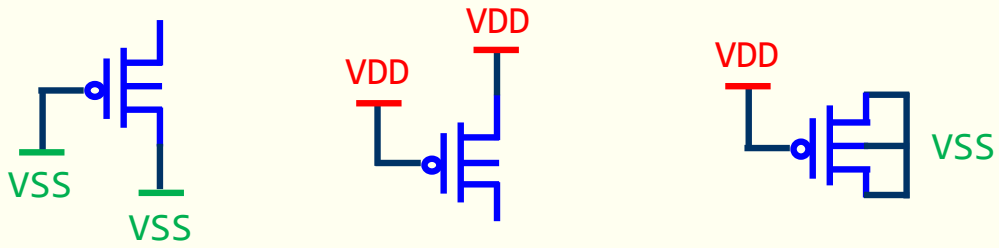


Rule 10: EOS.LV.Gate.PG

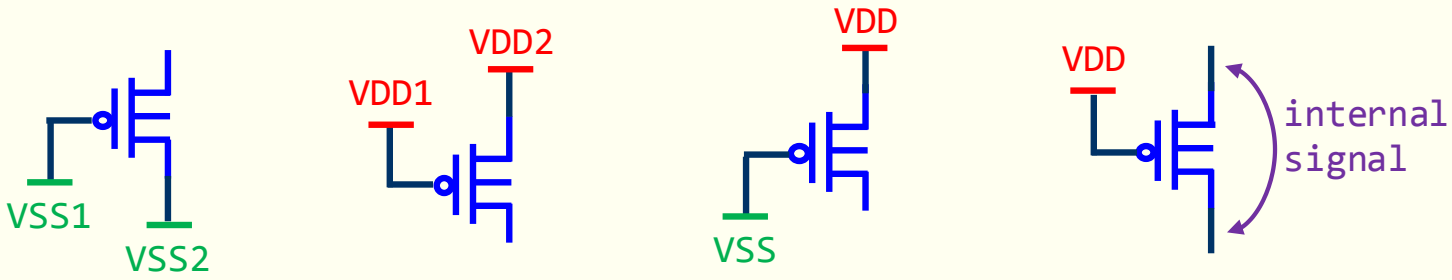
Return to rule list

- Description
  - Check LV MOS gate which is connected to power/ground directly
- Constraints
  - The voltage of S/D is different from the voltage of gate
  - Skip the case that voltages of S/D/B are the same

Passed



Failed

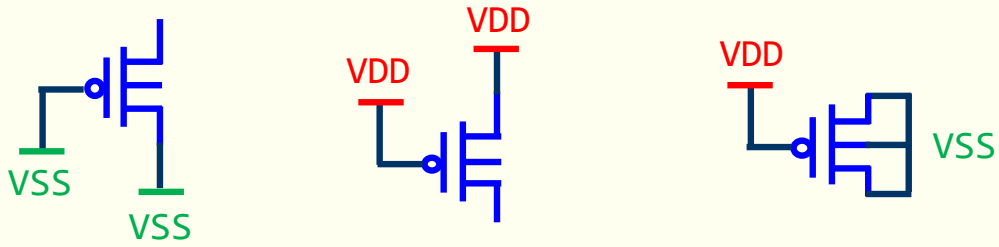


Rule 11: EOS.MVHV.Gate.PG

Return to rule list

- Description
  - Check MV and HV MOS gate which is connected to power/ground directly
- Constraints
  - The voltage of S/D is different from the voltage of gate
  - Skip the case that voltages of S/D/B are the same

Passed



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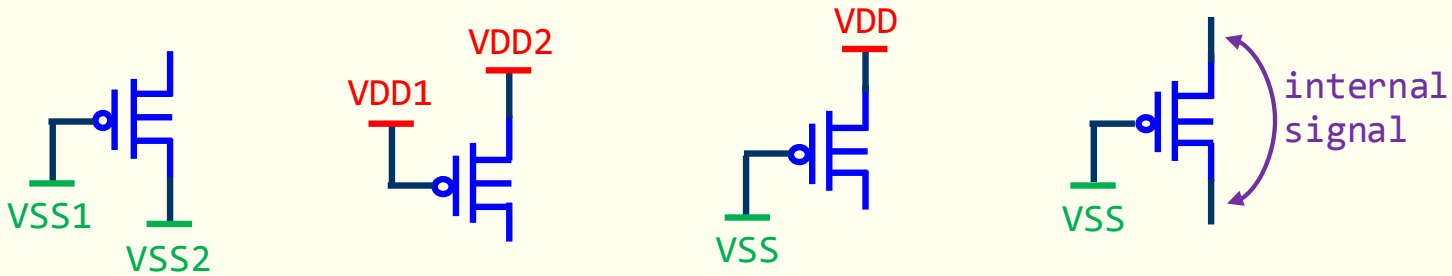
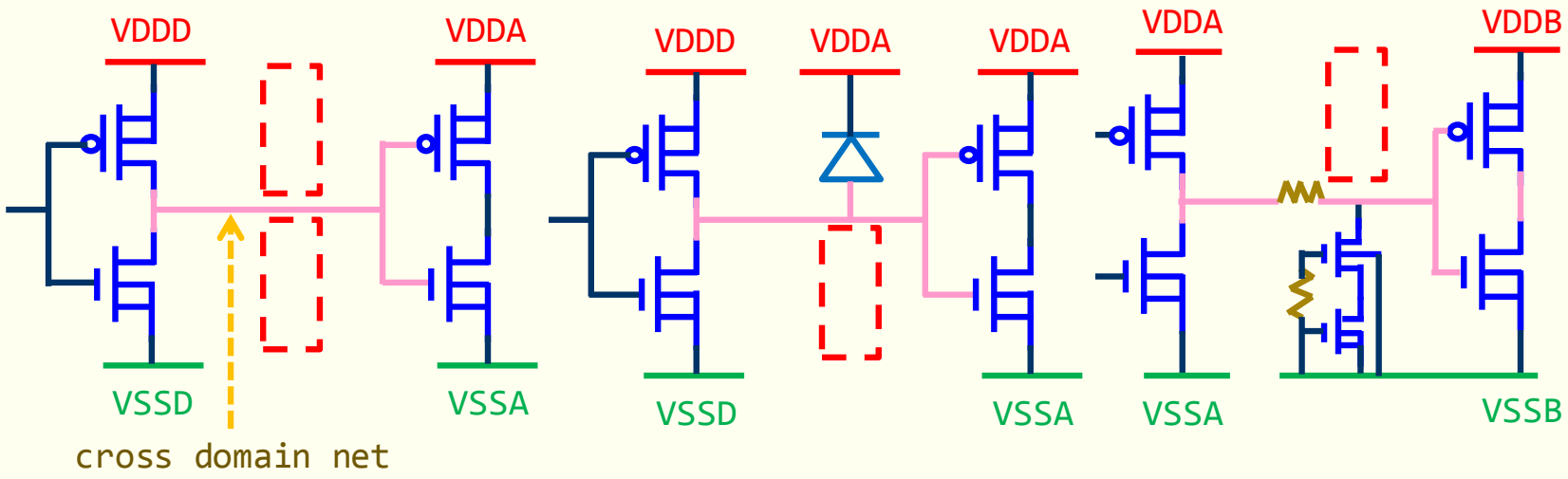


Rule 12: ESD.Cross.PG.1

Return to rule list

- Description
  - Check cross power/ground domain net without CDM protection (ggmos or diode)
- Constraints
  - The cross power domain net must have p-type CDM protection device
  - The cross ground domain net must have n-type CDM protection device
  - The decap on cross domain net should be recognized as receiver

Failed

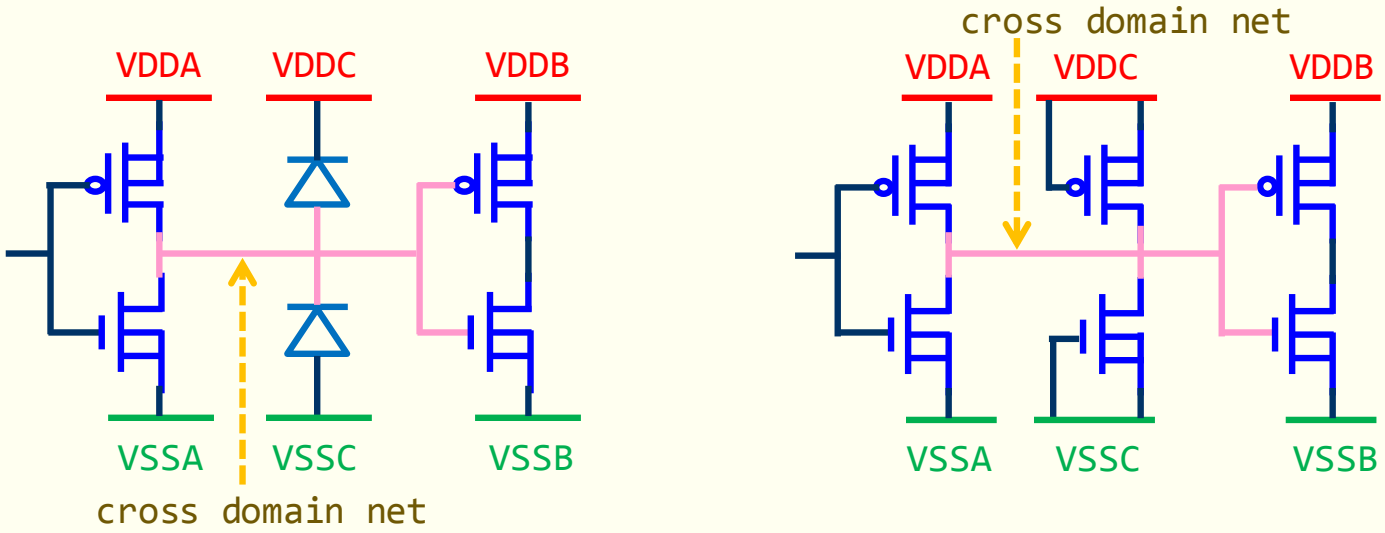


Rule 13: ESD.Cross.PG.2

Return to rule list

- Description
  - Check the voltage source of CDM device and receiver MOS on cross domain net are identical
- Constraints
  - Only check the cross domain net with CDM protection

Failed

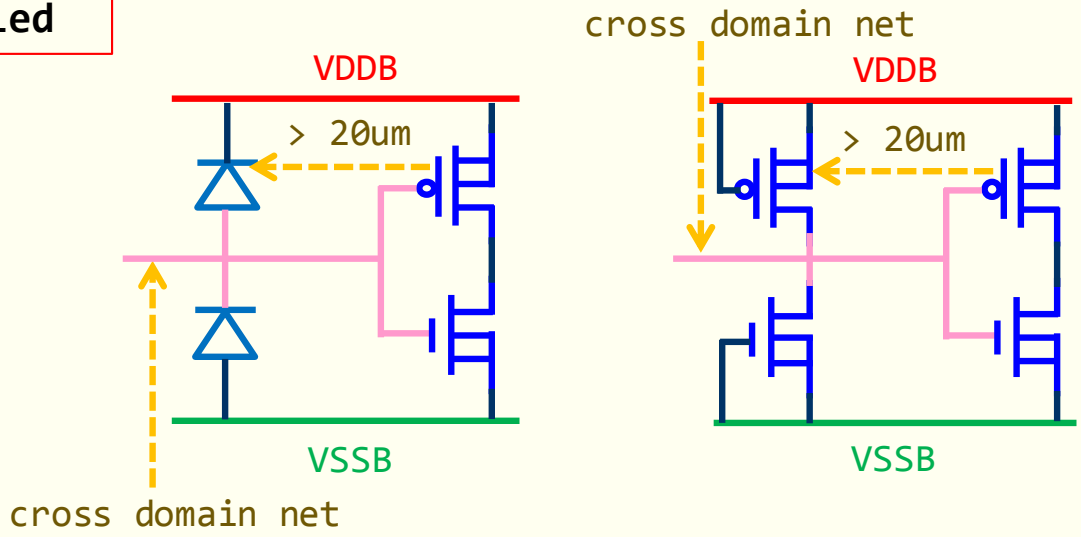


Rule 14: ESD.Cross.PG.3

Return to rule list

- Description
  - Check the distance between CDM device and receiver MOS on cross domain net
- Constraints
  - Only check the case that voltage source of CDM device and receiver MOS are identical
  - The distance between CDM device and receiver MOS should be < 20 um

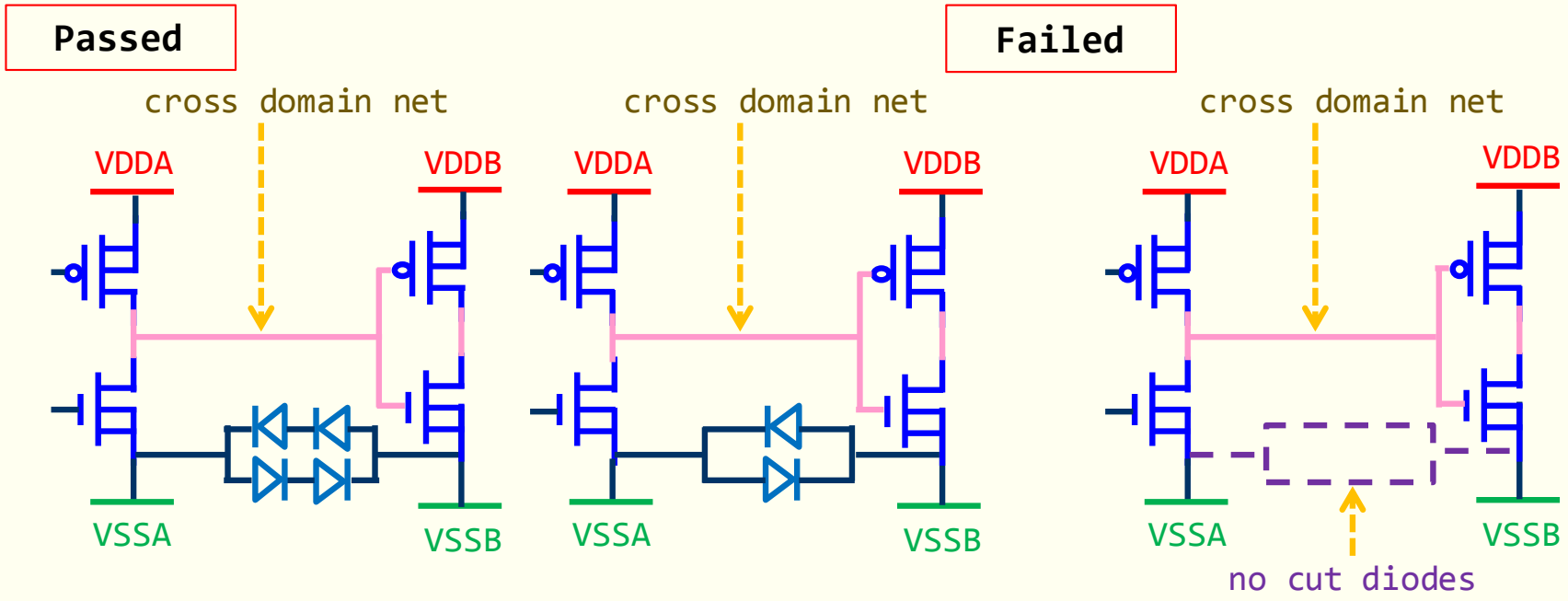
Failed



Rule 15: ESD.Pwr.Cut.Dio

Return to rule list

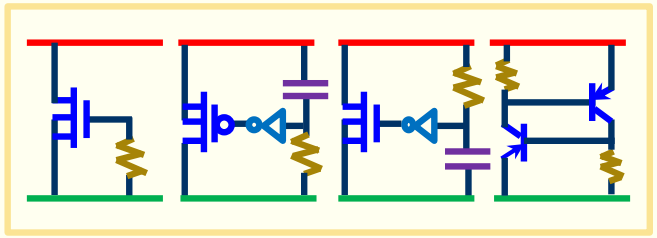
- Description
  - Check power cut diodes which are used on discharging path
- Constraints
  - Only check this rule on cross ground domain nets
  - The number of cut diodes can be either 1 or 2



Rule 16: ESD.Pwr.Clamp

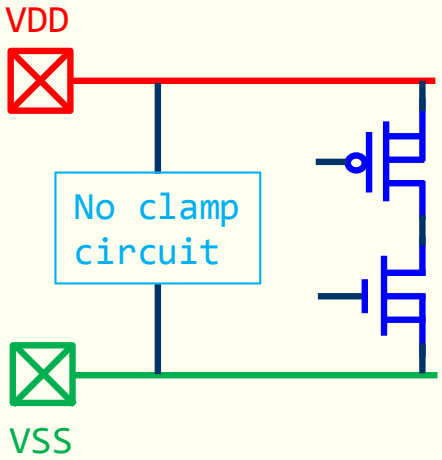
Return to rule list

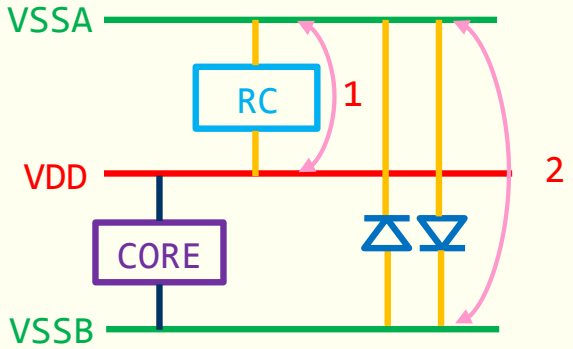
Power Clamp Structure



- Description
  - Check power to ground junction in core circuit
  - Protection structure: GGNMOS, RC-INV, SCR
- Constraints
  - Non-driver requires direct clamping from power to ground
  - Driver allows the second-degree clamping from power to ground

Failed



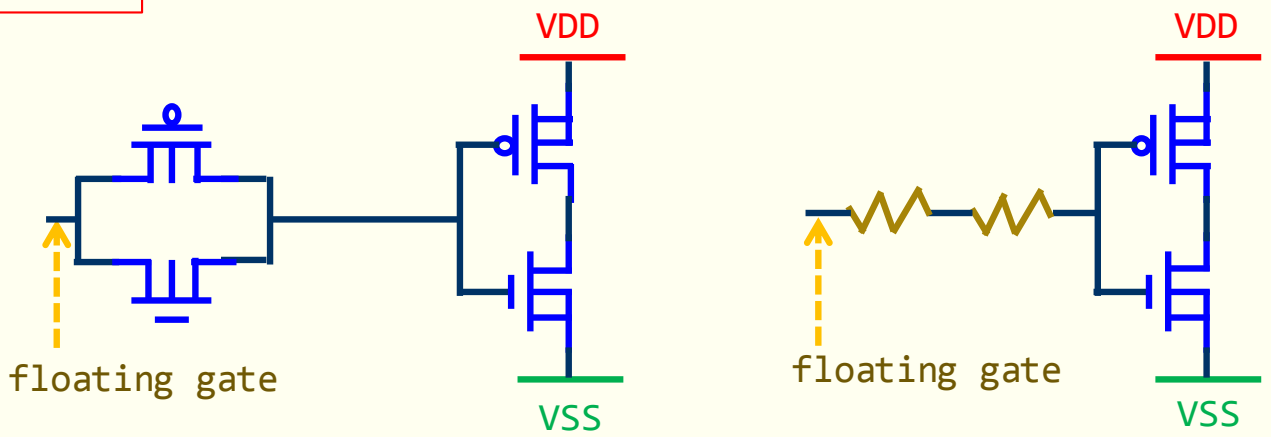


Rule 17: ERC.Floating.Gate

Return to rule list

- Description
  - Check the gate of MOS which is floating or not
  - The path can propagate through S/D of MOS, Resistor, and Capacitor
- Constraints
  - Disable path propagation of PMOS if the gate is connected to power
  - Disable path propagation of NMOS if the gate is connected to ground
  - Filter out floating gate on APR standard cell (FILLERC*)

Failed

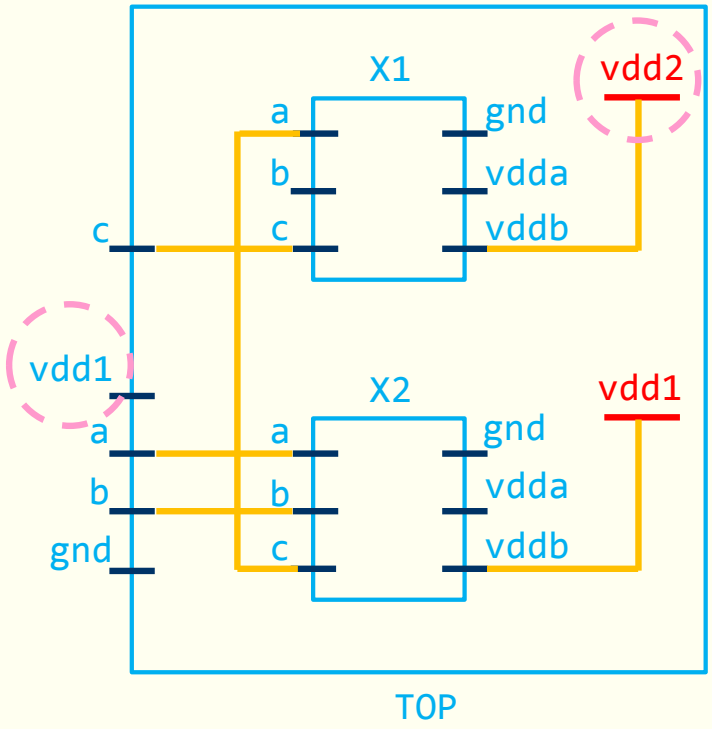


Rule 18: ERC.Floating.Power

Return to rule list

- Description
  - Check the power port is not floating
- Constraints
  - No floating power port

Failed



vdd1 and vdd2 are defined in voltage file

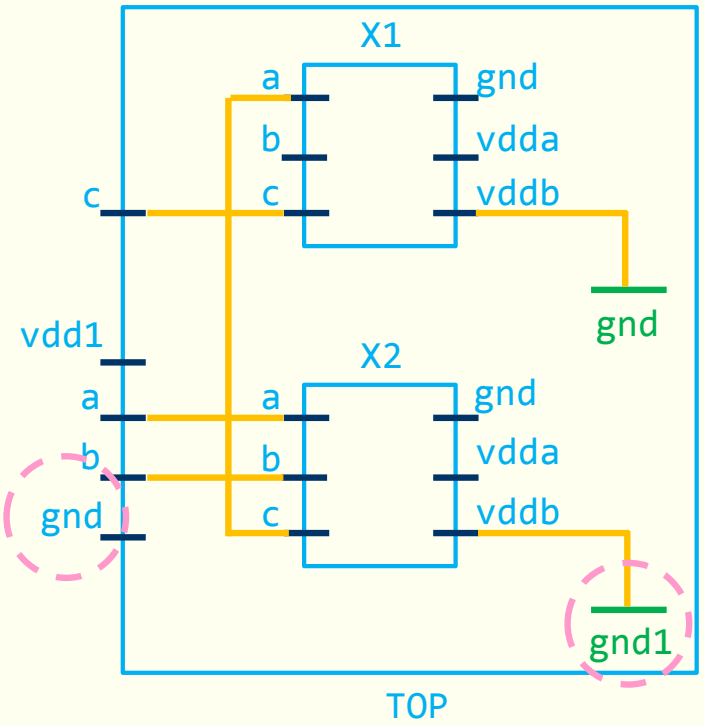
Highlight the case since vdd2 is not port

Rule 19: ERC.Floating.Ground

Return to rule list

- Description
  - Check the ground port is not floating
- Constraints
  - No floating ground port

Failed



gnd and gnd1 are defined in voltage file

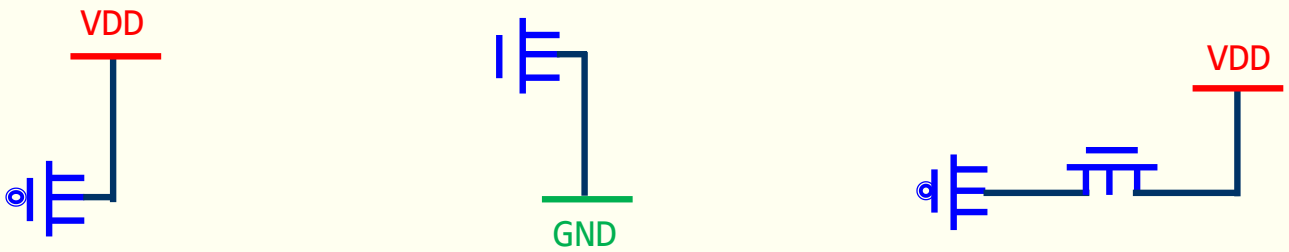
Highlight the case since gnd1 is not port

Rule 20: ERC.Bulk.Connect

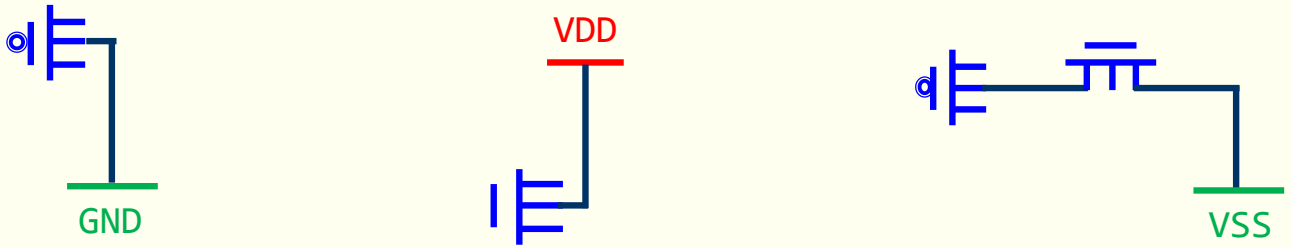
Return to rule list

- Description
  - Check that the bulk biasing of MOS device are applied correctly
  - The path can propagate through S/D of MOS and Resistors
- Constraints
  - The bulk pin of PMOS is connected to power
  - The bulk pin of NMOS is connected to ground

Passed



Failed

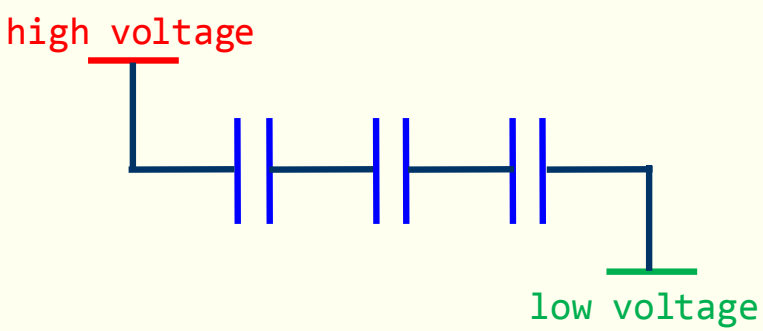


Rule 21: ERC.Cap.Voltage

Return to rule list

- Description
  - Check the voltage gap between P and N of capacitance
  - The total operating voltage is sum of the operating voltage of capacitors in series
- Constraints
  - The voltage gap must less than operating voltage of the capacitor(s)
  - Voltage definition file and capacitor definition file are required
  - This rule is turned off default

Failed



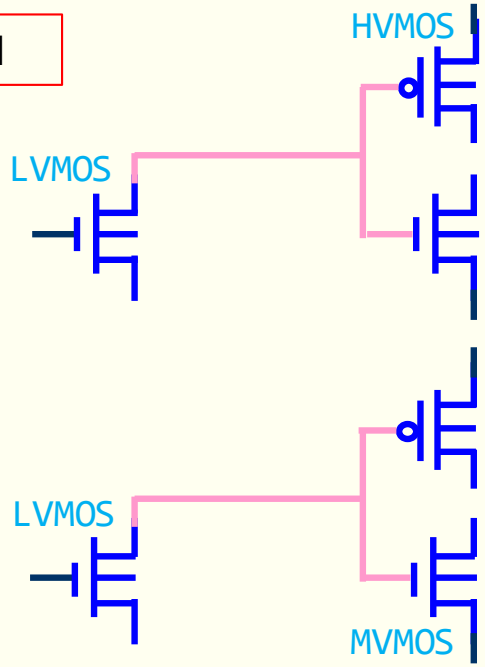

```
Operating voltage of one cap is 1
High voltage is 5
Low voltage is 0

Total Vop is 3 (1 * 3 = 3)
Voltage gap is 5 (5 - 0 = 5)
Voltage gap > Vop (5 > 3)
Check failed
```

Rule 22: ERC.LVMOS.To.MVHVMOS

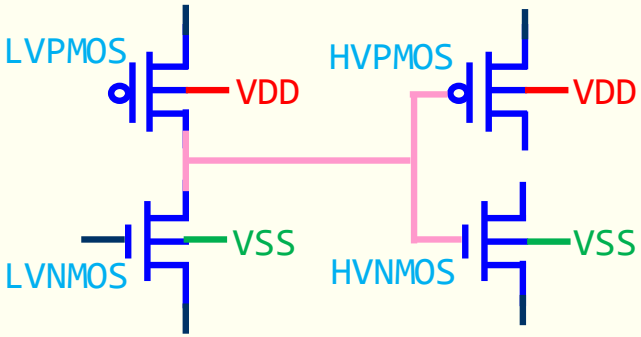
Return to rule list

- Description
  - Check case that S/D of LV MOS is connected to gate of MV/HV MOS
- Constraints
  - Filter out level shifter false alarms
  - Filter out the case which bulks connected to identical voltage source

Failed



Passed

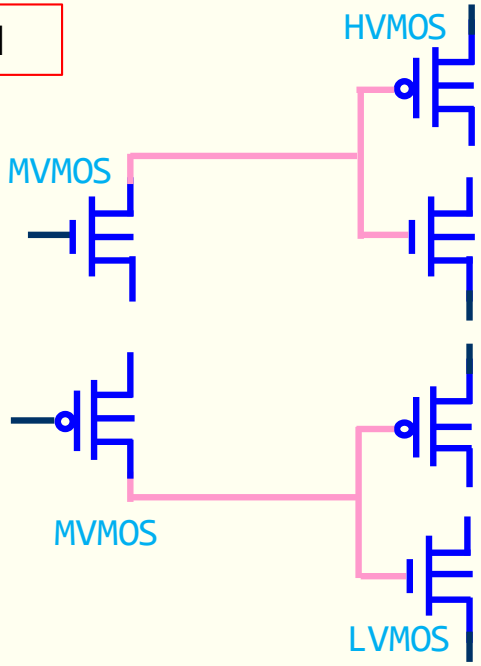


Rule 23: ERC.MVMOS.To.LVHVMOS

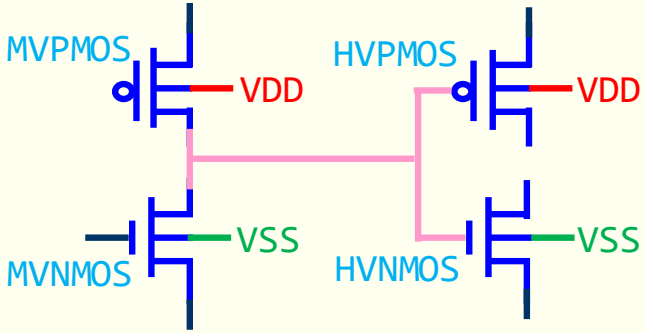
Return to rule list

- Description
  - Check case that S/D of MV MOS is connected to gate of LV/HV MOS
- Constraints
  - Filter out level shifter false alarms
  - Filter out the case which bulks connected to identical voltage source

Failed



Passed

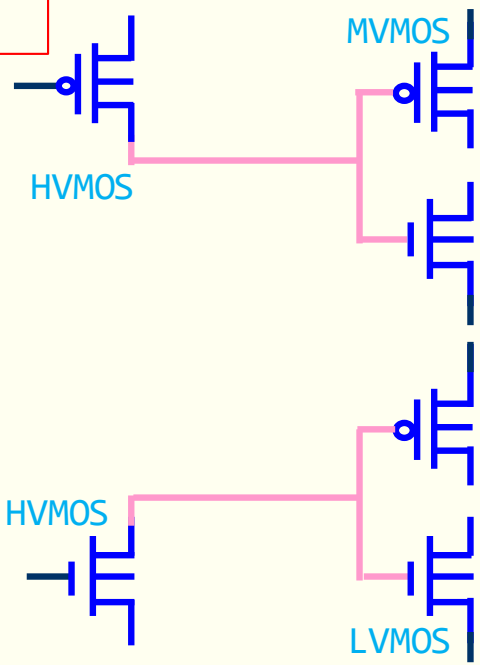


Rule 24: ERC.HVMOS.To.LVMVMOS

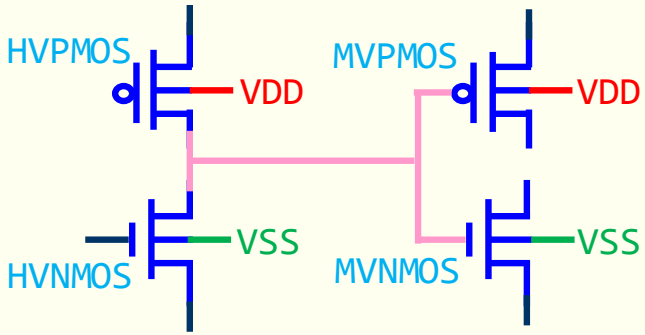
Return to rule list

- Description
  - Check case that S/D of HV MOS is connected to gate of LV/MV MOS
- Constraints
  - Filter out level shifter false alarms
  - Filter out the case which bulks connected to identical voltage source

Failed



Passed

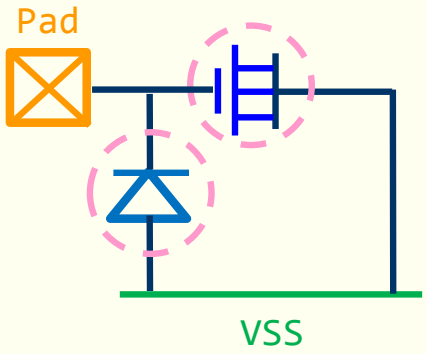


Rule 25: ESD.Decap.Protect

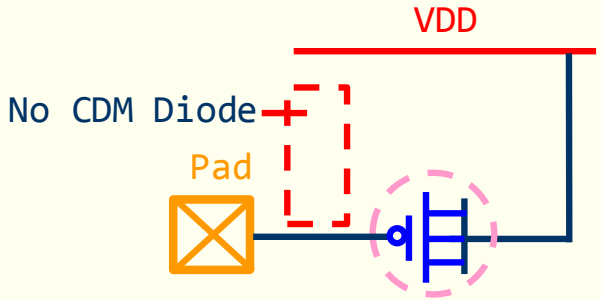
Return to rule list

- Description
  - Check CDM diode for decoupling capacitor
- Constraints
  - The gate and bulk of decoupling capacitor are connected to pads
  - The voltage source of CDM diode and decap must be the same

Passed



Failed

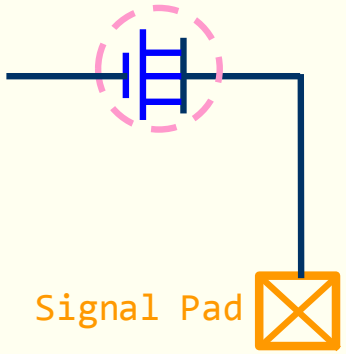


Rule 26: ESD.Decap.Connect

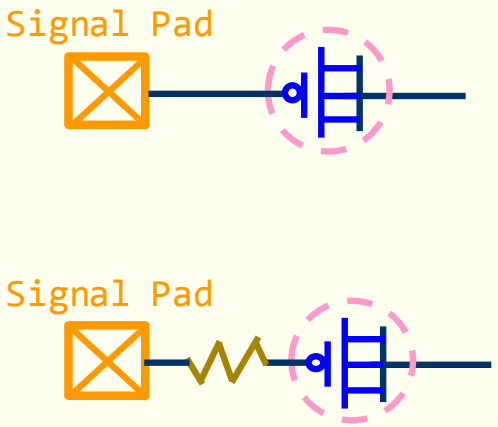
Return to rule list

- Description
  - Check the gate of decoupling capacitor which is not connected to signal pad
- Constraints
  - Filter out cases that gate of decoupling capacitor is connected to power and ground pads

Passed



Failed

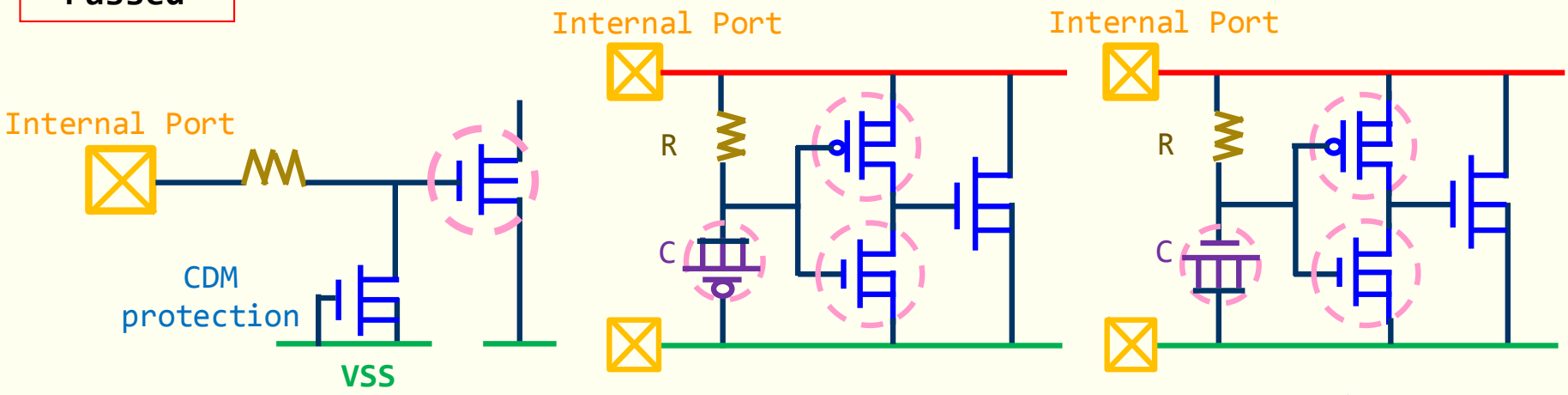


Rule 27: ESD.Int.GGMOS

Return to rule list

- Description
  - The internal gate connected to internal port requires ESD resistor(s) and ggmos as CDM protection device
- Constraints
  - Filter out the RC-inv-clamp structure
  - Filter out MOS which bulk connected to Power/Ground defined in WAIVE_PG_NAME in .top file
  - The receiver could be decoupling-capacitor

Passed

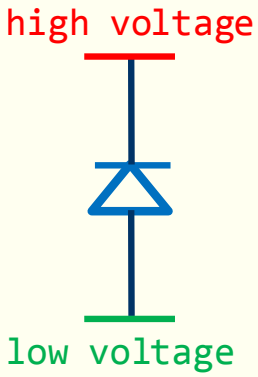


Rule 28: ERC.Foward.Diode

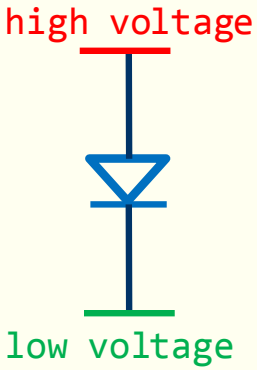
Return to rule list

- Description
  - Check that there are no forward-bias diodes between power and ground nets
  - To prevent short circuit from power to ground
- Constraints
  - No forward bias diode exists between power/ground nets
  - Voltage definition file is required

Passed



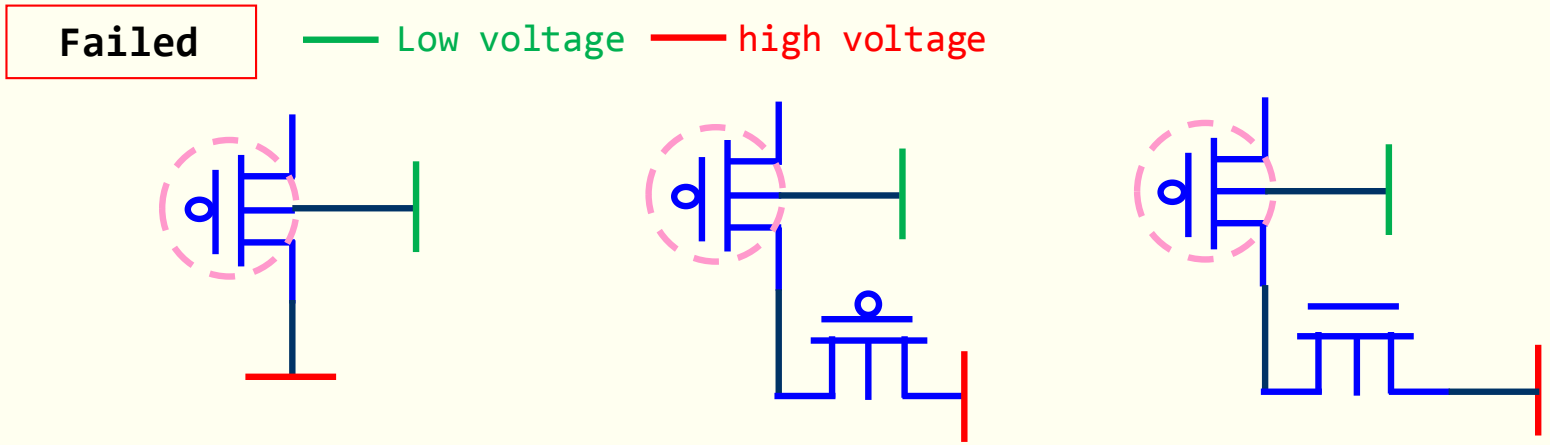
Failed



Rule 29: ERC.Foward.PMOS

Return to rule list

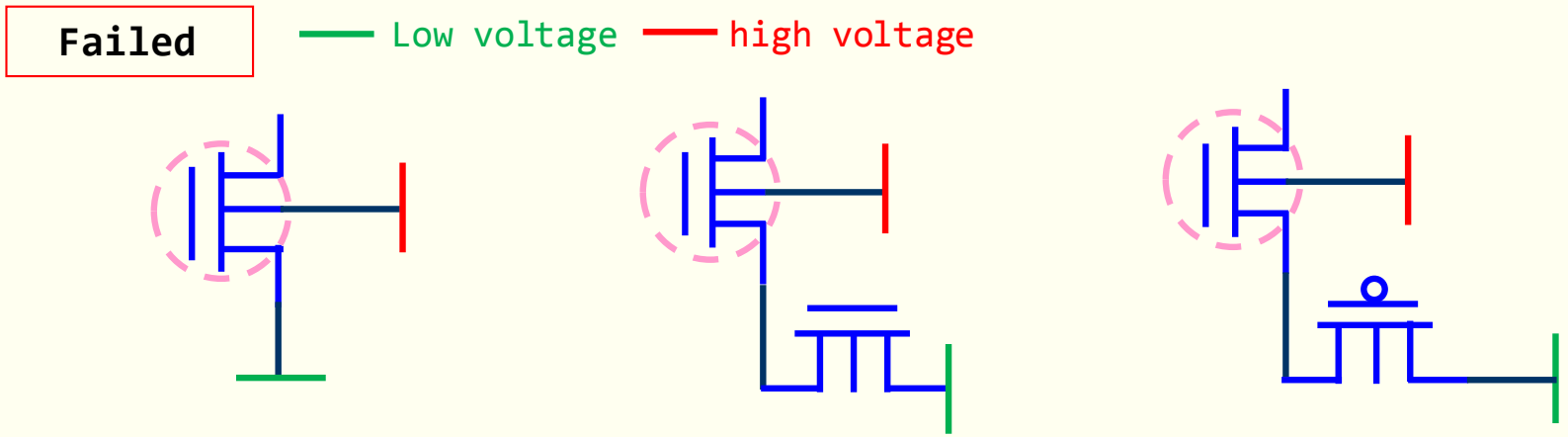
- Description
  - Check that there are no forward-bias PMOS
  - The voltage of S/D is derived from S/D of connected MOS or power/ground nets
- Constraints
  - Highlight PMOS that voltage of S/D is larger than voltage of bulk



Rule 30: ERC.Foward.NMOS

Return to rule list

- Description
  - Check that there are no forward-bias NMOS
  - The voltage of S/D is derived from S/D of connected MOS or power/ground nets
- Constraints
  - Highlight NMOS that voltage of S/D is smaller than voltage of bulk

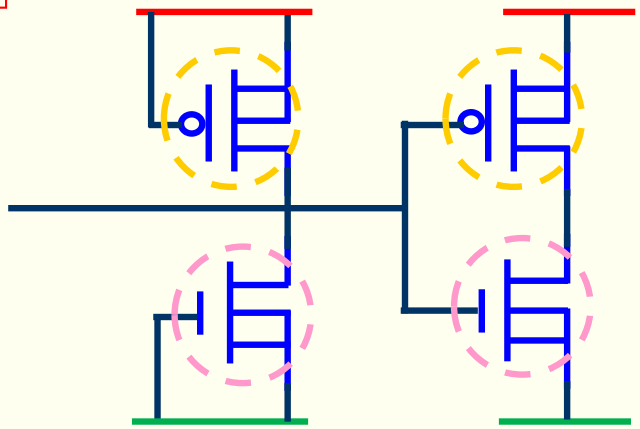


Rule 31: ESD.GGMOS.Width

Return to rule list

- Description
  - Check the width of GGMOS
- Constraints
  - The width of GGMOS is not smaller than finger width of corresponding MOS
  - The comparison is made only between MOS of the same type (LV, MV, HV)

Check



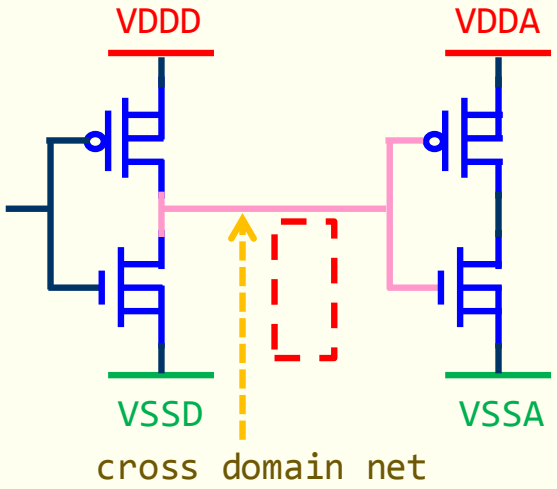
Compare p-type ggmos and receiver pmos,
and n-type ggmos and receiver nmos

Rule 32: ESD.Cross.PG.APR.1

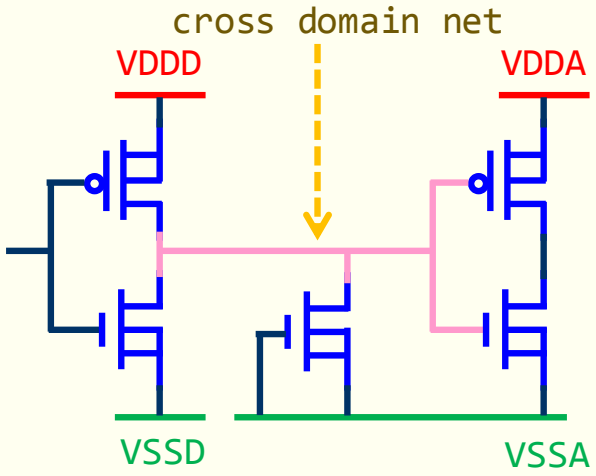
Return to rule list

- Description
  - Check cross power/ground domain net without N-type CDM protection (GGNMOS or N-diode)
- Constraints
  - The net cross power and ground should have N-type CDM device at least
  - The ground of receiver MOS is defined in APR_G in voltage file

Failed



Passed

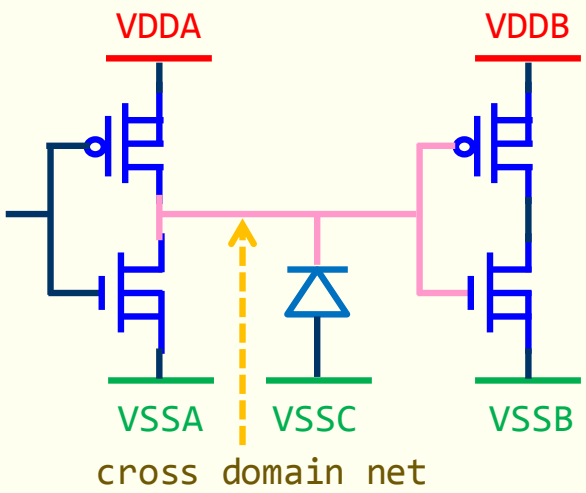


Rule 33: ESD.Cross.PG.APR.2

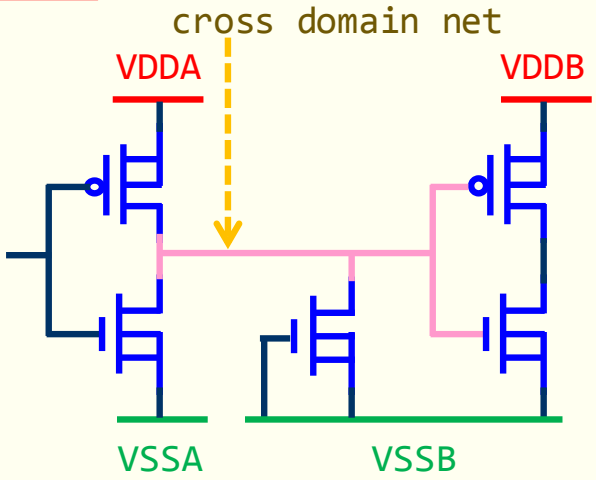
Return to rule list

- Description
  - Check the voltage source of N-type CDM device and receiver NMOS on cross domain net are identical
- Constraints
  - Only check the cross domain net with CDM protection
  - Once finding a CDM device with identical voltage source, the check is passed
  - The ground of receiver MOS is defined in APR_G in voltage file

Failed



Passed

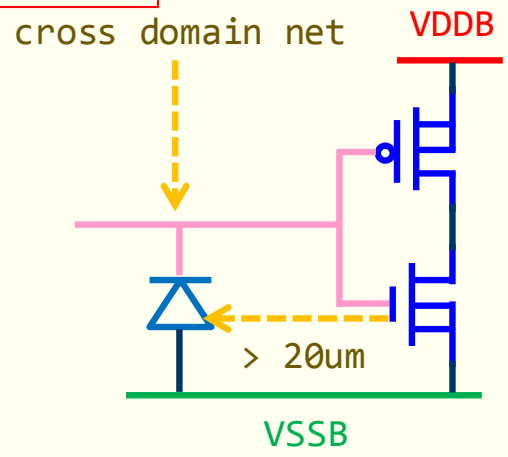


Rule 34: ESD.Cross.PG.APR.3

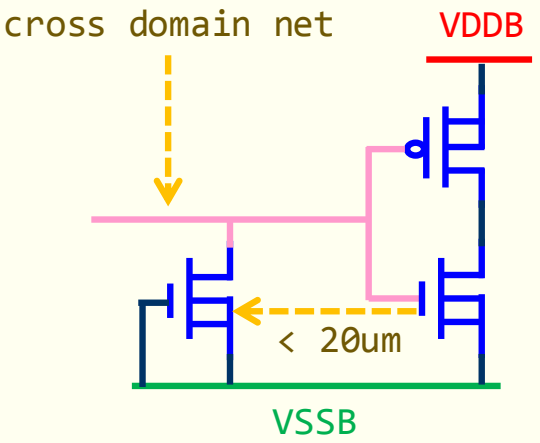
Return to rule list

- Description
  - Check the distance between N-type CDM device and receiver NMOS on cross domain net
- Constraints
  - the distance between N-type CDM device and receiver NMOS should be < 20 um
  - The ground of receiver MOS is defined in APR_G in voltage file

Failed



Passed

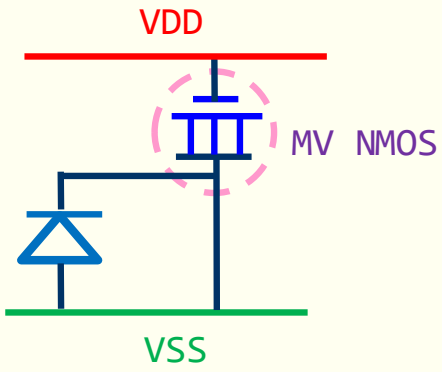


Rule 35: ESD.LV.Decap

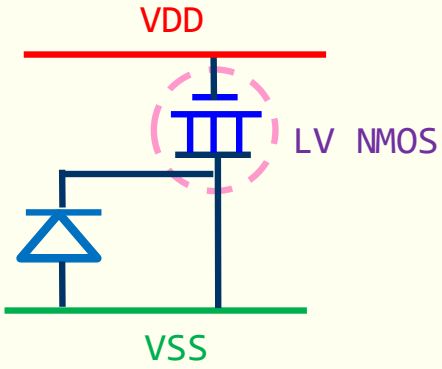
Return to rule list

- Description
  - Check the decap which is formed by MOS
- Constraints
  - Highlight all LV decoupling capacitors

Passed



Failed

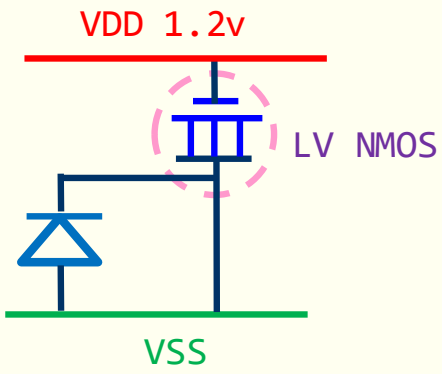


Rule 36: ESD.LV.Decap.MV.Pwr

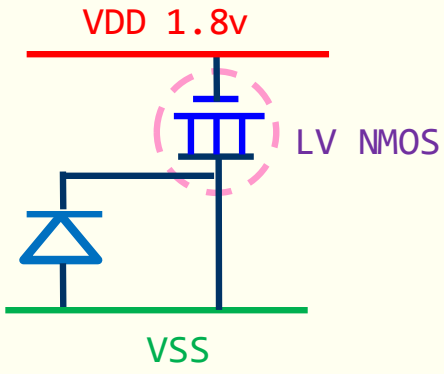
Return to rule list

- Description
  - Check LV decoupling capacitor connected to MV power
- Constraints
  - The voltage of power net which is larger than 1.2v is defined as MV power

Passed



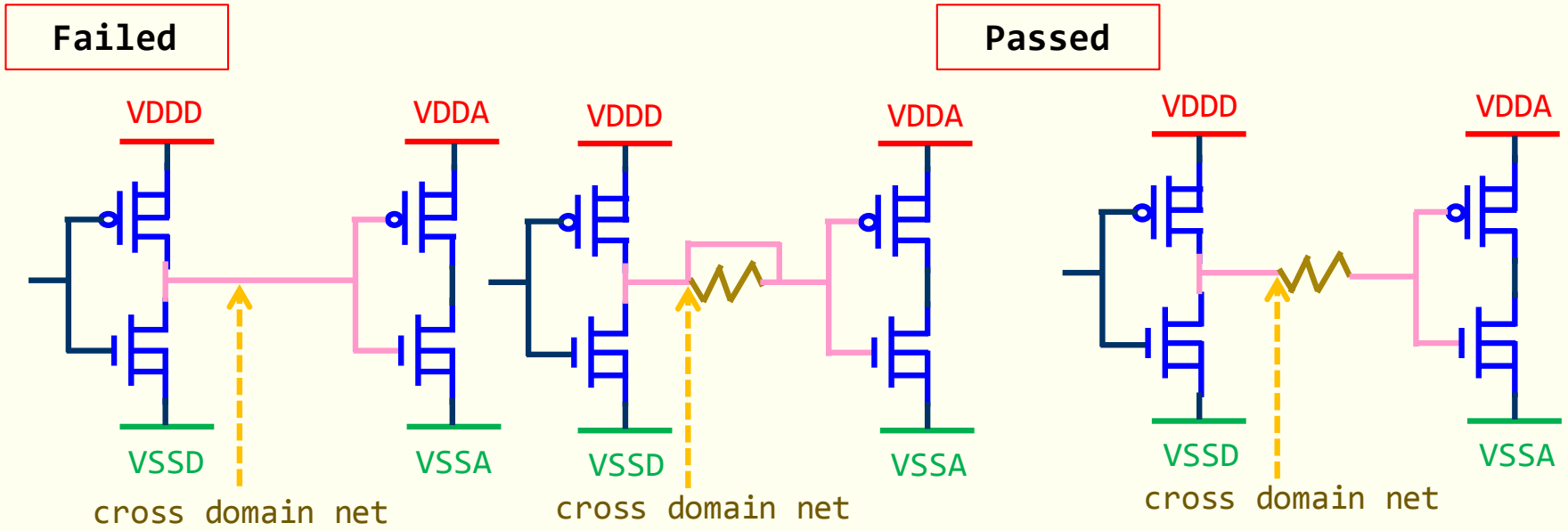
Failed



Rule 37: ESD.Cross.PG.Wo.R

Return to rule list

- Description
  - Check cross power/ground domain net without resistors
- Constraints
  - The resistor which P and N pins are shorted together is ignored

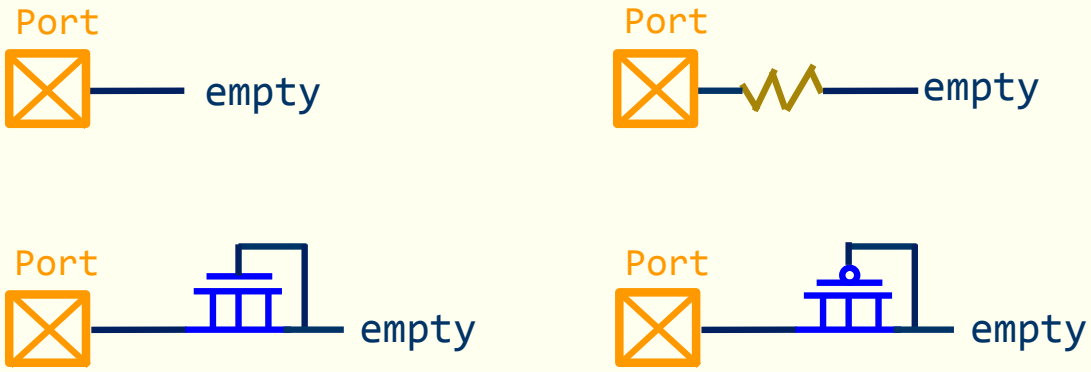


Rule 38: ERC.Floating.Port

Return to rule list

- Description
  - Check the port is not floating
- Constraints
  - The MOS which pins all tied together is recognized as dummy MOS

Failed



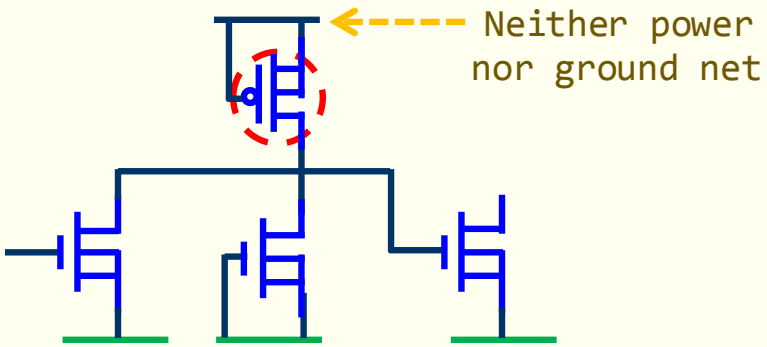
Rule 39: ESD.GGP.LDO

Return to rule list

- Description
  - Check all the GGPMOS connected to LDO power
- Constraints
  - The bulk of GGPMOS are not connected to real power nets.

Failed

Forward-bias probability

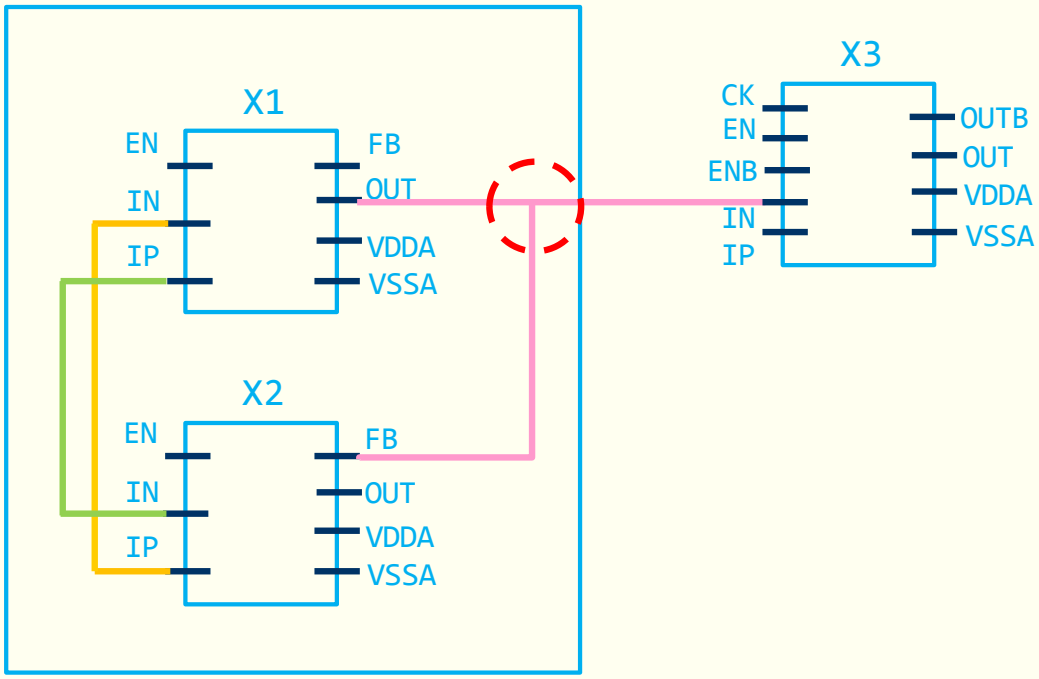


Rule 40: ERC.Content

Return to rule list

- Description
  - Detect the pre-defined latch circuit with contention issue
- Constraints
  - The latch circuit which is not connected to real power should also be selected

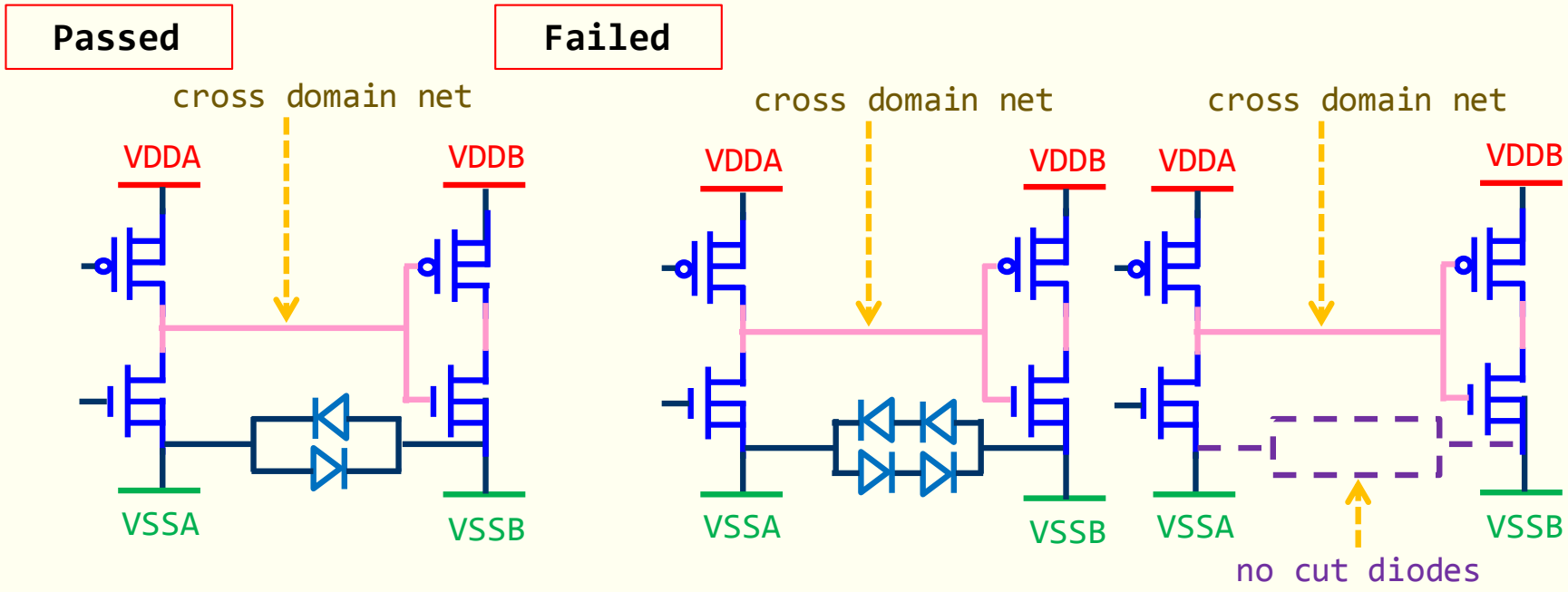
Failed



Rule 41: ESD.B2B.Diode

Return to rule list

- Description
  - Check power cut diodes which are used on discharging path
- Constraints
  - Only check this rule on cross ground domain nets
  - The number of cut diodes can only be one

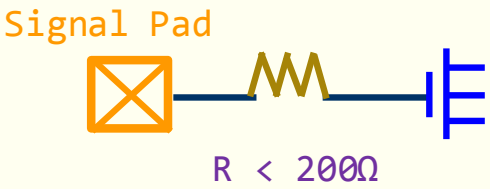


Rule 42: ESD.R.Sig.200

Return to rule list

- Description
  - Value of resistor between the gate oxide and Signal Pad >= 200 ohm
- Constraints
  - Compute the effective resistance from signal pad to MOS gate

Failed

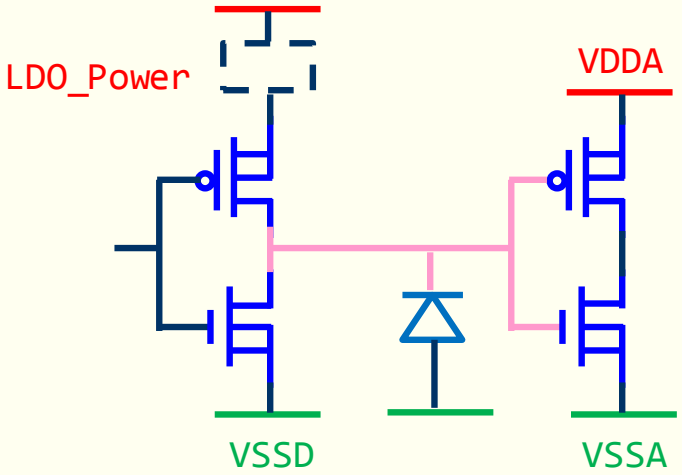


Rule 43: ESD.Cross.PG.UPF

Return to rule list

- Description
  - Check if there are transmitter MOS connected to LDO power and receiver MOS connected to real power on cross ground domain net
- Constraints
  - Highlight if only receiver PMOS tied to real power

Failed

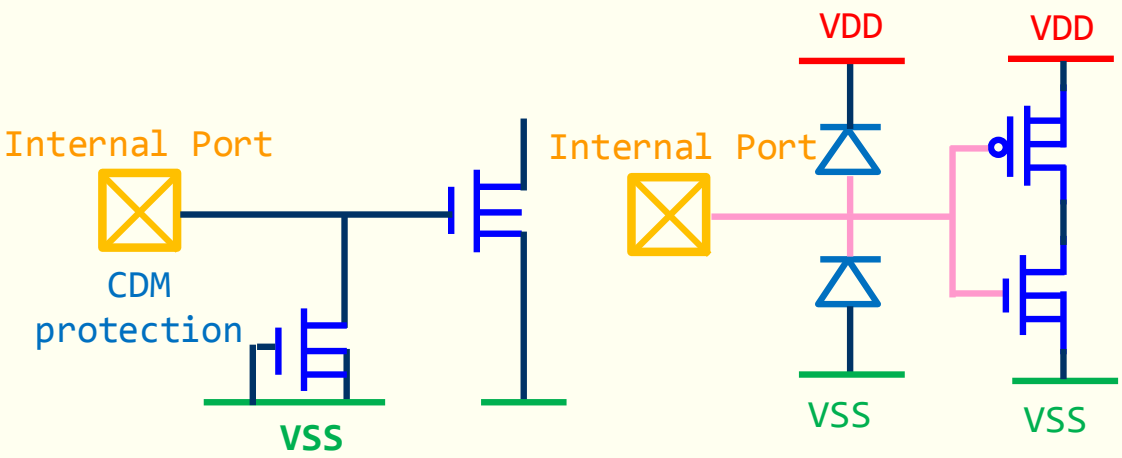


Rule 44: ESD.Int.CDM

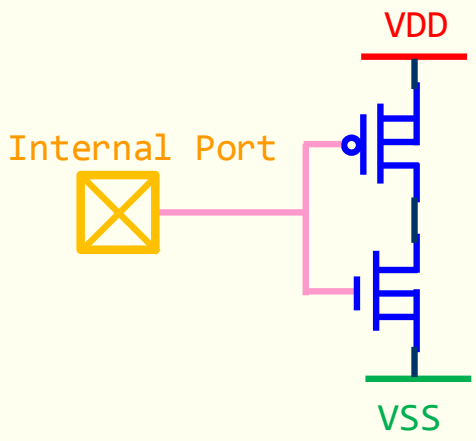
Return to rule list

- Description
  - The internal gate connected to internal port requires diode or ggmos as CDM protection device
- Constraints
  - The internal port must be connected to one CDM device at least

Passed



Failed

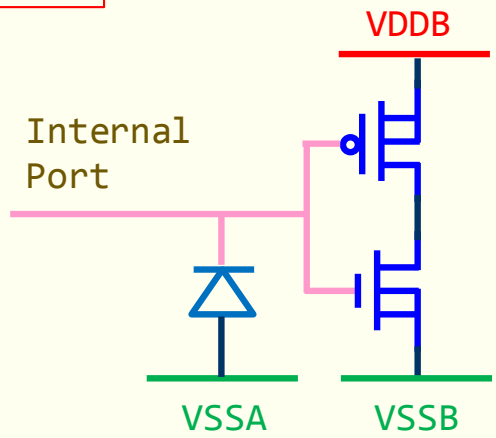


Rule 45: ESD.Int.CDM.PG

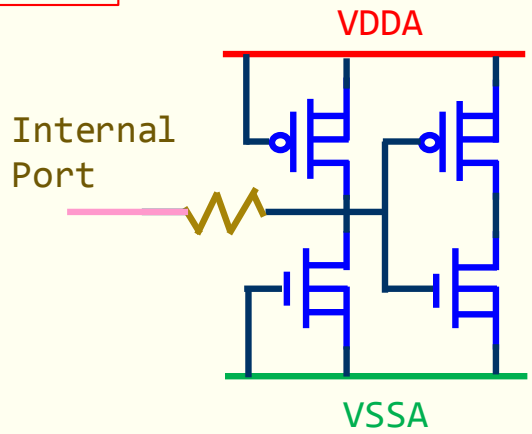
Return to rule list

- Description
  - Check the voltage source of CDM device and receiver connected to internal port are identical
- Constraints
  - Filter out the RC-inv-clamp structure
  - The receiver could be decoupling-capacitor
  - The receiver should be connected to real P/G

Failed



Passed

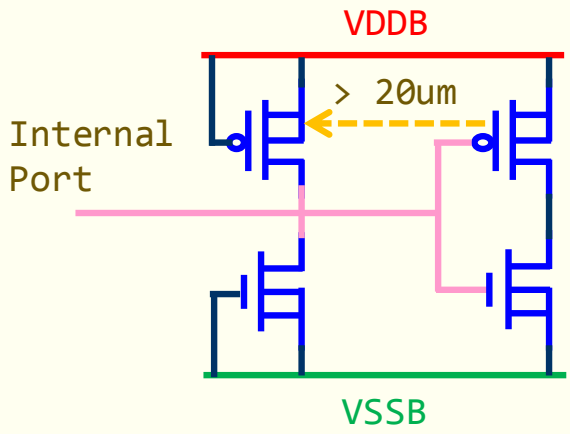


Rule 46: ESD.Int.CDM.Spc

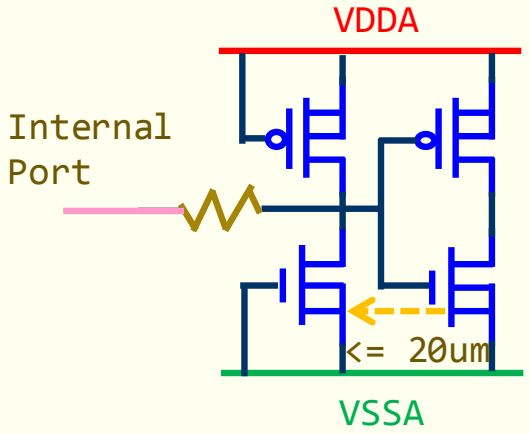
Return to rule list

- Description
  - Check the distance between CDM device and receiver MOS on path of internal port
- Constraints
  - The receiver should be connected to real P/G
  - The distance between CDM device and receiver MOS should be < 20 um

Failed



Passed

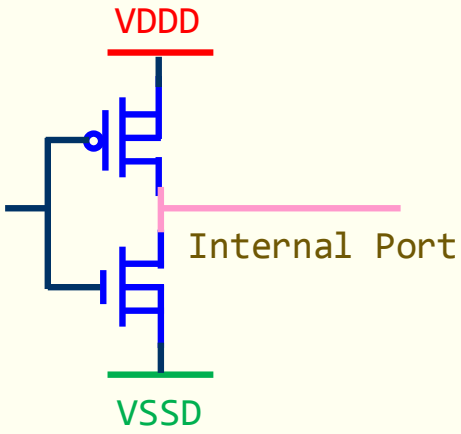


Rule 47: ESD.Int.APR.PG

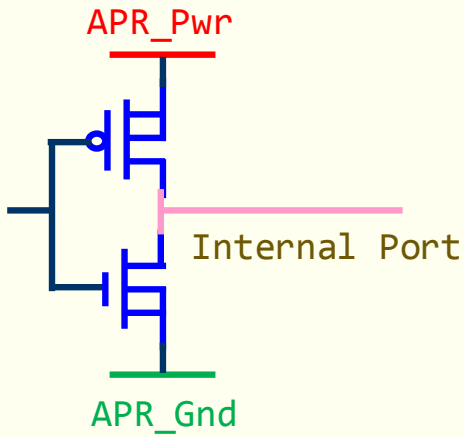
Return to rule list

- Description
  - Find the transmitter MOS that
    - One S/D is connected to internal port
    - The other S/D is connected to non-APR P/G
- Constraints
  - The transmitter connected to LDO power should be selected

Failed



Passed

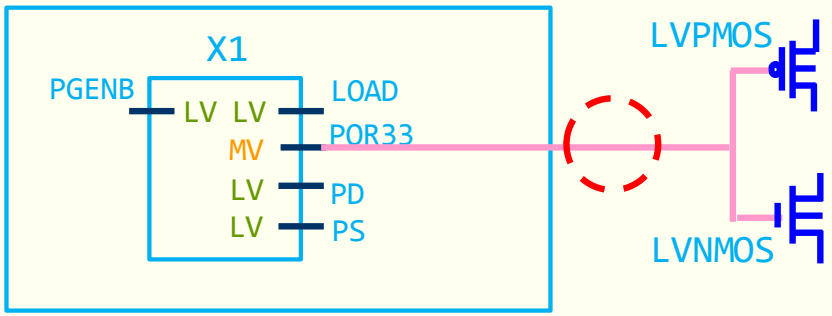


Rule 48: ERC.Subckt.Pin

Return to rule list

- Description
  - The subtypes of each selected pin in the third-party sub-circuit and devices on the pin must be the same
- Constraints
  - Define the variable THE_THIRD_PARTY_CELLS
  - Define the variable THE_THIRD_PARTY_VOLTAGE_FILE_PATH
  - Only pins in the voltage file will be checked in this rule
  - The voltage of selected pins <= 1.2v are LV devices, else are MV devices

Failed



The LV MOS is connected to MV pin

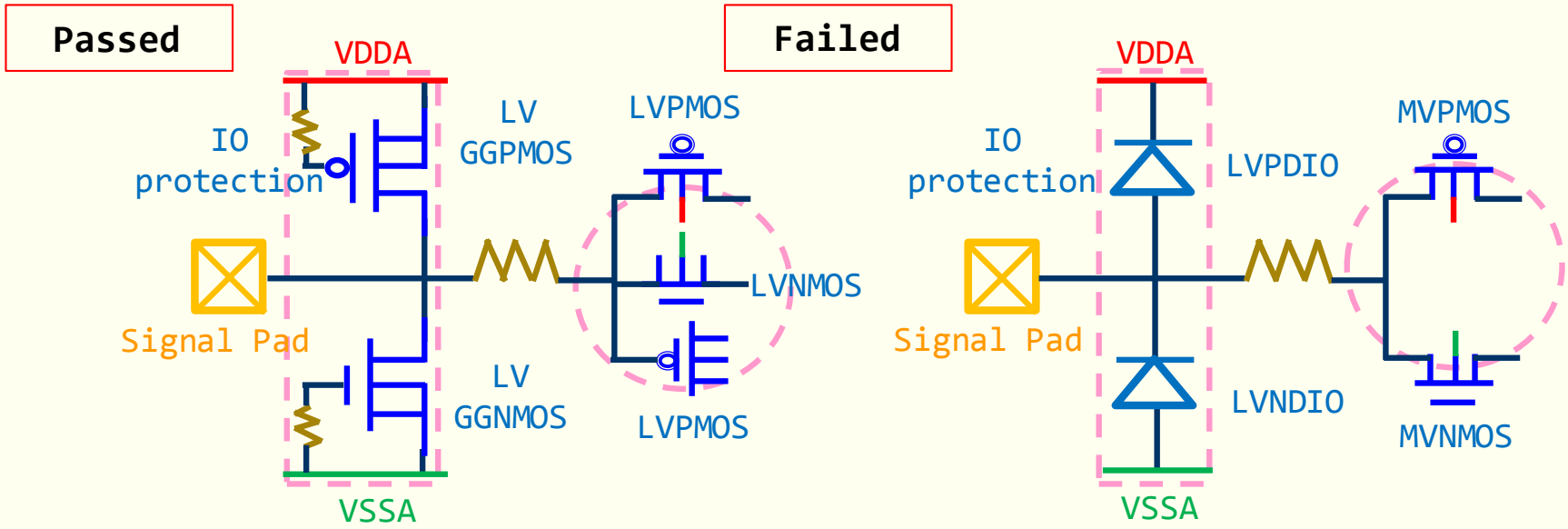
The third party voltage file

```
# Pin name and Voltage

POR33      3.3
VSS          0
VDD        1.1
```

Rule 49: ESD.IO.Subtype

Return to rule list

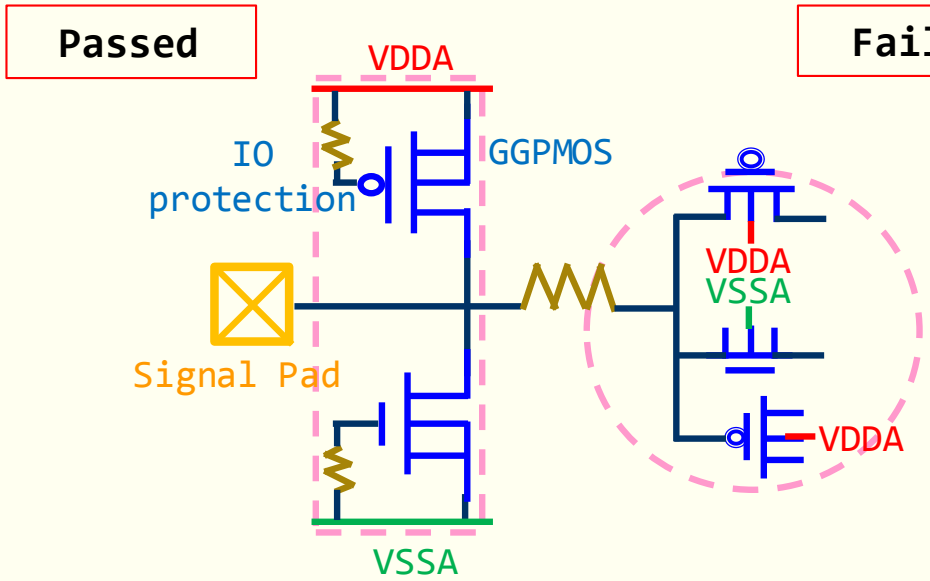
- Description
  - The type of internal MOS connected to signal pad should be the same as the type of IO protection devices
- Constraints
  - Check the MOS which gate and S/D are connected to net on signal path
  - The devices which are not connected to real P/G also should be selected

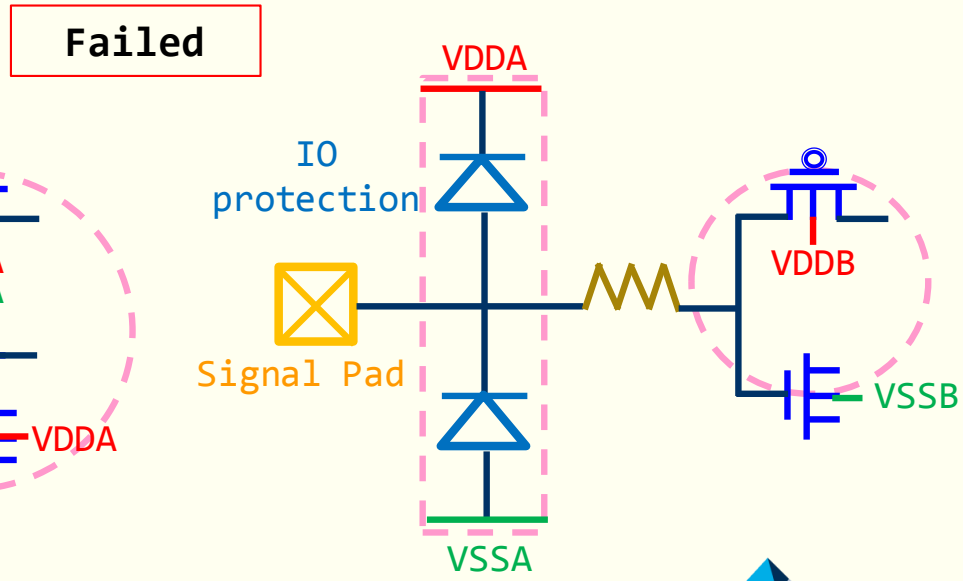


Rule 50: ESD.IO.PG

Return to rule list

- Description
  - The voltage of internal MOS connected to signal pad should be the same as the voltage of IO protection devices
- Constraints
  - The voltage of internal MOS is got from bulk pin
  - Replace the metal-resistor P/G name with real P/G pad name
  - The devices which are not connected to real P/G also should be selected



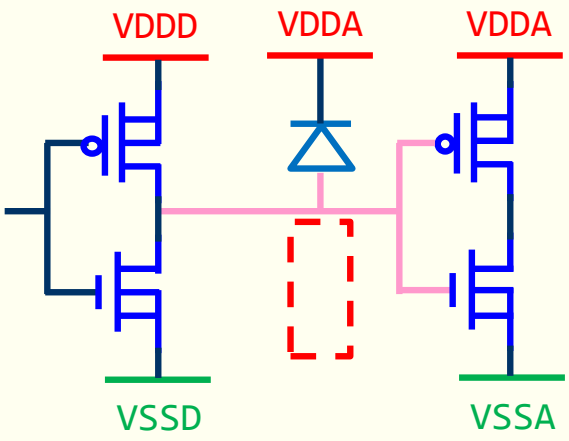


Rule 51: ESD.Cross.PG.LV.1

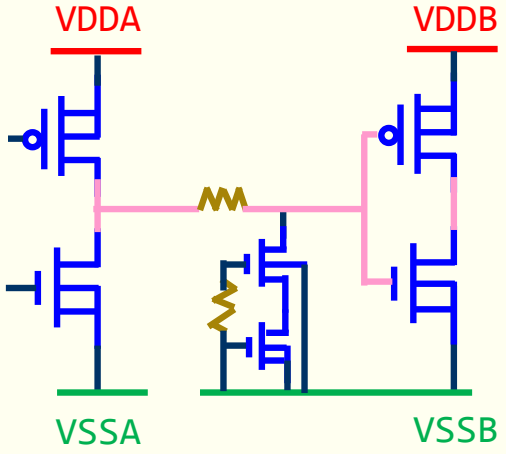
Return to rule list

- Description
  - Check cross power/ground domain net without cascoded GGNMOS
- Constraints
  - Only check LV receiver MOS
  - The cross power/ground net must have cascoded GGNMOS CDM device

Failed



Passed

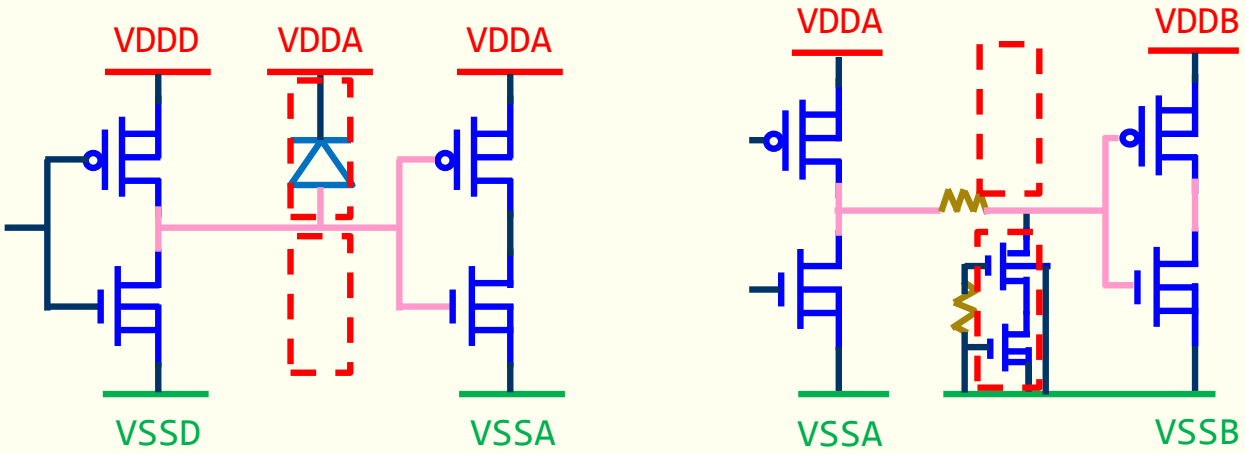


Rule 52: ESD.Cross.PG.MV.1

Return to rule list

- Description
  - Check cross power/ground domain net without GGMOS
- Constraints
  - Only check MV receiver MOS
  - The cross power net must have GGPMOS CDM device
  - The cross ground net must have GGNMOS CDM device

Failed

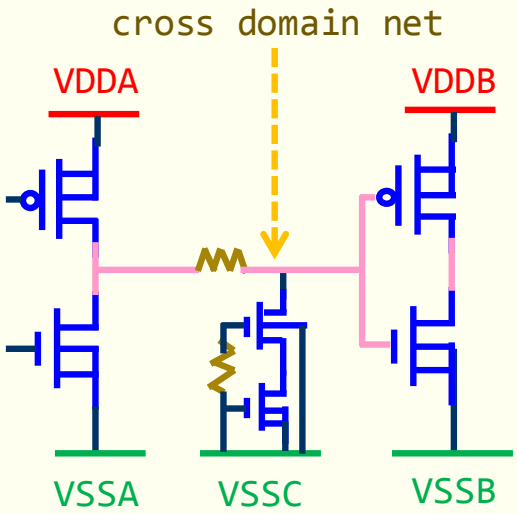


Rule 53: ESD.Cross.PG.LV.2

Return to rule list

- Description
  - Check the voltage source of CDM device and receiver NMOS on cross domain net are identical
- Constraints
  - Only check the cross domain net with cascoded GGNMOS protection
  - Only check LV receiver MOS

Failed

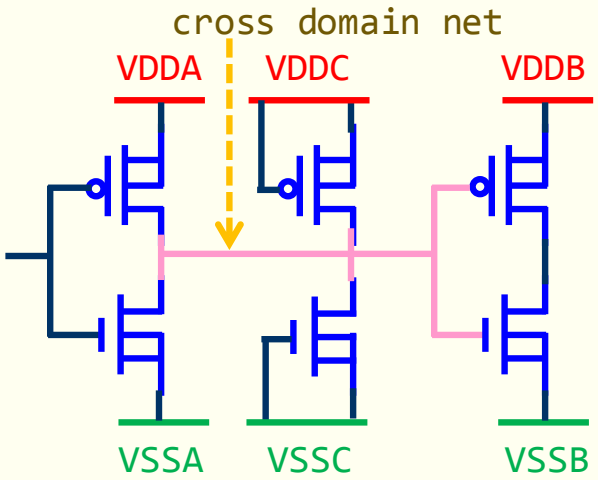


Rule 54: ESD.Cross.PG.MV.2

Return to rule list

- Description
  - Check the voltage source of GGMOS and receiver MOS on cross domain net are identical
- Constraints
  - Only check the cross domain net with GGMOS CDM protection
  - Only check MV receiver MOS

Failed

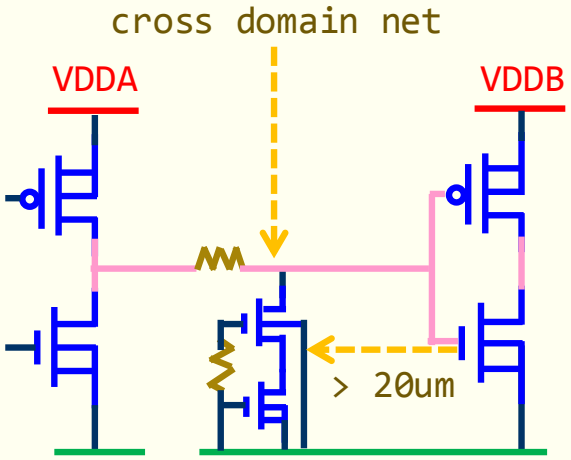


Rule 55: ESD.Cross.PG.LV.3

Return to rule list

- Description
  - Check the distance between CDM device and receiver MOS on cross domain net
- Constraints
  - Only check the case that voltage source of GGNMOS and receiver are identical
  - The distance between cascoded GGNMOS and receiver MOS should be < 20 um
  - Only check LV receiver MOS

Failed

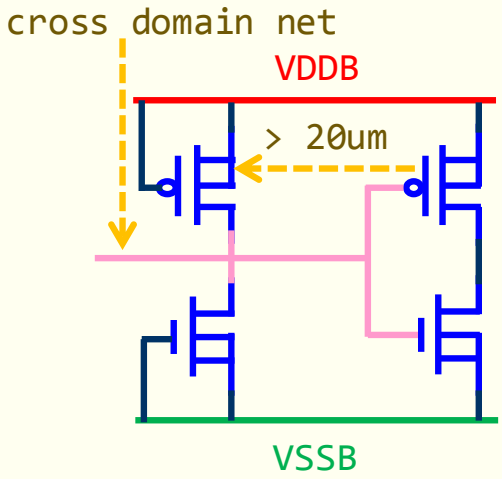


Rule 56: ESD.Cross.PG.MV.3

Return to rule list

- Description
  - Check the distance between CDM device and receiver MOS on cross domain net
- Constraints
  - The distance between GGMOS and receiver MOS should be < 20 um
  - Only check MV receiver MOS

Failed

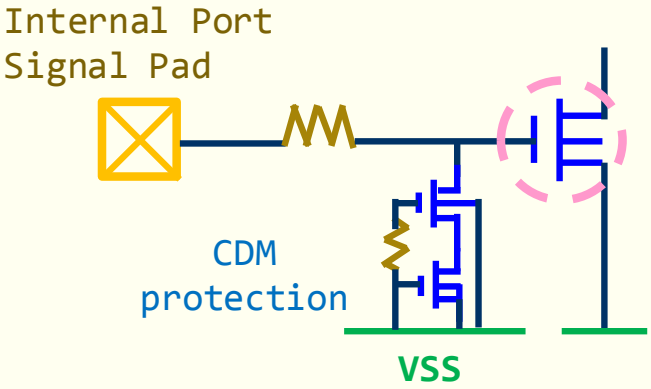


Rule 57: ESD.CDM.LV

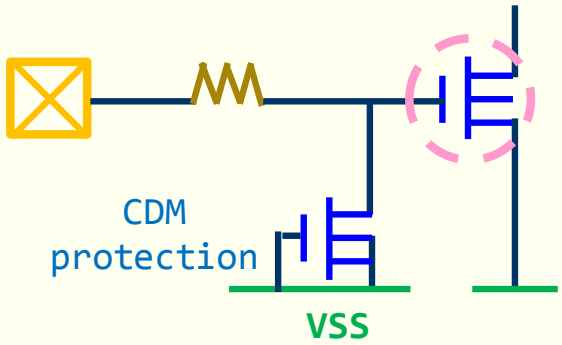
Return to rule list

- Description
  - The internal gate connected to internal port or signal pad requires resistor(s) and cascoded GGNMOS as protection device
- Constraints
  - Filter out the RC-inv-clamp structure
  - Filter out MOS which bulk connected to WAIVE_PG_NAME in .top file
  - Only check LV receiver MOS

Passed



Failed

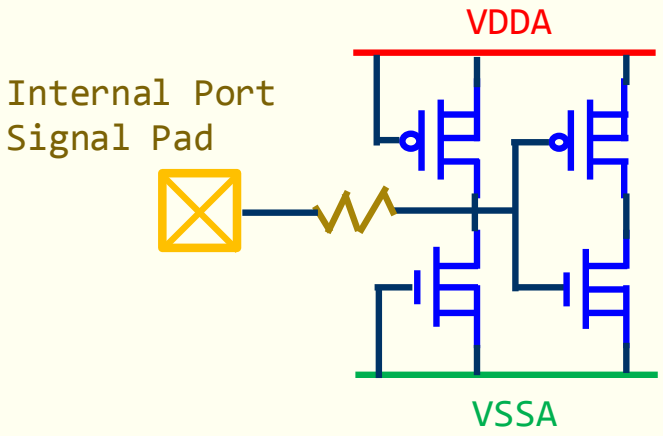


Rule 58: ESD.CDM.MV

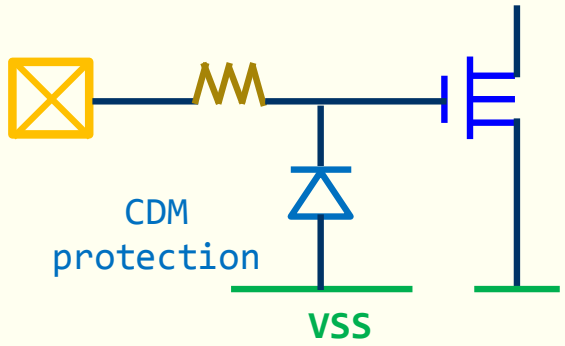
Return to rule list

- Description
  - The internal gate connected to internal port or signal pad requires resistor(s) and GGMOS as protection device
- Constraints
  - Filter out the RC-inv-clamp structure
  - Filter out MOS which bulk connected to WAIVE_PG_NAME in .top file
  - Only check MV receiver MOS

Passed



Failed

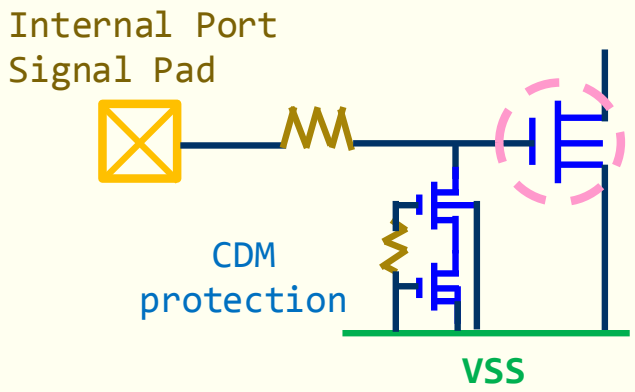


Rule 59: ESD.CDM.LV.PG

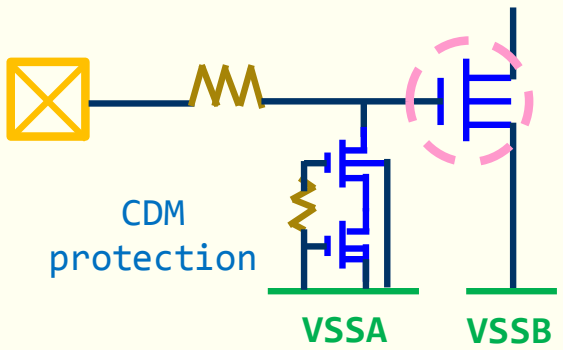
Return to rule list

- Description
  - Check the voltage source of cascoded GGNMOS and receiver connected to internal port or signal pad are identical
- Constraints
  - Filter out the RC-inv-clamp structure
  - The receiver should be connected to real P/G
  - Only check LV receiver MOS

Passed



Failed

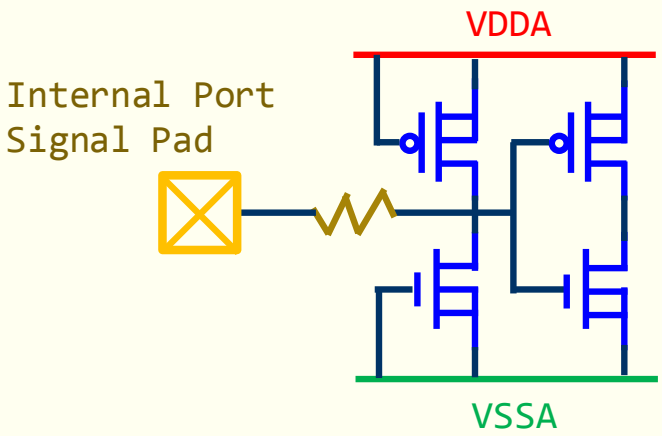


Rule 60: ESD.CDM.MV.PG

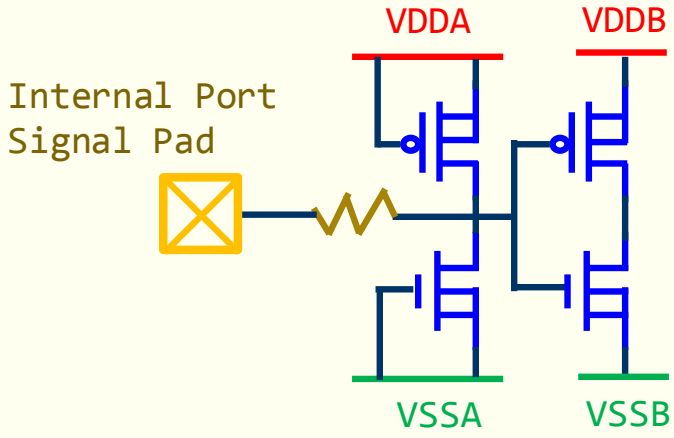
Return to rule list

- Description
  - Check the voltage source of GGMOS and receiver connected to internal port or signal pad are identical
- Constraints
  - Filter out the RC-inv-clamp structure
  - The receiver should be connected to real P/G
  - Only check MV receiver MOS

Passed



Failed

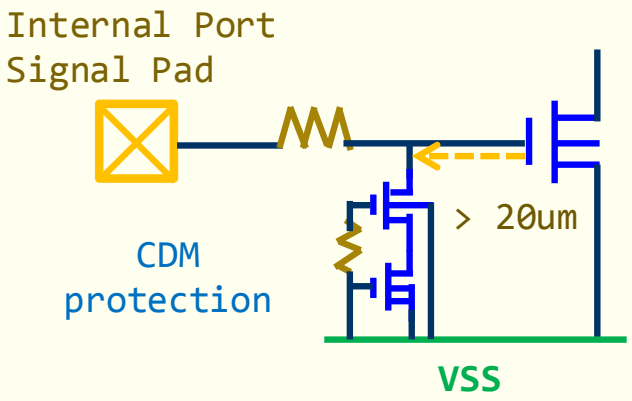


Rule 61: ESD.CDM.LV.Spc

Return to rule list

- Description
  - Check the distance between cascoded GGNMOS and receiver MOS on path of internal port or signal pad
- Constraints
  - The distance between CDM device and receiver MOS should be < 20 um
  - The receiver should be connected to real P/G
  - Only check LV receiver MOS

Failed

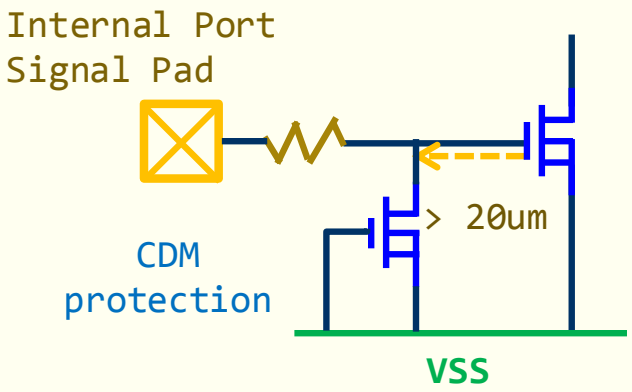


Rule 62: ESD.CDM.MV.Spc

Return to rule list

- Description
  - Check the distance between GGMOS and receiver MOS on path of internal port or signal pad
- Constraints
  - The distance between CDM device and receiver MOS should be < 20 um
  - The receiver should be connected to real P/G
  - Only check MV receiver MOS

Failed

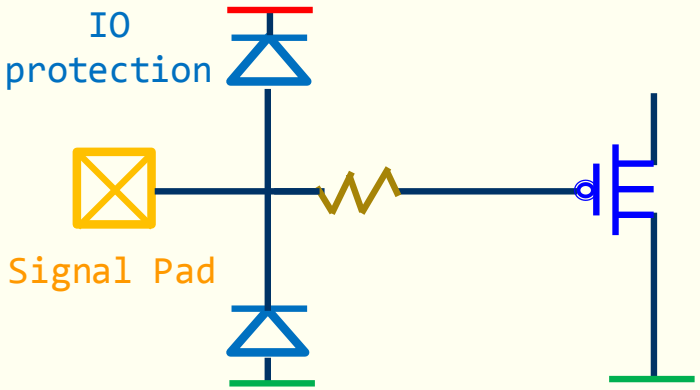


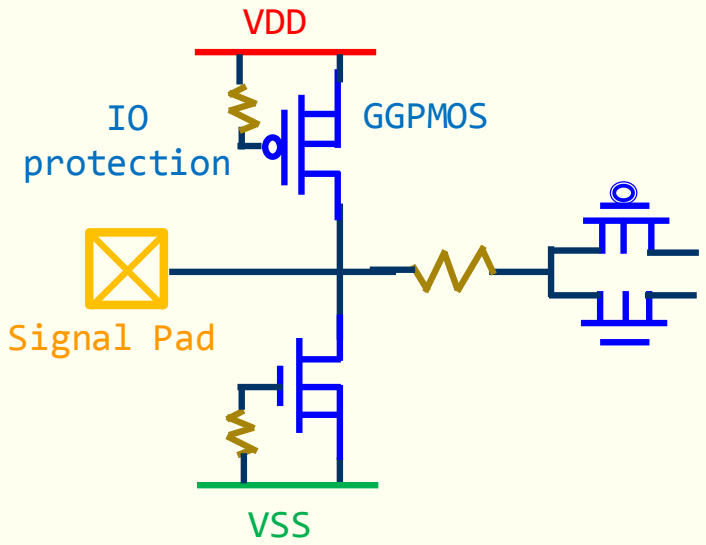
Rule 63: ESD.Sig.IO

Return to rule list

- Description
  - Check self-domain IO protection circuit (diode or GGMOS)
  - The internal gate connected to signal pad requires ESD resistor(s)
- Constraints
  - The IO protection must contain both p-type and n-type devices

Passed





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