

General Information

Date: Wed Mar 6 14:09:44 2019
Version: 2018.3 (Build 2405991 on Thu Dec 06 23:56:15 MST 2018)
Project: AES_Full
Solution: solution1
Product family: zynq
Target device: xc7z020clg400-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	11.010	1.25

Latency (clock cycles)

Summary

Latency		Interval		Type
min	max	min	max	
2	322	2	322	none

Detail

Instance

Instance	Module	Latency		Interval		Type
		min	max	min	max	
grp_AddRoundKey_fu_1964	AddRoundKey	1	1	1	1	none
grp_InvMixColumns_fu_2003	InvMixColumns	1	1	1	1	none
grp_MixColumns_fu_2025	MixColumns	1	1	1	1	none
grp_InvSubBytes_fu_2047	InvSubBytes	1	1	1	1	none
grp_SubBytes_fu_2069	SubBytes	1	1	1	1	none
grp_ShiftRows_fu_2091	ShiftRows	0	0	0	0	none
grp_InvShiftRows_fu_2111	InvShiftRows	0	0	0	0	none

Loop

N/A

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	598
FIFO	-	-	-	-
Instance	84	-	884	4786
Memory	-	-	-	-
Multiplexer	-	-	-	3605
Register	-	-	3363	-
Total	84	0	4247	8989

Available	280	220	106400	53200
Utilization (%)	30	0	3	16

Detail

Instance

Instance	Module	BRAM_18K	DSP48E	FF	LUT
AES_Full_AES_s_axi_U	AES_Full_AES_s_axi	4	0	232	216
grp_AddRoundKey_fu_1964	AddRoundKey	16	0	132	3166
grp_InvMixColumns_fu_2003	InvMixColumns	32	0	130	543
grp_InvShiftRows_fu_2111	InvShiftRows	0	0	0	0
grp_InvSubBytes_fu_2047	InvSubBytes	8	0	130	159
grp_MixColumns_fu_2025	MixColumns	16	0	130	543
grp_ShiftRows_fu_2091	ShiftRows	0	0	0	0
grp_SubBytes_fu_2069	SubBytes	8	0	130	159
Total	8	84	0	884	4786

DSP48

N/A

Memory

N/A

FIFO

N/A

Expression

Variable Name	Operation	DSP48E	FF	LUT	Bitwidth P0	Bitwidth P1
grp_fu_2195_p2	+	0	0	24	17	2
tmp_150_10_fu_4875_p2	+	0	0	23	16	5
tmp_150_11_fu_4880_p2	+	0	0	23	16	5
tmp_150_12_fu_4885_p2	+	0	0	23	16	5
tmp_150_1_fu_4825_p2	+	0	0	23	16	3
tmp_150_2_fu_4830_p2	+	0	0	23	16	3
tmp_150_3_fu_4835_p2	+	0	0	23	16	4
tmp_150_4_fu_4840_p2	+	0	0	23	16	4
tmp_150_5_fu_4845_p2	+	0	0	23	16	4
tmp_150_6_fu_4850_p2	+	0	0	23	16	4
tmp_150_7_fu_4855_p2	+	0	0	23	16	5
tmp_150_8_fu_4860_p2	+	0	0	23	16	5
tmp_150_9_fu_4865_p2	+	0	0	23	16	5
tmp_150_s_fu_4870_p2	+	0	0	23	16	5
tmp_3_fu_4820_p2	+	0	0	23	16	2
grp_fu_2344_p2	icmp	0	0	18	17	1
grp_fu_4738_p2	icmp	0	0	18	17	1
grp_fu_4744_p2	icmp	0	0	18	17	2
grp_fu_4750_p2	icmp	0	0	18	17	2
grp_fu_4756_p2	icmp	0	0	18	17	3
grp_fu_4762_p2	icmp	0	0	18	17	3
grp_fu_4768_p2	icmp	0	0	18	17	3
grp_fu_4774_p2	icmp	0	0	18	17	3
grp_fu_4780_p2	icmp	0	0	18	17	4

grp_fu_4786_p2	icmp	0	0	18	17	4
grp_fu_4792_p2	icmp	0	0	18	17	4
grp_fu_4798_p2	icmp	0	0	18	17	4
grp_fu_4804_p2	icmp	0	0	18	17	4
grp_fu_4810_p2	icmp	0	0	18	17	4
Total	29	0	0	598	479	103

☐ Multiplexer

Name	LUT	Input Size	Bits	Total Bits
ap_NS_fsm	1209	266	1	266
data_in_address0	149	33	4	132
data_out_address0	149	33	4	132
data_out_d0	149	33	8	264
grp_AddRoundKey_fu_1964_p_read	27	5	8	40
grp_AddRoundKey_fu_1964_p_read1	27	5	8	40
grp_AddRoundKey_fu_1964_p_read10	27	5	8	40
grp_AddRoundKey_fu_1964_p_read11	27	5	8	40
grp_AddRoundKey_fu_1964_p_read12	27	5	8	40
grp_AddRoundKey_fu_1964_p_read13	27	5	8	40
grp_AddRoundKey_fu_1964_p_read14	27	5	8	40
grp_AddRoundKey_fu_1964_p_read15	27	5	8	40
grp_AddRoundKey_fu_1964_p_read2	27	5	8	40
grp_AddRoundKey_fu_1964_p_read3	27	5	8	40
grp_AddRoundKey_fu_1964_p_read4	27	5	8	40
grp_AddRoundKey_fu_1964_p_read5	27	5	8	40
grp_AddRoundKey_fu_1964_p_read6	27	5	8	40
grp_AddRoundKey_fu_1964_p_read7	27	5	8	40
grp_AddRoundKey_fu_1964_p_read8	27	5	8	40
grp_AddRoundKey_fu_1964_p_read9	27	5	8	40
grp_AddRoundKey_fu_1964_round	141	31	16	496
grp_InvMixColumns_fu_2003_state_0_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_10_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_11_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_1213_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_13_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_14_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_15_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_1_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_2_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_3_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_4_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_5_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_6_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_7_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_8_read	62	15	8	120
grp_InvMixColumns_fu_2003_state_9_read	62	15	8	120
grp_InvShiftRows_fu_2111_state_0_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_10_read	15	3	8	24

grp_InvShiftRows_fu_2111_state_11_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_1213_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_13_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_14_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_15_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_1_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_2_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_3_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_4_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_5_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_6_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_7_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_8_read	15	3	8	24
grp_InvShiftRows_fu_2111_state_9_read	15	3	8	24
state_1_10_105_reg_1558	9	2	8	16
state_1_11_104_reg_1521	9	2	8	16
state_1_12_103_reg_1484	9	2	8	16
state_1_130_reg_1928	9	2	8	16
state_1_13_102_reg_1447	9	2	8	16
state_1_14_101_reg_1410	9	2	8	16
state_1_15_100_reg_1373	9	2	8	16
state_1_1_114_reg_1891	9	2	8	16
state_1_2_113_reg_1854	9	2	8	16
state_1_3_112_reg_1817	9	2	8	16
state_1_4_111_reg_1780	9	2	8	16
state_1_5_110_reg_1743	9	2	8	16
state_1_6_109_reg_1706	9	2	8	16
state_1_7_108_reg_1669	9	2	8	16
state_1_8_107_reg_1632	9	2	8	16
state_1_9_106_reg_1595	9	2	8	16
Total	3605	796	545	4490

Register

Name	Fi
Nr_read_reg_4890	16
ap_CS_fsm	265
grp_AddRoundKey_fu_1964_ap_start_reg	1
grp_InvMixColumns_fu_2003_ap_start_reg	1
grp_InvSubBytes_fu_2047_ap_start_reg	1
grp_MixColumns_fu_2025_ap_start_reg	1
grp_SubBytes_fu_2069_ap_start_reg	1
mode_cipher_read_reg_4914	1
mode_inverse_cipher_s_reg_4910	1
reg_2622	8
reg_2627	8
reg_2632	8
reg_2637	8
reg_2642	8
reg_2647	8
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reg_2652	8
reg_2657	8
reg_2662	8
reg_2667	8
reg_2672	8
reg_2677	8
reg_2682	8
reg_2687	8
reg_2692	8
reg_2697	8
reg_2702	8
reg_2711	8
reg_2720	8
reg_2729	8
reg_2738	8
reg_2747	8
reg_2756	8
reg_2765	8
reg_2774	8
reg_2783	8
reg_2792	8
reg_2801	8
reg_2810	8
reg_2819	8
reg_2828	8
reg_2837	8
reg_2846	17
reg_2850	8
reg_2856	8
reg_2862	8
reg_2868	8
reg_2874	8
reg_2880	8
reg_2886	8
reg_2892	8
reg_2898	8
reg_2904	8

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_AES_AWVALID	in	1	s_axi	AES	array
s_axi_AES_AWREADY	out	1	s_axi	AES	array
s_axi_AES_AWADDR	in	7	s_axi	AES	array
s_axi_AES_WVALID	in	1	s_axi	AES	array
s_axi_AES_WREADY	out	1	s_axi	AES	array
s_axi_AES_WDATA	in	32	s_axi	AES	array
s_axi_AES_WSTRB	in	4	s_axi	AES	array
s_axi_AES_ARVALID	in	1	s_axi	AES	array

s_axi_AES_ARREADY	out	7	s_axi	AES	array
s_axi_AES_RVALID	out	1	s_axi	AES	array
s_axi_AES_RREADY	in	1	s_axi	AES	array
s_axi_AES_RDATA	out	32	s_axi	AES	array
s_axi_AES_RRESP	out	2	s_axi	AES	array
s_axi_AES_BVALID	out	1	s_axi	AES	array
s_axi_AES_BREADY	in	1	s_axi	AES	array
s_axi_AES_BRESP	out	2	s_axi	AES	array
ap_clk	in	1	ap_ctrl_hs	AES_Full	return value
ap_rst_n	in	1	ap_ctrl_hs	AES_Full	return value
interrupt	out	1	ap_ctrl_hs	AES_Full	return value

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