Synthesis Report for 'AES_Decrypt'

General Information

Date: Wed Mar 6 13:01:03 2019

Version: 2018.3 (Build 2405991 on Thu Dec 06 23:56:15 MST 2018)

Project: AES_Decrypt
Solution: solution1
Product family: zynq

Target device: xc7z020clg400-1

Performance Estimates

☐ Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	9.441	1.25

Latency (clock cycles)

Summary

Late	ncy	Inte		
min	max	min	max	Туре
92	92	16	16	function

■ Detail

☐ Instance

		Late	ncy	Inte	rval		
Instance	Module	min	max	min	max	Туре	
grp_AddRoundKey_fu_1032	AddRoundKey	1	1	1	1	function	
grp_InvMixColumns_fu_1056	InvMixColumns	1	1	1	1	function	
grp_InvSubBytes_fu_1078	InvSubBytes	1	1	1	1	function	
grp_InvShiftRows_fu_1100	InvShiftRows	0	0	1	1	function	

- Loop

N/A

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	122	© C	6	32
Expression	858	±	0	638
FIFO	12	6	6	32
Instance	60	±	354	3621
Memory	120	6	6	32
Multiplexer	858	±		1797
Register	0	© C	2392	480
Total	60	0	2746	6536
Available	280	220	106400	53200
Utilization (%)	21	0	2	12

□ Detail

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Instance

Instance	Module	BRAM_18K	DSP48E	FF	LUT
AES_Decrypt_Decipher_s_axi_U	AES_Decrypt_Decipher_s_axi	4	0	218	212
grp_AddRoundKey_fu_1032	AddRoundKey	16	0	132	3013
grp_InvMixColumns_fu_1056	InvMixColumns	32	0	2	390
grp_InvShiftRows_fu_1100	InvShiftRows	0	0	0	0
grp_InvSubBytes_fu_1078	InvSubBytes	8	0	2	6
Total	5	60	0	354	3621

■ DSP48

N/A

■ Memory

N/A

□ FIFO

N/A

Expression

Variable Name	Operation	DSP48E	FF	LUT	Bitwidth P0	Bitwidth P1
tmp_1_fu_1521_p2	+	0	0	23	16	2
tmp_76_10_fu_1656_p2	+	0	0	23	16	5
tmp_76_11_fu_1661_p2	+	0	0	23	16	5
tmp_76_12_fu_1666_p2	+	0	0	23	16	5
tmp_76_1_fu_1541_p2	+	0	0	23	16	3
tmp_76_2_fu_1611_p2	+	0	0	23	16	3
tmp_76_3_fu_1616_p2	+	0	0	23	16	4
tmp_76_4_fu_1621_p2	+	0	0	23	16	4
tmp_76_5_fu_1626_p2	+	0	0	23	16	4
tmp_76_6_fu_1631_p2	+	0	0	23	16	4
tmp_76_7_fu_1636_p2	+	0	0	23	16	5
tmp_76_8_fu_1641_p2	+	0	0	23	16	5
tmp_76_9_fu_1646_p2	+	0	0	23	16	5
tmp_76_s_fu_1651_p2	+	0	0	23	16	5
tmp_s_fu_1529_p2	+	0	0	24	17	2
ap_block_pp0_stage0_11001	and	0	0	2	1	1
ap_predicate_op1016_call_state68_state67	and	0	0	2	1	1
ap_predicate_op1035_call_state69_state68	and	0	0	2	1	1
ap_predicate_op1089_call_state72_state71	and	0	0	2	1	1
ap_predicate_op1108_call_state73_state72	and	0	0	2	1	1
ap_predicate_op1162_call_state76_state75	and	0	0	2	1	1
ap_predicate_op1181_call_state77_state76	and	0	0	2	1	1
ap_predicate_op305_call_state26_state25	and	0	0	2	1	1
ap_predicate_op340_call_state27_state26	and	0	0	2	1	- 1
ap_predicate_op378_call_state30_state29	and	0	0	2	1	1
ap_predicate_op451_call_state34_state33	and	0	0	2	1	1
ap_predicate_op524_call_state39_state38	and	0	0	2	1	1
ap_predicate_op597_call_state43_state42	and	0	0	2	1	1
ap_predicate_op670_call_state47_state46	and	0	0	2	1	1
ap predicate op743 call state52 state51	and	0	0	2	1	-1

ap_predicate_op797_call_state55_state54	and	0	0	2	1	1
ap_predicate_op816_call_state56_state55	and	0	0	2	1	1
ap_predicate_op870_call_state59_state58	and	0	0	2	1	1
ap_predicate_op889_call_state60_state59	and	0	0	2	1	1
tmp_2_fu_1535_p2	icmp	0	0	18	17	1
tmp_78_10_fu_1596_p2	icmp	0	0	18	17	4
tmp_78_11_fu_1601_p2	icmp	0	0	18	17	4
tmp_78_12_fu_1606_p2	icmp	0	0	18	17	4
tmp_78_1_fu_1546_p2	icmp	0	0	18	17	1
tmp_78_2_fu_1551_p2	icmp	0	0	18	17	2
tmp_78_3_fu_1556_p2	icmp	0	0	18	17	2
tmp_78_4_fu_1561_p2	icmp	0	0	18	17	3
tmp_78_5_fu_1566_p2	icmp	0	0	18	17	3
tmp_78_6_fu_1571_p2	icmp	0	0	18	17	3
tmp_78_7_fu_1576_p2	icmp	0	0	18	17	3
tmp_78_8_fu_1581_p2	icmp	0	0	18	17	4
tmp_78_9_fu_1586_p2	icmp	0	0	18	17	4
tmp_78_s_fu_1591_p2	icmp	0	0	18	17	4
ap_enable_pp0	xor	0	0	2	1	2
Total	49	0	0	638	499	124

■ Multiplexer

Name	LUT
ap_NS_fsm	85
ap_enable_reg_pp0_iter0	9
ap_enable_reg_pp0_iter5	9
ap_phi_mux_state_phi_fu_445_p30	9
ap_phi_reg_pp0_iter1_state_10_63_reg_663	9
ap_phi_reg_pp0_iter1_state_11_62_reg_626	9
ap_phi_reg_pp0_iter1_state_12_61_reg_589	9
ap_phi_reg_pp0_iter1_state_13_60_reg_552	9
ap_phi_reg_pp0_iter1_state_14_59_reg_515	9
ap_phi_reg_pp0_iter1_state_15_58_reg_478	9
ap_phi_reg_pp0_iter1_state_1_72_reg_996	9
ap_phi_reg_pp0_iter1_state_2_71_reg_959	9
ap_phi_reg_pp0_iter1_state_3_70_reg_922	9
ap_phi_reg_pp0_iter1_state_4_69_reg_885	9
ap_phi_reg_pp0_iter1_state_5_68_reg_848	9
ap_phi_reg_pp0_iter1_state_6_67_reg_811	9
ap_phi_reg_pp0_iter1_state_7_66_reg_774	9
ap_phi_reg_pp0_iter1_state_8_65_reg_737	9
ap_phi_reg_pp0_iter1_state_9_64_reg_700	9
ap_phi_reg_pp0_iter1_state_reg_442	9
ap_phi_reg_pp0_iter2_state_10_63_reg_663	9
ap_phi_reg_pp0_iter2_state_11_62_reg_626	9
ap_phi_reg_pp0_iter2_state_12_61_reg_589	9
ap_phi_reg_pp0_iter2_state_13_60_reg_552	9
ap_phi_reg_pp0_iter2_state_14_59_reg_515	9
ap_phi_reg_pp0_iter2_state_15_58_reg_478	9

ap_phi_reg_pp0_iter2_state_1_72_reg_996	9
ap_phi_reg_pp0_iter2_state_2_71_reg_959	9
ap_phi_reg_pp0_iter2_state_3_70_reg_922	9
ap_phi_reg_pp0_iter2_state_4_69_reg_885	9
ap_phi_reg_pp0_iter2_state_5_68_reg_848	9
ap_phi_reg_pp0_iter2_state_6_67_reg_811	9
ap_phi_reg_pp0_iter2_state_7_66_reg_774	9
ap_phi_reg_pp0_iter2_state_8_65_reg_737	9
ap_phi_reg_pp0_iter2_state_9_64_reg_700	9
ap_phi_reg_pp0_iter2_state_reg_442	9
ap_phi_reg_pp0_iter3_state_10_63_reg_663	9
ap_phi_reg_pp0_iter3_state_11_62_reg_626	9
ap_phi_reg_pp0_iter3_state_12_61_reg_589	9
ap_phi_reg_pp0_iter3_state_13_60_reg_552	9
ap_phi_reg_pp0_iter3_state_14_59_reg_515	9
ap_phi_reg_pp0_iter3_state_15_58_reg_478	9
ap_phi_reg_pp0_iter3_state_1_72_reg_996	9
ap_phi_reg_pp0_iter3_state_2_71_reg_959	9
ap_phi_reg_pp0_iter3_state_3_70_reg_922	9
ap_phi_reg_pp0_iter3_state_4_69_reg_885	9
ap_phi_reg_pp0_iter3_state_5_68_reg_848	9
ap_phi_reg_pp0_iter3_state_6_67_reg_811	9
ap_phi_reg_pp0_iter3_state_7_66_reg_774	9
ap_phi_reg_pp0_iter3_state_8_65_reg_737	9
ap_phi_reg_pp0_iter3_state_9_64_reg_700	9
ap_phi_reg_pp0_iter3_state_reg_442	9

■ Register

Name	
Nr_read_reg_1826	
ap_CS_fsm	
ap_enable_reg_pp0_iter0_reg	
ap_enable_reg_pp0_iter1	
ap_enable_reg_pp0_iter2	
ap_enable_reg_pp0_iter3	
ap_enable_reg_pp0_iter4	
ap_enable_reg_pp0_iter5	
ap_phi_reg_pp0_iter1_state_10_63_reg_663	
ap_phi_reg_pp0_iter1_state_11_62_reg_626	
ap_phi_reg_pp0_iter1_state_12_61_reg_589	
ap_phi_reg_pp0_iter1_state_13_60_reg_552	
ap_phi_reg_pp0_iter1_state_14_59_reg_515	
ap_phi_reg_pp0_iter1_state_15_58_reg_478	
ap_phi_reg_pp0_iter1_state_1_72_reg_996	
ap_phi_reg_pp0_iter1_state_2_71_reg_959	
ap_phi_reg_pp0_iter1_state_3_70_reg_922	
ap_phi_reg_pp0_iter1_state_4_69_reg_885	
ap_phi_reg_pp0_iter1_state_5_68_reg_848	
ap_phi_reg_pp0_iter1_state_6_67_reg_811	
ap_phi_reg_pp0_iter1_state_7_66_reg_774	

ap_phi_reg_pp0_iter1_state_8_65_reg_737	
ap_phi_reg_pp0_iter1_state_9_64_reg_700	
ap_phi_reg_pp0_iter1_state_reg_442	
ap_phi_reg_pp0_iter2_state_10_63_reg_663	
ap_phi_reg_pp0_iter2_state_11_62_reg_626	
ap_phi_reg_pp0_iter2_state_12_61_reg_589	
ap_phi_reg_pp0_iter2_state_13_60_reg_552	
ap_phi_reg_pp0_iter2_state_14_59_reg_515	
ap_phi_reg_pp0_iter2_state_15_58_reg_478	
ap_phi_reg_pp0_iter2_state_1_72_reg_996	
ap_phi_reg_pp0_iter2_state_2_71_reg_959	
ap_phi_reg_pp0_iter2_state_3_70_reg_922	
ap_phi_reg_pp0_iter2_state_4_69_reg_885	
ap_phi_reg_pp0_iter2_state_5_68_reg_848	
ap_phi_reg_pp0_iter2_state_6_67_reg_811	
ap_phi_reg_pp0_iter2_state_7_66_reg_774	
ap_phi_reg_pp0_iter2_state_8_65_reg_737	
ap_phi_reg_pp0_iter2_state_9_64_reg_700	
ap_phi_reg_pp0_iter2_state_reg_442	
ap_phi_reg_pp0_iter3_state_10_63_reg_663	
ap_phi_reg_pp0_iter3_state_11_62_reg_626	
ap_phi_reg_pp0_iter3_state_12_61_reg_589	
ap_phi_reg_pp0_iter3_state_13_60_reg_552	
ap_phi_reg_pp0_iter3_state_14_59_reg_515	
ap_phi_reg_pp0_iter3_state_15_58_reg_478	
ap_phi_reg_pp0_iter3_state_1_72_reg_996	
ap_phi_reg_pp0_iter3_state_2_71_reg_959	
ap_phi_reg_pp0_iter3_state_3_70_reg_922	
ap_phi_reg_pp0_iter3_state_4_69_reg_885	
ap_phi_reg_pp0_iter3_state_5_68_reg_848	
ap_phi_reg_pp0_iter3_state_6_67_reg_811	

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_Decipher_AWVALID	in	1	s_axi	Decipher	array
s_axi_Decipher_AWREADY	out	1	s_axi	Decipher	array
s_axi_Decipher_AWADDR	in	6	s_axi	Decipher	array
s_axi_Decipher_WVALID	in	1	s_axi	Decipher	array
s_axi_Decipher_WREADY	out	1	s_axi	Decipher	array
s_axi_Decipher_WDATA	in	32	s_axi	Decipher	array
s_axi_Decipher_WSTRB	in	4	s_axi	Decipher	array
s_axi_Decipher_ARVALID	in	1	s_axi	Decipher	array
s_axi_Decipher_ARREADY	out	1	s_axi	Decipher	array
s_axi_Decipher_ARADDR	in	6	s_axi	Decipher	array
s_axi_Decipher_RVALID	out	1	s_axi	Decipher	array
s_axi_Decipher_RREADY	in	1	s_axi	Decipher	array
s_axi_Decipher_RDATA	out	32	s_axi	Decipher	array
s_axi_Decipher_RRESP	out	2	s_axi	Decipher	array

s_axi_Decipher_BVALID	out	1	s_axi	Decipher	array
s_axi_Decipher_BREADY	in	1	s_axi	Decipher	array
s_axi_Decipher_BRESP	out	2	s_axi	Decipher	array
ap_clk	in	1	ap_ctrl_hs	AES_Decrypt	return value
ap_rst_n	in	1	ap_ctrl_hs	AES_Decrypt	return value
interrupt	out	1	ap_ctrl_hs	AES_Decrypt	return value

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