Synthesis Report for 'AES_Full'

General Information

Date:	Sun Nov 11 20:53:53 2018
Version:	2018.2.2 (Build 2345119 on Mon Oct 01 18:48:11 MDT 2018)
Project:	aes_full
Solution:	full
Product family:	zynq
Target device:	xc7z020clg400-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	6.67	6.566	0.00

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
?	?	?	?	none

Detail

- Instance
- Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	321
FIFO	-	-	-	-
Instance	22	-	926	4373
Memory	2	-	0	0
Multiplexer	-	-	-	736
Register	-	-	290	-
Total	24	0	1216	5430
Available	280	220	106400	53200
Utilization (%)	8	0	1	10

Detail

- Instance
- DSP48
- Memory
- FIFO
- Expression
- Multiplexer
- Register

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_CRTLS_AWVALID	in	1	s_axi	CRTLS	array

s_axi_CRTLS_AWREADY	out	1	s_axi	CRTLS	array
s_axi_CRTLS_AWADDR	in	10	s_axi	CRTLS	array
s_axi_CRTLS_WVALID	in	1	s_axi	CRTLS	array
s_axi_CRTLS_WREADY	out	1	s_axi	CRTLS	array
s_axi_CRTLS_WDATA	in	32	s_axi	CRTLS	array
s_axi_CRTLS_WSTRB	in	4	s_axi	CRTLS	array
s_axi_CRTLS_ARVALID	in	1	s_axi	CRTLS	array
s_axi_CRTLS_ARREADY	out	1	s_axi	CRTLS	array
s_axi_CRTLS_ARADDR	in	10	s_axi	CRTLS	array
s_axi_CRTLS_RVALID	out	1	s_axi	CRTLS	array
s_axi_CRTLS_RREADY	in	1	s_axi	CRTLS	array
s_axi_CRTLS_RDATA	out	32	s_axi	CRTLS	array
s_axi_CRTLS_RRESP	out	2	s_axi	CRTLS	array
s_axi_CRTLS_BVALID	out	1	s_axi	CRTLS	array
s_axi_CRTLS_BREADY	in	1	s_axi	CRTLS	array
s_axi_CRTLS_BRESP	out	2	s_axi	CRTLS	array
ap_clk	in	1	ap_ctrl_hs	AES_Full	return value
ap_rst_n	in	1	ap_ctrl_hs	AES_Full	return value
interrupt	out	1	ap_ctrl_hs	AES_Full	return value

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