Synthesis Report for 'AES_Full'

General Information

Date: Mon Feb 11 19:33:39 2019
Version: 2018.3 (Build 2405991 on Thu Dec 06 23:56:15 MST 2018)
Project: aes_full
Solution: solution1
Product family: zynq
Target device: xc7z020clg400-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	8.00	6.987	0.40

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
?	?	?	?	none

Detail

Instance

		Latency		Interval		
Instance	Module	min	max	min	max	Type
grp_AddRoundKey_fu_1757	AddRoundKey	0	0	1	1	function
grp_InvMixColumns_fu_1877	InvMixColumns	1	1	1	1	function
grp_MixColumns_fu_1899	MixColumns	1	1	1	1	function
grp_InvSubBytes_fu_1921	InvSubBytes	1	1	1	1	function
grp_SubBytes_fu_1943	SubBytes	1	1	1	1	function
call_ret3_ShiftRows_fu_1981	ShiftRows	0	0	1	1	function
call_ret7_InvShiftRows_fu_2001	InvShiftRows	0	0	1	1	function

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- L_rounds	?	?	17	16	1	?	yes
- L_rounds	?	?	19	16	1	?	yes

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	1376
FIFO	-	-	-	-
Instance	70	-	448	1198
Memory	-	-	-	-

Multiplexer	-	-	-	2142
Register	-	-	1286	-
Total	70	0	1734	4716
Available	280	220	106400	53200
Utilization (%)	25	0	1	8

Detail

Instance

Instance	Module	BRAM_18K	DSP48E	FF	LUT
AES_Full_CRTLS_s_axi_U	AES_Full_CRTLS_s_axi	6	0	312	286
grp_AddRoundKey_fu_1757	AddRoundKey	0	0	0	128
grp_InvMixColumns_fu_1877	InvMixColumns	32	0	2	388
call_ret7_InvShiftRows_fu_2001	InvShiftRows	0	0	0	0
grp_InvSubBytes_fu_1921	InvSubBytes	8	0	2	4
grp_MixColumns_fu_1899	MixColumns	16	0	130	388
call_ret3_ShiftRows_fu_1981	ShiftRows	0	0	0	0
grp_SubBytes_fu_1943	SubBytes	8	0	2	4
Total	8	70	0	448	1198

DSP48

N/A

Memory

N/A

FIFO

N/A

Expression

Variable Name	Operation	DSP48E	FF	LUT	Bitwidth P0	Bitwidth P1
grp_fu_2085_p2	+	0	0	24	17	2
j_1_fu_3086_p2	+	0	0	23	16	1
j_fu_2442_p2	+	0	0	23	16	1
tmp_144_10_fu_2809_p2	+	0	0	28	21	5
tmp_144_11_fu_2819_p2	+	0	0	28	21	5
tmp_144_12_fu_2829_p2	+	0	0	28	21	5
tmp_144_13_fu_2645_p2	+	0	0	28	21	5
tmp_144_14_fu_2719_p2	+	0	0	28	21	5
tmp_144_1_fu_2481_p2	+	0	0	28	21	5
tmp_144_2_fu_2635_p2	+	0	0	28	21	5
tmp_144_3_fu_2729_p2	+	0	0	28	21	5
tmp_144_4_fu_2739_p2	+	0	0	28	21	5
tmp_144_5_fu_2749_p2	+	0	0	28	21	5
tmp_144_6_fu_2759_p2	+	0	0	28	21	5
tmp_144_7_fu_2769_p2	+	0	0	28	21	5
tmp_144_8_fu_2779_p2	+	0	0	28	21	5
tmp_144_9_fu_2789_p2	+	0	0	28	21	5
tmp_144_s_fu_2799_p2	+	0	0	28	21	5
tmp_165_10_fu_3230_p2	+	0	0	29	22	4
tmp_165_11_fu_3240_p2	+	0	0	29	22	4
tmp_165_12_fu_3250_p2	+	0	0	29	22	3

tmp_165_13_fu_3260_p2	+	0	0	29	22	3
tmp_165_14_fu_3350_p2	+	0	0	29	22	2
tmp_165_1_fu_3130_p2	+	0	0	29	22	5
tmp_165_2_fu_3140_p2	+	0	0	29	22	5
tmp_165_3_fu_3150_p2	+	0	0	29	22	5
tmp_165_4_fu_3160_p2	+	0	0	29	22	5
tmp_165_5_fu_3170_p2	+	0	0	29	22	5
tmp_165_6_fu_3180_p2	+	0	0	29	22	5
tmp_165_7_fu_3190_p2	+	0	0	29	22	5
tmp_165_8_fu_3200_p2	+	0	0	29	22	5
tmp_165_9_fu_3210_p2	+	0	0	29	22	4
tmp_165_s_fu_3220_p2	+	0	0	29	22	4
tmp_6_fu_2470_p2	+	0	0	28	21	5
tmp_9_fu_3113_p2	+	0	0	29	22	6
tmp_8_fu_3096_p2	-	0	0	24	17	17
ap_condition_399	and	0	0	2	1	1
ap_predicate_op317_call_state21_state33	and	0	0	2	1	1
exitcond_i1_fu_3081_p2	icmp	0	0	13	16	16
exitcond_i_fu_2437_p2	icmp	0	0	13	16	16
tmp_11_fu_3124_p2	icmp	0	0	18	17	17
tmp_1_fu_2452_p2	icmp	0	0	18	17	17
tmp_153_10_fu_2951_p2	or	0	0	20	20	4
tmp_153_11_fu_2961_p2	or	0	0	20	20	4
tmp_153_12_fu_2971_p2	or	0	0	20	20	4
tmp_153_13_fu_2981_p2	or	0	0	20	20	4
tmp_153_14_fu_2991_p2	or	0	0	20	20	4
tmp_153_1_fu_2861_p2	or	0	0	20	20	2
tmp_153_2_fu_2871_p2	or	0	0	20	20	2
tmp_153_3_fu_2881_p2	or	0	0	20	20	3
tmp_153_4_fu_2891_p2	or	0	0	20	20	3
tmp_153_5_fu_2901_p2	or	0	0	20	20	3
tmp_153_6_fu_2911_p2	or	0	0	20	20	3
tmp_153_7_fu_2921_p2	or	0	0	20	20	4
tmp_153_8_fu_2931_p2	or	0	0	20	20	4
tmp_153_9_fu_2941_p2	or	0	0	20	20	4
tmp_153_s_fu_2851_p2	or	0	0	20	20	1
ap_enable_pp0	xor	0	0	2	1	2
ap_enable_pp1	xor	0	0	2	1	2
Total	59	0	0	1376	1124	292

Multiplexer

Name	LUT	Input Size	Bits	Total Bits
ap_NS_fsm	433	98	1	98
ap_enable_reg_pp0_iter1	9	2	1	2
ap_enable_reg_pp1_iter1	9	2	1	2
ap_phi_mux_j_0_i1_phi_fu_1750_p4	9	2	16	32
ap_phi_mux_j_0_i_phi_fu_1595_p4	9	2	16	32
ap_phi_reg_pp0_iter1_state_0_1_43_reg_1737	9	2	8	16
ap_phi_reg_pp0_iter1_state_10_1_33_reg_1647	9	2	8	16

ap_phi_reg_pp0_iter1_state_11_1_32_reg_1638	9	2	8	16
ap_phi_reg_pp0_iter1_state_12_1_31_reg_1629	9	2	8	16
ap_phi_reg_pp0_iter1_state_13_1_30_reg_1620	9	2	8	16
ap_phi_reg_pp0_iter1_state_14_1_29_reg_1611	9	2	8	16
ap_phi_reg_pp0_iter1_state_15_1_28_reg_1602	9	2	8	16
ap_phi_reg_pp0_iter1_state_1_1_42_reg_1728	9	2	8	16
ap_phi_reg_pp0_iter1_state_2_1_41_reg_1719	9	2	8	16
ap_phi_reg_pp0_iter1_state_3_1_40_reg_1710	9	2	8	16
ap_phi_reg_pp0_iter1_state_4_1_39_reg_1701	9	2	8	16
ap_phi_reg_pp0_iter1_state_5_1_38_reg_1692	9	2	8	16
ap_phi_reg_pp0_iter1_state_6_1_37_reg_1683	9	2	8	16
ap_phi_reg_pp0_iter1_state_7_1_36_reg_1674	9	2	8	16
ap_phi_reg_pp0_iter1_state_8_1_35_reg_1665	9	2	8	16
ap_phi_reg_pp0_iter1_state_9_1_34_reg_1656	9	2	8	16
data_in_address0	149	33	4	132
data_out_address0	149	33	4	132
data_out_d0	149	33	8	264
expandedKey_address0	293	65	8	520
grp_AddRoundKey_fu_1757_p_read19	15	3	8	24
grp_AddRoundKey_fu_1757_p_read20	15	3	8	24
grp_AddRoundKey_fu_1757_p_read21	15	3	8	24
grp_AddRoundKey_fu_1757_p_read22	15	3	8	24
grp_AddRoundKey_fu_1757_p_read23	15	3	8	24
grp_AddRoundKey_fu_1757_p_read24	15	3	8	24
grp_AddRoundKey_fu_1757_p_read25	15	3	8	24
grp_AddRoundKey_fu_1757_p_read26	15	3	8	24
grp_AddRoundKey_fu_1757_p_read27	15	3	8	24
grp_AddRoundKey_fu_1757_p_read28	15	3	8	24
grp_AddRoundKey_fu_1757_p_read29	15	3	8	24
grp_AddRoundKey_fu_1757_p_read30	15	3	8	24
grp_AddRoundKey_fu_1757_p_read31	15	3	8	24
grp_AddRoundKey_fu_1757_state_0_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_10_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_11_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_1213_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_13_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_14_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_15_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_1_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_2_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_3_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_4_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_5_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_6_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_7_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_8_read	21	4	8	32
grp_AddRoundKey_fu_1757_state_9_read	21	4	8	32
j_0_i1_reg_1746	9	2	16	32

j_0_i_reg_1591	9	2	16	32
state_0_12_fu_214	15	3	8	24
state_10_12_fu_254	15	3	8	24
state_11_12_fu_258	15	3	8	24
state_12_12_fu_262	15	3	8	24
state_13_12_fu_266	15	3	8	24
state_14_12_fu_270	15	3	8	24
state_15_12_fu_274	15	3	8	24
state_1_12_fu_218	15	3	8	24
state_2_12_fu_222	15	3	8	24
state_3_12_fu_226	15	3	8	24
state_4_12_fu_230	15	3	8	24
state_5_12_fu_234	15	3	8	24
state_6_12_fu_238	15	3	8	24
state_7_12_fu_242	15	3	8	24
state_8_12_fu_246	15	3	8	24
state_9_12_fu_250	15	3	8	24
Total	2142	457	579	2742

Register

Name	FF	LUT	Bits	Const Bits
Nr_read_reg_3664	16	0	16	0
ap_CS_fsm	97	0	97	0
ap_enable_reg_pp0_iter0	1	0	1	0
ap_enable_reg_pp0_iter1	1	0	1	0
ap_enable_reg_pp1_iter0	1	0	1	0
ap_enable_reg_pp1_iter1	1	0	1	0
ap_phi_reg_pp0_iter0_state_0_1_43_reg_1737	8	0	8	0
ap_phi_reg_pp0_iter0_state_10_1_33_reg_1647	8	0	8	0
ap_phi_reg_pp0_iter0_state_11_1_32_reg_1638	8	0	8	0
ap_phi_reg_pp0_iter0_state_12_1_31_reg_1629	8	0	8	0
ap_phi_reg_pp0_iter0_state_13_1_30_reg_1620	8	0	8	0
ap_phi_reg_pp0_iter0_state_14_1_29_reg_1611	8	0	8	0
ap_phi_reg_pp0_iter0_state_15_1_28_reg_1602	8	0	8	0
ap_phi_reg_pp0_iter0_state_1_1_42_reg_1728	8	0	8	0
ap_phi_reg_pp0_iter0_state_2_1_41_reg_1719	8	0	8	0
ap_phi_reg_pp0_iter0_state_3_1_40_reg_1710	8	0	8	0
ap_phi_reg_pp0_iter0_state_4_1_39_reg_1701	8	0	8	0
ap_phi_reg_pp0_iter0_state_5_1_38_reg_1692	8	0	8	0
ap_phi_reg_pp0_iter0_state_6_1_37_reg_1683	8	0	8	0
ap_phi_reg_pp0_iter0_state_7_1_36_reg_1674	8	0	8	0
ap_phi_reg_pp0_iter0_state_8_1_35_reg_1665	8	0	8	0
ap_phi_reg_pp0_iter0_state_9_1_34_reg_1656	8	0	8	0
ap_phi_reg_pp0_iter1_state_0_1_43_reg_1737	8	0	8	0
ap_phi_reg_pp0_iter1_state_10_1_33_reg_1647	8	0	8	0
ap_phi_reg_pp0_iter1_state_11_1_32_reg_1638	8	0	8	0
ap_phi_reg_pp0_iter1_state_12_1_31_reg_1629	8	0	8	0
ap_phi_reg_pp0_iter1_state_13_1_30_reg_1620	8	0	8	0
ap_phi_reg_pp0_iter1_state_14_1_29_reg_1611	8	0	8	0

ap_phi_reg_pp0_iter1_state_15_1_28_reg_1602	8	0	8	0
ap_phi_reg_pp0_iter1_state_1_1_42_reg_1728	8	0	8	0
ap_phi_reg_pp0_iter1_state_2_1_41_reg_1719	8	0	8	0
ap_phi_reg_pp0_iter1_state_3_1_40_reg_1710	8	0	8	0
ap_phi_reg_pp0_iter1_state_4_1_39_reg_1701	8	0	8	0

Interface

Summary

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_CRTLS_AWVALID	in	1	s_axi	CRTLS	array
s_axi_CRTLS_AWREADY	out	1	s_axi	CRTLS	array
s_axi_CRTLS_AWADDR	in	10	s_axi	CRTLS	array
s_axi_CRTLS_WVALID	in	1	s_axi	CRTLS	array
s_axi_CRTLS_WREADY	out	1	s_axi	CRTLS	array
s_axi_CRTLS_WDATA	in	32	s_axi	CRTLS	array
s_axi_CRTLS_WSTRB	in	4	s_axi	CRTLS	array
s_axi_CRTLS_ARVALID	in	1	s_axi	CRTLS	array
s_axi_CRTLS_ARREADY	out	1	s_axi	CRTLS	array
s_axi_CRTLS_ARADDR	in	10	s_axi	CRTLS	array
s_axi_CRTLS_RVALID	out	1	s_axi	CRTLS	array
s_axi_CRTLS_RREADY	in	1	s_axi	CRTLS	array
s_axi_CRTLS_RDATA	out	32	s_axi	CRTLS	array
s_axi_CRTLS_RRESP	out	2	s_axi	CRTLS	array
s_axi_CRTLS_BVALID	out	1	s_axi	CRTLS	array
s_axi_CRTLS_BREADY	in	1	s_axi	CRTLS	array
s_axi_CRTLS_BRESP	out	2	s_axi	CRTLS	array
ap_clk	in	1	ap_ctrl_hs	AES_Full	return value
ap_rst_n	in	1	ap_ctrl_hs	AES_Full	return value
interrupt	out	1	ap_ctrl_hs	AES_Full	return value

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