Development of front-end readout electronics for silicon strip detectors

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Abstract: Front-end readout electronics have been developed for silicon strip detectors at our institute. In this system an Application Specific Integrated Circuit (ASIC) ATHED is used to realize multi-channel energy and time measurements. The slow control of ASIC chips is achieved by parallel port and the timing control signals of ASIC chips are implemented with the CPLD. The data acquisition is carried out with a PXI-DAQ card. The software has a user-friendly GUI developed with LabWindows/CVI in the Windows XP operating system. The test results show that the energy resolution is about 1.14% for alpha at 5.48 MeV and the maximum channel crosstalk of the system is 4.60%. The performance of the system is very reliable and is suitable for nuclear physics experiments.

Key words: front-end readout electronics，ASIC，PXI-DAQ

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1 Introduction

With the development of the silicon strip detector, it is now widely used in nuclear physics, high energy physics, astrophysics, and so on. Over the last decade, almost all high energy physics and nuclear physics laboratories in the world use it as a vertex detector, such as the ANKE spectrometer at the COoler SYnchrotron COSY Juelich [1], the tracking system of ALICE [2] , and the tracking measurement system of GLAST [3]. At the External Target Facility of Heavy Ion Research Facility in Lanzhou (HIRFL-ETF), silicon strip detectors will be equipped in the detection system. Because of the large number of channels, one highly integrated, low power electronics system is required to be developed. Based on the experimental requirement, a front-end readout electronics system has been developed by using an Application Specific Integrated Circuit (ASIC) ATHED. In this system an analog board can implement energy and time (E and T) measurement of multiple channels [4], and the readout is based on a PXI data acquisition (DAQ) card, which can meet the requirements of a high counting rate and a large number of readout channels [5]. The minimum readout time for 48 channels of output energy and time information is less than 32 μs.

In this paper, Section 2 describes the readout electronics. Section 3 introduces the DAQ. Performance of this system is presented in Section 4. Section 5 gives a brief summary.

2 Readout electronics

As shown in Fig. 1 the readout electronics consist of two identical analog boards (see the dashed boxs in Fig. 1), a digital board, a DAQ card (NI-6133) and a PXI chassis. A total of 6 ATHEDs are distributed on the two analog boards, which process 96 channels E and T from silicon strip detectors. To effectively reduce the crosstalk between the analog board and the digital board, the flat twisted-pair cables are used for data transfer and communications [6]. The digital board implements the slow control, analog output signal adapting, fast timing pulse generating, and the function interfacing to NI-6133. The DAQ card realizes the data acquisition of output signal.

2.1 ATHED description

ATHED is a 16-channel ASIC chip developed by Saclay for processing the E and T signals from silicon strip, Si(Li) and CsI detectors. The chip can deliver three types of information for each channel: deposited energy of the detected particle, time of flight and value of the DC leakage current. The block diagram of one channel of ATHED is shown in Fig. 2. The first stage of the channel is a charge sensitive amplifier (CSA) followed

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by energy and timing branches. In the readout phase, the analog energy and time information of sixteen channels will be transmitted through a Voltage to Current Converter (VCC) to the adapting circuit on the digital board. It will be possible to read only one of sixteen channels under each clock pulse. The transfer function of VCC is ±2 mA per output (differential outputs). The read out frequency is 2 MHz maximum. The slow control of ATHED is defined and based on the standard serial bus ^{I2}C.

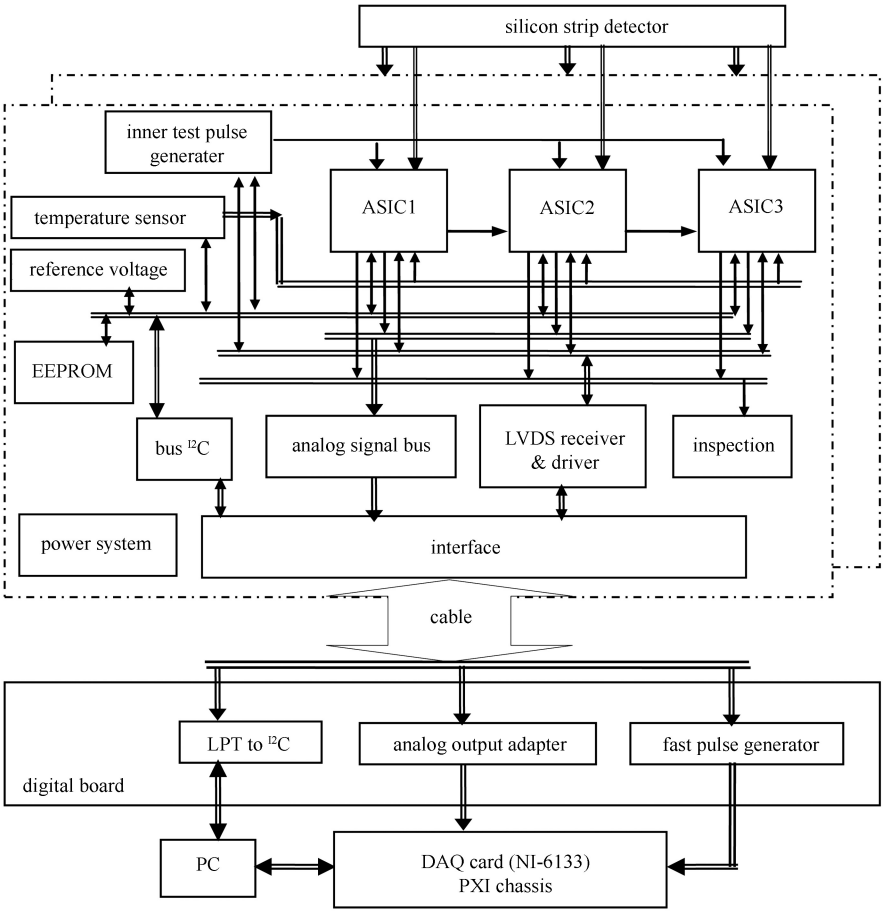

Fig. 1. Architecture of the readout electronics.

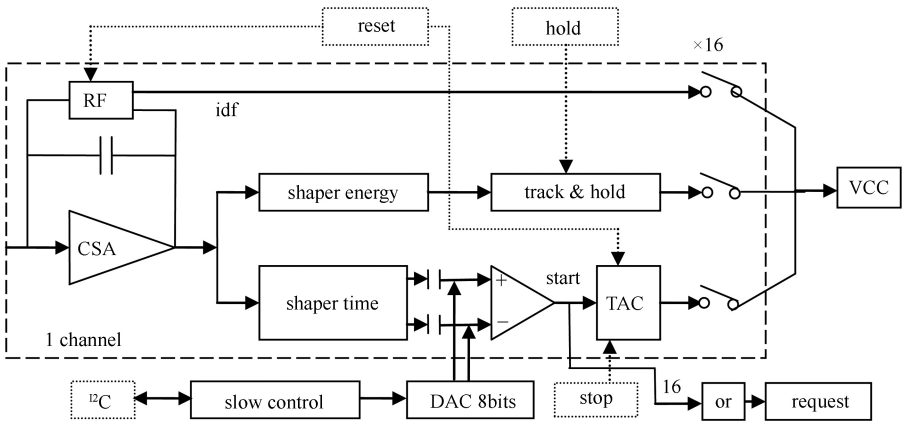

Fig. 2. One channel schematic diagram of ATHED.

2.2 Analog board

The analog board is composed of an input buffer, ASIC chips, test signal generator, reference voltage generator, LVDS (Low Voltage Differential Signal) transceivers, environmental temperature monitoring circuit, and memory cell (EEPROM). Each analog board carries three ASIC chips, and each of them can process 16 channels of energy and 16 channels of time signals. The outputs are carried out on one analogue line per board and sent in a current-differential mode to the external digital board. The test signal generator on the board is a programmable pulse generator, and it can check the operation function of all the ASIC chips and can do a calibration for each channel. A single calibration capacitor is used, so the injected charge is the same for all channels of the three ASIC chips.

All readout and control signals from the analog board are transmitted in LVDS standard to guarantee a good immunity against the electromagnetic interference. The trigger signal-Request (Req), which is generated by the ASIC chips, is transferred in a point-to-point configuration in which it provides the best signal quality due to the clear path. The control signals including Start，Stop，Hold and Reset are used in a multi-drop configuration. In this configuration, a driver can connect multiple receivers, so the same date can be sent to several loads.

2.3 Digital board

The digital board is composed of a slow control, analog output adapting unit, and a fast timing pulse generating circuit.

Because the electrical characteristics of the computer parallel port can meet the requirement of the ^{I2}C bus, we use it as ^{I2}C bus master interface for the communication between PC and ^{I2}C bus devices. The program is completed based on the Labwindows/CVI platform. The system library of LabWindows/CVI provides the functions which can be directly used to read and write the PC parallel port as the hardware port. So the PC parallel port is used as the input and output of SDA and SCL, and we can realize the function to send the ^{I2}C start signal, ^{I2}C stop signal, response, data, and receive data, etc. The slow control is assured via the ^{I2}C industrial protocol. By slow control it can be configured, including the operational mode of the ASIC chips, the setting of the temperature monitoring chip, the test signal injection, the choosing of test channels, the board identification and the memorization of experiment parameters. We use bus buffers (model: P82B96) to achieve the cascading of slow control between the two analog boards.

The fast timing signal generation unit is developed based on an Altera MAX Ⅱ device (model: EPM1270T144), and using Quartus to realize the software design. The main function of this circuit is to generate the necessary external fast timing pulse signal, which can make the front-end ASIC chips work normally and provide the external timing clock and trigger signals to perform data acquisition. Fig. 3 shows the time sequence diagram.

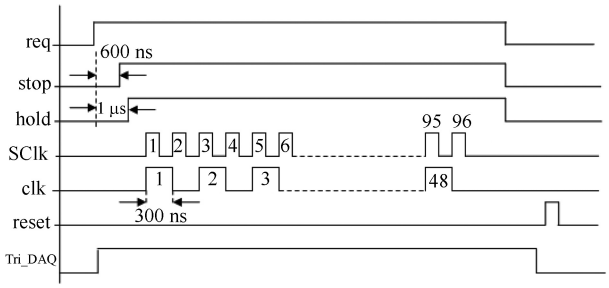

Fig. 3. The time sequence diagram generated by a fast timing signal module.

The analog output adapting unit is composed of a I-V converter, amplitude modulation unit, filter, etc. The differential current signal from the front-end ASIC chips is translated to differential voltage signal on a 50 Ω load, and the voltage signal is amplified and converted to single-ended output by a differential receiver. The single-ended output is subsequently processed by the second-order active low-pass filter (f_c=5 MHz), and finally the filter's output is sent to a DAQ card via a high-speed differential driver.

3 Data acquisition

The hardware of DAQ is composed of a DAQ card

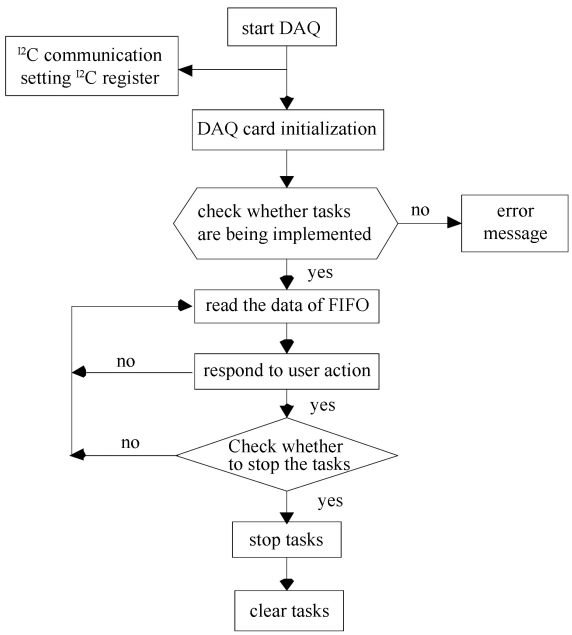

Fig. 4. Program flow chart for the DAQ software.

(PXI-6133) and a PXI chassis. The DAQ software has been developed using LabWindows/CVI which makes the software design easier. A Graphical User Interface (GUI) allows configuring parameters of the ASIC chips and other ^{I2}C devices on analog boards, as well as the acquisition settings (physical channel, trigger source, and sampling-clock source, etc.). The acquired data can be displayed in the GUI, so that we can check whether the detectors work normally. Under the management of this program, the acquired data can be buffered into the on-board FIFO, so that the data can be read out asynchronously by the PC, and saved in files for off-line analysis. The program flow chart is shown in Fig. 4.

4 Performance of the readout electronics

The performance of the readout electronics has been tested with an accurate variable pulse generator (ORTEC 448). The energy linearity of system is better than 0.20% for the dynamic range of 0.06–0.60 V. The energy resolution is less than 0.20% with an input at 37.40 MeV. The time resolution is less than 0.23% in the range of 0–300 ns. The linearity of time is less than 0.20% for the dynamic range of 86 −296 ns, tested with a precision charge/time generator from Phillips Scientific (Model 7120). The crosstalk of each channel was tested with ORTEC 448, and the maximum channel crosstalk of system is 4.60 %. Fig. 5 shows the odd channel crosstalk when we input signal to the dual-channel.

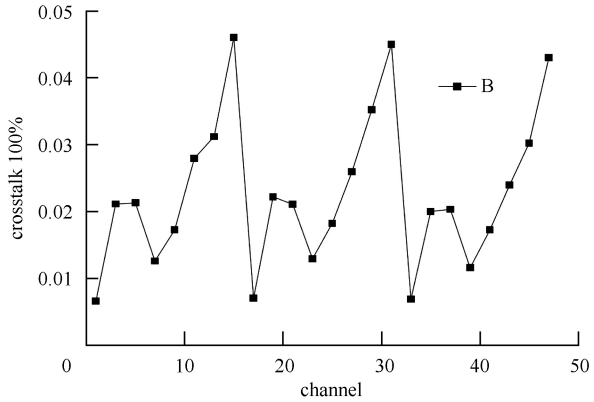

Fig. 5. Odd channel crosstalk curve, tested by inputting a signal to the dual-channel.

Also, the performance of the electronics has been tested with a silicon strip detector BB1 produced by Micron Semiconductor Ltd. [7]. The electronic boards are installed very close to the detector and linked to the detector via a 50 pin connector. The system works in vacuum at 7.40×10^{-2} mbar. The energy spectrum of a standard triple alpha source was measured as shown in Fig. 6. An energy resolution of 1.14 % was achieved at 5.48 MeV close to the result of 0.92% which is measured by a silicon strip detector in a MUST II telescope [8].

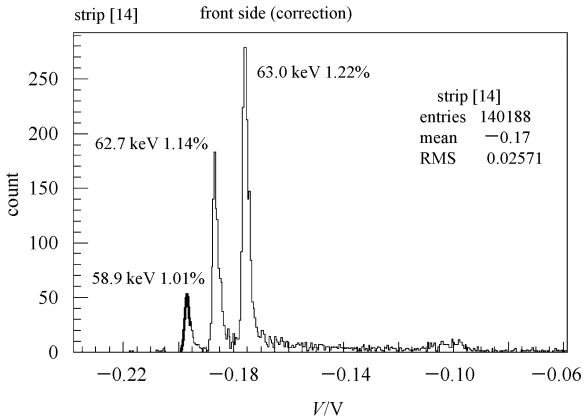

Fig. 6. Energy spectrum of an alpha source measured with a silicon strip detector.

5 Summary

In this paper we have described a front-end readout electronics system developed for silicon strip detectors to be equipped in the HIRFL-ETF. It shows that the system has a good energy resolution tested with a silicon strip detector and a standard alpha source. The performance of the system is accurate and reliable for future nuclear physics experiments.

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