A SKIROC2-based prototype electronics system for Silicon PIN array

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Abstract. A prototype electronics system, based on the SKIROC2 Application-Specific Integrated Circuit (ASIC), for silicon PIN (Si-PIN) array has been developed. The system consists of two electronics modules: the Front-End Board (FEB) module and the Data Interface (DIF) module. The FEB, which carries the SKIROC2 ASIC and the Si-PIN diodes array, is in charge of particle detection and analog-to-digital signal conversion, and the DIF is designed to control the FEB and to transfer data to PC. The equivalent noise level of all the 64 channels are below 0.4 fC, while most of them are below 0.2 fC. The dynamic range is up to +3000 fC with an Integral Non-Linearity (INL) of 0.2 %, and the gain non-uniformity is better than 5 %. A Si-PIN diodes component, S5980 from HAMAMATSU is utilized to assess the performance of the system. Tests with a [241]Am source and the cosmic ray have been carried out. The energy resolution with 59 keV X-rays from [241]Am is about 13.3 % (in RMS), while the Signal-to-Noise Ratio (SNR) reaches about 10.9 for Minimum Ionizing Particles (MIPs). The details of the system design, together with the test results, are presented in this paper.

Keywords: SKIROC2, Silicon PIN diode, Front-end electronics, Readout system.

1   Introduction

Silicon PIN (Si-PIN) diode has been widely used in high-energy physics experiments, such as the Silicon Pad Detector (as a charge identifier) of the CALorimetric Electron Telescope (CALET) and the Electromagnetic CALorimeter (ECAL) of the International Linear Collider (ILC) prototype[1][2]. The next generation experiments, such as the Circular Electron Positron Collider (CEPC) [3] and the ILC, require finer granularity for their detectors to achieve higher energy resolution and more accurate particle identification capability. This trend asks for a large amount of the Si-PIN diode arrays, leading to a requirement for the electronics system with features of higher integration and lower power consumption than the traditional ones[4].

The SKIROC2 (Silicon Kalorimeter Integrated ReadOut Chip 2), which is an ASIC developed by the CALICE collaboration for the Si-PIN signal readout[5], integrates 64

channels on one chip and has the features of low noise and large dynamic range. In this paper, a prototype of multi-channel electronics system, which is based on the SKIROC2 ASIC, is designed and implemented. The system is also considered as the pre-research of the Silicon Tungsten (Si-W) ECAL for CEPC.

2   Design and implementation of the system

Shown in Fig. 1 is the block diagram of the readout electronics, which is divided into two parts so that it has the potentiality for expansion of more readout channels by only changing the Front-End Board (FEB). The FEB, which carries a Si-PIN diode array and an ASIC of SKIROC2 on it, provides high voltage for the Si-PIN diodes and processes the signals as well. The FEB is configured by a Data InterFace board (DIF) and sends data to the DIF, which then transfers data to PC via USB interface after packing process.
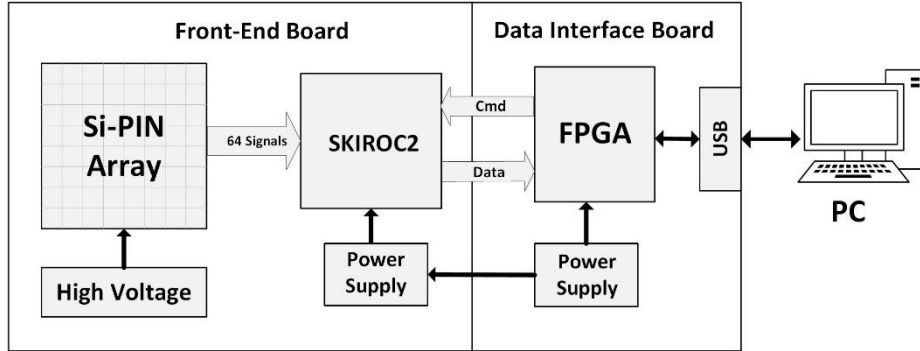

Fig. 1. Block diagram of the electronics system, which mainly consists of the FEB and the DIF.

2.1   SKIROC2 ASIC

Fig. 2 presents the schematic illustration of one channel of SKIROC2, on which 64 same channels are integrated. Each channel is composed of a Charge-Sensitive Amplifier (CSA), two slow shapers with different gains, one fast shaper with a discriminator, a time-to-digital convertor (TDC) for time measurement, three Switched Capacitor Arrays (SCA) of 15 depth to store analog signal and an Analog-to-Digital (ADC) to convert signal from analog to digital.
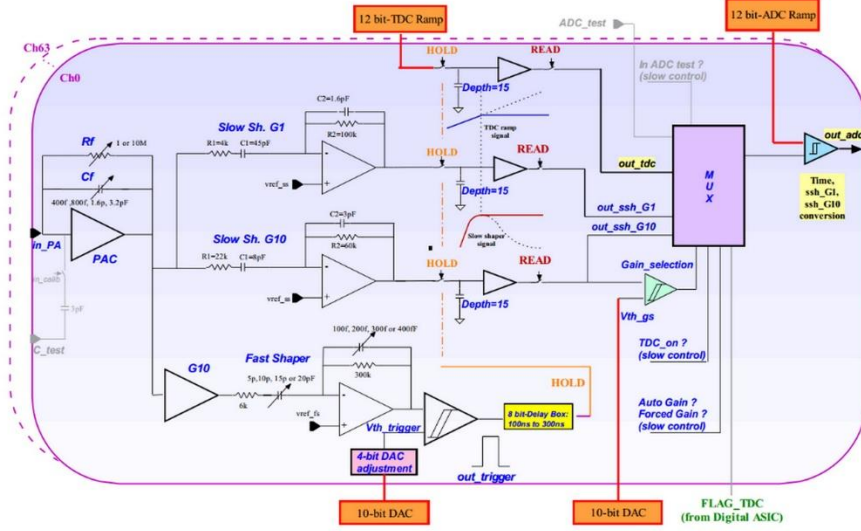
Fig. 2. The schematic illustration of the analog part of SKIROC2 (one channel).

The input signal passes through the CSA with the variable gain set by switchable Feedback Capacitance (C_f) array. And the output of the CSA is fed to a fast and two slow shapers for trigger and precision measurement, respectively. By comparing the fast shaper's output with a threshold set by a 10-bit on-chip Digital-to-Analog Convertor (DAC), the discriminator generates a trigger signal to hold the voltages at the two slow shaper outputs, which are optimized for low-noise charge measurement, on the SCAs. The signals on the SCAs are read out and converted by a 12-bit Wilkinson ADC, with a bunch ID tagged on a 10 MHz clock, then saved in the on-chip memory. Benefiting from the two different-gain slow shapers and the adjustable-gain CSA, the SKIROC2 has a wide dynamic range, ensuring a linear response for equivalent input charge up to +3000 fC, with a noise level as low as 0.2 fC in RMS. The peaking time of the chip is tuneable from 50 ns to 200 ns to suit different signals and the power consumption is only about 6 mW per channel. In addition, the SKIROC2 can be configured to be either self-triggered or external-triggered, and this satisfies different experimental conditions. With these features that meet the readout requirements of Si-PIN diode array in different experiments, the SKIROC2 is chosen as the front-end readout chip of the system.

2.2   Front-end Board

As shown in Fig. 3, the FEB, which accommodates one SKIROC2 chip and 64 Si-PIN components, is divided into two parts: the Detector-Part and the ASIC-Part, so that it is convenient to test different kinds of Si-PIN diodes without redesigning the ASIC-Part. The ASIC-part is mainly designed to make the SKIROC2 function well. PCB connectors (ERNI-154744) are used both for gathering detectors' outputs from the Detector-Part to SKIROC2 ASIC[6], and for connecting the ASIC with DIF.

In addition, there are two kinds of control signals, named by their speed: fast control and slow control. The fast control signals, which include SKIROC2's trigger and the reset or validity of the SCA, are sent to the control center of SKIROC2 directly based on the Low Voltage Differential Signal (LVDS) standard. While the slow control signals, on the other hand, are in a daisy chain cascade and configures the 616-bit registers on the chip, which store some configurations such as the feedback capacitance of the CSA and the trigger mode. The digitalized output data of the SKIROC2 are sent to the DIF through the Open Collector (OC) gate. Considering the OC gate and the daisy chain cascade, it is very convenient to expand the FEB for more ASICs without changing the definition of the connector to DIF. The SKIROC2 requires a supply voltage of + 3.3 V, which is supported by a Low-DropOut (LDO) regulator from a primary supply of + 5 V.
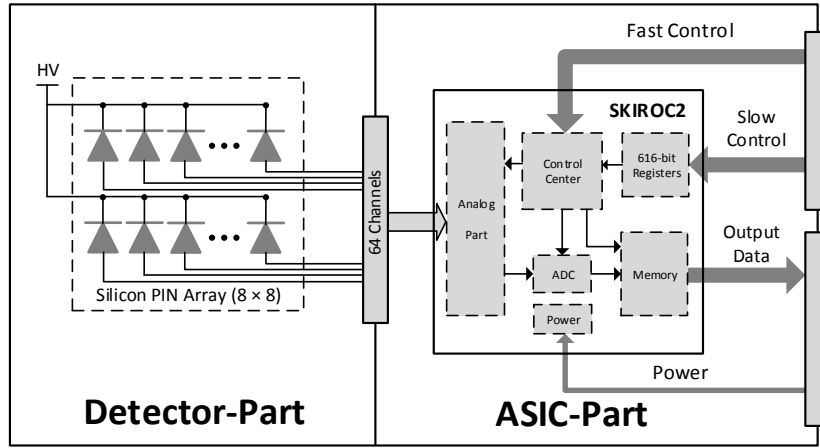

Fig. 3. Block diagram of Front-end Board, which consists of the Detector-Part and the ASIC-Part.

The Detector-Part carries a Si-PIN diodes array and supplies them. At present, a type of Si-PIN diode named S5980 from HAMAMATSU is adopted to verify the performance of the system[7]. The active area of the diode is 5×5 mm^2 and the thickness of depletion layer is about 460 μm, the dark current is only 100 pA while the thermal capacitance is as small as 10 pF. Since the output noise of the diode is sensitive to the bias voltage ripple, the cathode of the diode is connected to a bias voltage of +23 V, supported by a well-designed LDO regulator with an initial supply of +25 V from outside the board. The anode of the diode is directly connected to SKIROC2's input, which supplies a reference voltage about +1 V to ensure the correct working status of the Si-PIN diode.

2.3   Data Interface

The DIF consists of four main parts: the FPGA part, the connector part, the power supply part and the interface part. The FPGA part is mainly composed of an FPGA and a PROM. The function of the FPGA is to implement the required logic to control the FEB and to communicate with the PC. The supply part is implemented with a DC input

(5V) from outside and several LDO regulators, generating supply for the DIF and the FEB. The interface part is in charge of communication with PC through a mini-USB port, realized by a USB chip CY7C68013. In addition, an optical transceiver interface is implemented for compatibility with other readout device.
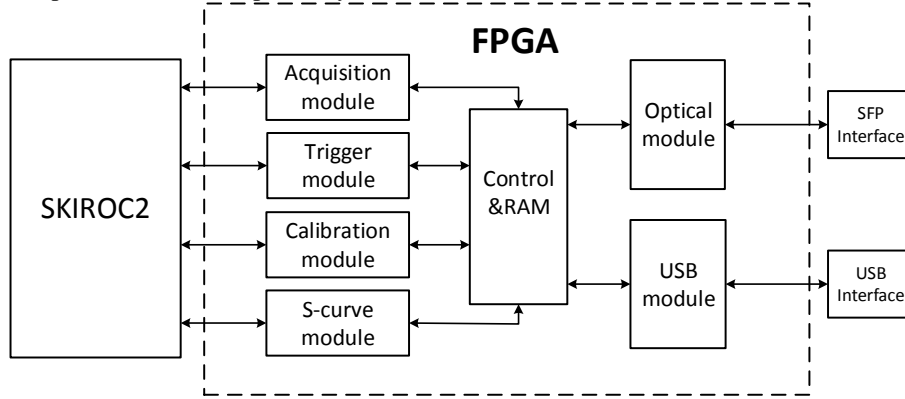

Fig. 4. Block diagram of logic implemented in the FPGA.

The logic diagram of the FPGA is presented in Fig. 4. The acquisition module controls the ASIC to work in normal mode and process the data from SKIROC2, which are first stored in the FIFO, then packed and finally transferred to the PC. The trigger module is in charge of generating a trigger when the external trigger is in need, while normally the chip is self-triggered. The calibration module and S-curve module are used to control the ASIC during calibration or testing, which is elaborated below. The optical module and USB module are responsible for receiving commands from and transmitting data to the PC.
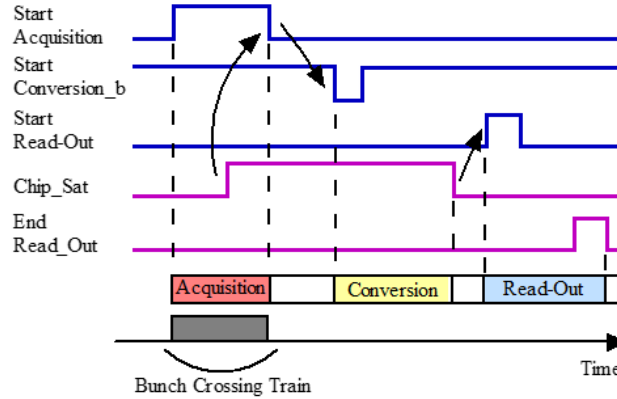

Fig. 5. Global timing control of data acquisition for SKIROC2.

The timing control sequence of the main signals during the normal acquisition process is shown in Fig. 5[5]. This global sequencing is made around three signals from FPGA on the DIF: StartAcquisition, StartConversionb and StartReadout. In response to the three signals, the SKIROC2 answers with two signals: Chip_Sat and End_Readout. The

acquisition is composed of 3 phases: Acquisition, Conversion and Readout. The acquisition phase starts when the StartAcquisition has a rising edge and ends when this signal falls. During the acquisition phase, the SKIROC2 outputs a rising edge of Chip_Sat signal, informing that the 15-depth SCA array is full. By giving a falling edge of StartConvsionb, the SKIROC2 begins to convert signals from analog to digital. When the conversion is finished, the Chip_Sat signal falls and a rising of StartReadout signal is sent from DIF to SKIROC2, to start the readout phase. The End_Readout rises when the transmission is over. It is worth noting that the End_Readout signal is in daisy chain structure that the following SKIROC2's readout phase could be started by this signal, if there are more than one ASIC.

The prototype electronics system has been implemented and the picture of the FEB together with the DIF is shown in Fig. 6.
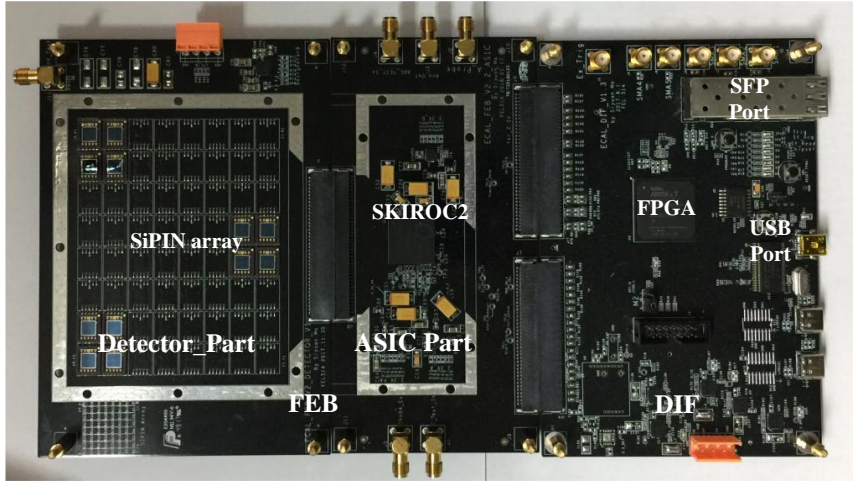

Fig. 6. The photograph of FEB and DIF.

3   Characterization

3.1   Basic output of SKIROC2

Although the SKIROC2 is designed to send out digitalized data, an analog probe is available to observe the outputs of analog part for debugging. The basic outputs, such as slow shaper, fast shaper and trigger, of every channel is observed to make sure that all channels function well. A typical waveform including outputs of the fast shaper, slow shaper and trigger of single channel is shown in Fig. 7. From the waveform, the fast shaper is about 200 ns ahead of the peaking time, so that a trigger from the discriminator next to the fast shaper could be used to hold the peak value of the slow shaper output to the SCA.
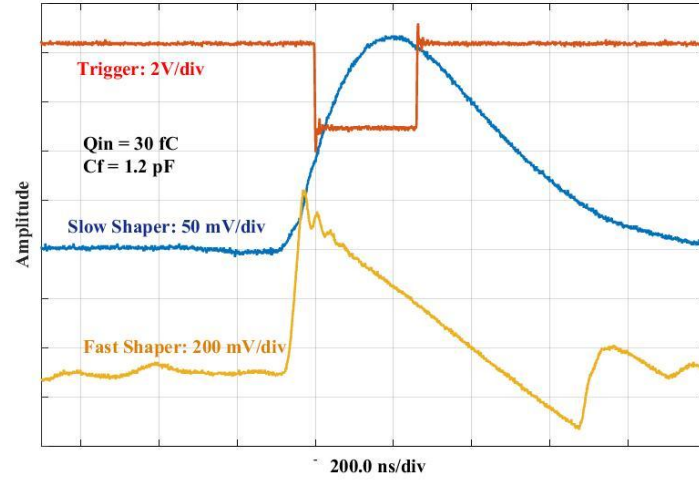
Fig. 7. The typical outputs of the fast shaper, slow shaper and trigger from single channel of SKIROC2.

3.2   Baseline and noise

In order to evaluate the noise level of the system, the external trigger function of SKIROC2 is used to get the pedestal of the system without detectors. Since the SKIROC2 requires 4 ms for conversion and readout, triggers in a fixed time interval of 10 ms are generated by the DIF, controlling the acquisition of the baseline. The chip holds the baselines of all 64 channels and converts them to digital values when triggered. Fig. 8 shows the average of baselines and sigma of noises from all channels. The results show that most channels demonstrate a noise level lower than 0.2 fC equivalent input charge.
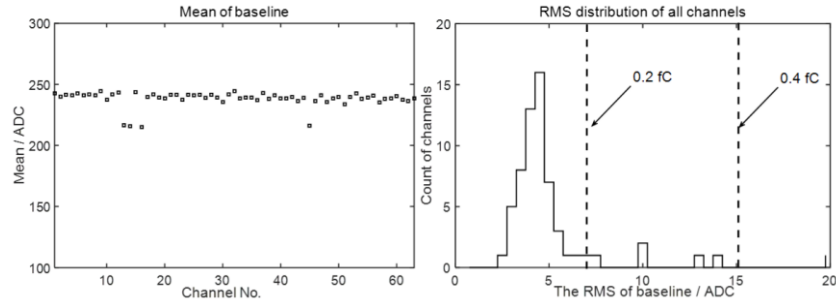

Fig. 8. The baseline and noise distribution of all 64 channels.
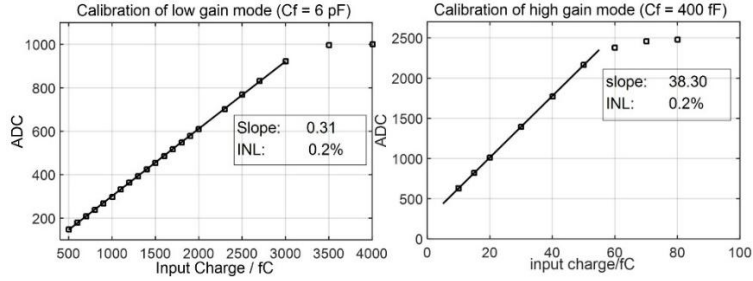
3.3 Calibration

Fig. 9. The linear fit results of two gain modes of SKIROC2.

The calibration procedure is carried out to obtain the linearity and dynamic range of the SKIROC2 chip. By using the SKIROC2's 3 pF calibration capacitor on each channel, the self-calibration is conducted by the procedure elaborated below. A waveform generator with attenuator is used to generate step pulses with different amplitudes. This voltage pulse is sent into the SKIROC2 through the calibration pin and applied to all the calibration capacitors at the same time. When the step pulses are applied to the on-chip capacitor, a certain amount of charge, which covered the full range, is injected into every channel of SKIROC2 for performance evaluation. The SKIROC2 chip has different operation modes by tuning the C_f array. The measurement is carried out with the highest gain mode (C_f = 400 fF) and the lowest gain mode (C_f = 6 pF). The gain non-uniformity between different channels is better than 3% and the typical linear curves of ADC output codes versus input charge, of the two modes, are shown in
Fig. 9, which shows that the linear range of the highest gain mode and the lowest gain mode are 50 fC and 3 pC, respectively. The Integral Non-Linearities (INL) of both modes are as low as 0.2%.
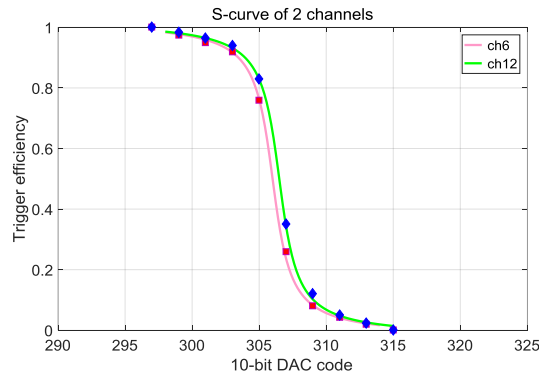
3.4 Trigger efficiency

Fig. 10. The trigger efficiency for two channels as a function of threshold setting for an input charge of 2 fC.

The trigger efficiency is obtained from an "S-curve" as presented in Fig. 10. The trigger threshold is set by two Digital-to-Analog Conversion (DAC) settings on chip: a global threshold with a 10-bit DAC and a 4-bit DAC on each channel. To measure the trigger

efficiency, a fixed amount of charge is introduced from the test pulse input. If the fast shaper's output exceeds the threshold, the SKIROC2 chip generates a trigger signal for counting. The S-curve is obtained by varying the trigger threshold 10-bit DAC and recording the efficiency at each DAC code and then fitted by a complementary error function. The centre value corresponded to the charge threshold and the sigma parameter represents the noise-induced width. The results of the curve are closed to the previous work finished by T. Suehara[8]. The 4-bit DAC adjustment for every channel should help get a better threshold uniformity, but this function does not work properly in SKIROC2 due to a detected bug, which has been fixed in a newer version of SKIROC2a.

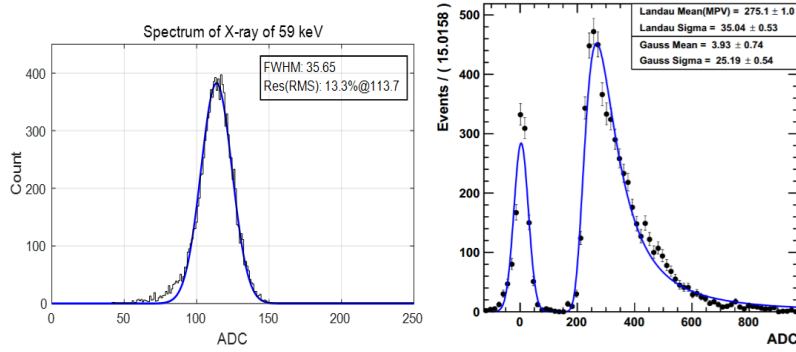## 3.5   X-ray test and Cosmic ray test

Fig. 11. The spectrum of the X-ray of [241]Am (left) and the pedestal and MIP distribution of cosmic ray (right).

Several S5980 Si-PIN diodes are soldered on the FEB to test the performance of the system. A joint test with a [241]Am source and a test with cosmic ray are carried out. During both tests, the outputs of diodes are directly sent to the SKIROC2, which is set to work in the highest gain mode. The spectrum of 59 keV X-ray is shown in the left plot of the Fig. 11. It can be observed that the shape is not a standard Gaussian, which is because in some case the photoelectric conversion occurs at the dead layer and losses some energy. According to the calibration results, the equivalent input charge was 2.89 fC and the resolution was 13.3% (in RMS). The right plot of the Fig. 11 is the result of the cosmic ray test from a single channel. The SKIROC2's trigger threshold is set at 0.5 Minimum Ionizing Particle (MIP, with about 5 σ separation of the noise) to get signal from cosmic ray. In addition, there is a random external trigger to get the pedestal noise. The spectrum of the cosmic ray is Landau fitted and the pedestal is Gaussian fitted. The results of the fits shows that the Signal-to-Noise Ratio (SNR) for MIP is 10.9, which is closed to the test results of other electronics using SKIROC2[9]. These tests show that the system has enough resolution to identify small signals such as X-ray and MIP.

4   Conclusion

In this paper, a SKIROC2-based prototype electronics system for Si-PIN array, as well as the performance test, have been presented. The system, which consists of FEB module and DIF module, has features of high integration, low noise and high dynamic range. Considering the daisy chain structure of the SKIROC2, it is easy to expand the FEB for more ASICs without changing the interface protocol. The SKIROC2, as well as the design concept of the electronics system can be applied to the preliminary prototype Si-W ECAL of CEPC.

5   Acknowledgement

References

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