Prototype Readout Electronics of Silicon PIN Diode Arrays for CEPC ECAL Pre-research

S. Ma,a, b S. Liu,a, b C. Feng,a, b C. Li, a, b H. Liu,a, b and Q. Ana, b

1. State Key Laboratory of Particle Detection and Electronics,  
   University of Science and Technology of China, No. 96, Jinzhai Road, Hefei, China.
2. Department of Modern Physics, University of Science and Technology of China.  
   No. 96, Jinzhai Road, Hefei, China.

*E-mail*: <liushb@ustc.edu.cn>

Abstract: A readout system, which is based on SKIROC2 Application-Specific Integrated Circuit (ASIC), for silicon PIN diode array detectors has been developed. The system, which is intended for preliminarily studying the design concept of Si-W Electromagnetic Calorimeter (ECAL) at Circular Electron Positron Collider (CEPC), mainly consists of three kinds of electronics modules: the Front-End Board modules (FEB), the Data-Interface modules (DIFs) and a Data Collection Module (DCM). The FEB, which carries the SKIROC2 ASIC and the silicon PIN diode arrays (S5980 from HAMAMATSU), is in charge of particles detection and converting the signals from analog to digital. The DIF is designed to control the FEB and transfer data to DCM via optical fiber. The DCM gathers data from all DIFs and transmits data to computer through Gigabit Ethernet interface. The equivalent noise levels of all the channels are below 0.4 fC while most of them are below 0.2 fC. The dynamic range is up to +3000 fC with an Integral NonLiearity (INL) of 0.2%, and the gain uniformity between different channels is better than 5%. Joint tests with a radioactive source (241Am) and cosmic rays have been carried out. The energy resolution with x-rays at 59 keV reaches 13.3% (in RMS). The Signal-to-Noise Ratio (SNR) is about 10.9 for Minimum Ionizing Particle (MIP) signal, which satisfies the design requirements. Details of the readout system, together with preliminary test results are to be presented in this paper.

Keywords: ECAL; CEPC; Prototype; Silicon PIN diode; SKIROC2; Readout system; FPGA; Analog-digital conversion; Data-acquisition, Modular electronics; Front-end electronics.

Contents

1. Introduction 1

2. Implement of the system 2

2.1 Architecture 2

2.2 ASIC 3

2.3 FEB 4

2.4 DIF 5

2.5 DCM 6

3. Test results 6

3.1 Baseline and noise 7

3.2 Calibration 7

3.3 Trigger efficiency 8

3.4 X-ray test 8

3.5 Cosmic test 9

4. Conclusion 9

1. Introduction

The Circular Electron Positron Collider (CEPC) is a proposing next-generation electron-positron collider in China [1]. The main target of CEPC is producing Higgs boson, whose separation depends on the success of the particle flow concept [2], and making precise measurements of it. The CEPC calorimeters, including the Electromagnetic Calorimeter (ECAL) and Hadron Calorimeter (HCAL), are in charge of precise energy measurements of electrons, photons, taus and hadronic jets. In order to obtain the supreme energy resolution, the particles inside the jets should be separated and the tracks should be assigned to calorimeter clusters one by one. To maximize the capability of particle separation, high-granularity is a most critical characteristic, and the Silicon-Tungsten-based ECAL (Si-W ECAL) is one of the most promising candidates.

According to the Preliminary Conceptual Design Report (Pre-CDR), the requirements towards the ECAL are an energy resolution of and an energy range up to 100 GeV [1].The Si-W ECAL is a sampling calorimeter with tungsten absorber and highly segmented readout layers made of pixelised silicon PIN diode arrays. According to the simulation for CEPC [3] and test results of CALICE ECAL physics prototype [4,5] for International Linear Collider (ILC) [6], the Si-W ECAL for CEPC needs dozens of layers of silicon PIN diode pad arrays and each pad’s size of silicon PIN should be about 1 × 1 cm2 or even smaller leading to a total number of tens of millions electronic channels.



Figure . The cascading relationship of ECAL prototype.

In order to study the principle and verify the key techniques of Si-W ECAL for CEPC, a small prototype is planned to be built. The cascading relationship outline of the prototype is shown in Figure 1. This prototype should have dozens of layers with pixelised silicon PIN arrays and a readout system with multi-channel and scalable features. The readout channel of each silicon PIN pad should have enough Signal-to-Noise Ratio (SNR) and energy range for MIP. The energy range should be at least 500 MIPs. To satisfy these requirements, the readout electronics are expected to have an equivalent noise level of better than 1 fC and a linear range up to at least +2000 fC (considering the equivalent charge of MIP is about 4 fC [5]). In addition, the integration should be as high as possible and the consumption of each channel should be lower than 10 mW.

Based on the above mentioned requirements, a multi-channel and scalable readout system is currently being developed to test the performance of silicon PIN diodes as well as to make a pre-design for the prototype. Details of the system and preliminary test results are introduced below.

1. Implement of the system
   1. Architecture



Figure . The architecture of the readout electronics system

The architecture of this system is shown in Figure 2. It’s composed of three kinds of modules, the detector and ASIC module called Front-End Board module (FEB), the Data Interface module (DIF) and the Data Concentration Module (DCM). The FEB receives and digitizes signal from the detectors as well as supplying high voltage to them. It is configured by the DIF controls and drives data to the latter, which then are transferred to the DCM via optical fibre after packing process. Each DIF and FEB pair is responsible for a single layer. The DCM is in charge of sending commands to DIFs, gathering all data from different DIFs, making compression and transferring data to PC. A prototype based on the architecture with up to six layers of detector arrays will be implemented.

* 1. ASIC

The core of the FEB is the chip SKIROC2 (Silicon Kalorimeter Integrated ReadOut Chip 2) designed by IN2P3/OMEGA group in France. SKIROC2 is an ASIC for the International Large Detector (ILD) [8] Si-W ECAL. Depicted in Figure 3 is the schematic diagram of SKIROC2. There are 64 channels integrated with one chip. Each channel is composed of a Charge-Sensitive Amplifier (CSA), two slow shapers with different gains, one fast shaper with a discriminator, a Time-to-Digital Convertor (TDC) for time measurement, three Switched Capacitor Arrays (SCAs) of 15 depth to store analog signal and an ADC to convert signal from analog to digital.

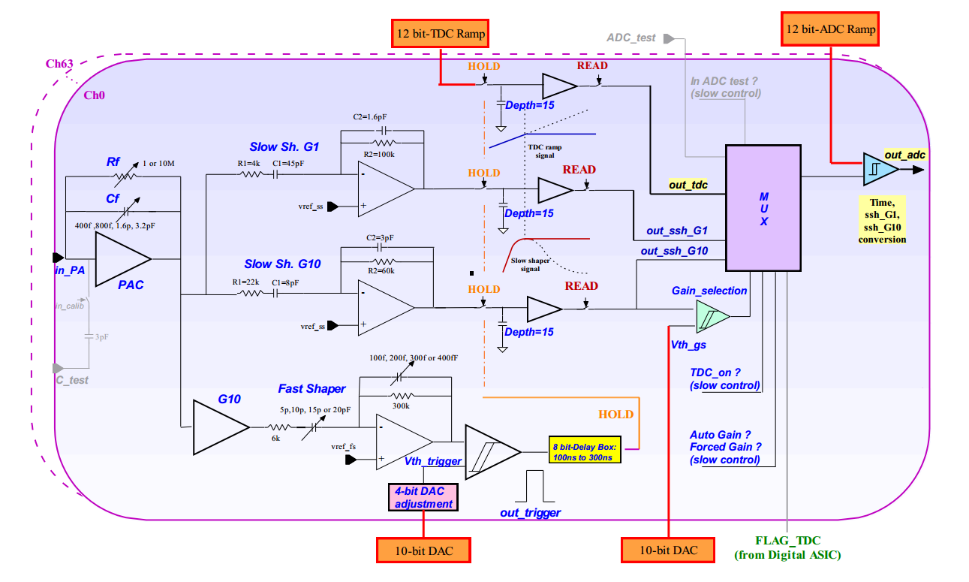


Figure 3. The schematic diagram of the analog part of SKIROC2

The input signal passes through the CSA with variable gain set by parallel feedback capacitance (Cf) array. The output of CSA is fed to the fast shaper and two slow shapers. By comparing fast shaper’s output with threshold, the discriminator generates trigger signal to hold the voltages at two slow shaper outputs on the SCAs. The signals on the SCAs are read out and converted by a 12-bit Wilkinson ADC and a multiplexer, with a bunch ID tagged with a 10MHz clock, then saved in the on-chip memory.

Benefited from the two different-gains slow shapers and the adjustable gain CSA, the SKIROC2 has a wide dynamic range, ensuring a linear response for 1-1500 MIP signals. The peaking time is tuneable between 50 ns and 100 ns. The power consumption is about 6 mW per channel. These features meet the requirements of the Si-W prototype. As a result, the SKIROC2 is chosen as readout chip of the system.

* 1. FEB

In current phase, the FEB accommodates one SKIROC2 chip to read 64 detector signals. The silicon PIN detector S5980, which has four outputs from the anode of diode and one common cathode, from HAMAMATSU is one of the candidate detector for the prototype [9]. The total active area is 5 × 5 mm2 and the thickness of depletion layer is 460 um. Its dark current and terminal capacitance suit SKIROC2’s input demand. According to simulation, the cosmic MIP signal of S5980 is about 7.5 fC. The schematic of detector to ASIC is shown in Figure 4. To make the best use of SKIROC2’s inputs, the detectors are formed an array of 8 × 8, which means the total active area is 1600 mm2. The S5980 claims a high-voltage of 13V. Since its output noise is very sensitive with the ripple of high-voltage, a well-designed Low-DropOut regulator (LDO) TPS7A4700 [10] from Texas Instruments company (TI) is employed, with the Power-Supply Ripple Rejection low to 82 dB and the output noise as little as 4 uVrms. The capacitor and resistor are used to decouple the high-voltage. The SKIROC2’s input supplies a reference voltage about 1V to ensure the detector working in correct status.



Figure 4. A schematic of connection of silicon PIN S5980

After being acquisited and converted, the signals from silicon PIN diode array are converted from analog to digital by SKIROC2 and stored in memory of it, waiting to be readout. The SKIROC2 is controlled by Field-Programmable Gate Array (FPGA) on DIF. There are two kinds of control data buses, fast control and slow control. Fast control buses, which are through Low Voltage Differential Signal (LVDS) pairs, are in charge of SKIROC2's clock, trigger and reset/ valid the SCA. Slow control, however, is in a daisy chain cascade. It configures a 616-bits registers to store many configurations such as Cf and trigger mode. The DIF controls the ASIC on FEB to readout memory data and transmit them to DIF over Open Collector (OC) gate. Considering the OC gate and daisy chain cascade, it’s very convenient to expend FEB for more detectors and ASICs without changing the interface definition to DIF. The DIF also supply an initial voltage of 5 V for FEB.

* 1. DIF



Figure . Picture of DIF

The picture of the DIF is shown in Figure 5. The DIF mainly has these parts: FPGA, connector, power supply and interface.

The FPGA part is composed of a FPGA (ARTIX 7, Xilinx) and a flash Programmable Read Only Memory (PROM, N25Q128). The function of FPGA is to implement the required logic to control FEB and to communicate with DCM board or directly to PC. The logic diagram is shown in Figure 6. The Acquisition module controls the ASIC to work in the normal mode and get data saved in the memory of SKIROC2. The data transferred into FPGA will be stored in the First-In-First-Out (FIFO) memory and then transferred to DCM or PC. The trigger module is in charge of generating trigger when using calibration mode or ex-trigger mode. Calibration module and S-curve module are used to control the ASIC to be calibrated or tested. These tests will be discussed below. The optical module transmits data from FIFO to DCM and gets command from DCM via optical fibre. The transmission is based on the high-speed transceiver GTP on FPGA. The USB module, however, is used to communicate with PC directly when debugging a single DIF.



Figure 6. Block diagram of logic implemented in the FPGA

Communication with FEB is via two ERNI-154744 connectors [11]. All control signals and reply signals as well as initial power supply for FEB are through the two connectors. Interface part is composed of a 1 Gbps bidirectional Small Form-factor Pluggable (SFP) optical transceiver and a USB interface realized by a USB chip CY7C68013 and a Mini-USB port. Supply part is implemented with a dc input level (5V) from outside and several LDO regulators (TPS74401, TI). From this dc supply rail, analog power supplies are generated for DIF.

* 1. DCM



Figure . Picture of DCM

The function of DCM board is to gather all DIFs’ data from optical fibres and to transmit data to PC server via a gigabit standard Ethernet network cable (RJ45). The current readout system is based on the DCM designed for PandaX-III prototype TPC project [12]. The picture of DCM is shown in Figure 7. It contains a FPGA of Zynq-7, a DDR3 RAM of 4 Gbits for data storage, a standard RJ45 port and six SFP for optical fibres, which means one DCM can carry six DIFs. The SFPs are implemented with FPGA-based gigabit serial link to read DIFs’ data and send commands to DIFs. This DCM has been used in the PandaX-III prototype and showed sufficient data bandwidth and stable performance [13].

1. Test results

Some tests were carried out with the readout system in order to determine its performance. Baseline noise and calibration of SKIROC2, trigger efficiency, X-ray test and cosmic test will be introduced below.

* 1. Baseline and noise



Figure . Baseline and noise distribution of all the 64 channels

In order to evaluate the noise level of electronic system, the external trigger function of SKIROC2 was used to get the pedestal of the system without detectors. The DIF generated triggers in a fixed time interval to FEB, controlling the acquisition of baseline. Concerning the time that SKIROC2 needs for conversion phase and readout phase is 4 ms, the DIF generated triggers at a fixed time interval of 10 ms. SKIROC2 held the baselines of all 64 channels and converted them to digital when trigger came. Figure 8 showed the average of baselines and sigma of noise of all the channels. From the graph, not all channels exhibited good baseline and noise results, but most channels’ noises were lower than 0.2 fC equivalent input charge. The maximum was less than 0.4 fC. Concerning the fact that the S5980’s MIP signal was about 7.5 fC, this noise level satisfied the requirements.

* 1. Calibration



Figure . The linear fit results of two gain modes of SKIROC2

Calibration test is to obtain the linearity and dynamic range of SKIROC2. Taking advantaging of the SKIROC2’s 3 pF calibration capacitors on each channel, the self-calibration was taken: a wave form generator with attenuator was used to generate step pulses with different amplitudes. When the step pulses were applied to on-chip capacitor, a certain amount of charge, which covered the full range, was injected into every channel of SKIROC2 from test pulse input for performance testing. SKIROC2 had many operation modes by tuning the Cf array. The measurement has been tested with the highest gain mode (with a Cf of 400 fF) and lowest gain mode (with a Cf of 6 pF). The consistency of gain between different channels was good and the typical non-linearity curves of output value versus input charge of the two modes were shown in Figure 9. The figure showed that the linear range of the highest gain mode and the lowest gain mode were 50 fC and 3 pC. The integral nonlinearities (INL) of both modes reached 0.2%.

* 1. Trigger efficiency



Figure . The S-curve of 2 channels when input is 2 fC

Trigger efficiency was obtained via the “S-curve”, shown in Figure 10. The trigger threshold was set by two Digital-to-Analog Conversion (DAC) settings, a global threshold with a 10-bit DAC and channel by channel adjustment with 4-bit DACs. To test trigger efficiency, a fixed amount of charge was introduced from the test pulse input. If the fast shaper pulse exceeded the threshold, SKIROC2 would output trigger signal. The S-curve was obtained by varying the trigger threshold 10-bit DAC and recording the efficiency at each DAC code. The curve was fitted by a complementary error function, whose center value stood for the threshold on the charge, and the sigma stood for the noise power. The 4-bit DAC adjustment for every channel should help to get a better threshold consistency. But there was a bug that this function did not work properly in SKIROC2. In the new version of SKIROC2a, this bug had been fixed.

* 1. X-ray test



Figure . The spectrum of X-ray of 241Am

Joint test with X-ray source of 241Am was carried out. A bias voltage of 13 V was applied as the high voltage of the silicon PIN detectors S5980. The output signals were directly sent into SKIROC2, which was set to work in highest gain mode. In Figure 11, the spectrum of 59 keV x-ray was shown. According to the results of calibration, the equivalent input charge was 2.89 fC and resolution was 13.3% (in RMS). Considering the fact that the X-ray’s total energy was 59 keV and the charge of 2.89 fC indicated 18109 electron-hole pairs, the ionization energy of silicon PIN diode was 3.25 eV. It was lower than the theoretical value of 3.6 eV. Concerning the Fano factor, the fact is reasonable. This test showed the system had enough resolution to identify small signals such as X-ray and MIP.

* 1. Cosmic test

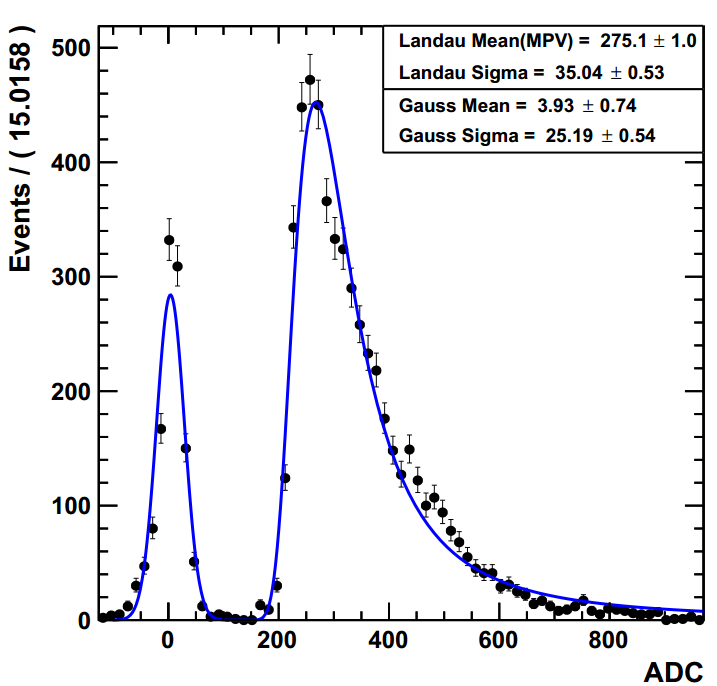


Figure . The spectrum of cosmic ray

A simple cosmic test with one layer silicon PIN array was carried out. 64 silicon PIN detectors of S5980 were installed to get cosmic muons. Figure 12 showed the first result obtained with the system. Since there was no coincidence to filter the cosmic ray, the input angle had a distribution. As a result, the spectrum had non-Gaussian tails instead of a Gaussian distribution. The spectrum of cosmic ray was Landau fitted and the pedestal was Gaussian fitted. The results of the fits showed the Most Probable Value (MPV) of cosmic muon’s equivalent input charge was 7.24 fC and the SNR was 10.9. This SNR satisfied the requirement of current phase. But considering the linear range of 3000 fC, the system didn’t meet the range demand of 500 MIPs. This could be improved by applying silicon PIN diodes with thinner depletion layer.

1. Conclusion

In this paper, a prototype readout electronics based on SKIROC2 for silicon PIN detectors has been presented. The system, which is intended for preliminarily studying the design concept of the prototype of Si-W ECAL for CEPC, consists of FEB module, DIF module and DCM module. The system is scalable because of the modular structure and the characteristics of SKIROC2 ASIC. The main performance of the system are discussed in detail. The joint tests with X-ray and cosmic ray showed encouraging results. In next step, a system with six layers of silicon PIN array and tungsten absorber will be implemented and a shower test will be carried out. An optimization can be made after further tests.

Acknowledgments

The authors would like to thank Stephane Callier of CALICE collaboration for his help in our system design progress. We also appreciate the discussion during the design with Yunlong Zhang of University of Science and Technology of China.

This work was supported by National Natural Science Foundation of China, under Grant No. 11635007.

References

1. CEPC-SPPC Study Group, CEPC-SPPC preliminary conceptual design report: Physics and detector, Tech. Rep. IHEP-CEPC-DR-2015-01, IHEP-TH-2015-01, IHEP-EP-2015-01, 2015.
2. M.A. Thomson, Particle Flow Calorimetry and the PandoraPFA Algorithm, Nucl. Instrum. Meth. A 611 (2009) 25 [arXiv:0907.3577].
3. H. Zhao et al., PFA Oriented ECAL Optimization for the CEPC, arXiv preprint (2017) [arXiv: 1712.09625].
4. CALICE collaboration, Response of the CALICE Si-W ECAL Physics Prototype to electrons, J. Phys. Conf. Ser. 160(2009) 012065 [arXiv: 0811.2354].
5. CALICE collaboration, J. Repond et al., Design and Electronics Commissioning of the Physics Prototype of a Si-W Electromagnetic Calorimeter for the International Linear Collider, 2008 JINST 3 P08001 [arXiv:0805.4833].
6. T. Behnke et al. (ed.), Reference Design Report “Volume 4: Detectors” (2007), available at http://lcdev.kek.jp/RDR.
7. S. Callier, F. Dulucq, C. de La Taille, G. Martin-Chassard and N. Seguin-Moreau, SKIROC2, front end chip designed to readout the Electromagnetic CALorimeter at the ILC, 2011 JINST 6 C12040.
8. H. Baer et al., The International Linear Collider Technical Design Report. Volume 2: Physics, [arXiv:1306.6352].
9. <http://www.hamamatsu.com/resources/pdf/ssd/si_pd_kspd0001e.pdf>
10. <http://www.ti.com/lit/ds/symlink/tps7a47.pdf>
11. http://www.erni.com/cn/produkte/show/product/154744/
12. X. Chen et al., PandaX-III: Searching for Neutrinoless Double Beta Decay with High Pressure 136Xe Gas Time Projection Chambers, Sci. China Phys. Mech. Astron. 60 (2017) 061011.
13. C. Li et al., Design of the FPGA-based gigabit serial link for PandaX-III prototype TPC, Radiation Detection Technology and Methods, 1 (2017) 25.