Prototype Readout Electronics of Silicon PIN Diode Arrays for CEPC ECAL Pre-research

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Abstract: A readout system, which is based on SKIROC2 ASIC (Application-Specific Integrated Circuit), for silicon PIN diode array detectors has been developed. The system, which is intended for preliminarily studying the design concept of Si-W Electromagnetic Calorimeter (ECAL) at CEPC (Circular Electron Positron Collider), mainly consists of three kinds of electronics modules: the Front-End Board modules (FEBs), the Data-Interface modules (DIFs) and a Data Concentration Card (DCC). The FEB, which carries the SKIROC2 ASIC and the silicon PIN diode array, is in charge of particles detection and converting the signals from analog to digital. The DIF is designed to control the FEB and transfer data to DCC via optical fiber. The DCC gathers data from all DIFs and transmits data to computer through Gigabit Ethernet interface. The electronic noise of the system is below 0.2 fC. The dynamic range is up to +3000 fC with an Integral NonLiearity (INL) of better than 0.2%. Joint tests with a silicon PIN diode array (S5980 from HAMAMATSU) and a radioactive source (???) has been carried out. The resolution of 59 keV x-ray reaches 13.3%（in RMS）. The cosmic ray tested with the system is also presented.

Keywords: ECAL; CEPC; Silicon PIN diode; SKIROC2; Readout system; FPGA; Analog-digital conversion; Data-acquisition, Modular electronics; Front-end electronics.

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1. Introduction

The Circular Electron Positron Collider (CEPC) is a proposing next-generation electron-positron collider in China, as Higgs and/or Z factory [1]. The main targets of CEPC are producing Higgs boson, whose separation depends on the success of the particle flow concept [2], and making precise measurements of it. the CEPC consists of a vertex detector, silicon trackers and time projection chamber for tracking charged particles, Electromagnetic Calorimeter (ECAL) and hadron calorimeter, a superconducting solenoid with a muon tracker in its return yoke. In order to obtain the supreme energy resolution, the particles inside the jets are separated and each track is assigned to calorimeter cluster one by one. To maximize the particle separation, a kind of high-granularity ECAL is critical. The Silicon-Tungsten-based ECAL (Si-W ECAL) is an important option.



Figure . The cascading relationship of tungsten and silicon PIN slab

According to the preCDR (…..), the requirements for the ECAL is a energy resolution of and an energy range up to 100 GeV [1].As shown in Figure 1, the Si-W ECAL is a sampling calorimeter with tungsten absorber and highly segmented readout layers made of pixelised silicon PIN pad sensor arrays. According to the simulation and test results of CALICE ECAL physics prototype [3,4] for International Linear Collider (ILC) [5], the Si-W ECAL for CEPC needs dozens layers of silicon PIN arrays and each pad’s size of silicon PIN is about 1 × 1 cm2 [1], which means the total number of electronic channels is tens of millions.

In order to verify the feasibility as well as to make a mature design of ECAL, a prototype is need to be built. As shown in Fig. 1, This prototype should have several layers of pixelised silicon PIN array and a readout electronics system which is multi-channel and scalable. An ASIC named SKIROC2, with 64 input channels, is one of the candidate chip for the front end electronics to handle the silicon PIN arrays’ outputs [6]. In order to test the performance of silicon PIN diod as well as to make a pre-design for the prototype, a scalable readout system based on SKIROC2 ASIC has been developed.

1. Implement of the system
   1. Architecture



Figure . The architecture of the readout system

The architecture of this system is shown in Figure 2. It’s mainly composed of three kinds of modules, the detector and ASIC module called Front-End-Board module (FEB), the Data Interface module (DIF), the Data Concentration Card module (DCC). The FEB supplies high voltage for silicon PIN detectors, receives and digitizes the signal from the detectors. The FEB is configured by the DIF controls and drives data to the latter, which then are transferred to the DCC via optical fibre after packing process. Each DIF and FEB pair is responsible for a single layer. The DCC is in charge of sending commands to DIFs, gathering all data from up to six DIFs, making necessary compression and transferring data to PC. A prototype with up to six layers of detector arrays will be implemented.

* 1. ASIC

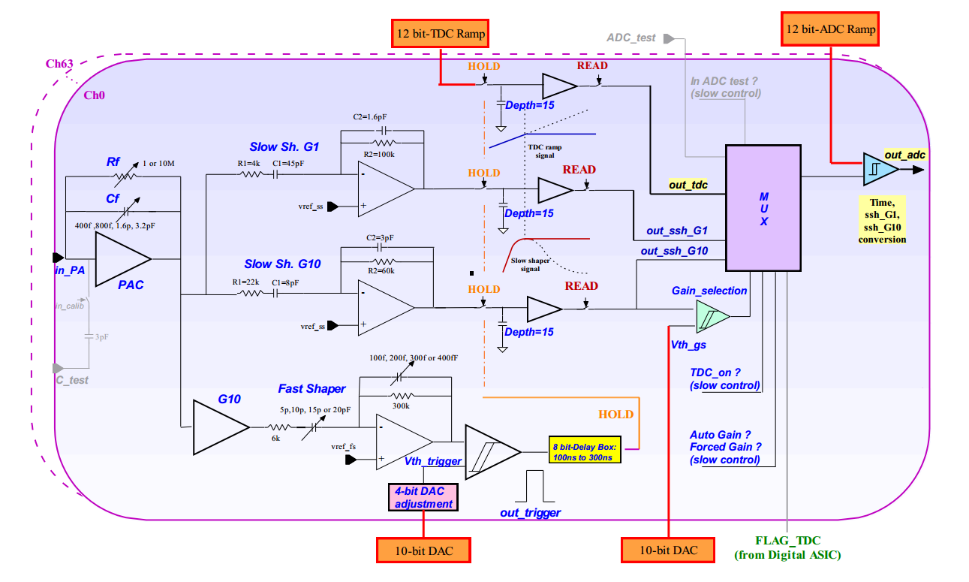


Figure . The schematic diagram of the analog part of SKIROC2

The core of the FEB is the chip SKIROC2 (Silicon Kalorimeter Integrated ReadOut Chip 2). SKIROC2 is an ASIC for the International Large Detector (ILD) [7] Si-W ECAL, which is designed by IN2P3/Omega group in France. Depicted in Figure. 3 is the schematic diagram of SKIROC2. There are 64 channels integrated with one chip. Each channel is composed of a Charge-Sensitive Amplifier (CSA), two slow shapers with different gains, one fast shaper with a discriminator, a Time-to-Digital Convertor for time measurement, three Switched Capacitor Arrays (SCA) of 15 depth to store analog signal and an ADC to convert analog signal to digital one. The SKIROC2 is available on Ball Grid Array (BGA) package, as well as Quad Flat Package (QFP).

The input signal passes through the CSA with variable gain set by feedback capacitance (Cf). The output of CSA is fed to the fast shaper and two slow shapers with different gains. By comparing output of fast shaper with threshold, the discriminator generates trigger signal to hold the voltages at two slow shaper outputs and an additional scanned voltage source for timing measurements to the SCAs. The signals on the SCAs are read out and converted by a 12-bit Wilkinson ADC and a multiplexer, with a bunch ID tagged with 10MHz slow clock, then saved in the on-chip memory.

Benefited from the two slow shaper with different gains and the adjustable gain CSA, the SKIROC2 has a wide dynamic range of 0.5-2500 Minimum Ionizing Particles (MIPs) equivalent charges. The peaking time is tunable between 50 ns and 100 ns.

* 1. FEB



Figure . A schematic of connection of silicon PIN S5980

The FEB accommodates one SKIROC2 chip to read 64 detector signals. The silicon PIN detector S5980 from HAMAMATSU is one of the candidate detector [8], which has four outputs from the anode of diode and one common cathode. The total active area is 5 × 5 mm2 and the thickness is 460 um. Its dark current and terminal capacitance suit SKIROC2’s input demand. The schematic of detector to ASIC is shown in Figure 4. To make the best use of SKIROC2’s inputs, the detectors are formed an array of 8 × 8, which means the total active area is 1600 mm2. The S5980 claims a high-voltage of 13V. Since its output noise is very sensitive with the ripple of high-voltage, a well-designed Low-DropOut regulator (LDO) TPS7A4700 [9] from Texas Instruments company (TI) is employed, with the Power-Supply Ripple Rejection low to 82 dB and the output noise as little as 4 uVrms. The capacitor and resistor are used to decouple the high-voltage. The SKIROC2’s input supplies a reference voltage about 1V to ensure the detector working in correct status, so the anode of the detector directly connects the ASIC.

Since SKIROC2 needs particular power supplies which are regulated by the local LDOs, the initial voltage of 5 V is supplied by connector to DIF, as the same way that the SKIROC2 controlling signals and the output digital data of SKIROC2. There are two kinds of control data buses, fast control and slow control. The fast control is composed of five Low Voltage Differential Signal (LVDS) controlling the clocks and normal operation of SKIROC2. Regarding the fast control signals, the fast clock (FAST-CLK) of 40 MHz is used for sampling signal to SCA and generating hit signal for output. The slow clock (SLOW-CLK) of 10 MHz is used for reading out data saved in SKIROC2’s and generating bunch ID. The reset signal (RAZ) is used for erasing the capacitors of SCA when the chips is triggered by noise. The valid signal (VAL) is used to disable discriminator output signal. The ex-tirgger signal (TRIG-EXT) is used as an external trigger input. The slow control configures a 616-bits registers to store many configurations such as feedback capacitance of CSA and various other parameters like trigger mode or calibration mode. If two or more chips are adopted on the FEB, their slow control registers could be configured in a daisy chain cascade. The output port of digital signals are in open collector (OC), which means the same signal between different chips share one data line. Considering the OC gate and daisy chain cascade, it’s very convenient to expand FEB for more detectors and ASICs because there is no need to change the interface definition from FEB to DIF.

* 1. DIF



Figure . Picture of DIF

The picture of the DIF is shown in Figure 5. The DIF mainly has these parts: FPGA, connector, power supply and interface.



Figure . Block diagram of logic implemented in the FPGA

The FPGA part is composed of a FPGA (ARTIX 7, Xilinx), a flash Programmable Read Only Memory (PROM, N25Q128) as well as a connector in order to program the FPGA via JTAG. The FPGA is clocked with an 80 MHz crystal. The FPGA’s function is to implement the required logic to control FEB and to communicate with DCC board or directly to PC. The logic diagram is shown in Figure 6. The Acquisition module controls the ASIC to work in the normal mode and get data saved in the memory of SKIROC2. The data transferred into FPGA will be stored in the First-In-First-Out (FIFO) and then transferred to DCC or PC. The trigger module is in charge of generating trigger when using calibration mode or ex-trigger mode. Calibration module and S-curve module is used to control the ASIC to be calibrated or tested. These tests will be discussed below. The optical module transmits data from FIFOs to DCC and gets command from DCC via optical fiber. The transmission is based on the high-speed transceiver GTP on FPGA. The GTP is responsible for descrambling data, 8B/ 10B encoding and clock recovery. The USB module, however, is used to communicate with PC directly when debugging a single DIF.

The communication with FEB is via two ERNI-154744 connectors [10]. All control signals and reply signals as well as power supply for FEB are through the two connectors.

Interface part is composed of a 1 Gbps bidirectional Small Form-factor Pluggable (SFP) optical transceiver for communication with DCC and a USB interface realized by a USB chip CY7C68013 and a Mini-USB port for communication with PC when debugging.

Supply part is implemented with a dc input level (5V) from outside and several LDO regulators (TPS74401, TI). From this dc supply rail, analog power supplies (1.0 V, 1.8 V, 2.5 V and 3.3 V) are generated by these LDO regulators for DIF.

* 1. DCC



Figure . Picture of DCC

The function of DCC board is to gather all DIFs’ data from optical fibers and to transmit data to PC server via a gigabit standard Ethernet network cable (RJ45). The current readout system is based on the DCC of PandaX-III prototype TPC project [11]. The picture of DCC is shown in Figure 7. The DCC contains a FPGA of Zynq-7, a DDR3 RAM of 4 Gbits for data storage, a standard RJ45 port and six SFP for optical fibers, which means one DCC can hold six DIFs. The SFPs are implemented with FPGA-based gigabit serial link to read DIFs’ data and send commands to DIFs. This DCC has been used in the PandaX-III prototype and showed sufficient data bandwidth and stable performance [12].

1. Test results

Some tests were carried out with the readout system in order to determine its performance. Baseline noise, calibration of SKIROC2, trigger efficiency, X-ray test and cosmic test will be introduced below.

* 1. Baseline and noise



Figure . Baseline and noise of all the 64 channels

To test the noise level of electronic system, the external trigger of SKIROC2 was used to get the pedestal noise of the system without the detectors. Concerning the time that SKIROC2 needs for conversion phase and readout phase is 4 ms, the DIF generated triggers at a fixed time interval of 10 ms. Figure 8 showed the sigma of noise and average of baselines of all the 64 channels. From the graph, not all 64 channels exhibited good baseline and noise results, but most channels’ noises were lower than 0.2 fC equivalent input charge.

* 1. Calibration



Figure . The linear fit results of two gain modes of SKIROC2

Taking advantaging of the SKIROC2’s 3pFcalibration capacitors on each channel, the self calibration was taken: a wave form generator with attenuator was used to generate step pulses with different amplitudes. When the step pulses were applied to on-chip capacitor, a certain amount of charge, which covered the full range, was injected into every channel of SKIROC2 from test pulse input for performance testing. SKIROC2 had many operation modes by tuning the callback capacitors array. The measurement has been tested with the highest gain mode (with a Cf of 400 fF) and lowest gain mode (with a Cf of 6 pF). The consistency of gain between different channels was good and the typical non-linearity curves of output value versus input charge of the two modes were shown in Figure 9. The figure showed that the linear range of the highest gain mode and the lowest gain mode were 50 fC and 3 pC. The integral nonlinearities (INL) in both modes were 0.2%.

* 1. Trigger efficiency

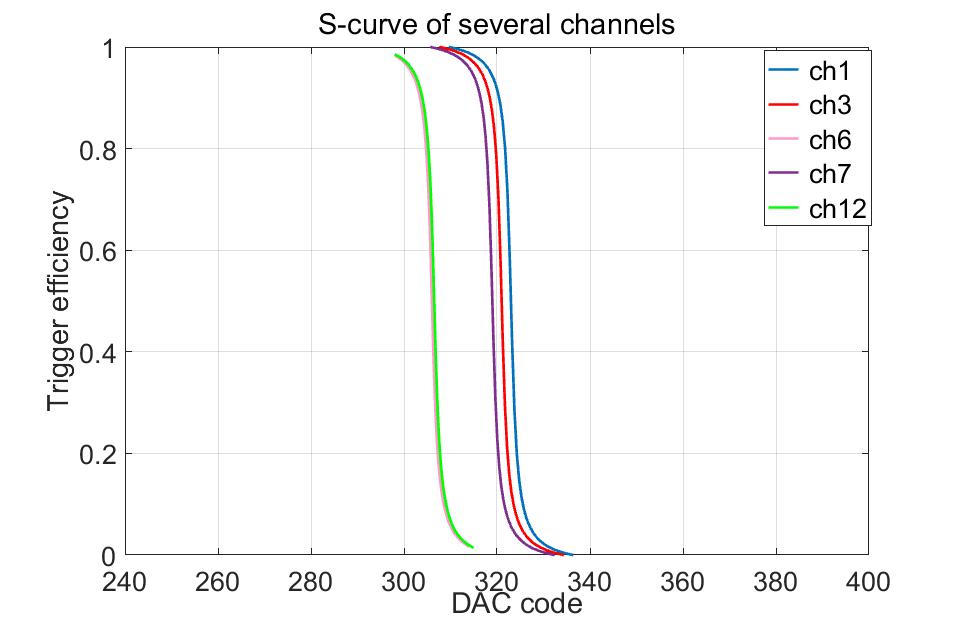


Figure . The S-curve of several channels when input is 2 fC

Trigger efficiency was obtained via the “S-curve”, shown in Figure 10. A fixed amount of charge was introduced from the test pulse input. By configuring the probe function of SKIROC2, the digital probe outputted the trigger signal if the fast shaper pulse exceeded the threshold. The S-curve was obtained with varying the trigger threshold. The curve was fitted by a complementary error function, whose center value stood for the threshold on the charge, and the sigma stood for the noise power. We obtained the S-curve from 1 fC to 15 fC of several typical channels, which covered 1 and 2 MIP equivalent charges. Since SKIROC2 has the function of “4-bit DAC adjustment” for every channel [6], the differences of thresholds between channels can be corrected.

* 1. X-ray test



Figure . The spectrum of X-ray of 241Am

Joint tesy with detector of S5980 was carried out with X-ray source of 241Am. In the test, a bias voltage of 13 V was applied as the high voltage of the silicon PIN detectors. The output signals were directly sent into SKIROC2, which was set to work in highest gain mode. In Figure 11, the spectrum of 59 keV x-ray was shown. According to the results of calibration, the equivalent input charge was 2.89 fC and resolution was 13.3%. The charge of 2.89 fC indicated that the average number of electron-hole pairs was 18109, which meant the average ionization energy of silicon was 3.25 eV. It was lower than the theoretical value of 3.6 eV. Concerning the Fano factor, the fact is reasonable.

* 1. Cosmic test

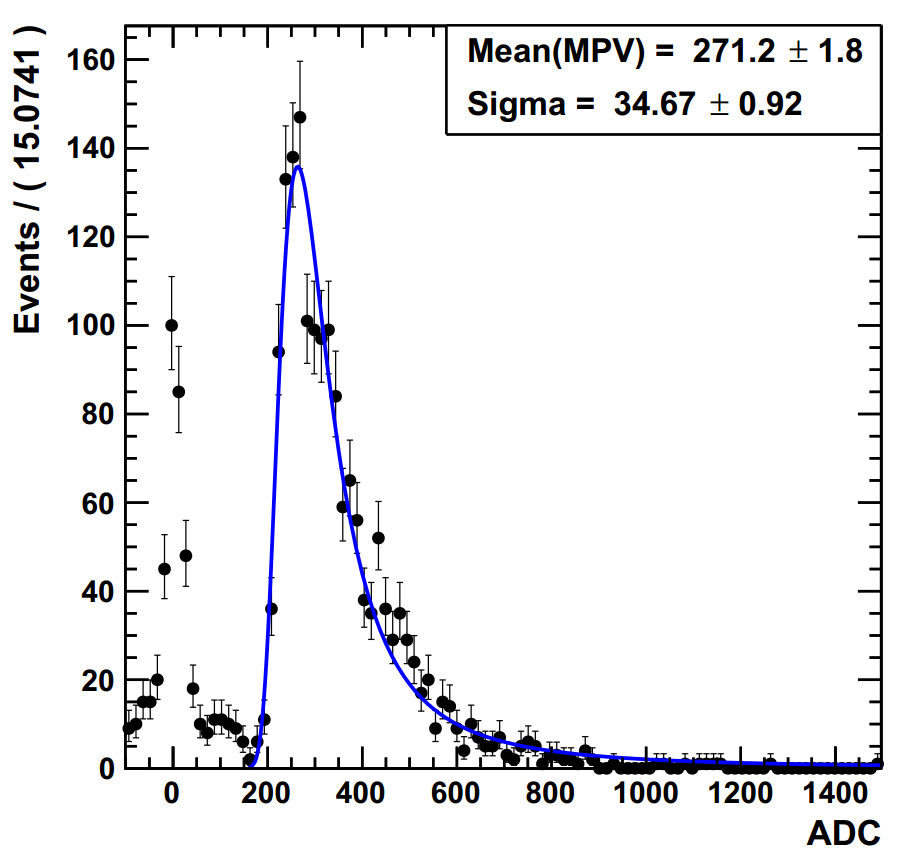


Figure . The spectrum of cosmic ray

A simple cosmic test of the system with one layer silicon PIN array was carried out. 64 silicon PIN detectors of S5980 were installed to get cosmic muons. Figure 12 showed the first result obtained with the system. Since there was no coincidence to filter the cosmic ray, the input angle had a distribution. As a result, the spectrum had non-Gaussian tails instead of a Gaussian distribution. The result of the Landau fit showed the mean of cosmic muon equivalent input charge was 7.13 fC.

1. Conclusion

In this paper, a prototype readout system for silicon PIN detectors based on SKIROC2 has been presented. The system, which is aimed to be the pre-design of the prototype of Si-W ECAL for CEPC, consists of FEB module, DIF module and DCC module. The system is scalable because of the modular structure. In addition, the feature of SKIROC2 allows the FEB to carry more detectors and ASICs without changing the interface to DIF. The main performance of the system are discussed in detail. The test results of X-ray and cosmic are shown in this paper.

Acknowledgments

The authors would like to thank Stephane Callier of Calice collaboration for his help in our system design. We also appreciate the discussion during the design with Yunlong Zhang of University of Science and Technology of China.

This work was supported by National Natural Science Foundation of China, under Grant No. 11635007.

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