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Development of a readout system for the $\overline{\text{P}}$ANDA Micro Vertex Detector

S. Esch,[a,1] **W. Erven,**[b] **M.C. Mertens,**[a] **M. Ramm,**[b] **J. Ritman**[a] **and T. Stockmanns**[a]

[a] *Institut für Kernphysik, Forschungszentrum Jülich, Wilhelm-Johnen-Straße, 52428 Jülich, Germany*
[b] *Zentralinstitut für Elektronik, Forschungszentrum Jülich, Wilhelm-Johnen-Straße, 52428 Jülich, Germany*

E-mail: s.esch@fz-juelich.de

ABSTRACT: The Micro Vertex Detector (MVD) is the innermost tracking detector of the $\overline{\text{P}}$ANDA (anti**P**roton **An**nihilation at **Da**rmstadt) experiment at the upcoming FAIR (**F**acility for **A**ntiproton and **I**on **R**esearch) facility in Darmstadt. The detector consists of four barrel and six disk layers of silicon pixel and strip sensors to obtain precise tracking of charged particles. For the development of a front-end ASIC a flexible and powerful readout system was designed to test different ASIC prototypes. We will present the upgrade of the FPGA-based Jülich Digital Readout System and measurements of the recent MVD pixel front-end prototype ToPix3. Tests of the implementation of the radiation hard GBT transfer protocol are also shown.

KEYWORDS: Hybrid detectors; Modular electronics; Electronic detector readout concepts (solid-state)

[1] Corresponding author.

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1 Introduction

Throughout the development of the Micro Vertex Detector (MVD) for $\overline{\text{P}}$ANDA, several iterations of electronics and detector parts must be evaluated. Different prototypes of the pixel front-end chip ToPix (**To**rino **Pix**el) need to be characterized under similar test conditions. To control these devices under test (DUT) and to store the recorded data, a suitable readout system is necessary. In order to ensure similar conditions for different prototypes and development stages, the readout system follows a modular concept. This makes it easily adaptable to the specific interface of different types of electronics. In addition the system must provide high performance to allow the evaluation of single front-end chips as well as fully assembled modules consisting of up to 6 front-end chips. The possibility to implement routines for online data processing is also desirable. A digital readout system has been designed to meet all these requirements for the development of the MVD, the Jülich Digital Readout System.

2 Jülich Digital Readout System

The Jülich Digital Readout System is a compact and powerful table top setup which allows quick testing of new detector components. The setup consists of the following components:

- Digital readout board
- FPGA firmware
- MVD readout framework (MRF) software with graphical user interface (GUI)

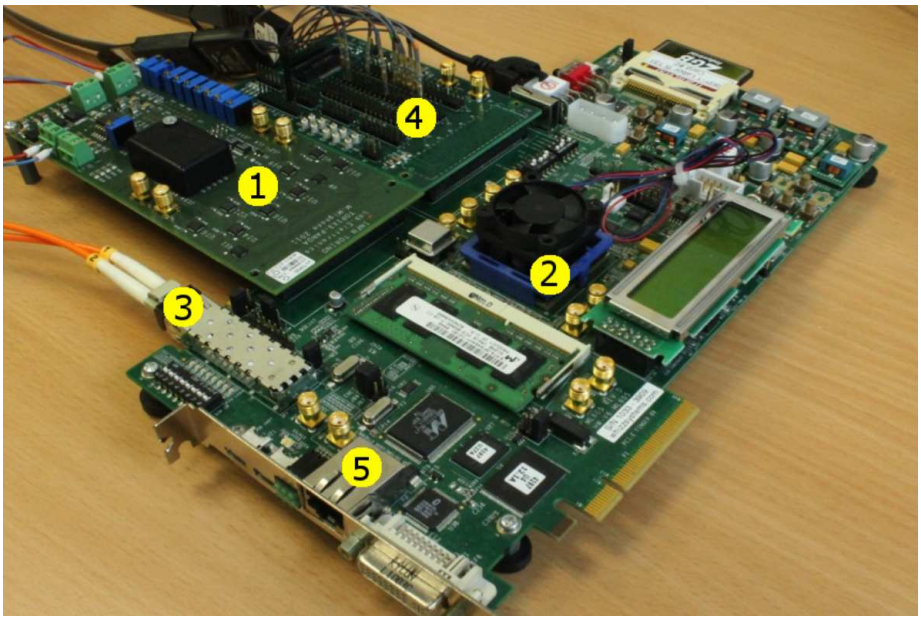

Figure 1. Jülich Digital Readout System setup. (1) ToPix3 test PCB connected via FMC, (2) Xilinx ML605, (3) SFP optical connection to readout PC, (4) XILINX Diagnostic Board FMC-X [3], (5) Tri speed ethernet PHY.

The central hardware component is the FPGA-based digital readout board. It is connected to the readout PC via an optical connection which is used to receive commands from the user and to send data via the SIS1100 [4] protocol to the PC for further processing. The corresponding software infrastructure is implemented within the MVD readout framework (MRF). The prototype is controlled by the user with a graphical user interface (GUI). On the other side the readout board is connected to the DUT on its test board. An intermediate adapter board converts the DUT signal interface to the interface of the digital readout board if necessary.

2.1 Readout hardware

The current readout system is based on the commercially available ML605 evaluation board from XILINX [2]. Its Virtex 6 FPGA and large number of I/O lines offer sufficient readout speed and connectivity to cope with the requirements of the upcoming full size ToPix prototype. The ML605 replaces the custom developed Virtex 4 based readout board which was used before [1]. The ML605 evaluation board (see figure 1) contains a DDR3 RAM slot for data storage and a Virtex 6 XC6VLX240T FPGA. The connection to the PC can be established via an SFP optical gigabit transceiver or standard ethernet network cable (RJ45). The interconnection to the DUT can be done via two FMC (FPGA Mezzanine Card) connectors with 68 (Low Pin Count - LPC) or 160 (High Pin Count - HPC) single ended user I/O lines.

2.2 FPGA firmware

The FPGA on the digital readout board is configured with a firmware which implements the desired functionality and configures the external interfaces. The firmware is written in VHDL, a hardware

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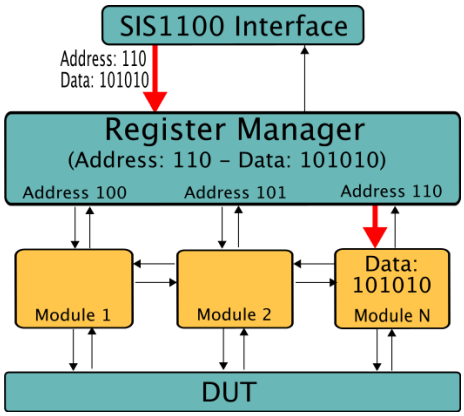

Figure 2. Schematic drawing of the firmware. Data which arrives at the firmware is distributed to the appropriate module according to its address. Data which shall be read is retrieved from the appropriate module according to its address and sent to the PC via the register manager.

description language, and then synthesized with the Xilinx development tools (ISE 14.1). The firmware is divided into different modules which handle the individual subtasks concerning the DUT, the onboard functionality and the communication. All modules are connected to a register manager which is itself connected to the SIS1100 interface (see figure 2). Data which arrives via the SIS1100 is formatted in address-data pairs. The register manager will distribute the data depending on the address to the concerning modules. If data should be read from the board, the register manager will take the data from the module indicated by its address. This modular design makes it easy to adapt the firmware to a different readout board or a different DUT respectively.

2.3 Software framework

The MVD Readout Framework (MRF) follows a modular design and defines different layers for communication inspired by the OSI model (see figure 3). The framework is written in C++ and has no external dependencies except the Standard Template Library (STL) to avoid conflicts with other libraries. This makes the MRF software a decoupled package which can be used in any environment. For every communication layer a basic set of commands is implemented to provide the data transport between adjacent layers. In addition specific commands for the used hardware are implemented. The layers are defined as follows:

GAL: Generic Access Layer. The generic access layer provides the basic functionality for communication with the digital readout board. The *read* and *write* commands provide basic access to registers over an open connection. All more complex commands of the upper layers are implemented using these basic functions. With the SIS1100 driver used by the GAL more powerful functionality is implemented: Direct Memory Access (DMA) or interrupt handling. The interrupt handling can be used for example to trigger a data transfer automatically.

TAL: Transport Access Layer. The transport access layer provides access to the functionality of the firmware. For both versions of the digital readout board certain basic functionality is available such as the online configuration of the FPGA's integrated clock generator and the controlling of status LEDs.

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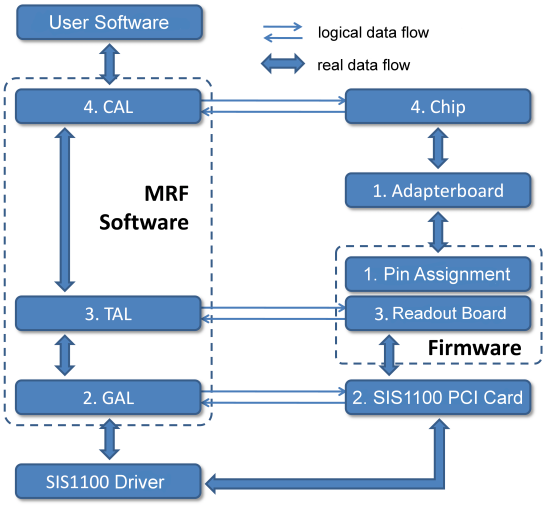

Figure 3. Schematic drawing of the Jülich Digital Readout System communication layers.

CAL: Chip Access Layer. The Chip Access Layer implements the functionality of the DUT and needs to be adapted to the specific hardware e.g. configuration of the chip or the readout sequence. Three versions have been made for the control of the Atlas FE-I3, ToPix2 and ToPix3. The complete readout and all testing procedures are available for all chips.

3 Measurements with the ToPix3

For the readout of the pixel part of the MVD a new front-end ASIC is under development. With a triggerless readout concept the ASIC has to provide a good spatial and timing resolution for each hit and must be able to handle high particle rates in a high radiation environment. The ToPix ASIC is under development to meet these requirements. The pixels have a size of $(100 \times 100)\,\mu\mathrm{m}^2$. For the measurement of the deposited charge the time-over-threshold (ToT) method is used. The ToPix3 is the recent reduced-scale prototype of the final ASIC [6]. For this ASIC 640 pixels are arranged in two 256 pixels double columns and two 64 pixels double columns covering an active area of $(3.2 \times 2)\,\mathrm{mm}^2$. The die itself has an area of $(4.5 \times 4)\,\mathrm{mm}^2$. For testing and calibration purposes a circuit is implemented to inject charge directly into the preamplifier. The following measurements have been done using this internal injection circuit.

3.1 Time-over-Threshold linearity

The relation between the deposited charge and the ToT is linear except for values of charge that are small compared to the applied threshold. This linear dependency should be valid even for large deposited charges. The ToPix is designed to cover a dynamic range of input charges up to 50 fC. In the experiment this would be equal to the most probable energy loss of protons with a momentum of $\sim$200 MeV/c. Figure 4 shows the ToT as a function of the injected charge and the deviation from the linear fit. For each charge value the mean of 100 ToT measurements is displayed. The measurement shows a linear behavior up to 1.2 V which is the maximum setting for the internal charge injection circuit with the recent testboard. This corresponds to a maximum injected charge

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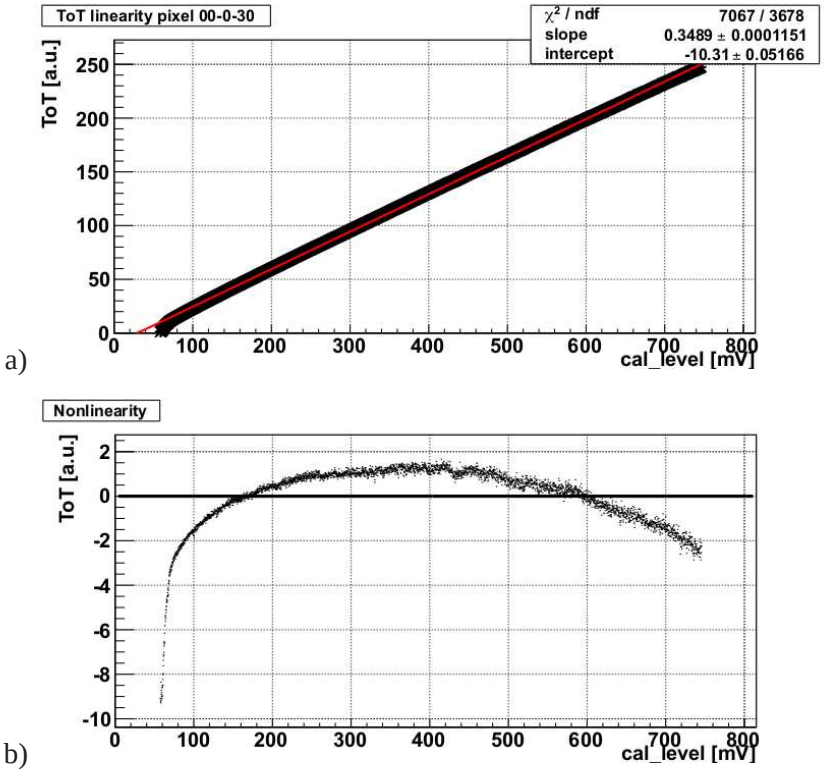

Figure 4. a) Time-over-Threshold (ToT) as a function of the injected charge. b) Deviation of the measurement from the expected linear behavior.

of 43.2 fC (calculated with the design value of the injection capacity of 36 fF). For charges below 3 fC one can see a deviation from the linear behavior which is expected and can be corrected in the reconstruction of the deposited charge from the ToT.

3.2 Threshold determination and tuning

The ideal behavior of a pixel threshold is a step-function, but due to noise this step-function is broadened (i.e. convoluted with the noise function which can be modeled by a Gaussian). The convolution of the step function with the Gaussian noise yields a characteristic S-shaped response function. The pixel's response function is measured by counting the number of hits compared to the number of injections while increasing the injected charge. Due to processing effects the effective threshold of different pixels can vary even if it is set to the same nominal threshold. Therefore, threshold determination and calibration are necessary. In the ToPix each pixel's threshold can be calibrated with a 5-bit DAC. In figure 5 the result of the threshold determination is shown. The measurement shows as expected the S-curve like shape. Figure 6 shows the result of the threshold tuning. The blue histogram shows the threshold distribution before the tuning. The black histogram shows a much narrower distribution after tuning as it is expected. The determined σ values correspond to 1177 electrons for the untuned distribution and to 247 electrons for the tuned distribution, calculated with the design injection capacitance of 36 fF.

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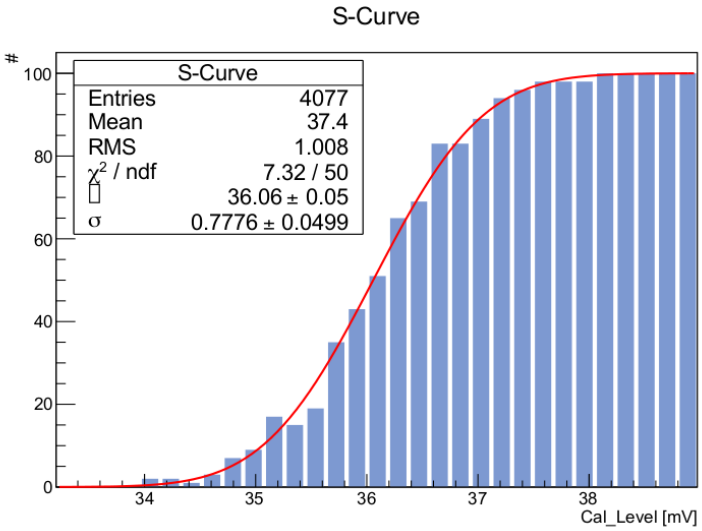

Figure 5. Determination of the threshold for a single pixel with the internal injection circuit. The red curve is a fit with an error function.

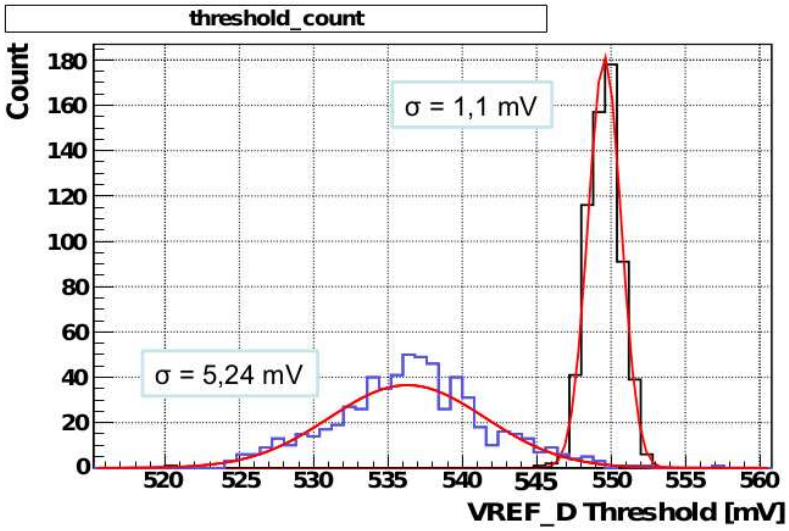

Figure 6. Tuning of the single pixel threshold for a ToPix 3 module. Blue curve: Threshold distribution before tuning. Black curve: Threshold distribution after tuning. Red curves: Gaussian fits.

3.3 Time walk

The front-end electronics detect a hit when the integrated charge is large enough for the preamplifier output to cross the applied threshold. However, this time varies depending on the total amount of charge. For small signals it takes longer to reach the threshold, thus also the threshold crossing is later compared to the physical hit time of the sensor. This effect is called the time walk of a signal and worsens the time resolution of the detector. Due to the dependency of the time walk on the amount of deposited charge the time walk can be corrected. In figure 7 one can see the leading edge of the hit i.e. the first crossing of the threshold as a function of the injected charge. The black curve

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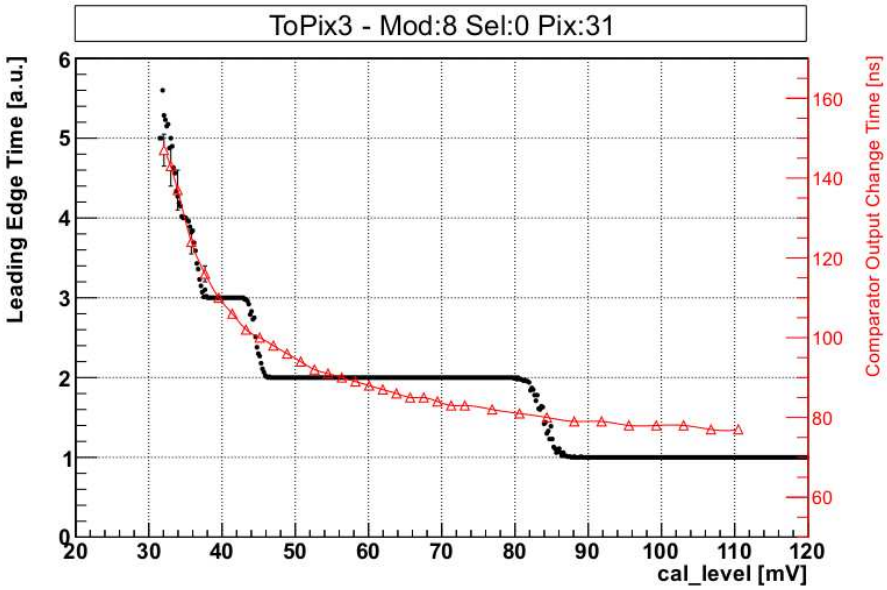

Figure 7. Time walk of the signal. Red curve: Analog time of the averaged time when the comparator output changes. Black curve: Averaged leading edge timestamp measured in ToPix clock cycles.

shows the mean digitized leading edge after 100 injections. One can see that the leading edge time gets larger with decreasing injected charge (in digital steps). The clock frequency is 50 MHz. The red curve shows the mean output of the comparator after 100 injections. One can see as expected the rising of the TimeWalk with decreasing injected charge.

4 MVD data transfer

Due to the triggerless readout principle and the high interaction rate in the $\overline{\text{P}}$ANDA detector the MVD has to transfer a high amount of data to the compute nodes where the actual event building and event selection takes place. It must be ensured that the data can be transferred without corruption despite the high radiation environment. Thus the GigaBit Transceiver (GBT) [7] and the Versatile Link, developed for the LHC experiments, are under investigation for the usage at $\overline{\text{P}}$ANDA. The GBT project has developed a radiation hard-hard bi-directional 4.8 Gb/s optical link to transfer data from the front-ends to the counting room. The Versatile Link group has developed radiation hard hardware for this purpose.

To test the GBT protocol, an FPGA code has been developed by the GBT group for the Virtex5 [8]. This code has been set up on two ML605 boards in order to test the communication between them using the GBT protocol. The boards have been connected with four coaxial cables to establish a differential sending and receiving line. Each board implements a counter which continuously increments its value. The counter value is sent to the respective other board via GBT and verified to be continuously incrementing by one. This setup ran for 21 hours without errors. Having passed this stability test, the code of the GBT protocol can be implemented in the Jülich Digital Readout System.

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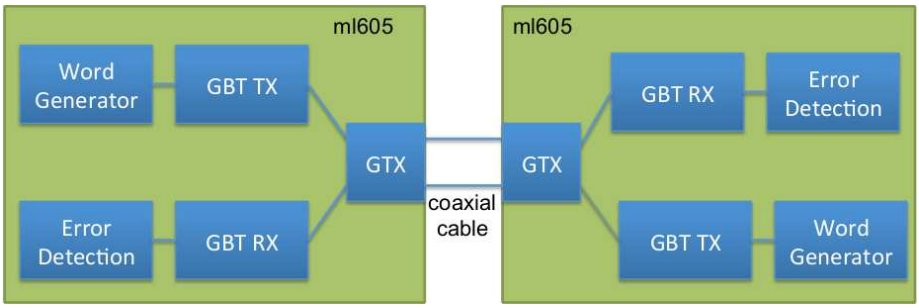

Figure 8. Schematic view on the GBT test setup. Two ML605 have been connected with two coaxial cables. Both boards are sending data and control the data from the other board.

5 Conclusion

A digital readout system for testing of various types of front-end chips and detector parts has been presented. With its modular concept it can be easily adapted to different front-end interfaces. The digital readout system has been used for measurements with the recent prototype ToPix3, the front-end ASIC foreseen for the pixel part of the Micro Vertex Detector for the $\overline{\text{P}}$ANDA experiment. The measurements are in good agreement with the expectations.A GBT test loop has been set up on the ML605 and its stability has been successfully tested on our development hardware. The GBT will be implemented into the Jülich Digital Readout System for the readout of the next prototype ToPix4.

Acknowledgments

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