Design of the FPGA-based Gigabit Serial Link for PandaX-III Prototype TPC

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Abstract. PandaX-III is aimed to search for Neutrinoless Double Beta Decay of ^{136}Xe at China Jin Ping underground Laboratory. To test various design features of PandaX-III detector, a prototype TPC with 20 kg Xe containing inside is built. Front-end boards installed inside the water-proof vessel integrate charge of Micromegas signal, digitize signal waveform and send data packet to back-end board. Front-end boards receive synchronous information (global clock, global trigger, etc.), as well as command messages from back-end board. In order to satisfy the requirement of high data throughput and multiple types of synchronous data transmission, we propose a user-defined protocol optical fiber link to communicate between front-end board and back-end board. Communication of serial transmission is performed using FPGA based Gigabit Transceiver with a 1 Gbit/s point-to-point speed. To validate the performance of this link, bit error rate and eye diagram are tested. Preliminary joint test with detector is conducted in Shanghai, which shows sufficient data bandwidth and stable performance.

Keywords: Gigabit Transceiver, TPC, Micromegas, PandaX-III.

1 Introduction

1.1 PandaX-III Experiment

Particle And Astrophysical Xenon Experiment III (PandaX-III) is the neutrinoless double beta decay detection experiment in China Jin Ping underground Laboratory (CJPL) [1]. This experiment targeting to discover the rare nuclear weak-decay could uncover the possible Majorana nature of neutrinos, thus would be an important breakthrough in fundamental physics.[2] The gas TPC technology for NLDBD provides high energy resolution and the capability of track detection, which is critical for identifying NLDBD events. Fig.1 shows the schematic of PandaX-III TPC. PandaX-III TPC is shielded by ultra-clean water in all directions to reduce background. Digitized signal data of front-end board need to be transferred back to back-end board, and then to PC farm running software. One critical requirement of this readout scheme is to

design an appropriate link between electronics, which needs high throughput, low material, water proof and robustness. The development of modern communication technology has offered optical fiber as a mature technology for high-speed, simple, waterproof and reliable data transmission. This paper describes the design of gigabit optical fiber link for PandaX-III prototype TPC.

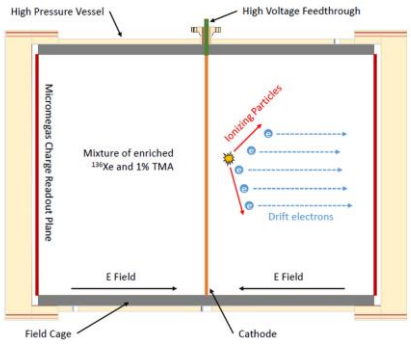

Fig. 1. Schematic of the PandaX-III TPC.

1.2 Requirement of Serial Data Transfer

In the current design, Front-End Card (FEC) is designed with 256 readout channels, covering 2 Micromegas modules. Each FEC contains 4 ASIC chip AGETs, each in charge of amplifying, shaping and 512 analog sampling for 64 channels. Besides, a discriminator for multiplicity building and self-trigger is provided in it [3] [4]. Sampled analog signal from AGET is digitized by an ADC, and then the digitized waveform is processed in an on-board FPGA, and finally sent back through optical fiber.
According to Monte Carlo simulation, in PandaX-III experiment the trigger rate is at about 10 Hz trigger rate, event data rate of each FEC is about 21 Mbps. Considering the possibility of significant higher event rate in calibration runs, 1 Gigabit data bandwidth is necessary for FEC data transmission.
To realize a complete 3D track reconstruction, synchronizing clock and trigger of all FECs is necessary. A feasible way to realize global clock and trigger is using clock and trigger from the same source. FECs recover clock from serial data and generate clocks for ADCs and AGETs. Triggers from all FECs would be assembled by back-end board to generate global trigger, which then get distributed via optical fiber.

2 Realization of gigabit serial link

2.1 Design of serial link

To implement gigabit serial link that satisfies requirement of sending synchronous clock and trigger, configuration command and raw data simultaneously, we use FPGA based high-speed transceiver, GTP on FEC and GTX on back-end DAQ board respectively. 1 Gbps bidirectional small form-factor pluggable (SFP) optical transceiver transforms optical signal to high-speed serial data, and then this serial data is sent to

FPGA. GTP/GTX integrated in FPGA is responsible for descrambling data, 8B/10B encoding and clock recovery. To reduce trigger latency and accommodate requirement for decoding various type of data, we develop a user defined protocol. When no valid data is transmitting, K28.5 (a specific control K character) is send. The high 8-bit of the first valid data is used as the header of data package (currently 8'h0, 8'h1 and 8'h4 are indicators of trigger, command and payload data). The structure of payload data packet is composed of START_OF_PACKET constant, data indicator, valid event data and END_OF_PACKET constant. The logic on DAQ FPGA is responsible of data package verification.

2.2 Prototype TPC for PandaX-III

To test the features of Micromegas detector for PandaX-III, a small-scale prototype TPC equipped with 7 Micromegas modules is built by Shanghai Jiao Tong University group. A readout electronic system for this prototype TPC is designed, comprising of 4 FECs and 1 DAQ. Fig. 2 shows the block diagram of TPC prototype readout electronic system and the proposed serial link is implemented and verified.

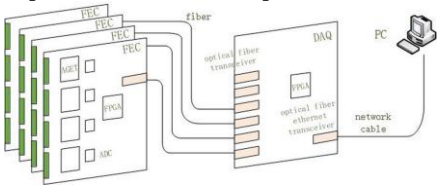

Fig. 2. Schematic block diagram of readout electronic system for prototype TPC.

3 Performances

3.1 Optical fiber signal transmission quality test

To confirm the validation and stability of data communication between FEC and DAQ, two tests are conducted: eye diagram measurement and Bit Error (BER) test. Oscilloscope eye diagram test result is shown in Fig. 3. To conduct BER test, we firstly employ Xilinx IP core IBERT, and test result shows BER lower than 1×10^{-13}. IBERT core analyses RX margin and produce a 2D plot of transceiver eye margin, as Fig. 4 shows. Both of the test results indicate good timing margin. Then we use FPGA logic to generate RPBS7 (one telecom widely used PRBS pattern) and send it through optical fiber to FEC. FPGA on FEC detects the received data and compares it with local generated PRBS7 data. Test was conducted over 24 hours continuously, and no bit error is detected. We can conclude that BER is lower than 1.15×10^{-14}.

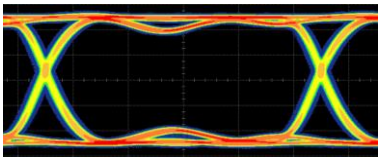

Fig. 3. Oscilloscope test eye diagram.

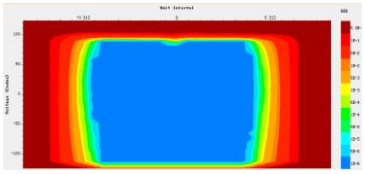

Fig. 4. IBERT analysis eye scan diagram.

3.2 Joint test with prototype TPC

To evaluate the function of user defined protocol and processing logic, preliminary joint test with prototype TPC is conducted in Shanghai Jiaotong University, as Fig. 5 shows. One Micromegas module is readout by a FEC board and then event data transmitted to a DAQ board via optical fiber. During calibration test, full strips data are readout at about 700 Mbps data rate. Joint test prove this serial link satisfies requirement for PandaX-III readout system.

Fig. 5. (Left) Picture of a FEC board connecting one Micromegas module. The FEC is placed on the top of prototype TPC high pressure vessel. (Right) Picture of a DAQ board. These two boards communicate through optical fiber.

4 Conclusion

To satisfy the requirement for synchronous clock, trigger and high-bandwidth data transmission in PandaX-III experiment, a FPGA-based gigabit serial link with user defined protocol is designed. Detailed tests of transmission quality and a preliminary joint test with prototype TPC show this link meets experiment requirement. This work will be applied to R&D of PandaX-III Micromegas detector.

5 Acknowledgement

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