Prototype Readout Electronics of Silicon PIN Diode Arrays for CEPC ECAL Pre-research

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Abstract: A readout system, which is based on SKIROC2 ASIC (Application-Specific Integrated Circuit), for silicon PIN diode array detectors has been developed. The system, which is intended for preliminarily studying the design concept of Si-W ECAL (Electromagnetic Calorimeter) at CEPC (Circular Electron Positron Collider), mainly consists of three kinds of electronics modules: the Front-End Board modules (FEB), the Data-Interface modules (DIFs) and a Data Concentration Card (DCC). The FEB, which carries the SKIROC2 ASIC and the silicon PIN diode array (S5980 from HAMAMATSU), is in charge of particles detection and converting the signals from analog to digital. The DIF is designed to control the FEB and transfer data to DCC via optical fiber. The DCC gathers data from all DIFs and transmits data to computer through Gigabit Ethernet interface. The electronic noise of all the channels is below 0.4 fC, and most of them are below 0.2 fC. The dynamic range is up to +3000 fC with an Integral NonLiearity (INL) of 0.2%, and the consistency of gain between different channels is good. Joint tests with a radioactive source (241Am) and cosmic ray have been carried out. The x-ray resolution at 59 keV reaches 13.3% (in RMS). The Signal-to-Noise Ratio (SNR) of cosmic muon is ., which satisfies the requirement of current phase.

Keywords: ECAL; CEPC; Prototype; Silicon PIN diode; SKIROC2; Readout system; FPGA; Analog-digital conversion; Data-acquisition, Modular electronics; Front-end electronics.

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1. Introduction

The Circular Electron Positron Collider (CEPC) is a proposing next-generation electron-positron collider in China, as Higgs and/or Z factory [1]. The main targets of CEPC are producing Higgs boson, whose separation depends on the success of the particle flow concept [2], and making precise measurements of it. The CEPC calorimeters, including the Electromagnetic Calorimeter (ECAL) and hadron calorimeter, are in charge of precise energy measurements of electrons, photons, taus and hadronic jets. In order to obtain the supreme energy resolution, the particles inside the jets are separated and each track is assigned to calorimeter cluster one by one. To maximize the particle separation, a kind of high-granularity ECAL is critical. The Silicon-Tungsten-based ECAL (Si-W ECAL) is an important option.

According to the Preliminary Conceptual Design Report (Pre-CDR), the requirements for the ECAL are an energy resolution of and an energy range up to 100 GeV [1].The Si-W ECAL is a sampling calorimeter with tungsten absorber and highly segmented readout layers made of pixelised silicon PIN pad sensor arrays. According to the simulation and test results of CALICE ECAL physics prototype [3,4] for International Linear Collider (ILC) [5], the Si-W ECAL for CEPC needs dozens layers of silicon PIN arrays and each pad’s size of silicon PIN is about 1 × 1 cm2 [1], which means the total number of electronic channels is tens of millions.



Figure 1. The cascading relationship of ECAL prototype.

In order to verify the feasibility of principle and key techniques of ECAL, a prototype is need to be built. As shown in Figure. 1, this prototype should have several layers of pixelised silicon PIN array and a readout electronics system which is multi-channel and scalable. For each silicon PIN pad, the Signal-to-Noise Ratio (SNR) of Minimum Ionizing Particle (MIP) should be better than 2 and the energy range should be at least 500 MIPs. An ASIC named SKIROC2 [6], with 64 input channels and self-trigger function, is one of the candidate chip for the front end electronics to handle the silicon PIN arrays’ outputs. In order to test the performance of silicon PIN diod as well as to make a pre-design for the prototype, a scalable readout electronics based on SKIROC2 ASIC has been developed.

1. Implement of the system
   1. Architecture



Figure 2. The architecture of the readout electronics system

The architecture of this system is shown in Figure 2. It’s mainly composed of three kinds of modules, the detector and ASIC module called Front-End-Board module (FEB), the Data Interface module (DIF), the Data Concentration Card module (DCC). The FEB supplies high voltage for silicon PIN detectors, receives and digitizes the signal from the detectors. The FEB is configured by the DIF controls and drives data to the latter, which then are transferred to the DCC via optical fibre after packing process. Each DIF and FEB pair is responsible for a single layer. The DCC is in charge of sending commands to DIFs, gathering all data from up to six DIFs, making necessary compression and transferring data to PC. A prototype with up to six layers of detector arrays will be implemented.

* 1. ASIC

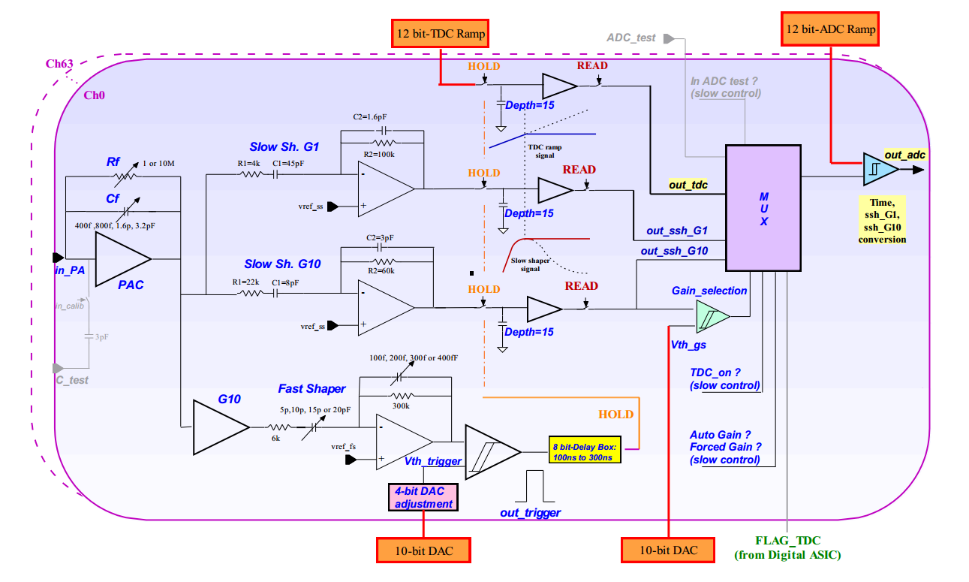


Figure 3. The schematic diagram of the analog part of SKIROC2

The core of the FEB is the chip SKIROC2 (Silicon Kalorimeter Integrated ReadOut Chip 2). SKIROC2 is an ASIC for the International Large Detector (ILD) [7] Si-W ECAL, which is designed by IN2P3/Omega group in France. Depicted in Figure. 3 is the schematic diagram of SKIROC2. There are 64 channels integrated with one chip. Each channel is composed of a Charge-Sensitive Amplifier (CSA), two slow shapers with different gains, one fast shaper with a discriminator, a Time-to-Digital Convertor for time measurement, three Switched Capacitor Arrays (SCA) of 15 depth to store analog signal and an ADC to convert analog signal to digital one. The SKIROC2 is available on Ball Grid Array (BGA) package, as well as Quad Flat Package (QFP).

The input signal passes through the CSA with variable gain set by feedback capacitance (Cf). The output of CSA is fed to the fast shaper and two slow shapers with different gains. By comparing fast shaper’s output with threshold, the discriminator generates trigger signal to hold the voltages at two slow shaper outputs and an additional scanned voltage source for timing measurements on the SCAs. The signals on the SCAs are read out and converted by a 12-bit Wilkinson ADC and a multiplexer, with a bunch ID tagged with 10MHz slow clock, then saved in the on-chip memory.

Benefited from the two slow shaper with different gains and the adjustable gain CSA, the SKIROC2 has a wide dynamic range ensuring a linear response for 1-1500 MIP signals. The peaking time is tunable between 50 ns and 100 ns. These features satisfy the requirements of silicon PIN detector. As a result, the SKIROC2 is chosen as readout chip of the system.

* 1. FEB



Figure 4. A schematic of connection of silicon PIN S5980

In current phase, the FEB accommodates one SKIROC2 chip to read 64 detector signals. The silicon PIN detector S5980, which has four outputs from the anode of diode and one common cathode, from HAMAMATSU is one of the candidate detector for the prototype [8]. The total active area is 5 × 5 mm2 and the thickness is 460 um. Its dark current and terminal capacitance suit SKIROC2’s input demand. According to simulation, the cosmic MIP signal of S5980 is about 7.5 fC. The schematic of detector to ASIC is shown in Figure 4. To make the best use of SKIROC2’s inputs, the detectors are formed an array of 8 × 8, which means the total active area is 1600 mm2. The S5980 claims a high-voltage of 13V. Since its output noise is very sensitive with the ripple of high-voltage, a well-designed Low-DropOut regulator (LDO) TPS7A4700 [9] from Texas Instruments company (TI) is employed, with the Power-Supply Ripple Rejection low to 82 dB and the output noise as little as 4 uVrms. The capacitor and resistor are used to decouple the high-voltage. The SKIROC2’s input supplies a reference voltage about 1V to ensure the detector working in correct status, so the anode of the detector directly connects the ASIC.

After being acquisited and converted, the signals from silicon PIN diode array are converted from analog to digital by SKIROC2 and stored in memory of it, waiting to be readout. The SKIROC2 is controlled by Field-Programmable Gate Array (FPGA) on DIF. There are two kinds of control data buses, fast control and slow control. Fast control buses, which are through Low Voltage Differential Signal (LVDS) pairs, are in charge of SKIROC2's clock, trigger and reset/ valid the SCA. Slow control, however, is in a daisy chain cascade. It configures a 616-bits registers to store many configurations such as Cf and trigger mode. The DIF controls the ASIC on FEB to readout memory data and transmit them to DIF over Open Collector (OC) gate. Considering the OC gate and daisy chain cascade, it’s very convenient to expend FEB for more detectors and ASICs without changing the interface definition to DIF. The DIF also supply an initial voltage of 5 V for FEB.

* 1. DIF



Figure 5. Picture of DIF

The picture of the DIF is shown in Figure 5. The DIF mainly has these parts: FPGA, connector, power supply and interface.



Figure 6. Block diagram of logic implemented in the FPGA

The FPGA part is composed of a FPGA (ARTIX 7, Xilinx), a flash Programmable Read Only Memory (PROM, N25Q128) as well as a connector in order to program the FPGA via JTAG. The FPGA is clocked with an 80 MHz crystal. The FPGA’s function is to implement the required logic to control FEB and to communicate with DCC board or directly to PC. The logic diagram is shown in Figure 6. The Acquisition module controls the ASIC to work in the normal mode and get data saved in the memory of SKIROC2. The data transferred into FPGA will be stored in the First-In-First-Out (FIFO) and then transferred to DCC or PC. The trigger module is in charge of generating trigger when using calibration mode or ex-trigger mode. Calibration module and S-curve module are used to control the ASIC to be calibrated or tested. These tests will be discussed below. The optical module transmits data from FIFOs to DCC and gets command from DCC via optical fiber. The transmission is based on the high-speed transceiver GTP on FPGA. The GTP is responsible for descrambling data, 8B/ 10B encoding and clock recovery. The USB module, however, is used to communicate with PC directly when debugging a single DIF.

The communication with FEB is via two ERNI-154744 connectors [10]. All control signals and reply signals as well as power supply for FEB are through the two connectors.

Interface part is composed of a 1 Gbps bidirectional Small Form-factor Pluggable (SFP) optical transceiver for communication with DCC and a USB interface realized by a USB chip CY7C68013 and a Mini-USB port for communication with PC when debugging.

Supply part is implemented with a dc input level (5V) from outside and several LDO regulators (TPS74401, TI). From this dc supply rail, analog power supplies (1.0 V, 1.8 V, 2.5 V and 3.3 V) are generated by these LDO regulators for DIF.

* 1. DCC



Figure 7. Picture of DCC

The function of DCC board is to gather all DIFs’ data from optical fibers and to transmit data to PC server via a gigabit standard Ethernet network cable (RJ45). The current readout system is based on the DCC designed for PandaX-III prototype TPC project [11]. The picture of DCC is shown in Figure 7. It contains a FPGA of Zynq-7, a DDR3 RAM of 4 Gbits for data storage, a standard RJ45 port and six SFP for optical fibers, which means one DCC can carry six DIFs. The SFPs are implemented with FPGA-based gigabit serial link to read DIFs’ data and send commands to DIFs. This DCC has been used in the PandaX-III prototype and showed sufficient data bandwidth and stable performance [12].

1. Test results

Some tests were carried out with the readout system in order to determine its performance. Baseline noise and calibration of SKIROC2, trigger efficiency, X-ray test and cosmic test will be introduced below.

* 1. Baseline and noise



Figure 8. Baseline and noise of all the 64 channels

In order to evaluate the noise level of electronic system, the external trigger function of SKIROC2 was used to get the pedestal of the system without detectors. The DIF generated triggers in a fixed time interval to FEB, controlling the acquisition of baseline. Concerning the time that SKIROC2 needs for conversion phase and readout phase is 4 ms, the DIF generated triggers at a fixed time interval of 10 ms. SKIROC2 held the baselines of all 64 channels and converted them to digital when trigger came. Figure. 8 showed the average of baselines and sigma of noise of all the 64 channels. From the graph, not all 64 channels exhibited good baseline and noise results, but most channels’ noises were lower than 0.2 fC equivalent input charge. The maximum was less than 0.4 fC. Concerning the fact that the S5980’s MIP signal was about 7.5 fC, this noise level satisfied the requirements.

* 1. Calibration



Figure 9. The linear fit results of two gain modes of SKIROC2

Calibration test is to obtain the linearity and dynamic range of SKIROC2. Taking advantaging of the SKIROC2’s 3 pF calibration capacitors on each channel, the self-calibration was taken: a wave form generator with attenuator was used to generate step pulses with different amplitudes. When the step pulses were applied to on-chip capacitor, a certain amount of charge, which covered the full range, was injected into every channel of SKIROC2 from test pulse input for performance testing. SKIROC2 had many operation modes by tuning the Cf array. The measurement has been tested with the highest gain mode (with a Cf of 400 fF) and lowest gain mode (with a Cf of 6 pF). The consistency of gain between different channels was good and the typical non-linearity curves of output value versus input charge of the two modes were shown in Figure 9. The figure showed that the linear range of the highest gain mode and the lowest gain mode were 50 fC and 3 pC. The integral nonlinearities (INL) of both modes reached 0.2%.

* 1. Trigger efficiency



Figure 10. The S-curve of 2 channels when input is 2 fC

Trigger efficiency was obtained via the “S-curve”, shown in Figure 10. The trigger threshold was set by two Digital-to-Analog Conversion (DAC) settings, a global threshold with a 10-bit DAC and channel by channel adjustment with 4-bit DACs. To test trigger efficiency, a fixed amount of charge was introduced from the test pulse input. If the fast shaper pulse exceeded the threshold, SKIROC2 would output trigger signal. The S-curve was obtained by varying the trigger threshold 10-bit DAC and recording the efficiency at each DAC code. The curve was fitted by a complementary error function, whose center value stood for the threshold on the charge, and the sigma stood for the noise power. The 4-bit DAC adjustment for every channel should help to get a better threshold consistency. But there was a bug that this function did not work properly in SKIROC2. In the new version of SKIROC2a, this bug had been fixed.

* 1. X-ray test



Figure 11. The spectrum of X-ray of 241Am

Joint tesy with detector of S5980 was carried out with X-ray source of 241Am. In the test, a bias voltage of 13 V was applied as the high voltage of the silicon PIN detectors. The output signals were directly sent into SKIROC2, which was set to work in highest gain mode. In Figure 11, the spectrum of 59 keV x-ray was shown. According to the results of calibration, the equivalent input charge was 2.89 fC and resolution was 13.3%. The charge of 2.89 fC indicated that the average number of electron-hole pairs was 18109, which meant the average ionization energy of silicon was 3.25 eV. It was lower than the theoretical value of 3.6 eV. Concerning the Fano factor, the fact is reasonable.

* 1. Cosmic test

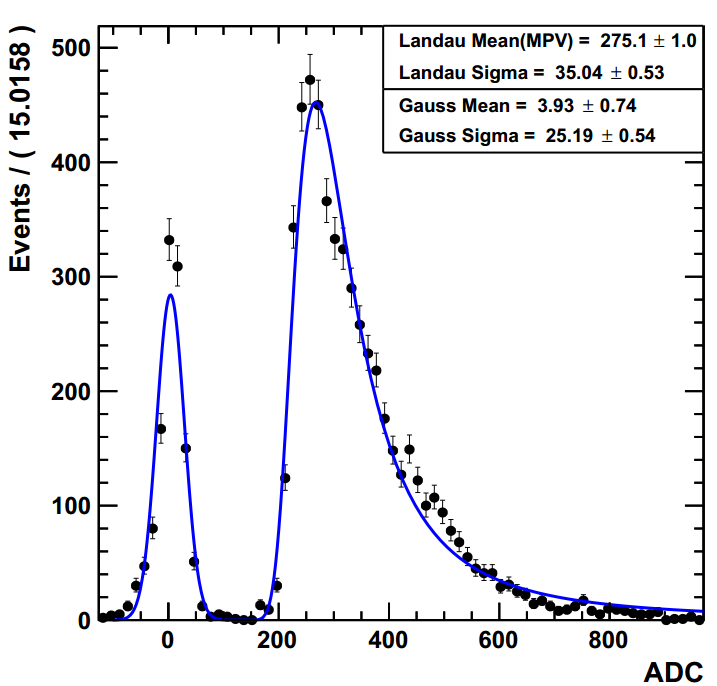


Figure 12. The spectrum of cosmic ray

A simple cosmic test of the system with one layer silicon PIN array was carried out. 64 silicon PIN detectors of S5980 were installed to get cosmic muons. Figure 12 showed the first result obtained with the system. Since there was no coincidence to filter the cosmic ray, the input angle had a distribution. As a result, the spectrum had non-Gaussian tails instead of a Gaussian distribution. The result of the Landau fit showed the mean of cosmic muon equivalent input charge was 7.23 fC.

1. Conclusion

In this paper, a prototype readout system for silicon PIN detectors based on SKIROC2 has been presented. The system, which is aimed to be the pre-design of the prototype of Si-W ECAL for CEPC, consists of FEB module, DIF module and DCC module. The system is scalable because of the modular structure. In addition, the feature of SKIROC2 allows the FEB to carry more detectors and ASICs without changing the interface to DIF. The main performance of the system are discussed in detail. The test results of X-ray and cosmic are shown in this paper.

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