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Front-end readout electronics considerations for Silicon Tracking System and Muon Chamber

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Abstract: Silicon Tracking System (STS) and Muon Chamber (MUCH) are components of the Compressed Baryonic Matter (CBM) experiment at FAIR, Germany. STS will be built from 8 detector stations located in the aperture of the magnet. Each station will be built from double-sided silicon strip detectors and connected via kapton microcables to the readout electronics at the perimeter of each station. The challenging physics program of the CBM experiment requires from the detector systems very high performance. Design of the readout ASIC requires finding an optimal solution for interaction time and input charge measurements in the presence of: tight area (channel pitch: 58 μm), noise (<1000 e- rms), power (<10 mW/channel), radiation hardness and speed requirements (average hit rate: 250 khit/s/channel).

This paper presents the front-end electronics' analysis towards prototype STS and MUCH readout ASIC implementation in the UMC 180 nm CMOS process and in-system performance with the emphasis on preferable detector and kapton microcable parameters and input amplifiers' architecture and design.

Keywords: Front-end electronics for detector readout; Analogue electronic circuits

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Contents

1 Introduction

一样的套路，先讲大背景，再讲探测器背景

Compressed Baryonic Matter (CBM) experiment at FAIR center, Darmstadt, Germany is aimed towards investigation of the QCD phase diagram in the region of high baryon densities using nucleus-nucleus collisions. The Silicon Tracking System (STS) is one of the CBM detector systems and provides track reconstruction and momentum determination of charged particles from the beam-target interactions [1]. Each of 8 tracking stations will be placed in the acceptance of magnet within a distance between 30 cm and 100 cm from the target. The station is built from light-weight ladders holding double-sided AC-coupled 300 μm thick silicon microstrip sensors. Sensors will be connected with the Read-Out Integrated Circuit (ROIC) located at the station's perimeter via the kapton microcables. The expected hit rate ranges from ~ 10 MHz/cm^2 in the central regions of the detector stations to ~ 0.1 MHz/cm2 in the outer regions of detector stations. The detector system uses different detector strip lengths (and therefore microcable lengths) to adapt to the expected occupancy [1, 2]. To achieve the desired track reconstruction efficiency, hits should be processed with Equivalent Noise Charge (ENC) close to 1000 e- rms and the processing chain should be able to handle an average input hit rate of 250 kHz/channel.

探测器需求，hit rate and noise

This paper includes the STS detector system noise optimization with an emphasis on the selection of the ROIC input amplifier together with results of the sensor and microcable parameters' optimization. Recommendations towards the power supply noise performance to achieve the design goal are also included.

和文章主题联系起来

2 Front-end electronics design

More than 14000 ROICs will be located at the perimeter of the STS detector stations. The STS readout ASIC is supposed to digitize each detector hit crossing to 5-bit charge information and 14-bit timestamp with 3.125 ns bin. The requirements towards the STS readout chip are the following:

- Scalability in terms of expected hit rate (both in analog — shaping time and digital domain — configurable number of output data streams).

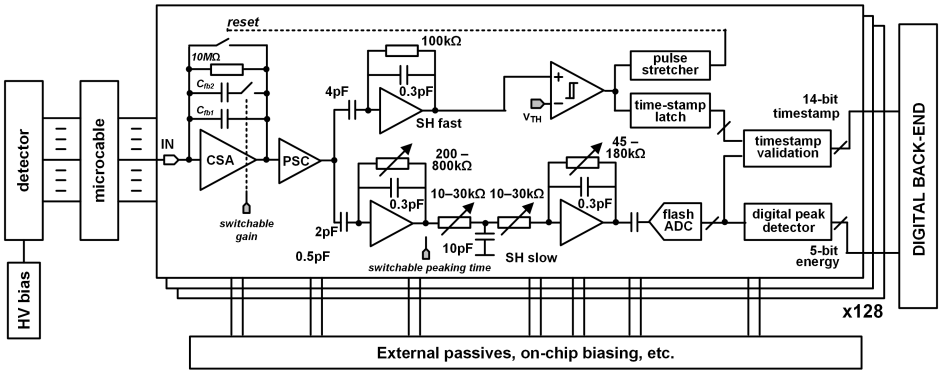

Figure 1. Simplified diagram of the single processing channel in the STS-XYTER2 chip including off-chip components affecting the noise performance.

- Possible application also in the Muon Chamber (MUCH) detector in the CBM experiment: dynamic range: 0–12 fC (STS mode) and 0–100 fC (MUCH mode)
- Power consumption: maximum 10 mW/channel.
- Number of channels per chip: 128, channel pitch: 58 μm.
- Chip size: approximately 10 mm × 6.7 mm.
- Radiation-hardened design.
- Self-contained architecture requiring little number of external components (power supplies, LVDS termination, bypass capacitors)
- Fast, scalable digital interface and protocol compatible with GBTx e-link able to provide tens of MHit/s of bandwidth and pre-sorted stream of hit frames.
- Testability features: wafer-level probing, tests with pogo pin prober, diagnostics options, built-in calibration etc.

Based on the above mentioned requirements, a new prototype of the STS read-out is currently being developed: STS-XYTER2 (see figure 1). The chip uses a low-noise Charge Sensitive Amplifier (CSA) to aggregate the charge generated in the detector active volume and to convert it into the voltage step. The CSA feedback is built of a parallel connection of a C_{fb1} = 100 fF capacitor (resulting in nominal charge gain k_{q_csa} =10 mV/fC) and a PMOS transistor operating as a high-value resistor (R_{fb} > 10 MΩ) to slowly discharge the C_{fb1}. The preamplified pulse passes through the Polarity Selection Circuit (PSC) unifying the pulse polarity to support double-sided sensors. The signal is then split into *fast* and *slow* paths. The *fast* path is optimized for timestamping of events and uses a single-stage shaper with 30 ns shaping time, a discriminator and a 14-bit timestamp latch working with Gray-encoded timestamp counter. The slow path consists of a CR-$(RC)^3$ shaper working with a 5-bit flash ADC and a digital peak detector. It is optimized for low-noise charge measurement. The shapers' design is very similar to the implementation in the previous prototype chip, STS-XYTER [3, 4].

To support operation in the MUCH detector regime, the CSA has implemented gain switching by the use of the switchable CSA feedback capacitor C_{fb2} = 500 fF (resulting in k_{q_csa} =1.6 mV/fC). Front-end uses also shaper switchable peaking time t_{p_slow} (90 ns, 150 ns, 180 ns, 280 ns) in the *slow* signal path by means of switchable resistors in all the filter's stages. The ASIC is designed in the UMC 180 nm CMOS process and uses ELT NMOS transistors and guarding techniques [5] for enhanced radiation hardness of analog and digital circuits. It is expected to be taped-out via engineering run in Q1 2016.

Many detector system components (on and off-chip) have an influence on the ROIC analog part performance. Therefore, at the design stage the complex parametrized model of: silicon strip detector, microcable and off-chip circuits (PCB power lines, wire bonds, decoupling capacitors, etc.) have to be used to emulate the detector system real operation. The simulation scheme uses 5 adjacent channels to study their impact on the middle channel performance. It can be expected that the noise performance depends mostly on detector/microcable parameters and their combinations. The ROIC analog part noise is affected not only by the sensor/cable capacitances, but also by their series resistance [6].

2.1 Detector and cable

Different lengths of the silicon strip detectors will be used in the STS (from 2 cm up to 12 cm). The distributed sections of sensor simulation model include parasitic components in the transverse and longitudinal directions [7, 8]. The AC-coupled sensors exhibit important parameters, like strip-bulk capacitance C_{b-p} = 0.19 pF/cm, strip-strip capacitance C_{p-p} = 0.8–1.4 pF/cm, AC coupling capacitance C_{p-m} = 14 pF/cm, biasing resistance R_{bias} = 500 MΩ, diffusion strip resistance R_d = 44–66 kΩ/cm and aluminum readout strip resistance R_s = 12 Ω/cm [9, 10]. Previous studies on the topic [6, 8] revealed that the metal strip resistance is a significant noise source directly affecting the performance of the readout system and needs to be minimized. Changing the sensor's series resistance from 12 Ω/cm to 6 Ω/cm results in approximately 7% noise improvement in a particular case [8]. Therefore it is favorable to reduce the sensor's aluminum strip resistance by thickening the strip. For the new detector design, thicker strips will be used.

Low-mass multilayer custom-designed microcables tab-bonded to the read-out ASIC and detector connect 128 detector channels and detector bias voltage [1]. Three conducting layers (2 signal layers and 1 reference ground layer) are built with aluminum foils on a polyimide film and dielectric spacer material [2]. Several cable lengths will be used in the STS detector (from 20 cm up to 50 cm). The cable affects the noise performance by introducing the additional capacitance and series resistance to the one presented by the sensor itself and therefore can be optimized for low noise with reasonable yield. Currently fabricated cables exhibit 0.95 pF/cm capacitance and 0.472 Ω/cm of series resistance. As a result of the previous studies [8], we have recommended a new design of cable with new spacer material (Fasson Foamtac II) and narrower metal traces which significantly reduces the capacitance introduced by the cable.

As new microcable and detector design based on the recommendations is currently in progress and subject to manufacturability studies, for the purpose of noise evaluation in this paper, a cable with capacitance 0.95 pF/cm, series resistance 0.472 Ω/cm and an end-tapped detector with series resistance R_s = 12 Ω/cm will be used, which is close to the current design parameters while keeping

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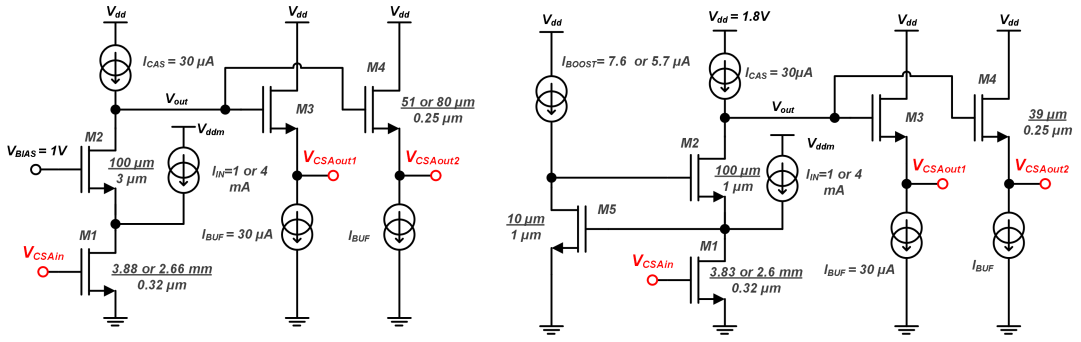

Figure 2. Considered NMOS-based architectures for the CSA core amplifier.

in mind that it can be improved further. As a representative case, an 12 cm sensor attached to 37 cm microcable was used to evaluate the system performance.

2.2 Selection of the CSA core amplifier

Design of the CSA (the processing chain input amplifier) is very important for the performance of the whole system. Selection of the input transistor type, size and biasing conditions (gate capacitance C_{g-g} and transconductance g_m), as well as the CSA core amplifier bandwidth and open-loop gain directly translates to the speed and noise parameters [12].

Literature study [11, 12] is not conclusive in terms of PMOS vs. NMOS selection as the CSA input transistor. The theoretical calculations of the optimum CSA input transistor's gate capacitance C_{g-g} (and therefore the optimal dimensions) lead to the values of few pF (calculated for sensor capacitance within 30 pF–50 pF range). Moreover, complex structure of cable/sensor and presence of non-ideal power supplies, impact of wire-bonds series resistance and inductance, realistic models of external passives make theoretical studies less effective than simulations in the design procedure.

To select the optimal solution for described specific operating conditions, we have evaluated four different CSA core amplifier architectures:

- *NMOS_1* — an NMOS-based, direct cascode amplifier [13] (figure 2a).
- *NMOS_2* — an NMOS-based, direct cascode amplifier with gain-boosting technique (figure 2b).
- *PMOS_1* — a PMOS-based, folded cascode amplifier with cascoded input transistor [4, 14] (figure 3a).
- *PMOS_2* — a PMOS-based, folded cascode with boosting transistor [15] (figure 3b).

Amplifiers use standard, and low V_t PMOS transistors, and standard NMOS transistors constrained to the ELT layout. The transistors are in 1.8 V power supply version. Transistor models are provided by the UMC 180 nm CMOS design kit. Approximate parameters of transistors in 0.18 μm node can be found in the literature [18]. Amplifiers' outputs were buffered with an NMOS source followers biased with 30 μA. Performance of the amplifiers was evaluated for two different CSA input transistor currents (within the considered power budget) I_d = 1 mA and 4 mA.

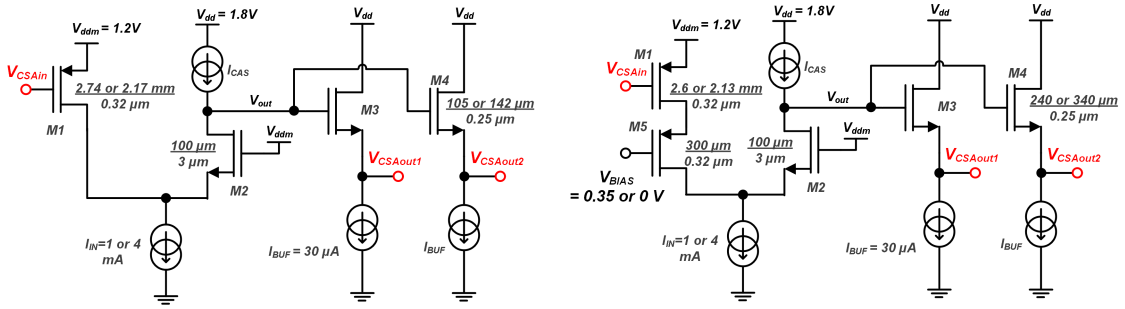

Figure 3. Considered PMOS-based architectures for the CSA core amplifier.

The methodology in selecting the amplifier's architecture was to compare their performance in several steps while keeping their parameters constant: input transistor's gate capacitance C_{gg} = 5 pF, input transistor's drain current I_d = 1 mA or 4 mA, CSA rise time with purely capacitive sensor model C_{det} = 30 pF equals t_{p_CSA} = 40 ns, which resulted in different set of transistor dimensions in every case. To prevent short-channel effects the length of the input transistor was set to 320 nm.

The performance was compared in the following steps, every time narrowing the selection of architecture variants:

- First level selection: select the most promising architectures built with simple models of amplifiers using ideal current sources.
- Second level: add current mirrors and biasing circuit as in the integrated circuit, optimize the mirrors for best performance, compare the performance.
- Third level: post-layout simulation of the selected architecture.

Table 1 shows the comparison of the architectures. In spite of the fact that the gain-boosted versions of the amplifiers exhibit better charge collection efficiency (higher charge gain), the noise performance is better for simple solutions *NMOS_1* and *PMOS_1*. These two architectures were promoted to the second level tests.

Table 2 shows the noise performance of the *PMOS_1* and *NMOS_1* circuits with ideal and real current sources for all selectable slow shaper's peaking times while operating with I_d = 4 mA. The biasing circuits for *NMOS_1* circuit are shown on figure 4, the dimensions are the same for *PMOS_1* version. When using real biasing circuit, *PMOS_1* variant was in this case much worse than *NMOS_1*. The main reason is that the noise from the I_{IN} current source affects the circuits' noise more due to the higher transconductance of the transistor in NMOS-based (g_m = 16.3·10^{-3} Ω^{-1}) current mirror rather than PMOS (g_m = 6.7·10^{-3} Ω^{-1}). Moreover, potential V_{in_csa} is crucial for low noise. If this potential is left unfiltered, noise of all the source transistor contribute significantly to the total noise (see. table 2, cases with and without C_{ext}). Based on the results, *NMOS_1* was selected as the best candidate for implementation, C_{ext}=100 nF will be used since now to decouple the main current source I_{IN}.

A simulation with post-layout model of the CSA with *NMOS_1*-based core amplifier biased with I_d = 4 mA was prepared (see figure 4 for relevant dimensions). The layout of the core

Table 1. First-level comparison for 90 ns and 160 ns slow shaper's peaking times.

Case	t_p (ns)	Id (mA)	$W_{\_in}$ (mm)	GBW (GHz)	Open-loop gain (kV/V)	K_{q_csa} (mV/fC)	K_{q_SHslow} (mV/fC)	ENC (e^- rms)
NMOS_1	**90**	**1**	3.89	8.74	5.116	8.11	33.6	**700**
NMOS_2			3.8	9.7	280	9.57	39.7	**842**
PMOS_1			2.74	7.2	11.180	8.69	35.7	**843**
PMOS_2			2.61	5.5	524	9.5	38.4	**925**
NMOS_1	**160**	**1**	3.89	8.74	5.116	7.85	33	**672**
NMOS_2			3.8	9.7	280	9.57	39.4	**755**
PMOS_1			2.74	7.2	11.180	8.66	35.7	**709**
PMOS_2			2.61	5.5	524	9.4	38.6	**773**
NMOS_1	**90**	**4**	2.66	11.7	5.045	8.15	33.8	**707**
NMOS_2			2.6	11.9	266	9.9	41	**790**
PMOS_1			2.17	10.2	7.547	8.96	35.5	**673**
PMOS_2			2.13	10.6	603	9.34	37.75	**680** ~
NMOS_1	**160**	**4**	2.66	11.7	5.045	8.4	34.75	**647**
NMOS_2			2.6	11.9	266	9.88	41	**717**
PMOS_1			2.17	10.2	7.547	8.63	34.4	**617**
PMOS_2			2.13	10.6	603	9.31	37.8	**620**

Table 2. Second-level comparison with real biasing circuits and I_d = 4 mA.

Architecture & parameters	t_p at slow shaper (ns)	K_q at SHslow (mV/fC)	ENC (e^- rms) Ideal sources	ENC (e^- rms) Real sources no C_{ext}	ENC (e^- rms) Real sources, C_{ext}=100 nF	Noise contributions for T_p=90 ns (%)	
						No C_{ext}:	C_{ext}=100 nF
NMOS_1 I_{in}=4 mA I_{cas}=30 μA k_q=7.73 mV/fC GBW=12.1 GHz Gain: 4150 V/V G_{mM1}=81·10^{-3} Ω^{-1}	89	34	**712**	**816**	**737**	**M1+M2: 38% M_{IIN}: 21.6% MI_{ICAS}: 1.6% Detector: 19% Cable: 17.6%**	**M1+M2: 46% M_{IIN}: 3% MI_{ICAS}: 1.6% Detector: 24% Cable: 22%**
	159	34	**672**	**732**	**683**		
	220	34	**686**	**727**	**696**		
	280	33	**712**	**743**	**720**		
PMOS_1 I_{in}=4 mA I_{cas}=30 μA k_q=8.12 mV/fC GBW=8.7 GHz Gain: 5153 V/V G_{mM1}=52·10^{-3} Ω^{-1}	86	33	**695**	**1034**	**792**	**M1+M2: 21% M_{IIN}: 50% I_{ICAS}: 2.7% Detector: 15% Cable: 11%**	**M1+M2: 35% M_{IIN}: 17% I_{ICAS}: 4.7% Detector: 15% Cable: 19%**
	158	33	**616**	**852**	**684**		
	221.5	33	**619**	**803**	**673**		
	281	32	**640**	**793**	**685**		

Table 3. Post-layout simulations of the selected *NMOS_1* architecture.

T_{p_SHslow} (ns)	K_{q_SHslow} (mV/fC)	ENC (e- rms) A / C_{ext}	ENC (e- rms) A — pure capacitance	ENC (e- rms) B
89	32	1192	1100	772
159	32	971	851	667
220	32	908	752	259
280	32	889	697	673

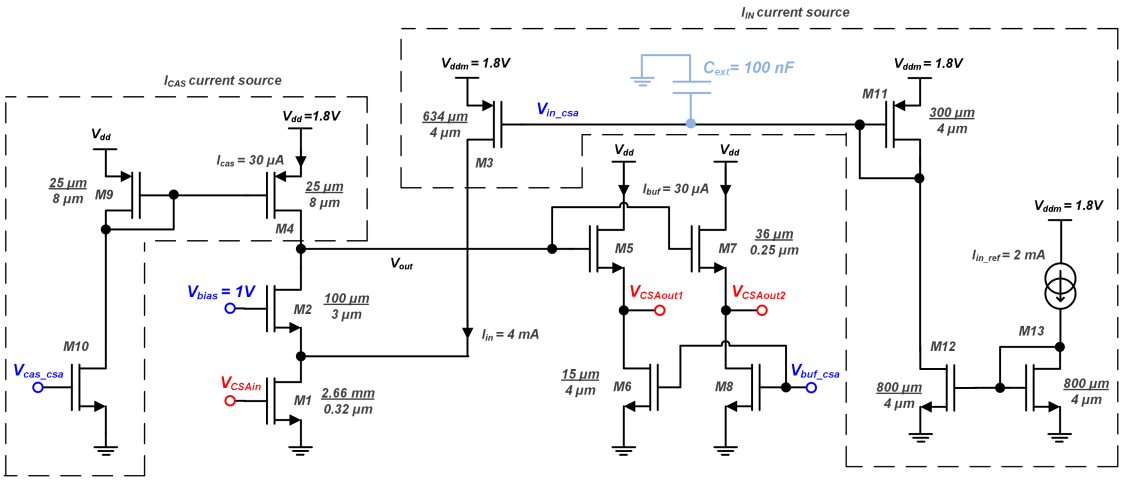

Figure 4. Schematic of the CSA core amplifier selected.

amplifier occupies approximately 58 μm × 180 μm of silicon area and therefore can be fitted into the processing channel of the STS-XYTER2 chip. The noise was evaluated for two variants of detector/cable. Variant A uses parameters of current cable design as before, while variant B uses parameters which are planned to achieve in new design (cable capacitance 0.578 pF/cm, cable series resistance: 1.48 Ω/cm, sensor series resistance: 10 Ω/cm). For reference, simulation results using a single capacitor to emulate the total cable and detector capacitance (47 pF for case A) is included.

3 Summary

This paper presents simulation results of the full analog charge processing chain designed for the CBM Silicon Tracking System and possibly Muon Chamber detector with the emphasis on the selection of the input amplifier's architecture in the presence and expected noise level in the presence of non-ideal detector, cable and power supply. Moreover, the paper summarizes the recommendations towards detector and microcable and presents the CSA core amplifier selection. Presented simulation results show that achieving the STS readout ROIC specification is feasible within the given power and silicon area budget. The analyzed set of cable and detector lengths case is one of the most demanding combination in the designed detector (expected total capacitance ranges between 15 pF–50 pF) therefore it can be expected that in many cases the noise performance

will be significantly better. The real-world effects, like electromagnetic compatibility — related phenomena [16, 17], cross-talks etc. might however degrade the noise measured in the final system. The presented architecture after further fine-tuning will be implemented in the STS-XYTER2 prototype STS/MUCH readout ASIC.

Acknowledgments

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