**A scalable readout system for Silicon PIN arrays**

**based on SKIROC2 ASIC**

Abstract:

A scalable readout system for silicon PIN detectors based on SKIROC2 has been developed, aiming for the pre-design of SiW ECAL prototype used in CEPC. It mainly consists of three kinds of modules: the Front-End Board (FEB), the Data-Interface (DIF) and Data-Acquisition (DAQ). The FEB, which has Application-Specific Integrated Circuit (ASIC) of SKIROC2 and silicon PIN detectors on it, is in charge of receiving detector signals and converting the signals from analog to digital. The DIF is designed to control the FEB and transfer data to DAQ via USB bus or optical fiber. The DAQ gathers data from all DIFs and transmits data to PC through Gigabit Ethernet protocol. The main characteristics of the system will be described. The results of pedestals, calibration and “S-curve” are presented. The measurements with silicon PIN detector S5980 from HAMAMATSU using radioactive source have been carried out and the Signal-to-Noise (S/N) ratio of 59 keV x-ray reached 13.4.

Index Terms: Scalable, Silicon PIN detector, SKIROC2, readout system, FPGA, analog-digital conversion, data-acquisition, Modular electronics.

1. Introduction

The Circular Electron Positron Collider (CEPC) is a next-generation electron-positron collider, which is planned to be built in Qinhuangdao city of China as Higgs and/or Z factory[1]. The main targets of CEPC are producing Higgs boson and making precise measurements of it. The CEPC consists of a vertex detector, silicon trackers and time projection chamber for tracking charged particles, Electromagnetic Calorimeter (ECAL) and hadron calorimeter, a superconducting solenoid with a muon tracker in its return yoke. In order to obtain the supreme energy resolution, the particles inside the jets are separated and each track is assigned to calorimeter cluster one by one. To maximize the particle separation, a kind of high-granularity ECAL is critical. The Silicon-Tungsten-based ECAL (SiW ECAL) is an important option.



**Fig. 0. The cascading relationship of tungsten and silicon PIN slab**

The SiW ECAL is a sampling calorimeter with tungsten absorber and highly segmented readout layers made of pixelised silicon PIN pad sensor arrays. According to the simulation and test results of Calice ECAL physics prototype for ILC [2], the ECAL prototype for CEPC needs dozens layers of silicon PIN arrays and each pad’s size of silicon PIN is about 1 × 1 cm2, which means the total number of electronic channels is tens of thousands. To overcome the challenge, a kind of ASIC, named SKIROC2, with 64 input channels is chosen as the front end chip to read the signal from silicon PIN arrays. In order to test the performance of silicon PIN detector as well as to make a pre-design for the prototype, a scalable readout system based on SKIROC2 ASIC has been developed.

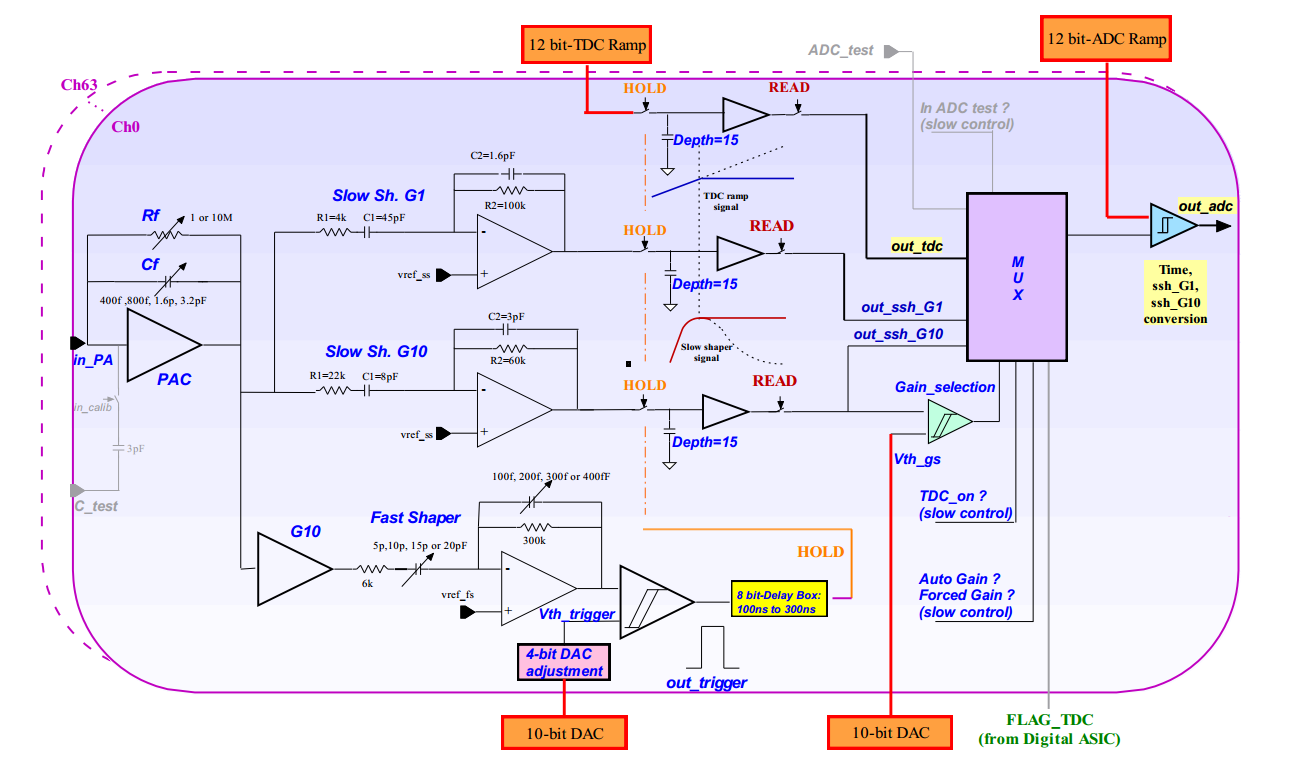


**Fig. 1. The architecture of the readout system**

1. Architecture

The architecture of this system is shown in **Fig. 1.** It’s mainly composed of three kinds of modules, the detector and ASIC module called Front-End-Board (FEB), the data interface module (DIF), the data acquisition module (DAQ). The FEB supplies high voltage to silicon PIN detectors, gets analog signal of detectors to ASIC and transfers data from analog to digital. The DIF controls the ASIC to work and gets data from FEB, packs the data and transfer them to DAQ. The DAQ is in charge of sending commands to DIFs, gathering all data from different DIFs, making necessary compression and transferring data to PC. Under this architecture, a prototype with up to eight layers of detector arrays could be implemented.

* 1. FEB



**Fig. 2. A Schematic diagram of the analog part of SKIROC2**

FEB is based on the ASIC of SKIROC2 (Silicon Kalorimeter Integrated ReadOut Chip 2). SKIROC2 is an ASIC for the International Large Detector (ILD) SiW ECAL [2], which is designed by IN2P3/Omega group in France. The schematic diagram of SKIROC2 is shown in Fig. 2. There are 64 channels on one chip. Each channel is composed of a Charge-Sensitive Amplifier (CSA), two slow shapers with different gains, one fast shaper with a discriminator, a Time-to-Digital Convertor for time measurement, three Switched Capacitor Arrays (SCA) of 15 depth to store analog signal and an ADC to convert analog signal to digital one. The SKIROC2 is available on Ball Grid Array (BGA) package, as well as Quad Flat Package (QFP).

The signal from outside passes through the CSA with variable gain set by feedback capacitance (Cf). The output of CSA is sent to the fast shaper and two slow shapers with different gains. By comparing output of fast shaper with threshold, the discriminator generates trigger signal to hold the voltages at two slow shaper outputs and an additional scanned voltage source for timing measurements to the SCAs. The charges on the SCAs are readout after acquisition by a 12-bit Wilkinson ADC and a multiplexer, with a bunch ID tagged with 10MHz slow clock. The digital data output from ADC are saved in the memory, waiting to be readout.

With the two slow shaper of different gains, the SKIROC2 has a wide acceptable signal strength of 0.5-2500 Minimum Ionizing Particles (MIPs) equivalent charges. The peaking time is tunable between 50 ns and 100 ns.



**Fig. 3. A schematic of connection of silicon PIN S5980**

The FEB accommodates one SKIROC2 chip to read 64 detector signals. The silicon PIN detector S5980 from corporation HAMAMATSU is adopted to be the sensor of the system. This silicon PIN detector of S5980 has an active area of 5 mm × 5 mm and its thickness is 460 um. [3] Its dark current and terminal capacitance suits SKIROC2’s input demand. To get an acceptable counting rate of cosmic ray, the detectors make up an array of 8 × 8, which means the total active area is 1600 mm2. The schematic of detector to ASIC is shown in Fig. 3. The S5980 needs a high-voltage of 13V. Since the output noise is very sensitive with the ripple of high-voltage, it is supplied by a Low-DropOut regulator (LDO) TPS7A4700, whose Power-Supply Ripple Rejection is 82 dB and output noise is 4 uVrms [5], from Texas Instruments company (TI). The capacitor and resistor are used to decouple the high-voltage. The SKIROC2 supplies a reference voltage about 1V, so the anode of the detector directly connects the ASIC.

Since SKIROC2 needs particular power supplies which are regulated by the local LDOs, the initial voltage of 5 V is supplied by connector to DIF, as the same way that the SKIROC2 controlling signals and the output digital data of SKIROC2. There are two kinds of control data buses, fast control and slow control. The fast control is composed of five Low Voltage Differential Signal (LVDS) controlling the clocks and normal operation of SKIROC2. Regarding the fast control signals, the fast clock (FAST-CLK) of 40 MHz is used for sampling signal to SCA and generating hit signal for output. The slow clock (SLOW-CLK) of 10 MHz is used for reading out data saved in SKIROC2’s and generating bunch ID. The reset signal (RAZ) is used for erasing the capacitors of SCA when the chips is triggered by noise. The valid signal (VAL) is used to disable discriminator output signal. The ex-tirgger signal (TRIG-EXT) is used as an external trigger input. The slow control configures a 616-bits registers to store many configurations such as feedback capacitance and various other parameters like trigger mode or calibration mode. If two or more chips are adopted on the FEB, their slow control registers could be configured in a daisy chain cascade. The output port of digital signals are in open collector (OC), which means the same signal between different chips share one data line. Considering the OC gate and daisy chain cascade, it’s very convenient to expand FEB for more detectors and ASICs because there is no need to change the interface definition from FEB to DIF.

* 1. DIF



**Fig. 4. Block diagram and the picture of DIF.**

The DIF block diagram as well as a picture of the DIF are shown in Fig. 4.

The DIF mainly has these parts: FPGA part, connector-to-FEB part, supply part and interface part.



**Fig. 5. Block diagram of logic implemented in the FPGA.**

The FPGA part is composed of a FPGA (ARTIX 7, Xilinx), a flash Programmable Read Only Memory (PROM, N25Q128) as well as a connector in order to program the FPGA via JTAG. The FPGA is clocked with an 80 MHz crystal. The FPGA’s function is to implement the required logic to control FEB and to communicate with DAQ board or directly to PC. The logic diagram is shown in Fig. 5. The Acquisition module controls the ASIC to work in the normal mode and get data saved in the memory of SKIROC2. The data transferred into FPGA will be stored in the First-In-First-Out (FIFO) and then transferred to DAQ or PC. The trigger module is in charge of generating trigger when using calibration mode or ex-trigger mode. Calibration module and S-curve module is used to control the ASIC to be calibrated or tested. These tests will be discussed below. The optical module transmits data from FIFOs to DAQ and gets command from DAQ via optical fiber. The transmission is based on the high-speed transceiver GTP on FPGA. The GTP is responsible for descrambling data, 8B/ 10B encoding and clock recovery. The USB module, however, is used to communicate with PC directly when debugging a single DIF.

The communication with FEB is via two ERNI-154744 connectors [3]. All control signals and reply signals as well as power supply for FEB are through the two connectors.

Interface part is composed of a 1 Gbps bidirectional small form-factor pluggable (SFP) optical transceiver for communication with DAQ and a USB interface realized by a USB chip CY7C68013 and a Mini-USB port for communication with PC when debugging.

Supply part is implemented with a dc input level (5V) from outside and several LDO regulators (TPS74401, TI). From this dc supply rail, digital power supplies (1.0 V, 1.8 V, 2.5 V and 3.3 V) are generated by these LDO regulators for DIF.

* 1. DAQ



**Fig. 6. Picture of DAQ.**

The function of DAQ board is to gather all DIFs’ data from optical fibers and to transmit data to PC server via a gigabit standard Ethernet network cable (RJ45). The current readout system is based on the DAQ of PandaX-III prototype TPC project [5]. The picture of DAQ is shown in Fig. 6. The DAQ contains a FPGA of Zynq-7, a DDR3 RAM of 4 Gbits for data storage, a standard RJ45 port and eight SFP for optical fibers, which means one DAQ can hold eight DIFs. The SFPs are implemented with FPGA-based gigabit serial link to read DIFs’ data and send commands to DIFs. This DAQ has been used in the project of PandaX-III and showed sufficient data bandwidth and stable performance. [6]

1. Measurements

Some measurements were carried out with the readout system in order to determine its performance. Baseline noise, calibration of SKIROC2, trigger efficiency and X-ray test will be introduced below.

* 1. Baseline and noise



**Fig. 6.baseline and noise of all the 64 channels**

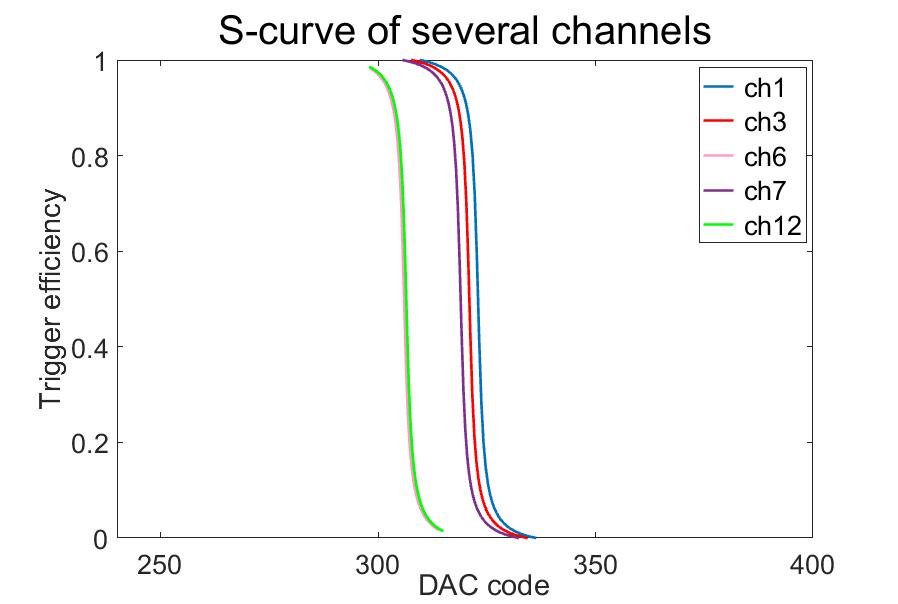
To test the noise level of electronic system, the external trigger of SKIROC2 was used to get the pedestal noise of the system when the detectors were not welded. Concerning the time that SKIROC2 needs for conversion phase and readout phase is 4 ms, the DIF generated triggers at a fixed time interval of 10 ms. Fig. 7 showed the sigma of noise and average of baselines of all the 64 channels. From the graph, not all 64 channels exhibited good baseline and noise results, but most channels’ noises were lower than 0.2 fC equivalent input charge.

* 1. Calibration

**Fig. 7.the linear fit results of two gain modes of SKIROC2**

Due to the SKIROC2 having calibration capacitors of 3 pF on each channel, this testing method was taken: a wave form generator (A.., Tektronix) with attenuator was used to generate step pulses with different amplitudes. When the step pulses were applied to on-chip capacitor, a certain amount of charge, which covered the full range, was injected into every channel of SKIROC2 from test pulse input for performance testing. SKIROC2 had many operation modes by tuning the callback capacitors array. The measurement has been tested with the highest gain mode (with a Cf of 400 fF) and lowest gain mode (with a Cf of 6 pF). The typical linearity curves of output value versus input charge of the two modes were shown in Fig. 7. The figure showed that the linear range of the highest gain mode and the lowest gain mode were 50 fC and 3 pC. The integral nonlinearities (INL) in both modes were better than 0.5%

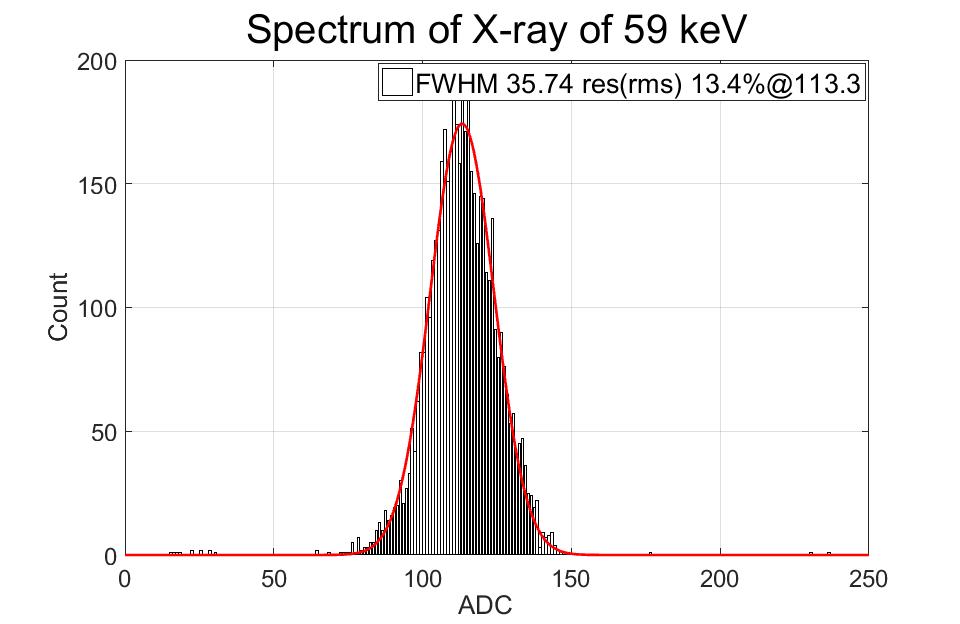
* 1. Trigger efficiency



**Fig. 7.the S-curve of several channels**

Trigger efficiency was obtained via the “S-curve”, shown in Fig. 8. A fixed amount of charge was introduced from the test pulse input. By configuring the probe function, the digital probe outputted the trigger signal if the fast shaper pulse exceeded the threshold. The S-curve was obtained with varying the trigger threshold. The curve was fitted by a complementary error function, whose center value stood for the threshold on the charge, and the sigma stood for the noise power. We obtained the S-curve from 1 fC to 15 fC of several typical channels, which covered 1 and 2 MIP equivalent charges. Since SKIROC2 has the function of “4-bit DAC adjustment” for every channel, the differences of thresholds between channels can be corrected.

* 1. X-ray test



**Fig. 8.the spectrum of X-ray of 241Am**

Measurement with detector of S5980 was carried out with X-ray source of 241Am. In the test, a bias voltage of 15 V was applied as the high voltage of the silicon PIN detectors. The output signals were directly sent into SKIROC2, which was set to work in highest gain mode. In Fig. 8, the spectrum of 59 keV x-ray was shown. According to the results of calibration, the equivalent input charge was 2.89 fC and resolution was 13.4%. The charge of 2.89 fC indicated that the average number of electron-hole pairs was 18109, which meant the average ionization energy of silicon was 3.25 eV. It was lower than the theoretical value of 3.6 eV. Concerning the Fano factor[8], the fact is reasonable.

1. Conclusions

In this paper, a scalable readout system for silicon PIN detectors based on SKIROC2 has been presented. The system, which is aimed to be the pre-design of the prototype of SiW ECAL for CEPC, consists of FEB module, DIF module and DAQ module. The system is scalable because of the modular concept. In addition, the feature of SKIROC2 allows the FEB to carry more detectors and chips without changing the interface to DIF. The main performance of the system are discussed in detail. In the near future, a cosmic ray test system with four layers of detector arrays will be built.

Foundation:

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