A Portable Readout System for Microstrip Silicon Sensors (ALIBAVA)

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***Abstract*—A readout system for microstrip silicon sensors has been developed. This system is able to measure the collected charge in one or two microstrip silicon sensors by reading out all the channels of the sensor(s), up to 256. The system can operate either with non-irradiated and irradiated sensors as well as with n-type and p-type microstrip silicon sensors. Heavily irradiated sensors will be used at the Super Large Hadron Collider, so this system can be used to research the performance of microstrip silicon sensors in conditions as similar as possible to the Super Large Hadron Collider operating conditions. The system has two main parts: a hardware part and a software part. The hardware part acquires the sensor signals either from external trigger inputs, in case of a radioactive source setup is used, or from a synchronised trigger output generated by the system, if a laser setup is used. The software controls the system and processes the data acquired from the sensors in order to store it in an adequate format. The main characteristics of the system will be described. Results of measurements acquired with n-type and p-type non-irradiated detectors using both the laser and the radioactive source setup will be also presented and discussed.**

***Index Terms*—Analog-digital conversion, analog processing circuits, charge collection, charge sensitive amplifier, data acquisition systems, detector instrumentation, digital integrated circuits, electronics, FPGAs, front-end electronics, high energy physics instrumentation, logic design, microprocessors, semiconductor detectors, time to digital converters.**

I. Introduction

THE main properties of highly irradiated microstrip silicon sensors must be studied since a high luminosity is intended to be achieved at SLHC (Super Large Hadron Collider) experiments. Particularly, the charge collected when a charged particle crosses the detector is important for the detector performance. It is difficult to carry out meaningful measurements. First, a custom and expensive laboratory set up is needed. The measurements obtained with different setups could be not comparable if they are not calibrated correctly. Finally, this type of sensors may have hundreds of channels in order to read out. It would be also interesting to test this kind of detectors with an electronic system as similar as possible to those used at the LHC (Large Hadron Collider) experiments, so a front-end readout chip as those used at the LHC experiments should be used. Furthermore, an analogue measurement of the front-end pulse shape is preferred over a binary one for charge collection research.

Therefore, an electronic system which can acquire an analogue measurement has been developed. The system can be used with a laser setup, where a laser light is generated exciting a laser source with a pulsed signal. It can be used also with a radioactive source setup, where the charged particles are generated randomly. The aim is reconstructing the analogue pulse shape at the readout chip front-end with the highest fidelity.

In order to fulfill these requirements the system has specific characteristics. It is compact and portable. It has its own supply system and it contains two Beetle readout chips [1] to acquire the detector signals. It is connected via USB (Universal Serial bus) to a PC host, which stores and processes the data acquired. The user controls the system with the PC software in communication with a FPGA (Field programmable Gate Array) which interprets and executes the orders. The system can be used with two different laboratory setups so it has an external trigger input, from one or two photomultipliers (radioactive source), and it generates a trigger output for pulsing an external excitation source (laser setup).

The hardware is made of a daughter board and a mother board. The daughter board contains two Beetle readout chips as well as the circuitry necessary to connect the Beetle chips with the motherboard. Fan-ins and a detector board are used to interface the sensors. The mother board is intended to process the analogue data that come from the daughter board readout chips, to process the trigger input signal in case of radioactive source setup or to generate a trigger signal if a laser setup is used, to control the whole system and to communicate with the PC software via USB.

The main reason for dividing the hardware into two boards is to preserve the rest of the hardware from the aggressive environment (radiation or very low temperatures) where the detectors work. Analogue data signals coming from the daughter board, control digital signals to the Beetle chips as well as the power supply for the daughter board circuitry run across a twisted flat cable. The detector's high voltage is provided by an external power supply.

The software controls the whole system and processes the data acquired by the sensors in order to store it in an adequate format. This format is compatible with software used for further data analysis, as the ROOT framework. With this software the system can be configured and calibrated. Acquisitions with a laser setup or a radioactive source setup can be carried out as well.

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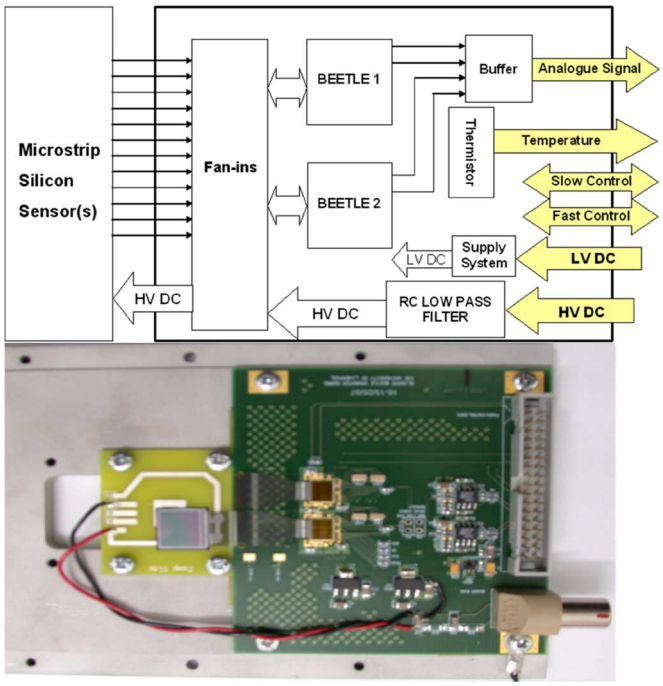

Fig. 1. Daughter board block diagram and the corresponding picture of a daughterboard prototype.

II. Daughter

The daughter board (Fig. 1) accommodates two Beetle chips to read detector signals, a temperature sensor placed close to the chips and the fewest additional components. A 5 V supply level is sent from the mother board. This supply level is regulated by two LDO (Low Drop Out) linear regulators for obtaining the dc supply levels required by the readout chips (2.5 V) and the buffer stage (3.3 V). The detector high voltage power supply is supplied directly to the daughter board. This supply level is decoupled prior to the detector.

The main characteristics and the internal architecture of the Beetle readout chip can be found on [1]. For this system the Beetle chip analogue output or[illegible]is case the analogue front-end pulse signal is sampled into the pipeline with the frequency of the Beetle chip clock (40 MHz). The peak voltage of the front-end pulse signal is proportional to the collected charge at the detector channel, the peak time of this signal is about 25 ns (depending on the load capacitance among other parameters) and the remainder of the peak voltage after 25 ns is below 30% (i.e. the ratio between the signal voltage 25 ns after the peak and the peak voltage). Therefore, a 65–70 ns pulse length is considered in order to reconstruct the pulse. For reading out a particular position of the pipeline, a pulse of 25 ns (TRIGGER) is generated by the mother board. This pulse is sampled with the falling edge of the readout chip clock (CLK). The analogue pipeline latency has been fixed to 128 clock cycles, so this TRIGGER pulse is generated 128 CLK cycles (3.2 μs) after a particular front-end signal point has been sampled and stored in the pipeline.

For the laser setup the TRIGGER pulse is generated for each event (i.e. laser pulse) with a delay programmed by the user regarding the event occurrence. For the radioactiv[illegible] the TRIGGER pulse is generated with a fixed delay regarding the event occurrence (i.e. a particle crossing the detector) and a time stamp for each event is obtained with a TDC in the mother board. Therefore, just one sample of the analogue pipeline is required per event in both setups. The pulse shape can be reconstructed by acquiring enough number of events.

Once the TRIGGER has been activated, the readout of the analogue output on one port data will start synchronously to CLK. A DATAVALID signal will be activated 25 ns before the readout starts and it will be deactivated 50 ns before the readout ends. On this analogue output, 128 data channels are multiplexed. The voltage amplitude corresponds to the particular front-end sample on each input channel. The duration of each header bit or each channel is 25 ns, so the length of each readout frame will be 3.6 μs. The header bits will not be used on this system.

The Beetle chip has two types of control. A fast control composed of five LVDS (Low-Voltage Differential Signalling) signals for normal chip operation and two slow control signals for chip configuration. Regarding the fast control signals, three of them (CLK, TRIGGER and DATAVALID) have been already presented. The RESET signal is used for resetting the Beetle while the TESPULSE signal is used for calibration. The slow control interface is a standard mode I2C (Inter Integrated Circuit Control) slave. The bias settings and various other parameters like the trigger latency or the injected test pulse amplitude can be controlled via I2C.

The analogue output buffer is a current buffer since the Beetle chips analogue output signals are current differential signals. The loop for each signal is closed with a 100 Ω resistor on the daughterboard so the voltage across that resistor is the analogue output voltage. These outputs are buffered at the daughterboard with a differential line driver (AD8130, Analog Devices). Line equalization is not required if the cable is no longer than 10 m [illegible]r, the buffer can provide line equalization by adding two capacitors if cable longer than 10 m is required. The analogue output dynamic range will be linear [illegible] trons ($\pm$17,6 fC) , as could be seen on [5], which is enough for this application where the charge collected seldom exceeds this linear dynamic range. A parallel configuration for the Beetle chips has been considered. There are two different analogue data lines, one for each Beetle chip, but the fast and slow control lines are shared by both chips. Each Beetle chip has its own I2C address.

A mechanical connection system and fan-ins are provided for connecting the detectors. The connection scheme (Fig. 2) consists of three fan-ins, two on the daughter board (chip fan-in and intermediate fan-in) and another on the detector board (detector fan-in). Each fan-in has in-line pads with 80 μm pitch and 10 rows for multiple wire bonding. The purpose is to support detectors with different bonding schemes. The detector(s) are glued to the detector board which is bonded to the daughterboard using the detector fan-in and the intermediate fan-in. Two flavours of detector boards have been designed to accommodate detectors of 1 cm^2 and 3 cm^2.

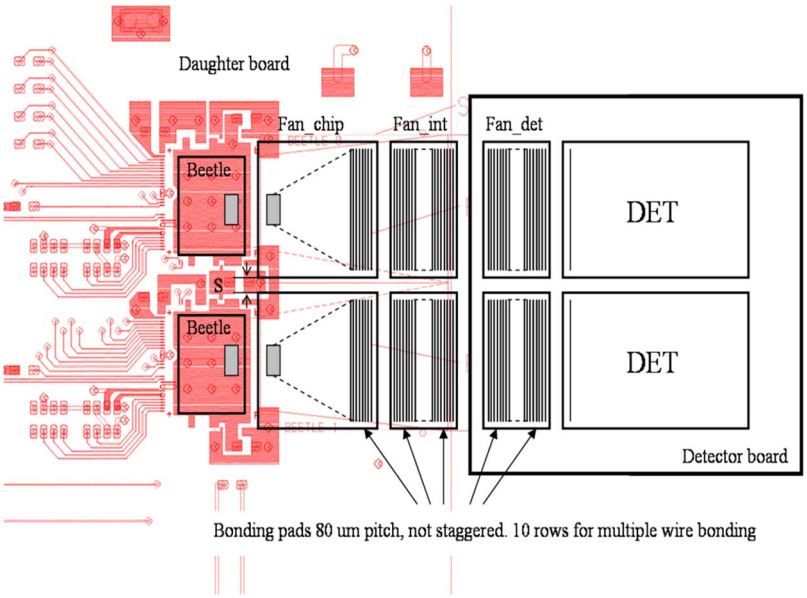

Fig. 2. Diagram of the connection scheme of the detectors to the daughter board including the fan-ins design.

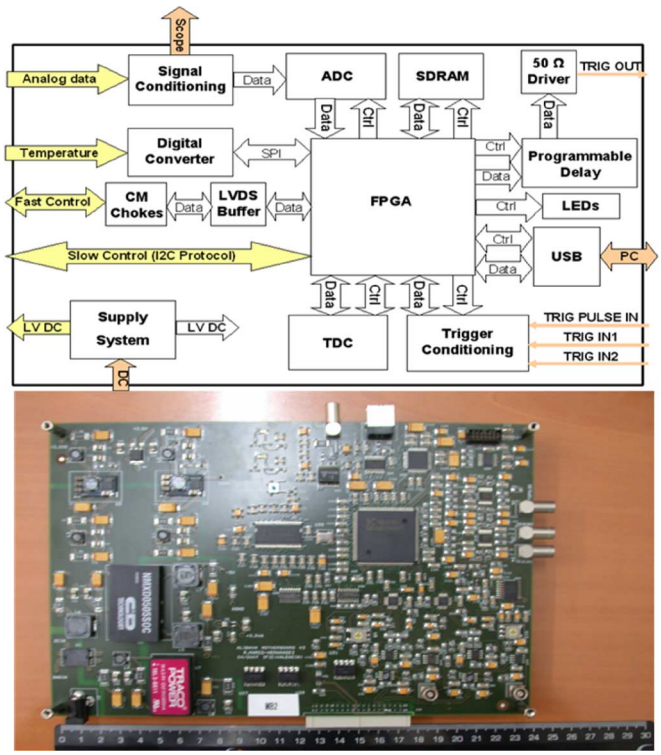

Fig. 3. Motherboard block diagram and the corresponding picture of a motherboard prototype.

III. Mother Board

The mother board block diagram as well as a picture of the motherboard prototype are shown in Fig. 3.

A. Motherboard Hardware

First, a differential to single ended voltage amplifier with unity gain (AD8130, Analog Devices) is used for each input signal. The output signal of each block is split in two signals; one is connected to a unity gain buffer (the scope output) and the other one is connected to a single ended to differential voltage amplifier with unity gain (AD8139, Analog Devices). Each signal can be shifted by three different dc levels (1.65 V, 1.138 V or 2.162 V) depending on the full-scale range desired by means of a three position rotary switch connected to the output references of each ADC. There are two ADC blocks, each one is composed of a differential RC low pass filter for suppressing some of the wideband noise associated with high speed amplifiers and an ADC. The ADC is a 10 bit flash type with a sampling rate of 40 MHz (MAX1448, Maxim IC). The nominal resolution of this ADC is 1 mV and the dynamic range ±512 mV over the dc shifting level chosen.

The thermistor signal coming from the daughterboard is digitized at the digital converter block. The fast con[illegible] buffered with two LVDS repeaters. Also a comm[illegible] suppressor choke have been provided for each signal. There is a SDRAM (Synchronous Dynamic Random Access Memory) of 256 Mbits. The function of this memory is temporally storing the digitized data in each acquisition prior to be read by the software.

外触发功能

In case of the radioactive source setup, a trigger from an external source is used for obtaining a time stamp. This input trigger can come from one or two photomultipliers (TRIG IN1 or TRIG IN2) or can be a positive or negative pulse up to ±5 V, or fast negative NIM (TRIG PULSE IN). From these inputs, the trigger conditioning block generates four signals in LVPECL (Low Voltage Positive Emitter Coupled Logic) indicating if TRIG IN1 or TRIG IN2 is active (with a leading edge discriminator), or if a negative or a positive pulse have been received on TRIG PULSE IN (with two discriminators). The four discriminators are implemented with two dual LVPECL high speed comparators. Four voltage thresholds are needed in this block. These voltage thresholds are programmable by the user via a 12-bit DAC (Digital to Analogue Converter). The TDC (Time to Digital Converter) block is used also with radioactive source

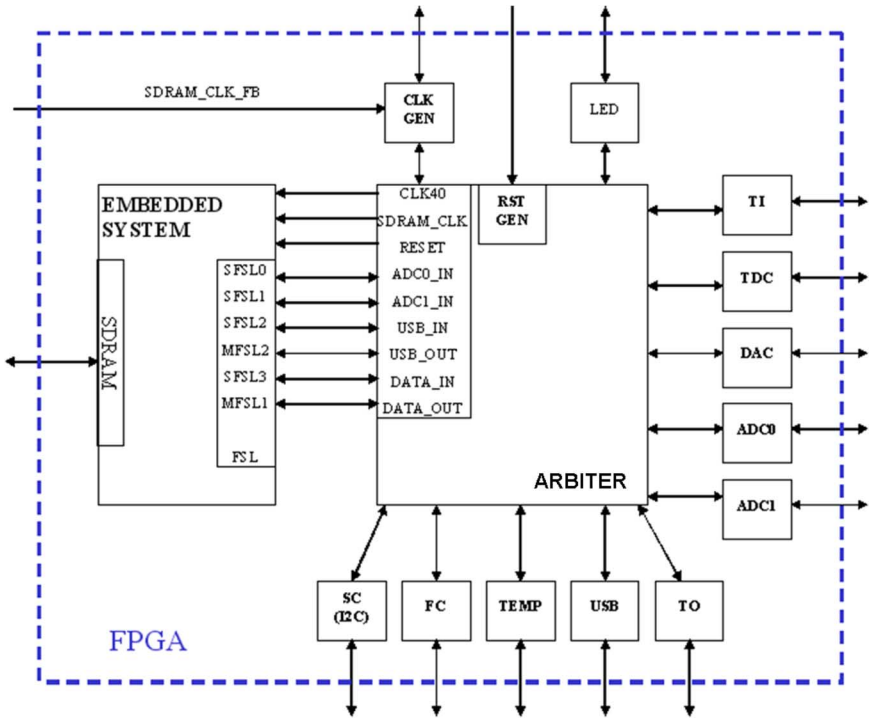

Fig. 4. Block diagram of the logic implemented in the FPGA including the embedded system.

setup. This block is composed only of a TDC integrated circuit with a resolution of 600 ps and a dynamic range of 100 ns.

In case of the laser setup, a synchronised trigger signal (TRIG OUT) is generated to fire a laser source. A programmable delay circuit (3D7428, Data Delay Devices) with a resolution of 1 ns and a dynamic range of 255 ns is used. Following this block a 50 Ω driver has been incorporated for driving a pulse generator input that pulses the laser source. A USB controller (FT245R, FTDI) is used for USB to FIFO (First In First Out) parallel (8 bits) bidirectional data transfer.

The supply system has been implemented on the mother board. A dc input level (5 V) is generated by a portable ac desktop adapter. From this supply rail digital power supplies (1.2 V, 2.5 V and 3.3 V) are generated by means of two DC-DC converters and a LDO regulator. The analogue power supplies (5 V, −5 V and 3.3 V) are generated with a DC-DC converter and a LDO regulator. The daughter board power supply (3.3 V) is generated by a

FPGA部分描述

B. FPGA Logic

The FPGA block is composed of a FPGA (Spartan 3, Xilinx) a flash PROM (Programmable Read Only Memory) as well as a connector in order to program the FPGA via JTAG. The FPGA is clocked with a 40 MHz crystal. The FPGA implements the required logic in order to control the hardware and to communicate with the PC software. The logic (Fig. 4) has been divided in custom logic blocks which manage the different hardware blocks.

The logic includes a 32-bit Microblaze softcore [4] and a SDRAM controller as a peripheral. The interface between the embedded system and the custom logic blocks consists of six FSLs (Fast Simplex Link) and a custom arbiter block. These FSLs are unidirectional FIFOs (First In First Out) integrated in the Microblaze. Four FSLs have been implemented for direct communication with the ADC block and USB block and two FSLs has been implemented for general communication with the rest of the blocks. The arbiter block implements the required logic in order to manage the FSLs and the signal interfaces of the custom logic blocks.

The slow control block includes an I2C bus controller in order to program the Beetle configuration registers. The fast control block generates the LVDS output signals (CLK, RESET, TRIGGER and TESPULSE) for the Beetle fast control. The TESTPULSE is generated from an internal calibration signal. The TRIGGER signal is generated either from an internal TRIG_L signal (in case of laser setup) or from an internal TRIG_R signal (in case of radioactive source setup) taking into account both the Beetle analogue pipeline latency and the particular synchronization delay.

The trigger out block generates external trigger signal that will be delayed with the programmable delay and an internal trigger signal (TRIG_L) for the Beetle fast control block. This block also controls the programmable delay circuit. In this way, by programming a variable delay (up to 6375 ns in 1 ns steps) between TRIG OUT and TRIG_L the system can acquire a desired sampled point of the Beetle front-end analogue pulse.

The trigger in block generates an external and internal trigger signal (TRIG and TRIG IN, respectively) from signals coming from the trigger conditioning block. The coincidence of these signals can be programmed by the user as well as which inputs will be used. The DAC control block deals with the external DAC via SPI (Serial Peripheral Interface).

The TDC block controls the external TDC, which measures the time from the leading edge of a start signal to the leading

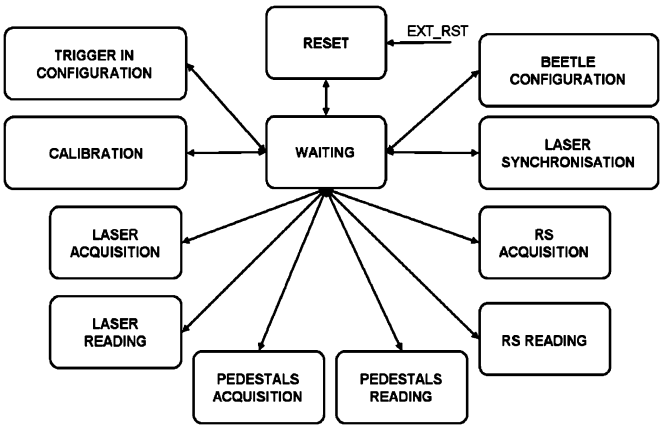

Fig. 5. States of the finite state machine (FSM).

edge of a stop signal. The start signal is generated by the FPGA from the TRIG pulse signal which will be active when a trigger input is detected. The stop signal is also generated by the FPGA from a signal with a period of 100 ns and a pulse width of 25 ns if a start signal has been generated previously. The period of 100 ns is established in order to reconstruct the Beetle chip analogue pulse shape considering a time window of 75 ns. The TDC block also generates a TRIG_R signal, related in time to the stop signal, when the last will be active.

The ADC block reads the digitized data frames when the corresponding DATAVALID signal is active and it stores these frames in an internal FIFO memory. The temperature control block reads the digital conversion of the thermistor signal from the digital converter via SPI. The USB control manages the USB controller in order to communicate with the PC software. The clock generator and reset generator blocks block supply the FPGA internal clock and reset signals.

By using this architecture in the FPGA, the functionality of the system could be easily defined by the embedded processor software. On the other hand, this functionality can be easily redesigned by means of new software without changing the implementation of the FPGA logic. The functionality of the system has been defined by programming a Finite State Machine (FSM) in the embedded processor.

C. Embedded Processor Software

The embedded processor software is included in the FPGA bitstream since its memory size is not very large. Therefore it is stored in the external PROM with the FPGA bitstream. The FSM main state is a waiting state. When FSM is in this state, it waits for an order coming from the PC software by means of the USB control. Depending on the order, the FSM will choose among the rest of states as it is shown in Fig. 5.

When the system is powered on or after an external reset, the FSM goes to the reset state prior to the waiting state. In this state, all the system is initialized. After the FPGA configuration, the system also goes to this state.

In the Beetle configuration state, the configuration registers of the Beetle chips are programmed by slow control. In the calibration state, the system is calibrated by the Beetle internal test pulse generator, i.e. known amplitude readouts are acquired in order to have calibration data. In the trigger in configuration state, the DAC voltage thresholds are programmed as well as the trigger inputs scheme is configured. In the laser synchronization state, the system is synchronized in order to sample a particular point of the Beetle front-end pulse. This point is programmable by the user in 1 ns steps.

In the laser acquisition state, a programmable number of readouts can be acquired with a specific delay between TRIG OUT and TRIG_L. Up to 64776 readouts can be stored in the SDRAM. For each event, a readout of the Beetle chips (256 by 16 bits) and a temperature readout (16 bits) are stored in the SDRAM. The TRIG OUT frequency is fixed to 1 KHz.

In the RS (Radioactive Source) acquisition state, a programmable number of readouts can be acquired from the external trigger inputs by using the TDC. Up to 64776 readouts can be stored in the SDRAM. For each event, a readout of Beetle chips, a TDC readout (32 bits) and a temperature readout are stored in the SDRAM.

In the pedestals acquisition state, up to 64776 readouts can be acquired and stored in the SDRAM. For each event, a readout of the Beetle chips and a temperature readout are stored in the SDRAM. In this type of acquisition, there is no charge acquired with the Beetle chips. The readout is just used to determine the baseline for each input channel of the Beetle chips. In the reading states, the last type of acquisition is read from SDRAM and data are sent to PC software.

讲软件部分

IV. Software

The main task of the system software is controlling the whole system and processing the data acquired from the sensors as well as storing this data with an adequate format in a PC for further processing.

The software has two levels. The low level software deals with the data exchange by USB with the motherboard and with the low level data processing. No driver design is required at this level since the manufacturer of the USB controller provides with a ready-to-use driver (Virtual Com Port Driver). The high level software implements the GUI for the communication between the user and the system, the data monitoring as well as the data output file generation.

The software has been designed initially for running in a Linux operating system. However, a Windows version of the software is envisaged as well. Both the low level software and the high level software have been implemented in the same package and they have been designed using C++. Some macros for the ROOT framework have been developed in order to process the data obtained with the software.

V. Measurements

Some measurements were carried out with a prototype of the system in order to determine its performance. Non-irradiated n-type ($\mathrm{P^{+}N}$) and p-type ($\mathrm{N^{+}P}$) microstrip silicon sensors of 300 μm thickness and 128 channels were used for these measurements. Three types of measurements were carried out at room temperature (i.e. without cooling the detectors): calibration measurements, measurements with a laser system and measurements with a β source. A different daughterboard was used for each type of detector. In each daughterboard used, one

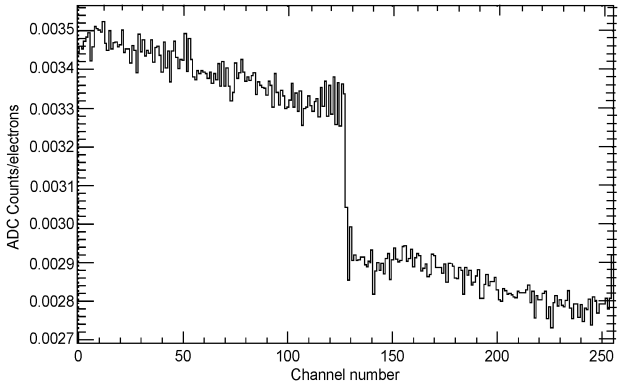

Fig. 6. ADC counts per electron versus channel number for a p-type detector connected to one Beetle chip (channels 128–255).

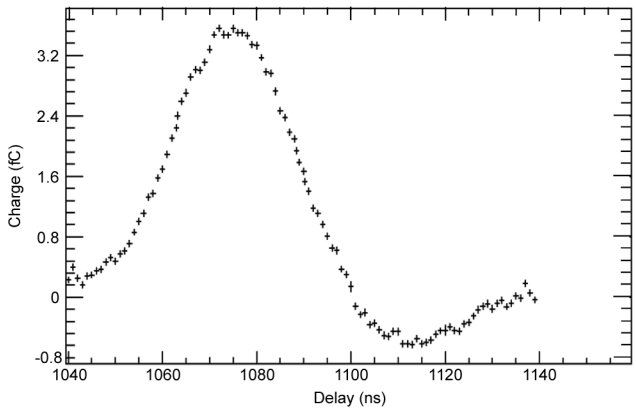

Fig. 7. Laser setup measurements with a non-irradiated n-type detector connected to one Beetle chip (channels 129–256). Pulse reconstruction of the Beetle front-end pulse shape.

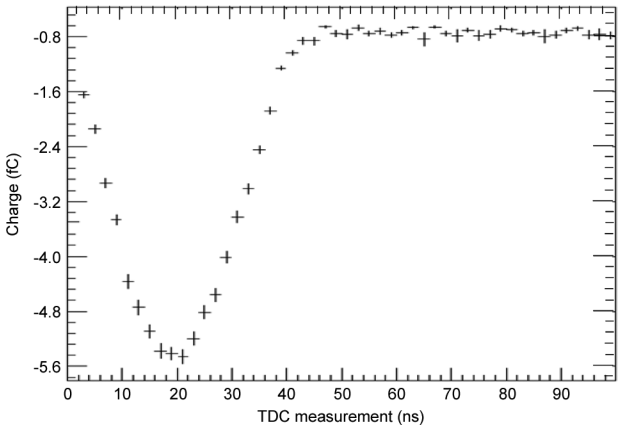

Fig. 8. β source setup measurements with a non-irradiated p-type detector connected to one Beetle chip (channels 129–256). Pulse reconstruction of the Beetle front-end pulse shape.

Beetle chip was connected to the detector (channels 129–256) and the other one was not connected (corresponding to channels 1–128).

First of all, calibration measurements were carried out for both types of sensors. In this case, the acquired data correspond to internal injected charge by each Beetle chip. The amount of injected charge is programmed in the Beetle chips via I2C. However, the input capacitance in the input channels of the Beetle chip with the detector connected is higher and it has influence on the measurements.

The ADC counts per electron versus the channel number are shown in Fig. 6 for all channels with a p-type detector connected (channels 129–256). These data are used to calculate the equivalent signal amplitude in electrons from the signal amplitude in ADC counts. A full depletion voltage of -100 V was applied to the detector. The different conversion factors are due to the capacitive loading of the second 128 channels by the strips. The plot shows that the conversion factor does not change in a significant way for the Beetle chip connected to the detector, which was the expected behaviour.

Measurements with the laser setup were carried out with both detectors types at a wavelength of 1060 nm. The laser is placed over the detectors. In the case of the non-irradiated n-type detector, a full depletion voltage of 200 V was applied to the detector. A laser scan was carried out with the system with a programmed delay range of 100 ns (from a delay of 1040 ns to a delay of 1140 ns) in 1 ns steps and 100 samples per step were acquired. This delay is found experimentally once the laser beam has been focused on the detector by trying different delay ranges with larger delay steps. Once the signal is found, the delay range as well as the delay step can be constrained in order to reconstruct the Beetle front-end analogue pulse shape generated by the detector signal from the laser light pulse. In Fig. 7, the collected charge in fC versus the delay in ns is represented. It can be seen that the analogue Beetle front-end pulse has been reconstructed with a peaking time about 25 ns and the subsequently undershoot. Since the detector is a n-type detector the pulse is positive (i.e. holes are collected in the detector).

Finally, measurements with a low activity $^{90}Sr\beta$ source were acquired with both detectors. As a trigger input for this measurement, the output signal from one photomultiplier placed under the detector and the radioactive source was used. This signal was connected to the motherboard TRIG IN1 input and discriminated with a -40 mV threshold level.

In the case of the non-irradiated p-type detector, a bias voltage of -100 V was applied. A number of 20000 samples were acquired for this measurement. In Fig. 8, the reconstruction of the Beetle analogue front-end pulse shape is shown. The averaged collected charge in fC versus the TDC measurement in ns is plotted. It can be seen a peaking time of 25 ns corresponding with the expected value. The pulse is negative since electrons are collected with the p-type detector (negative current pulse). In Fig. 9, the signal spectrum for the Beetle chip connected to the detector is shown. It represents the number of events versus the collected charge in fC. The sigma of the curve fitting in the plot (0.191 fC) represents the noise corresponding to each Beetle chip (i.e. detector noise, Beetle chip noise and electronics noise). This noise is consistent with the expected noise of the Beetle chip including the capacitive load (i.e. about 800 electrons).

In Fig. 10, the spectrum signal (number of events vs. $|\mathrm{charge}|$ in fC) is shown with a time cut between 12 ns and 22 ns. This time cut includes the events acquired with TDC measurements between 12 ns and 22 ns. These events correspond to the peak of the pulse shape reconstructed (Fig. 8). It can be seen that the

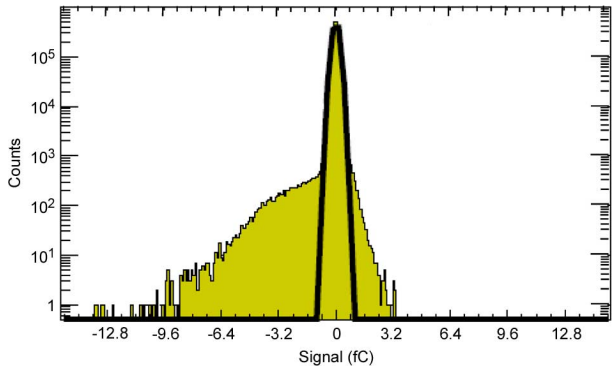

Fig. 9. β source setup measurements with a non-irradiated p-type detector connected to one Beetle chip (channels 129–256). Spectrum of the signal.

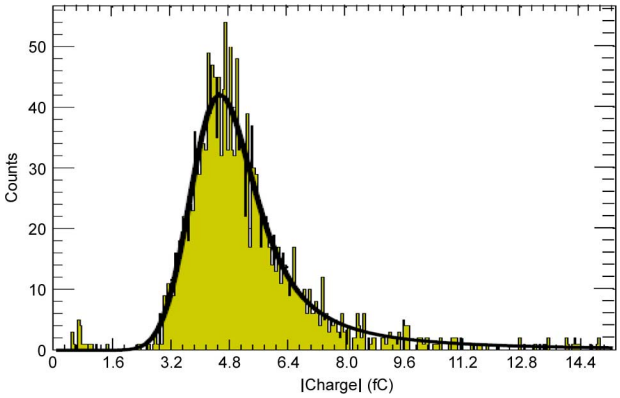

Fig. 10. β source setup measurements with a non-irradiated p-type detector connected to one Beetle chip (channels 129–256). Spectrum of the signal with a time cut (12–22 ns).

spectrum fits a distribution similar to the Landau distribution [5] with a long tail for greater collected charges. This was the result expected for this type of measurement since it would be directly related to the energy loss in the silicon detector with a thickness of 300 μm. The peak of this distribution at 4.316 fC corresponds to the mpv charge of a mip (minimum ionizing particle). Comparing this to the noise of 0.191 fC from Fig. 9, it yields a SNR of 22. For a non-irradiated p-type detector the SNR calculation is the same.

VI. Conclusions

The design of a readout system for microstrip silicon sensors has been reported. This system has been developed in the framework of the ALIBAVA collaboration (University of Liverpool, CNM of Barcelona and IFIC of Valencia) which is integrated in the RD50 collaboration. The system can operate with different types (p-type and n-type) and different sizes (up to 3 cm^2) of microstrip silicon sensors. The system has up to 256 input channels and it has been designed to operate with both irradiated and non-irradiated sensors. The hardware and software used in order to design the system are generally applicable to microstrip silicon sensors. The key numbers of the system are summarized in Table I.

Two different laboratory setups (laser setup or radioactive source setup) can be used with the system, which is useful for comparing results with the same detector. The system has been tested with these two laboratory setups and works correctly. For non-irradiated detectors the SNR with a β source is 22. For irradiated detectors the noise will increase, although there is room for this noise increase in order to have a reasonable SNR. With the laser setup, the signal is much larger, so there is no concern about the SNR.

It is envisaged to distribute the system among different research groups of the RD50 collaboration which are interested in using it for their research lines. Other research groups not integrated in the RD50 collaboration but involved in silicon detectors research have also shown interest in the system.

The next step is to accomplish measurements with irradiated microstrip silicon detectors. The SNR in irradiated detectors is lower since the noise increases because of the radiation effects and the collected charge is reduced. However, the measurements can be acquired with the detectors cooled (i.e. the daughterboard). Decreasing the detectors temperature will minimize the noise in the system. On the other hand, the radiation effects on the collected charge can be partially counteracted by increasing the depletion voltage of the detector. Therefore, it is expected that the system will operate correctly with irradiated detectors taking into account the SNR obtained for non-irradiated detectors. Moreover, preliminary results of measurements acquired with the system for irradiated detectors have shown that the gain of the Beetle front-end increases at low temperatures so the SNR do not diminishes despite the noise increase. However, a calibration at room temperature is required.

TABLE I
Key Numbers of the System

Characteristic	Value	Comments
Number of Beetle chips	2	Per daughterboard
Number of input channels	256	128 per Beetle chip
Beetle chip clock rate	40 MHz	
Beetle output type	Analogue	
Beetle output ports used	1 of 4	Per chip
Slow control format	I2C	Configuration of the Beetle chip
Fast control format	LVDS	Operation of the Beetle chip
ADC sampling rate	40 Msps	ADC active just during Beetle readout (3.6 µs)
ADC resolution	10 bits	
Number of trigger inputs	3	
Trigger inputs format	50 Ω	Range up to ± 5V
Rate of input triggers	200 kHz	Limited by TDC calculation time (5 µs) and Beetle readout (3.6 µs)
Number of trigger outputs	1	
Trigger output format	3.3 V LVCMOS	50 Ω output
Trigger output rate	1 kHz	Limited just by Beetle readout (3.6 µs)
SDRAM capacity	256 Mb	
USB type	USB 2.0	Full speed (480 Mb/s)
Noise of the system	700-1200 electrons	Non-irradiated detector

The ALIBAVA collaboration has already envisaged a system upgrade in order to use various systems synchronized in a testbeam. This would required design changes both in the hardware and the software in order to synchronize the data acquisition of various systems to a common clock and trigger signal as it is usual in a testbeam. Moreover, the data acquired by various synchronized systems will be able to be collected by means of a software package running in only one PC. This fact will require hardware and software changes in order to send the acquired data from slave systems to a master system. The master system would send all the collected data to the PC by USB communication.

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