Response to the reviewers

(TNS-00233-2014)

Reviewer1:

General recommendations:
- I suggest to write carefully the key paragraphs of this paper.
- I would avoid contractions (e.g. doesn't) in formal paper.
- Check the many English typos (e.g. Mutiple->Multiple)
- Explain the acronyms the first time they appear in the paper

Response to the general recommendations:

Some paragraphs of this paper have been rewritten and the. The contractions and English typos in the paper have been modified and explanations to acronyms have been added the first time they appear in the paper. All modifications in the paper are highlighted and the specific modifications are list below.

0-MI: I'd write the meaning of the acronym FPGA the first time it appears in the text.

Answer:

"Field-Programmable Gate Array (FPGA)" has been added in the paper (first page line 8 and first page line43).

1-MA (line 19), the reference nr.3 should be changed. The reference refers to the sentence "The BGO calorimeter is in charge of observation of high energy electrons/positrons and gamma rays(3)".
In Ref. (3) it is discussed the requirements for the PMT which will be used in DAMPE and a BGO fluorescence simulator and its linearity of the PMT.

I would suggest to find a different paper to refer to.

Answer:

The reference has been changed to *"[3] Jin C. Dark Matter Particle Explorer: The First Chinese Cosmic Ray and Hard γ-ray Detector in Space[J]. 空间科学学报, 2014, 34(5): 550-557."* (fifth page right column line 86).

2-OP If the pictures are taken from different papers/data sheets, I would refer to them in the captions.

Answer:

Fig. 2 is taken from *"ProASIC A, FPGA E P. Features and Advantages http://www. actel. com/documents[J]. PA3_E_Tech_WP. Pdf"* and the reference has been added to the caption of the figure (first page line 56).

3-MI (right column. line 56): "Therefore the configuration unit is insensitive to SEE"
It is the first time you refer to "SEE" without explaining the acronym.

Answer:

"Single Event Effect (SEE)" has been added in the paper (second page line 6).

4-MI (left column, line 4) ".. shows that the SEU LET value for DFF is less than 3 MeV·cm2/mg". Does this threshold refer to Altera devices or ProASIC?
In reference (5) the value for upset in FF for the ProASIC is < 10 MeV·cm2/mg.

Answer:

The threshold refers to ProASIC. The abstract of the reference paper said that LET threshold of SEU for ProASIC is below 10 MeV·cm2/mg. However, the main body of the paper showed that the SEU threshold for ProASIC is less than 3 MeV·cm2/mg (TABLE III and Fig. 7). I think both of these two values are correct but the value of 3 MeV·cm2/mg is more precise, so I use it in my paper.

5-MI (left column, line 16 to 22). I would try to reformulate this paragraph. In fig.4 I would add where the trigger comes. Is it handled by the "scientific data acquisition part".

Answer:

The paragraph has been reformulated (second page line 69 to line 77) and the Fig. 4 has been modified (second page line 78). The reformulated paragraph is as follows:
"When a command comes from the controlling computer, the control part begins to handle it. And when a trigger signal comes from the trigger board, it is handled by the scientific data acquisition part. There are many steps in both the command handling procedure and the scientific data acquisition handling procedure. When a command handling procedure or a scientific data acquisition procedure is finished, the part of the logic is under reset state until next command or trigger signal arrives."

6-OP (left column, line 54-54): what if a power cycle is needed? Did you consider such case?
Can you argument such case?

Answer:

I think the power cycle can solve the problem too, but it three are some difficulties in realizing it. The FEE Board is connected with the signal from the detector, which is supplied with high pressure voltage. The high pressure voltage must be cut off before the FEE board powering off to protect the FEE board. However, the many times of high pressure voltage powering on the off to the detector may damage it. So power cycle cannot be used in FEE board.

7-MA (left column, line24) In the sentence: "..If the data acquisition process doesn't finish in a certain time because of SEU or something else.." What do you mean for "something else"? This is a vague statement.
What to you mean for a "certain time"? When does an acquisition stop?

Answer:

I have explain “something else” in detail in paper (third page line 88 to forth page line 4) and it states as follows:
“In the FPGA logic, each procedure is implemented by a Finite-state machine (FSM). The FSM controls the peripheral devices and needs the feedback signals from peripheral devices for state transformation. In space, SEU happening in the FSM or loss of peripheral device signals may lead the control part or the scientific data acquisition part into an infinite loop status at which the system cannot work properly and needs to be reset.”
I have specified the acquisition time in the paper (forth page line 22 to line 25), and it states as follows:
“If the data acquisition process does not finish in 1ms which is about 1.5 times as long as the time of a normal scientific data acquisition procedure, the sci_path_rstn becomes active and resets the scientific data acquisition part automatically.”

8-MA (left column, line 33) In the sentence: ".. the reset signals are active and set the two parts into sleep.."
What do you mean for sleep? What is the difference between "sleep" and idle state?

Answer:

By “sleep” I wanted to express that this part of logic was reset by reset signal and by “idle state” I wanted to express that this part of logic did not need to work at some time. To avoid misleading, I have replaced the word “sleep” by “reset state” (second page line 76 and third page line 33).

9-MI (left column, line 12) "..there’re" -> there are

Answer:

All contractions in the paper have been changed.

10-MA (left column, line 12) ".. key registers and RAMs". Can you specify what they are and why the have to be "valid" all the time?

Answer:

I have specified the reason in the paper (second page line 63 to line 68), and it states as follows:
“In the status part, there are some key registers and RAMs which are used to set the operating status of the system. Other parts get operating settings from the status part. The monitor part provides some parameters describing the operating status for real-time monitoring.”

11-OP (left column): in the sentence "to avoid that Multiple Bit Upset (MBU) ... different physical areas" Is it proven that the placement of component in different physical areas reduces the MBU? If yes can you add the reference to other works?

Answer:

The placement of components in different physical areas cannot reduces the MBU. But by putting three replicas of one register in different physical areas, the probability that MBU happens one TMR structure can be reduced.

12-MA Fig.7, I would write in the caption or/and in the text what is shown in the pictures. (e.g. beam line, target...) and add the beam characteristics (energy, intensity, beam spot....).

Answer:

The caption of Fig. 7 has been rewritten as follows (forth page line 9 to line 13):
*“Fig. 7 SEU Test Site. The test is performed at HIRFL-TR5 terminal, using Krypton ions. Irradiations were conducted in air, at ambient room temperature, with heavy ions passing through a vacuum/air transition foil. The LET values of the ions could be adjusted from 22.7 to 39.9 MeV*cm2/mg.”*
Besides, the caption of Fig .1 (first page line 23), Fig. 2 (first page line 56), Fig. 3 (second page line 23), Fig. 4 (second page line 80), Fig. 5 (third page line 9) and Fig. 8 (forth page line 72) are modified.

13-MI (line 21) what is the meaning of the acronym DUT?

Answer:

“device under test (DUT)” has been added to the paper (forth page line 17).

14-MI (line 28) I would reformulate the sentence: "the DUT... function well." What is the meaning of "functioning well"?

Answer:

By “functioning well”, I wanted to expressed that the host computer and the Master Board are not influenced by the radiation environment. The statement has been modified as follows (forth page line 24 to line 26):
“With the architecture of host PC-Master Board-DUT Board, the host-PC and Master Board can work without the influence of radiation.”

15-MI (line 37) "APA600" it is used the first time, can you specify what "600" refers to?

Answer:

It means this kind of chip has 600000 system gates. The explanation has been added to the paper (first page line 50) as follows:
“APA300 (APA300) which has 300000 system gates and ProASIC Plus APA600 (APA600) which has 600000 system gates are chosen as the BGO FEE controlling chips.”

16-OP (line 38) For completeness you should write why the "package lid" is removed during the experiment.

Answer:

The reason has been added to the paper (forth page line 35) as follows:
“Because the Bismuth ions cannot go through the package lid of the APA600 chip, the package lid is removed.”

17-MA Sentence: "During this time, the supply current of FPGA is monitored and no abnormal current is found". This is an important point in the experiment. *What currents* have been monitored? What is the precision of the amperometer used and the values of the currents?

Answer:

The explanation has been added to paper (forth page line 37 to line 40) as follows:
"The current of logic array power supply and I/O pad power supply of FPGA can be monitored by a monitor circuit on the Master Board which has the precision of 0.1mA."

18-MI (line 48-49), I suggest to check English language.

Answer:

The sentence has been rewritten as follows (third page line 48):
"which means the structure of flash switch in APA is immune to SEU and the configuration information in APA will not be changed when it works in space."

19-OP (left column, Paragraph 40-50). At the end of the paragraph you reach the conclusion
that the APA is immune to SEU in space environment. This agrees with ref.(5)
where similar conditions are considered. In your case the board will be
exposed in radiation in space for 3 years.
In addition, can you say something about the accumulated dose and its effects on the APA?

Answer:

Total ionizing dose (TID) test for the front end electronics (FEE) board with APA600 was conducted at National Institute of Metrology, China and University of Science and Technology of China (USTC). A ^{60}Co gamma source was used as in the TDI test. The whole FEE board was irradiated up to 10Krad (Si) with a dose rate of 2.61rad/s at the room temperature. Accelerated ageing with power-on at 100℃ for 60 hours was done after irradiation exposure. The experiment results showed that no evident degradation of FPGA was found. All function of FPGA worked well during the

experiment. The supply current of FPGA was monitored and no abnormal value was found. After the experiment, the APA600 chip could be reconfigured with new logic, which meant the configuration part of the chip was not damaged either.
The information of the TID test and the results are stated as above. However, I think this part are not relevant to study of this paper, so I have not added them to the paper.

20-MI (line 54): "lite version": what does it mean? You could add the percentage of the logic used and give some quantitative numbers.
You are using APA300 for the first time. Same comment as before for APA600.

Answer:

The part talking about the “lite version” has been added to the paper (forth page line 55 to line 60) as follows:
“Because on DUT Board there are no peripheral devices which participate in data acquisition and other function on FEE, the logic parts communicating with these devices are removed and the science data package is simply filled by “55AA”. With these changes, the resource consumption is reduced by about 10%.”
The instruction for APA300 has been added to paper (first page line 50) as follow:
“APA300 (APA300) which has 300000 system gates and ProASIC Plus APA600 (APA600) which has 600000 system gates are chosen as the BGO FEE controlling chips.”

21-MI (line 56) Be consistent with symbols (MeV*cm2/mg or MeVcm2/mg)

Answer:

The symbols has been unified and modified in the paper (second page line4, second page line 13, forth page line 13, forth page line 32, forth page line 62, fifth page line 42).

22-MA (line 29-37, paragraph A). I would be more descriptive in the model used. Also the figure

can be explained in better details:
How the "system's reliability" is defined?
What are the parameter in the figure?
To which "correction" do you refer?

Answer:

"system reliability" is defined as the probability that all registers in the system are correct. λ, which represents the rate that the value in a DFF transitions from correctness to error per unit time is assumed to be 10^{-7} $hour^{-1}$. μ, which represents the repair rate per unit time is assumed to be 1 $hour^{-1}$ in the architecture of TMR DFF. By "correction", I wanted to refer to the write-back line in the TMR structure. This part has been rewritten in the paper (forth page line 70 to fifth page line 39) as follows:

"Using Markov model in fault-tolerant computing, a system's reliability can be predicted [10]. According to the study of McMurtrey D, if defining reliability as the probability that the value in a single DFF register is still correct after a certain time, then

$$R_{DFF1}(t) = e^{(-\lambda t)} \quad (1)$$

Where λ *represents the rate that the value in a DFF transitions from correctness to error per unit time and t represents time.*

Concerning structure with TMR DFF, then

$$R_{DFF2}(t) = \frac{(\mu+5\lambda)\sinh\left(\frac{1}{2}t\sqrt{\mu^2+10\lambda\mu+\lambda^2}\right)e^{-\frac{1}{2}(\mu+5\lambda)t}}{\sqrt{\mu^2+10\lambda\mu+\lambda^2}} + \cosh\left(\frac{1}{2}t\sqrt{\mu^2+10\lambda\mu+\lambda^2}\right)e^{-\frac{1}{2}(\mu+5\lambda)t} \quad (2)$$

Where λ *represents the rate that the value in a DFF transitions from correctness to error per unit time,* μ *represents the repair rate per unit time and t represents time.*

Concerning there are 3000 key registers in the FPGA logic, if defining system reliability as the probability that all registers in the system are correct, then

$$R_{system}(t) = R_{DFF}{}^{3000} \quad (3)$$

As CREME96 predicts that the SEU probability for the APA chip is about 6.8×10^{-7} $bit^{-1}\cdot day^{-1}$ *at the altitude of 500km [6], [7], [8],* λ *is assumed to be* 10^{-7} $hour^{-1}$. *And because there is write-back line in the structure of TMR in the design,* μ *is very much closed to 1. Combining these two parameters with equations 1, 2 and 3, the system reliability changing with time can be derived and the results are shown in Fig. 8. Compared with the one of system without TMR, the reliability of system with TMR almost does not change with time and is still very close to 1 after 30000 hours.*

Therefore, the structure of TMR with write-back line can highly improve the reliability of a system.

Using the system reliability, Mean Time Between Failure (MTBF) of the system can be calculated. As shown in equation 4 and 5, the MTBF of the system can be improved by 10^6 times if using the structure of TMR with write-back line.

$$MTBF_{Without\ TMR} = \frac{\int_0^{\infty} \frac{d(1-R_{DFF1}{}^{3000})}{dt} * t dt}{\int_0^{\infty} \frac{d(1-R_{DFF1}{}^{3000}{}_1)}{dt} dt} := 3000 hours \quad (4)$$

$$MTBF_{With\ TMR} = \frac{\int_0^{\infty} \frac{d(1-R_{DFF2}{}^{3000})}{dt} * t dt}{\int_0^{\infty} \frac{d(1-R_{DFF2}{}^{3000})}{dt} dt} := 10^9 hours \quad (5)$$

"

23-MI (line 40, right). This is repetition. Please correct the typo (attitude->altitude)

Answer:

The typo has been corrected (fifth page line 42).

24-OP (line 43, right) The number quoted are very old (1997), is there any recent simulation supporting these numbers?

Answer:

Actually, I use the data on https://creme.isde.vanderbilt.edu, data of which is updated recently. If publishing results use the data produced by this site, the paper published in 1997 must be referenced as required. Besides, two more articles have been referenced in my paper (page fifth line 97 to sixth page line 2) as follows:

"R.A. Weller, M. H. Mendenhall, R. A.Reed, R. D. Schrimpf, K. M. Warren, B. D. Sierawski, and L. W. Massengill, "Monte carlo simulation of single event effects," IEEE Trans. Nucl. Sci., vol. 57, no. 4, pp. 1726-1746, Aug. 2010.

Marcus H. Mendenhall and Robert A. Weller, "A probability-conserving cross-section biasing mechanism for variance reduction in Monte Carlo particle transport calculations", Nucl. Inst. & Meth. A, Volume 667, 1 March 2012, Pages 38-43,

doi:10.1016/j.nima.2011.11.084.”

25-OP (line 1-10): You refer to "requirement of the design". Can you give some numbers?
What is "required"? What are the limits which the design should respect in terms of frequency, power consumption etc..?

Answer:

For logic tile usage, it must guarantee that the Place&Route can be finished. For highest work frequency, it must be higher than the work frequency. And for the power, it won’t cause a problem as long as it does not increase too much. The statements have been added to the paper (fifth page line 60 to line 67) as follows:
“From the table we can see that due to the SEU mitigation design, the logic tile increases from 57.1% to 77.0% which is still very low and the Place&Route can be finished by computer automatically without any problems. The highest work frequency declines to 33.2 MHz which still has margin of more than 50% compared to the work frequency of 20MHz.”