Response to the reviewers

(TNS-00233-2014)

Reviewer3:

1. English: there are a few English language problems in the paper, please consider revisions and polish. The following are some obvious ones.

Answer:

Some English language problems have been revised and highlighted in the paper. The obvious ones are listed below.
Page 1, column 2:
line 16: is one main "concern" ...
Revised. First page line 38.

line 21: "And on each of the FEE board", please remove "And"
Revised. First page line 43.

line 25: engineering "parameters" …
Revised. First page line 48.

line 47: "And it uses a live…", please remove "And"
Revised. First page line 61

Page 2, column 1
line 34: The TMR technique "improves" the reliability …, but it "causes" some problems …
Revised. Second page line 35

line 37: "difficulty" in placing and routing and so on.
Revised. Second page line 38.

Page 2, column 2
line 17: two very long sentences should be rewritten for better explanation.
Revised. Second page line 69 to line 77.

line 24: next command or trigger signal "arrives".

Revised. Second page line 77.

line 50: can't work normally and "needs" to be reset.
Revised. Third page line 3.

Page 3, column 1
line 16: from "an external" reset chip.
Revised. Third page line 15.

line 17: to their default "value"…
Revised. Third page line 16.

line 19: RAMS "except" a shift …
Revised. Third page line 18.

line 25: sci_path_rstn "becomes active" and resets…
Revised. Third page line 26.

line 28: present the system "from" entering infinite…
Revised. Third page line 29.

Page 3, column 2
line 36: the data in RAMs are so many, they can't be monitored in real-time
Revised. Third page line 68.

line 39; The CRC result is calculated "first" and attached at the …
Revised. Third page line 73.

line 45: engineering parameter and used as a call …, remove "is"
Revised. Forth page line 1.

line 52: to evaluate the SEU tolerance, remove "to"
Revised. Forth page line 6.

Page 4, column 1
line 28: system "is functioning" well…
Revised. Forth page line 24 to line 26.

line 36: 90 MeV*cm^2/mg…
Revised. Forth page line 32.

line 37: which is much higher than what chip will be exposed in space.
Revised. Forth page line 33.

line 46: no configuration "corruption" is observed.
Revised. Forth page line 47.

line 48: APA won't be "changed"…
Revised. Forth page line 49.

line 58: works "without errors".
Revised. Forth page line 64.

Page 4, column 2
line 30: can be "predicted".
Revised. Forth page line 78.

line 50: has the SEU tolerance…, remove "ability of"
Revised. Fifth page line 50.

line 53: have efficiently "reduced" the …
Revised. Fifth page line 53.

line 58: Table I shows "the" comparison of the …
Revised. Fifth page line 58.

Page 4, column 1
line 6: 33.2 MHz which "still" meets the requirements…
Revised. Fifth page line 66.

line 24: The last sentence should be rewritten for better explanation.
Revised. Fifth page line 69.

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2. Some captions of figures should be rewritten for clarification. For example, figure 7 should be given more details, labels to different components would be useful. Figure 8 should have a detailed explanation of parameters of lambda and mu.

Answer:

Captions for figures have been rewritten in the paper.
Fig. 1 (first page line 23)
"DAMPE Detector Cross Section. The DAMPE consists of PSD, STK, BGO and ND."
Fig. 2 (first page line 56)
"Structure of APA FPGA from Ref. [4]."
Fig. 3 (second page line 23)

"Structure of TMR. Three replicas for one memory cell are used and a voter identifies the correct result among the three ones on the basis of a majority vote."
Fig. 4 (second page line 80)
"Structure of FPGA of BGO FEE. The control part and the scientific data acquisition part implement the main function of the logic and take up about 78% of all logic resource consumption; system settings saved in the registers and RAMs in the status part and the monitor part is used for real-time monitoring.:
Fig. 5 (third page line 9)
"Multi-domain reset signal. Hw_rstn is the global hardware reset signal; Soft_rstn is the global software signal; Cmd_path_rstn and sci_path_rstn is used to reset the control part and the scientific data acquisition part respectively."
Fig. 7 (forth page line 9)
*"SEU Test Site. The test is performed at HIRFL-TR5 terminal, using Krypton ions. Irradiations were conducted in air, at ambient room temperature, with heavy ions passing through a vacuum/air transition foil. The LET values of the ions could be adjusted from 22.7 to 39.9 MeV*cm2/mg."*
Fig. 8 (forth page line 72)
"System Reliability Changes with Time. λ, which represents the rate that the value in a DFF transitions from correctness to error per unit time is assumed to be 10-7 hour-1. μ, which represents the repair rate per unit time is assumed to be 1 hour-1 in the architecture of TMR DFF."

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3. Section III, subsection A: a brief description of monitor part and status manager part could be provided for completeness.

Answer:

The description of monitor part and status manager part has been added in the paper (second page line 63 to line 68) as follows:
"In the status manager part, there are some key registers and RAMs which are used to set the operating status of the system and need to be valid all the time. Other parts get operating settings from the status part. The monitor part provides some parameters describing the operating status for real-time monitoring."

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4. Section IV, subsection B & C: it is not clear why the ion beam test uses two different FPGA part numbers, APA600 and APA300. Which one is used on the FEE?

Answer:

APA300 and APA600 are both used in the BGO calorimeter. The characteristics of them are same except the number of system gates. The instructions have been added in the paper (first page line 48 to line 53) as follows:
"Two kinds of flash-based FPGA of Actel, ProASIC Plus APA300 (APA300) which has 300000 system gates and ProASIC Plus APA600 (APA600) which has 600000 system gates are chosen as the BGO FEE controlling chips. These two types of chips are same expect the number of resources."

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5. Section IV, subsection B & C: it would be nice to spell out what the expected fluence of FPGA is for 3 years of running of DAMPE. With this as reference, people could possibly draw conclusion based on the total fluence accumulated in beam test.

Answer:

Because that SEU is transient effect which does not accumulate with time, there is no need to compare the total fluence accumulated in the beam test with the expected fluence of FPGA in space for 3 years. As the fluxes and LET values in the experiment are much higher than the ones in the space, people could possible draw conclusion that the FPGA could work properly in space.
What can accumulate with time is Total ionizing dose (TID) effect, and the TID test was performed for the FPGA. Total ionizing dose (TID) test for the front end electronics (FEE) board with APA600 was conducted at National Institute of Metrology, China and University of Science and Technology of China (USTC). A ^{60}Co gamma source was used as in the TDI test. The whole FEE board was irradiated up to 10Krad (Si) with a dose rate of 2.61rad/s at the room temperature. Accelerated ageing with power-on at 100℃ for 60 hours was done after irradiation exposure. The experiment results showed that no evident degradation of FPGA was found. All function of FPGA worked well during the experiment. The supply current of FPGA was monitored and no abnormal value was found. After the experiment, the APA600 chip could be reconfigured with new logic, which meant the configuration part of the chip was not damaged either.
The information of the TID test and the results are stated as above. However, because that the main topic of this paper is to talk about the SEU mitigation in logic design, I have not added them to the paper.

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6. Section V, subsection A: it would be nice to provide more details about the simulation study using Markov model.

Answer:

Some calculation has been added to Section V. The model has been analyzed in detail and MTBF of the system with and without TMR has been calculated. This part of paper has been rewritten (forth page line 70 to fifth page line 39) as follows:

"Using Markov model in fault-tolerant computing, a system's reliability can be predicted [10]. According to the study of McMurtrey D, if defining reliability as the probability that the value in a single DFF register is still correct after a certain time, then

$$R_{DFF1}(t) = e^{(-\lambda t)} \quad (1)$$

Where λ *represents the rate that the value in a DFF transitions from correctness to error per unit time and t represents time.*

Concerning structure with TMR DFF, then

$$R_{DFF2}(t) = \frac{(\mu+5\lambda)\sinh\left(\frac{1}{2}t\sqrt{\mu^2+10\lambda\mu+\lambda^2}\right)e^{-\frac{1}{2}(\mu+5\lambda)t}}{\sqrt{\mu^2+10\lambda\mu+\lambda^2}} + \cosh\left(\frac{1}{2}t\sqrt{\mu^2+10\lambda\mu+\lambda^2}\right)e^{-\frac{1}{2}(\mu+5\lambda)t} \quad (2)$$

Where λ *represents the rate that the value in a DFF transitions from correctness to error per unit time,* μ *represents the repair rate per unit time and t represents time.*

Concerning there are 3000 key registers in the FPGA logic, if defining system reliability as the probability that all registers in the system are correct, then

$$R_{system}(t) = R_{DFF}{}^{3000} \quad (3)$$

As CREME96 predicts that the SEU probability for the APA chip is about 6.8×10^{-7} $bit^{-1}\cdot day^{-1}$ *at the altitude of 500km [6], [7], [8],* λ *is assumed to be* 10^{-7} $hour^{-1}$. *And because there is write-back line in the structure of TMR in the design,* μ *is very much closed to 1. Combining these two parameters with equations 1, 2 and 3, the system reliability changing with time can be derived and the results are shown in Fig. 8. Compared with the one of system without TMR, the reliability of system with TMR almost does not change with time and is still very close to 1 after 30000 hours. Therefore, the structure of TMR with write-back line can highly improve the reliability of a system.*

Using the system reliability, Mean Time Between Failure (MTBF) of the system can be calculated. As shown in equation 4 and 5, the MTBF of the system can be improved by 10^6 *times if using the structure of TMR with write-back line.*

$$MTBF_{Without\ TMR} = \frac{\int_0^\infty \frac{d(1-R_{DFF1}{}^{3000})}{dt} * t dt}{\int_0^\infty \frac{d(1-R_{DFF1}{}^{3000}{}_1)}{dt} dt} := 3000 hours \quad (4)$$

$$MTBF_{With\ TMR} = \frac{\int_0^{\infty} \frac{d\left(1-R_{DFF2}{}^{3000}\right)}{dt} * t dt}{\int_0^{\infty} \frac{d\left(1-R_{DFF2}{}^{3000}\right)}{dt} dt} := 10^9\, hours \qquad (5)"$$

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7. Section V, subsection B: Again it would be nice to compare expected fluence of experiment, and the accumulated fluence in beam test, before any conclusion is drawn.

Answer:

The answer is the same as question 5.