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The Belle II SVD data readout system

R. Thalmeier [b,*], K. Adamczyk [u], H. Aihara [q], C. Angelini [i,j], T. Aziz [g], V. Babu [g], S. Bacher [u], S. Bahinipati [d], E. Barberio [a], Ti. Baroncelli [a], To. Baroncelli [a], A.K. Basith [e], G. Batignani [i,j], A. Bauer [b], P.K. Behera [e], T. Bergauer [b], S. Bettarini [i,j], B. Bhuyan [f], T. Bilka [c], F. Bosi [j], L. Bosisio [k,l], A. Bozek [u], F. Buchsteiner [b], L. Bulla [b], G. Casarosa [j], M. Ceccanti [j], D. Cervenkov [c], S.R. Chendvankar [g], N. Dash [d], S.T. Divekar [g], Z. Doleźal [c], D. Dutta [g], F. Forti [i,j], M. Friedl [b], K. Hara [n], T. Higuchi [m], T. Horiguchi [p], C. Irmler [b], A. Ishikawa [p], H.B. Jeon [s], C. Joo [m], J. Kandra [c], K.H. Kang [s], E. Kato [p], T. Kawasaki [o,1], P. Kodyś [c], T. Kohriki [n], S. Koike [n,2], M.M. Kolwalkar [g], P. Kvasnićka [c], L. Lanceri [k,l], J. Lettenbicher [b], T. Lueck [i,j], M. Maki [n], P. Mammini [j], S.N. Mayekar [g], G.B. Mohanty [g], S. Mohanty [g,h], T. Morii [m], K.R. Nakamura [n], Z. Natkaniec [u], K. Negishi [p], N.K. Nisar [g], Y. Onuki [q], W. Ostrowicz [u], A. Paladino [i,j], E. Paoloni [i,j], H. Park [s], F. Pilo [j], A. Profeti [j], K.K. Rao [g], I. Rashevskaya [l,3], G. Rizzo [i,j], M. Rozanska [u], J. Sasaki [q], N. Sato [n], S. Schultschik [b], C. Schwanda [b], Y. Seino [o], N. Shimizu [q], J. Stypula [u], J. Suzuki [n], S. Tanaka [n], K. Tanida [t], G.N. Taylor [a], R. Thomas [g], T. Tsuboyama [n], S. Uozumi [s], P. Urquijo [a], L. Vitale [k,l], S. Watanuki [p], I.J. Watson [q], J. Webb [a], J. Wiechczynski [u], S. Williams [a], B. Würkner [b], H. Yamamoto [p], H. Yin [b], T. Yoshinobu [n,r]

[a] School of Physics, University of Melbourne, Melbourne, Victoria 3010, Australia
[b] Institute of High Energy Physics, Austrian Academy of Sciences, 1050 Vienna, Austria
[c] Faculty of Mathematics and Physics, Charles University, 12116 Prague, Czech Republic
[d] Indian Institute of Technology Bhubaneswar, Satya Nagar, India
[e] Indian Institute of Technology Madras, Chennai 600036, India
[f] Indian Institute of Technolog y Guwahati, Assam 781039, India
[g] Tata Institute of Fundamental Research, Mumbai 400005, India
[h] Utkal University, Bhubaneswar 751004, India
[i] Dipartimento di Fisica, Universita' di Pisa, I-56127 Pisa, Italy
[j] INFN Sezione di Pisa, I-56127 Pisa, Italy
[k] Dipartimento di Fisica, Universita' di Trieste, I-34127 Trieste, Italy
[l] INFN Sezione di Trieste, I-34127 Trieste, Italy
[m] Kavli Institute for the Physics and Mathematics of the Universe (WPI), University of Tokyo, Kashiwa 277-8583, Japan
[n] High Energy Accelerator Research Organization (KEK), Tsukuba 305-0801, Japan
[o] Department of Physics, Niigata University, Niigata 950-2181, Japan
[p] Department of Physics, Tohoku University, Sendai 980-8578, Japan
[q] Department of Physics, University of Tokyo, Tokyo 113-0033, Japan
[r] Department of Physics, Tokyo University of Science, Chiba 278-8510, Japan
[s] Department of Physics, Kyungpook National University, Daegu 702-701, Republic of Korea
[t] Department of Physics and Astronomy, Seoul National University, Seoul 151-742, Republic of Korea
[u] H. Niewodniczanski Institute of Nuclear Physics, Krakow 31-342, Poland

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A B S T R A C T

The Belle II Experiment at the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan, will explore the asymmetry between matter and antimatter and search for new physics beyond the standard model.

172 double-sided silicon strip detectors are arranged cylindrically in four layers around the collision point to be part of a system which measures the tracks of the collision products of electrons and

* Corresponding author.
E-mail address: Richard.Thalmeier@oeaw.ac.at (R. Thalmeier).
[1] Presently at Kitasato University, Sagamihara 252-0373, Japan.
[2] Deceased.
[3] Presently at INFN-TIFPA, I-38123 Trento, Italy.

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positrons. A total of 1748 radiation-hard APV25 chips read out 128 silicon strips each and send the analog signals by time-division multiplexing out of the radiation zone to 48 Flash Analog Digital Converter Modules (FADC).

Each of them applies processing to the data; for example, it uses a digital finite impulse response filter to compensate line signal distortions, and it extracts the peak timing and amplitude from a set of several data points for each hit, using a neural network.

We present an overview of the SVD data readout system, along with front-end electronics, cabling, power supplies and data processing.

1. Introduction

The Belle II experiment (Fig. 1, [1]) will take place in Tsukuba, about 60 km northeast of Tokyo in Japan. Electrons and positrons are accelerated to different energies in two contra rotating rings of about 1 km in diameter, and made to collide in a single point, producing B-mesons and anti-B-mesons. These subatomic particles have a very short lifespan and thus fly only some 100 μm before they decay into well-known particles, whose tracks are measured by different detectors. By doing so, we are able to identify them and calculate the spatial difference of their origins, again in the order of 100 μm. To precisely measure these tracks, high spatial and timing resolutions are required.

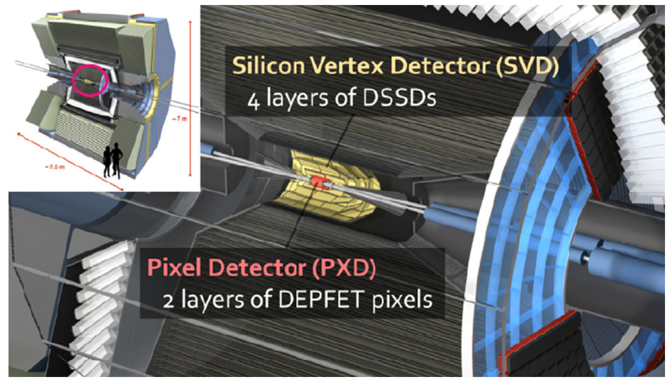

Fig. 2. Silicon detectors.

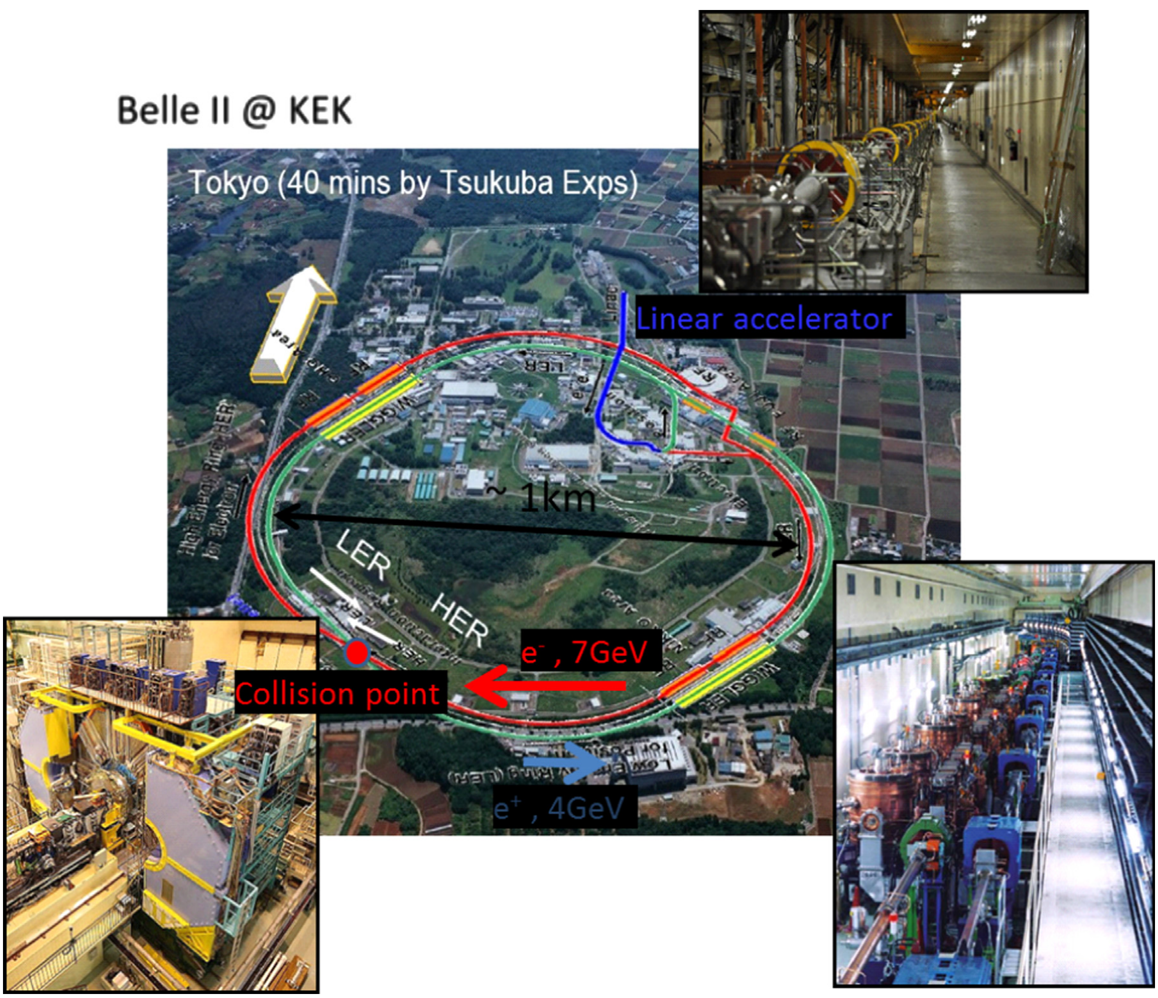

Fig. 1. Belle II experiment.

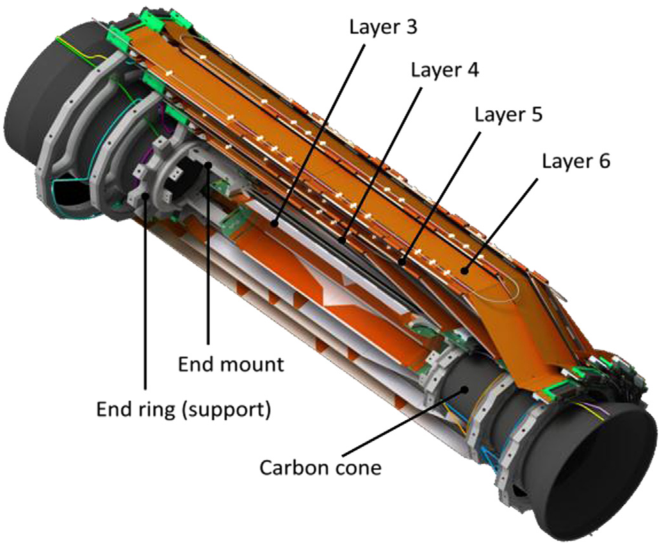

Fig. 3. SVD.

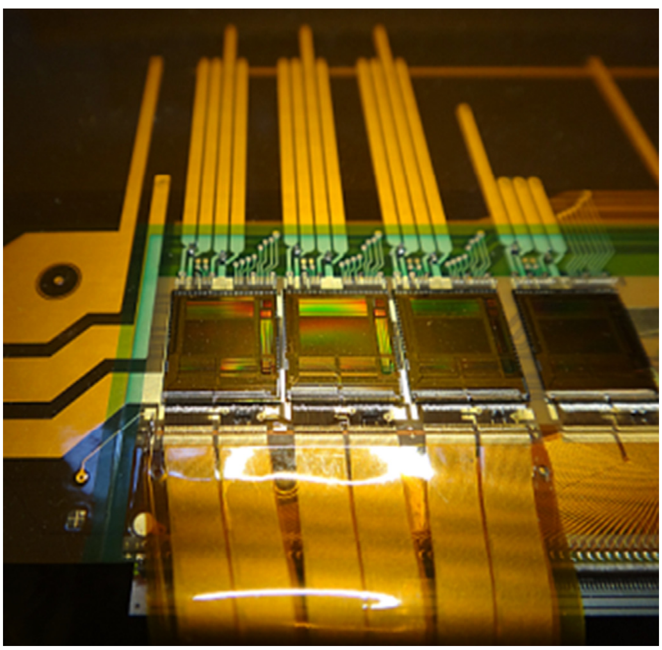

Fig. 4. SVD hybrid.

2. The silicon vertex detector (SVD)

The inner tracking device is composed of six layers of silicon detectors (Fig. 2), whose two innermost layers make up the pixel detector (PXD, [2]) and the outer four are part of the silicon vertex detector (SVD, Fig. 3, [3]). They reside with their front-end readout electronics in a volume with radiation and strong magnetic field, where conventional electronics would not work at all or survive only for a short time.

Fig. 6. Cabling.

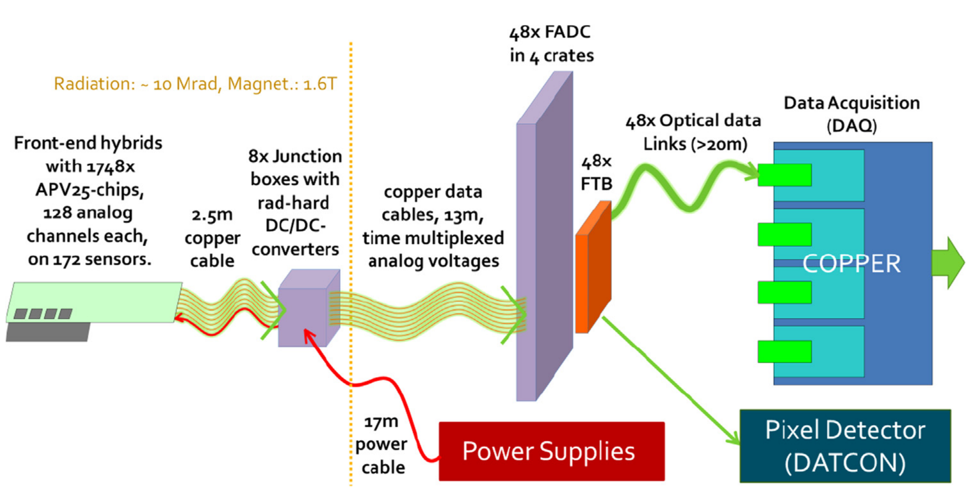

Fig. 5. SVD readout concept.

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In the SVD, 172 silicon sensors are arranged cylindrically in four layers around the collision point. They are double-sided with orthogonally arranged strips to obtain both x and y coordinates. The SVD readout system (Fig. 5) consists of a total of 1748 radiation-

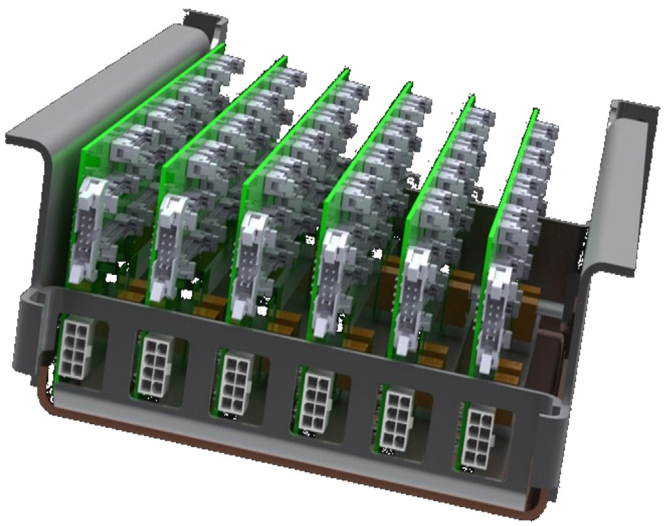

Fig. 7. Junction box.

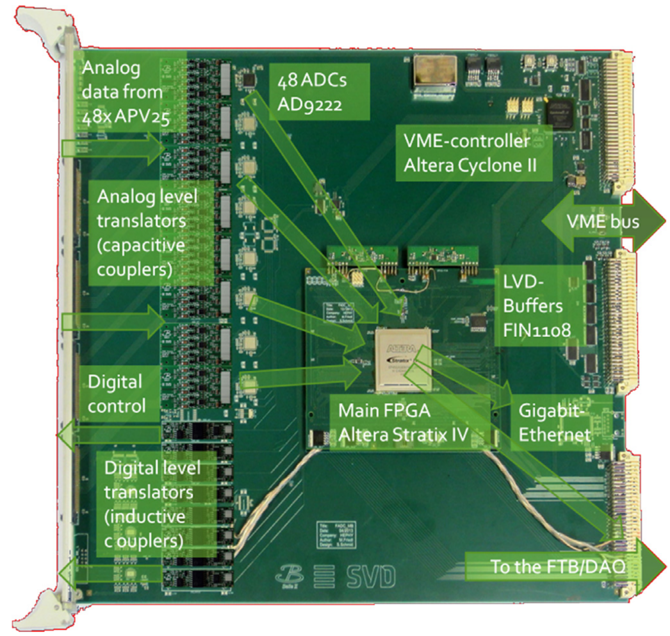

Fig. 9. FADC module prototype.

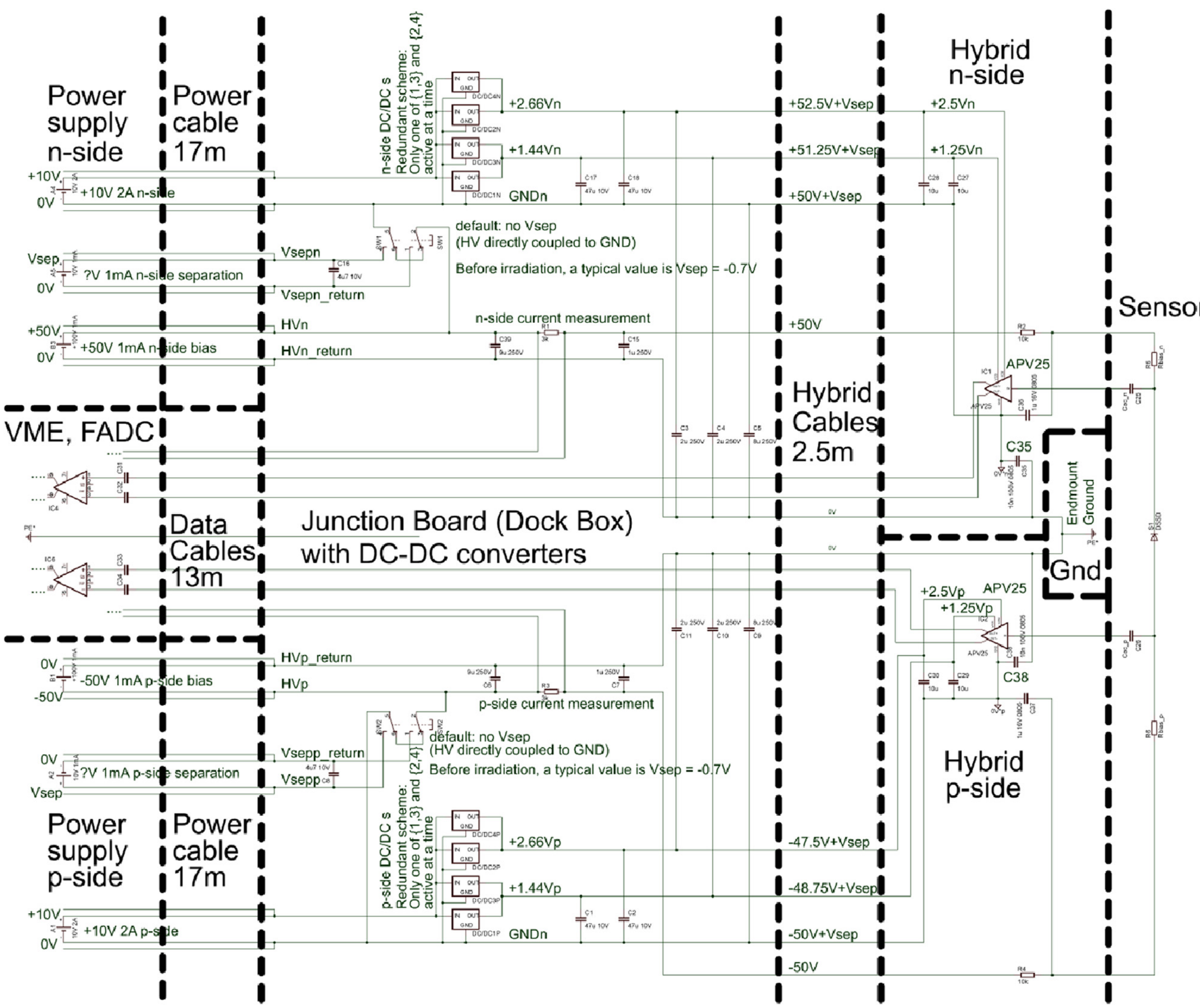

Fig. 8. Power supply scheme.

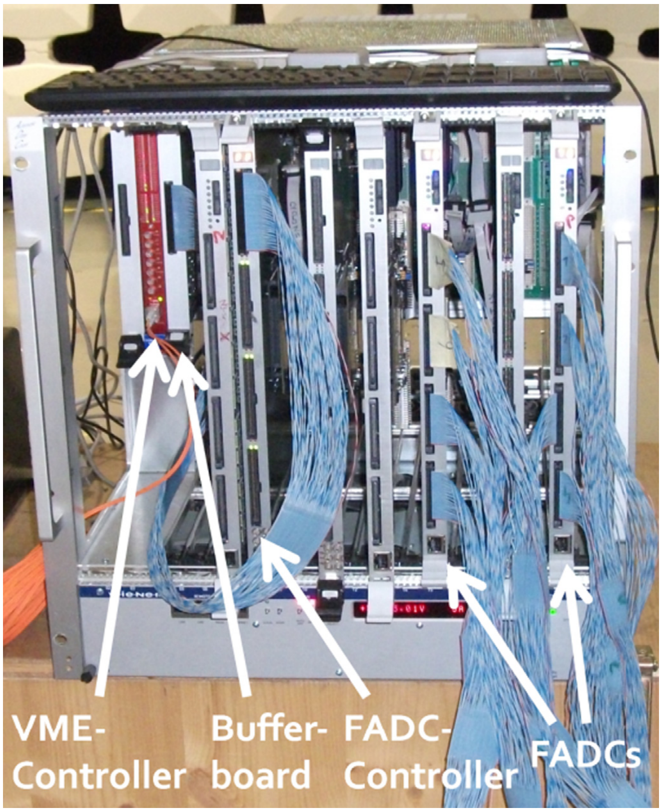

Fig. 10. VME crate prototype.

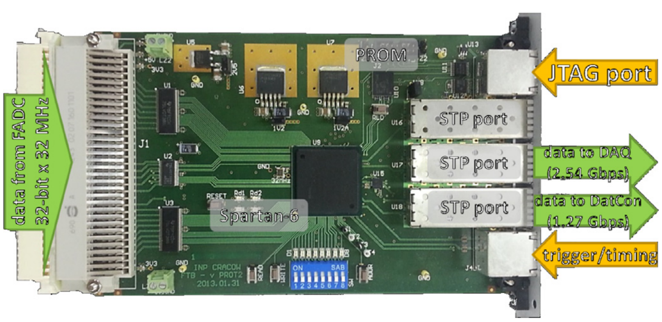

Fig. 11. FTB.

hard APV25 chips [4] glued and wire bonded to hybrids (Fig. 4), which readout 128 silicon strips each and send the analog signals by time-division multiplexing over an approximately 15.5 m long copper cable out of the radiation zone to Flash Analog Digital Converter modules (FADCs).

3. Junction box, SVD power supply scheme, cabling

The SVD system is powered by several power supply units located on the top of Belle II. These units supply the “high voltage” (HV, about 50 V) required to bias the sensors and the “low voltage” (LV, 10 V) to power the Front End Electronics (FEE). The HV line feeds the sensors directly whereas the LV is distributed to eight junction boxes (Fig. 7) located 2.5 m away from the SVD FEE. At that location, DC/DC converters transform the 10 V into the 2.5 V and 1.25 V required to operate the APV25. One characteristic of these double-sided silicon sensors is that there is no “ground” connection, but both sides of the sensors are silicon strips which are biased with resistors to high voltages (positive and negative, respectively) and which are read out individually by the APV25 chips, 128 strips per chip. Two DC/DC converters in the junction boxes power 4 hybrid boards with four (n-side of layers 4–6) or six (all the others) APV25 chips each. The power supply concept (Fig. 8) has only one single grounding point, on the end mount metal structure of the detector, where all the high voltage return lines are connected to. All other components including the power supplies are left floating with respect to this point. Thus, there is no grounding loop or other structure in the cabling (Fig. 6) which could conduct low frequency noise with low impedance into the APV25 zone. Comprehensive electromagnetic compatibility (EMC) studies have been performed at ITA, Zaragoza, Spain [5]. The SVD power system has been fully characterized in terms of its EMC behavior, and some knowledge gained thereby has already been implemented into the system to improve its robustness. For example, the capacitors C35 and C38 in Fig. 8 have been exchanged retroactively from 10 nF to 100 nF, and additional filters were implemented into the power supplies. Some further improvements resulting in a reduction of possible HF grounding loops will be implemented in the next revision of the junction box boards and the FADC boards.

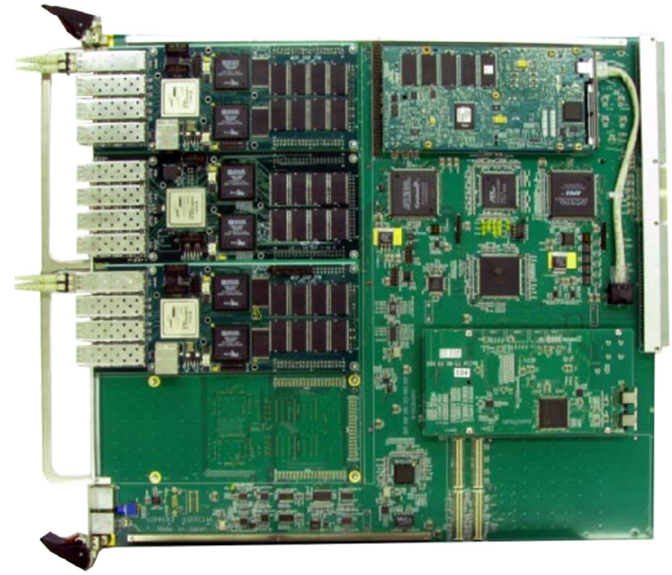

Fig. 12. COPPER.

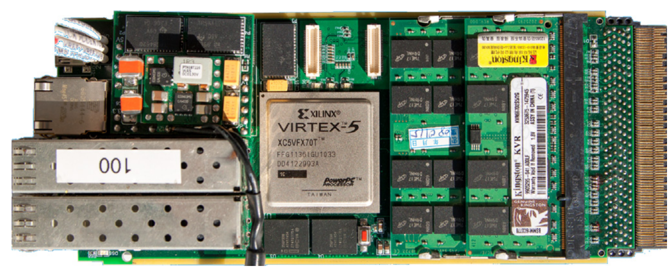

Fig. 13. DATCON.

4. The flash analog digital converter (FADC) modules

In each of the 48 FADC modules (Fig. 9) residing in 4 VME crates (Fig. 10) there are 48 analog-to-digital converters, one per APV25-chip plus some spares, and one Field Programmable Gate Array (FPGA), namely an Altera Stratix IV GX, which processes the data. It uses a digital finite impulse response (FIR) filter to compensate line signal distortions, performs Signal Extraction, Strip Reordering, Pedestal Subtraction, Common Mode Correction and

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Zero Suppression. Along with its trigger system it extracts the peak timing and amplitude for each hit from a set of data points with a precision of about 3 ns using a neural network.

5. Data acquisition system (DAQ)

Eventually, the processed data are converted to the optical domain by Finesse Transmitter Boards (FTB, Fig. 11) and sent in parallel to two different locations: the COPPER readout boards (Fig. 12, [6]) as part of the Data Acquisition System (DAQ) and the DATCON boards (Fig. 13, [7]), which belong to the PXD system and take care of their data reduction by calculating of Regions of Interest (RoI) on the PXD layers from the SVD tracks.

6. Conclusions

The complete SVD data readout system has been tested successfully at several test beams (CERN, DESY) with prototypes. Conclusive developments are being made now, mainly to further improve the EMC robustness. The mass production is planned for March to May 2017.

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