A Front-End Electronics Prototype Based on Gigabit Ethernet for the ATLAS Small-Strip Thin Gap Chamber

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FPGA的写法

***Abstract*— A front-end electronics prototype for the ATLAS small-strip Thin Gap Chamber (sTGC) based on gigabit Ethernet has been developed. The prototype is designed to read out signals of pads, wires, and strips of the sTGC detector. The prototype includes two VMM2 chips developed to read out the signals of the sTGC, a Xilinx Kintex-7 field-programmable gate array (FPGA) used for the VMM2 configuration and the events storage, and a gigabit Ethernet transceiver PHY chip for interfacing with a computer. The VMM2 chip is designed for the readout of the Micromegas detector and sTGC detector, which is composed of 64 linear front-end channels. Each channel integrates a charge-sensitive amplifier, a shaper, several analog-to-digital converters, and other digital functions. For a bunch-crossing interval of 25 ns, events are continuously read out by the FPGA and forwarded to the computer. The interface between the computer and the prototype has been measured to reach an error-free rate of 900 Mb/某段结束语 making a very effective use of the available bandwidth. Additionally, the computer can control several prototypes of this kind simultaneously via the Ethernet interface. At present, the prototype will be used for the sTGC performance test. The features of the prototype are described in detail.**

***Index Terms*— ATLAS strip thin gap chamber (sTGC) trigger electronics, field-programmable gate array (FPGA), front-end electronics, gigabit Ethernet transceiver.**

I. Introduction

ATLAS [1], [2] is one of four experiments that are located at the Large Hadron Collider constructed at CERN, Geneva, Switzerland. The ATLAS detector accepts the events from the proton–proton collision at a rate of 40 MHz. The tracks containing events of interest are selected via a series of trigger decisions. At high luminosity, the performance of the muon tracking chambers, both in terms of efficiency and resolution, degrades with the increase of the background rate, especially in the end-cap region. Moreover, the low-energy protons, generated in the magnet materials between the Small Wheel (SW) and the end-cap muon detector (EM), hit the end-cap trigger chambers, thus producing fake triggers. As the already existing muon Trigger (trigger signal) is not capable of determining the direction of the muon before the magnetic field, muon not emerging from the interaction point (IP) can be misidentified as primary trigger candidates. To cope with these problems, it is proposed by ATLAS collaboration to replace the current muon SW with the "New Small Wheel" (NSW). The Thin Gap Chamber (TGC) technology, developed in 1983 [3], is an important part of the SW. The small-strip TGC (sTGC) in which the strip pitch is much smaller than that of the current ATLAS TGC will be applied for the NSW upgrade. Each sTGC detector consists of four pad-wire-strip planes. The pads are used through a 3-out-of-4 coincidence to identify muon tracks approximately pointing to the IP. They are also used to determine which strips need to be read out to obtain a precise position measurement in the precision coordinate. The charges of the wires are read out to obtain the azimuthal coordinate of a muon trajectory.

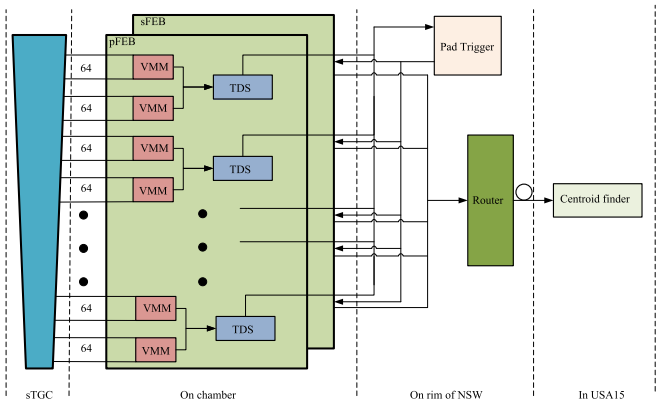

Fig. 1. Block diagram of the trigger logic in NSW.

The simplified block diagram of the front-end trigger logic is shown in Fig. 1. The signals from the sTGC detector are initially received by a VMM [4], an Application-Specific Integrated Circuit (ASIC), which is being developed to read out the pads, strips, and wires of the sTGC detectors. Then, data from

Manuscript received June 21, 2016; revised January 19, 2017; accepted March 11, 2017. Date of publication March 14, 2017; date of current version June 26, 2017. This work was supported in part by the National Natural Science Foundation of China under Grant 11375179 and Grant 11461141010 and in part by the Fundamental Research Funds for the Central Universities under Grant WK2360000005.

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Digital Object Identifier 10.1109/TNS.2017.2682188

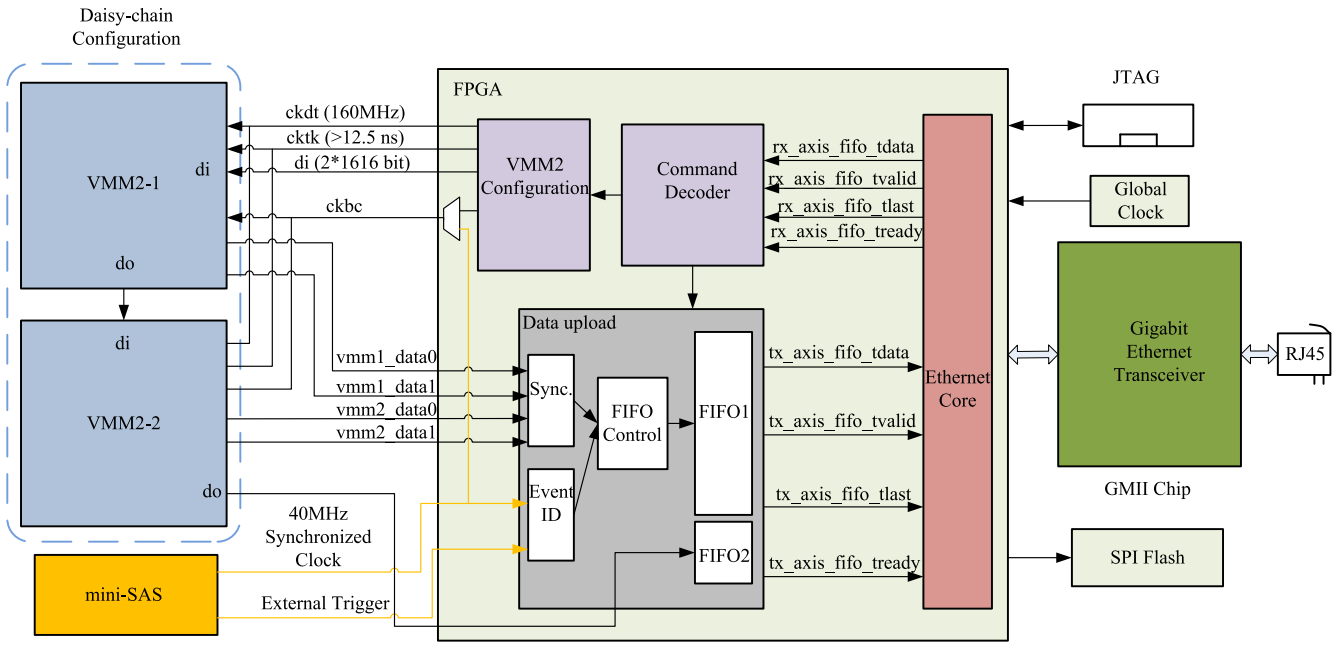

Fig. 2. Schematic of the prototype based on the gigabit Ethernet interface.

VMMs are processed by the Trigger-Data-Serializer (TDS) ASIC before being transmitted to the router. The signals from strips and pads of sTGC detectors will be read out by two front-end boards (FEBs), strip FEB (sFEB) and pad FEB (pFEB), respectively. The pFEB is used for the pad trigger. The pad "hit" event from all channels are serialized and sent to the pad trigger on the rim of the NSW. The trigger logic uses a 3-out-of-4 coincidence of pads in each of the four-layer quadruplets. The pad coincidence is sent back to the sFEB to determine which band of strips needs to be read out to the router for further processing. After processing, the output of the router is sent to the Centroid Finder circuit in the ATLAS underground counting room. After the Phase-I upgrade of the muon spectrometer (MS), a muon angle determination in front of and behind the end-cap magnet will be available.

The current version, the VMM2 chip, is able to read out both positive and negative polarity signals for each channel. The VMM2 chip consists of 64 linear front-end channels. Each channel integrates a charge-sensitive amplifier (CSA), a shaper, a stable bandgap-referenced baseline, several analog-to-digital converters (ADCs), and other functions. At present, the TDS is under design. To simulate the trigger logic used for the NSW upgrade and read out the signals of the sTGC detector, a front-end electronics prototype of the sTGC detector, the so-called "mini-FEB," is built. For an input event rate of 40 MHz, the events are continuously read out by the field-programmable gate array (FPGA). Therefore, a high-speed data transfer interface is required to send out the events from the sTGC. For the multiple sTGCs, a one-to-many interconnection of the prototype is needed.

In this paper, we will introduce a front-end electronics prototype of the sTGC detector based on a high-speed gigabit Ethernet interface. The prototype includes two VMM2 chips, a Xilinx Kintex-7 FPGA, and a gigabit Ethernet transceiver working in the data link layer of the Ethernet. The data format of an Ethernet packet can be defined by the user, and the transfer protocol is based on the media access control (MAC) layer that is neither UDP nor TCP. Additionally, the prototype integrates a high-speed mini-SAS interface, which is used for the acceptance of an external trigger signal. The Windows Packet capture (WinPcap) technique provides a driver to capture the Ethernet traffic that the prototype returns. The graphical user interface (GUI) is written based on a Qt application platform, achieving the initialization and control of the prototype.

II. Prototype Architecture

A. Hardware

The schematic block diagram of the prototype is shown in Fig. 2. The core of the prototype is based on a Kintex-7 FPGA, which is configured by a serial peripheral interface flash. Two VMM2s, which are interconnected using a daisy chain, are used to read out the signals from the sTGC detector. The mini-SAS connector is designed to receive the external trigger and the 40-MHz synchronized clock. The external trigger emerges from a coincidence of two scintillation detectors over and below the sTGC detector, which is used for an sTGC efficiency test in the future. The 88E1111 gigabit Ethernet transceiver is a physical layer device for 1000BASE-T, 100BASE-TX, and 10BASE-T application, which incorporates an optional 1.25-GHz SERDES (Serializer/Deserializer). In our design, the gigabit Ethernet transceiver is configured as the gigabit media-independent interface. The RJ45 port is used for the connection between the hardware and a computer.

B. Signal Flow in FPGA

The block diagram of the signal flow in the FPGA is shown in the middle of Fig. 2. The Ethernet core, generated via the core generator of the Xilinx ISE software, is embedded

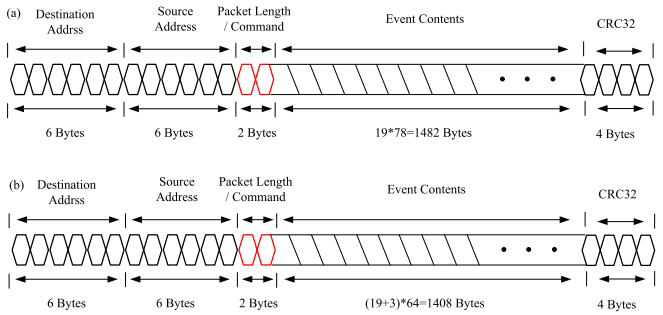

Fig. 3. Data format of an Ethernet packet (a) without and (b) with the external trigger.

in the FPGA. The Ethernet interface is implemented in the MAC layer, which is a sublayer of the data link layer. The Ethernet interface accepts the user-defined commands and VMM2 configuration bits. The different commands can be derived from the command decoder. At initialization, all the FIFOs and status registers are reset. Then, a VMM2 configuration command arrives. The VMM2 configuration module is implemented via a state machine. After the configuration, the VMM2 data (*data0*, *data1*) will output when one of the VMM2 channels receive a charge signal. Once sending a user-defined *data upload* command, events from two VMM2s are stored in an internal FIFO. Then, these events are sent back to a computer.

C. Data Format

The data format of an Ethernet packet is shown in Fig. 3. The data are transferred via an Ethernet interface. For a scenario without an external trigger, each Ethernet packet has 78 events. Each event from the VMM2 contains a total of 38 b, shifted out in parallel to the data0 and data1 pins using 19 clock edges. The data0 and data1 signals are inserted in an 8-b Ethernet bus. Then, each event takes 19 B of an Ethernet packet. The total size of an Ethernet packet is 1500 B, which is less than the maximum size of a standard Ethernet packet (1518 B). It includes a 6-B destination MAC address, a 6-B source MAC address, a 2-B user-defined token, 1482-B data (78 events) from VMM2, and a 4-B CRC check [5]. For a case with an external trigger, however, an event identification with 3 B is added after every event, which is generated via an internal counter driven by the external trigger signal. The total size of an Ethernet packet for this case is 1426 B. The 88E1111 chip transfers data via an 8-b bus. The low 4 b are used for two VMM2's data while the high 4 b are zeros. The low 4 b are sequently *vmm2_2_data1*, *vmm2_2_data0*, *vmm2_1_data1*, and *vmm2_1_data0*, respectively. The 2-B token means a user-defined command when its value is higher than 1500. It also means an Ethernet packet length when lower than 1500.

III. Software Structure

To configure and control the prototype, a GUI software is built, which is implemented on the basis of the Qt platform. The GUI has access to the Ethernet packet using the popular WinPcap technology.

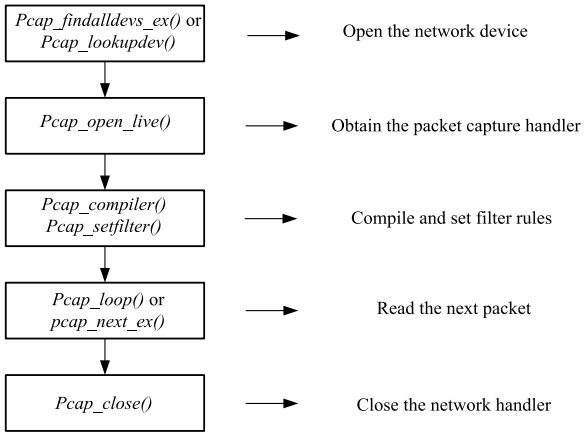

Fig. 4. Basic process of the WinPcap.

A. WinPcap Technology

The WinPcap is a system framework of packet captures and network analyzers based on the Windows platform [6]–[8]. It can capture and send the underlying raw data. In our design, the network is set to promiscuous mode using the API function *pcap_open_live()*. In this mode, the network interface controller (NIC) passes all traffic it receives, including the Ethernet packet the user sends. That means the network card does not make any judgment. Therefore, compiling and setting filter rules play a vital role in the WinPcap. It is implemented by use of the function *pcap_compile()* and *pcap_setfilter()*. Subsequently, the NIC transmits all the frames to the WinPcap handler via the function *pcap_next_ex()*. The basic process of the WinPcap is shown in Fig. 4.

B. Graphical User Interface

The GUI panel mainly achieves several functions: global reset and parameter set, the VMM2 configuration, VMM2 data acquisition, and some test modes. The application software is written using the standard C++. For each VMM2 data, the GUI not only displays the channel number tested but also the corresponding amplitude histogram.

IV. Test Results

A. Noise Test

The noise test is carried out after the VMM2 configuration. The signal from the monitor (MO) pin of the VMM2 is captured by a high-bandwidth Tektronix oscilloscope. Fig. 5 shows the output noise of the prototype. The noise voltage with a Gaussian distribution is plotted in a histogram. The root mean square (rms) is less than 2 mV_{rms}. The noise is mainly contributed by the thermal noise of components and the high-frequency noise in digital components, such as FPGA. From Fig. 5, the mean value is 173 mV, generated by a stable bandgap-referenced baseline.

B. VMM2 Performance

The VMM2 chip consists of 64 front-end channels and a digital processing circuit [9]. The architecture of the

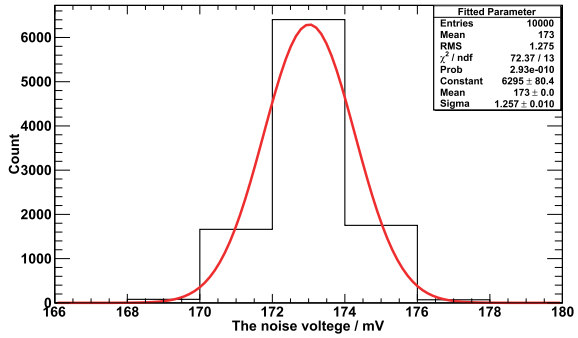

Fig. 5. Output noise of the prototype shielding the input charge signal.

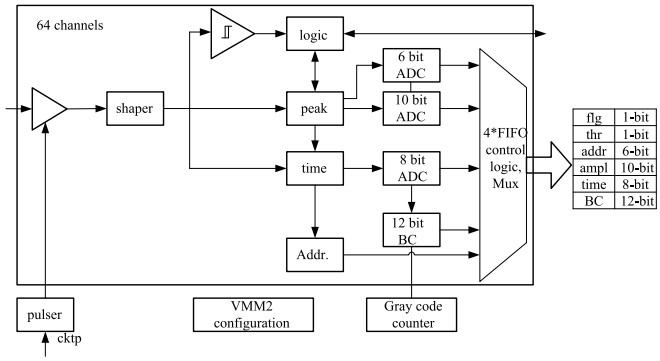

Fig. 6. Architecture of the VMM2 chip.

VMM2 chip is shown in Fig. 6. Each channel is composed of a CSA and shaper. Next to the shaper are the discriminator, the peak detection, and the time detection. The VMM2 can operate in three modes. In our VMM2 configuration, the continuous mode is used. In this mode, the peak and the time detection convert the voltages into currents that are routed to the 10-b ADC and 8-b ADC, respectively. The 10-b ADC provides a high-resolution A/D conversion for the peak value. The 8-b ADC is applied to convert the peak timing, which is measured using a time-amplitude conversion (TAC). The TAC stop signal occurs at the next clock period of a shared 12-b gray-code counter incremented using an external bunch clock. In the continuous mode, a total of 38-b are generated for each event, which is stored in a 4-events deep FIFO.

The shaper has an adjustable peaking time and a stabilized referenced baseline. The baseline can be read out on the oscilloscope via its analog MO capability. The baselines of the 64 channels for a VMM2 chip are shown in Fig. 7. The mo pin output of the VMM2 is to MO the analog signal from the shaper while the pdo pin output is used for peak detection. From the graph, not all 64 channels exhibit good baseline results. There are some channels showing a drop.

Each channel is calibrated by a pulser and a 1.2-pF test capacitor. The pulser is adjustable with a global 10-b DAC, triggered with an external test pulse clock. The digital value is sent to the VMM2 with the configuration bit sequence. The linearity of the pulser is measured by means of stepping up the DAC value. The results are shown in Fig. 8. In the linear region, the relationship between the digital input (DI) and the analog output (AO) is given by

$$\mathrm{AO} = \mathrm{DI} \times 0.7 - 65.9. \tag{1}$$

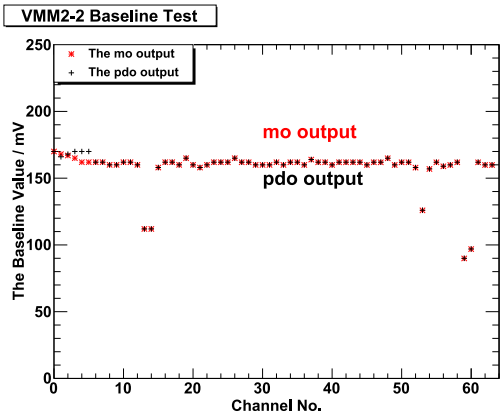

Fig. 7. Baseline test of the 64 front-end channels.

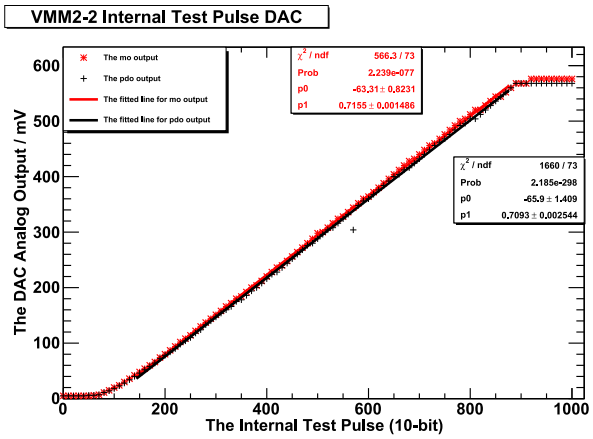

Fig. 8. Test results between the DI and the AO of the pulser.

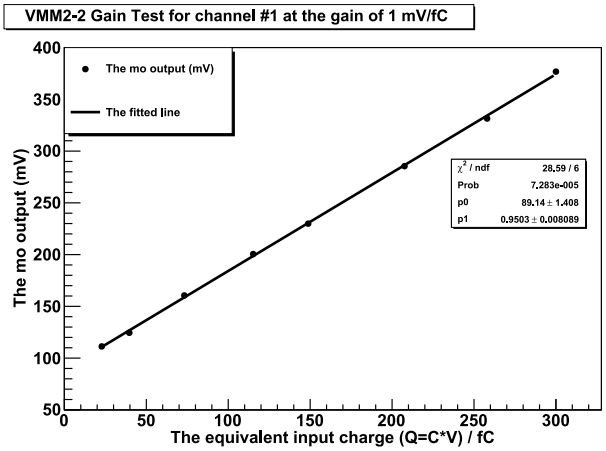

Fig. 9. Linearity test of a channel at the gain of 1 mV/fC.

Each channel has adjustable eight channel gains (0.5–12 mV/fC), offering higher analog dynamic ranges. For a given DAC value of the pulser and a given channel gain, we can obtain a histogram of the peak value. Stepping up the DAC value, a linearity test of the VMM2 channel is performed. The linearity test results are shown in Fig. 9. The equivalent input charge for the channel is described as $Q = \mathrm{CV}$ $(1.2* \mathrm{AO})$. The slope of the fit line means the actual channel gain we obtain. From Fig. 9, the channel gain is 0.95 mV/fC, slightly less than the nominal value.

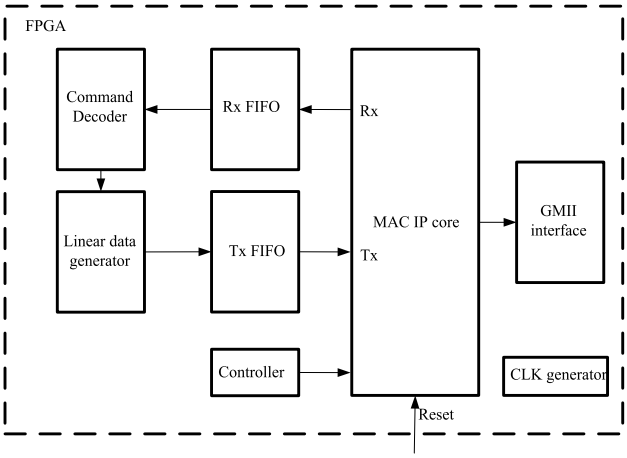

Fig. 10. Block diagram of the network test module.

C. Multiboard Interconnection

For the multiple sTGC detectors, one-to-many interconnection of the prototype is needed. The Ethernet interface is implemented in the MAC layer, then we can achieve the interconnection through a commercial Ethernet switch. Each prototype is assigned a different MAC address. Therefore, the computer can control each board via its address. We carried out an interconnection test. After the interconnection, each one works normally.

V. Gigabit Ethernet Test

A. Features and Implementation

To evaluate the gigabit Ethernet performance, a network test module is built in the FPGA, which is shown in Fig. 10. It can send and receive the Ethernet traffic at gigabit line speed. The hardware sends data only in reply to requests coming from a computer. When the computer issues a request, the command decoder analyzes the request, enabling the linear data generator. The request is usually a small packet, less than 20 B. The reply consists of 256 packets; each packet is less than the maximum size of 1518 B. In the generator, a counter outputting the binary code is used as a data source. For the Tx FIFO, the programmable full flag is used. The counter value is continuously written into the Tx FIFO until the number of entries in the FIFO is greater than or equal to the user-defined threshold. It means that if there are enough data in the FIFO, then an outgoing packet is sent to the computer. Also, the packet loss is tested in real time by embedding a sequence number into each packet sent to the computer. The measurement is called "linear data test" because the test results show a line in the software.

B. Ethernet Transmission Rate

In our design, the data format of an Ethernet packet has two possible ways: 1500 B and 1426 B. Therefore, we carry out a long-time stability test for the two ways, as is shown in Fig. 11. The transfer rate is measured for 10 h. The average transfer rate is calculated by the software per minute. From the figure, the average Ethernet transfer rate can reach up

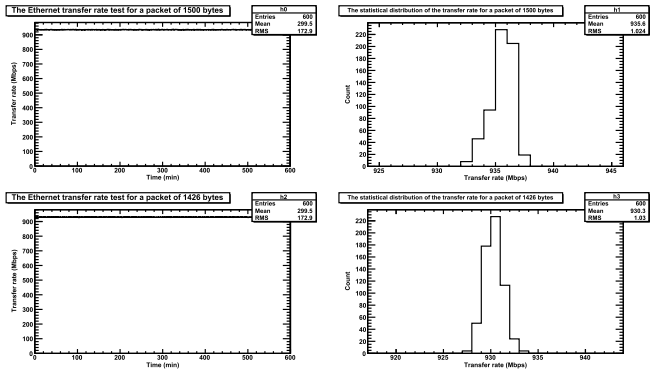

Fig. 11. Long-term stability test of the gigabit Ethernet.

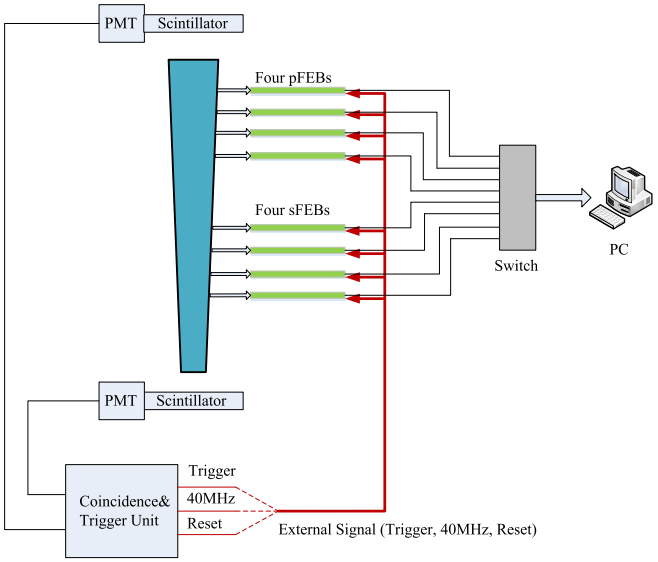

Fig. 12. Schematic of the cosmic ray DAQ system for sTGC prototype.

to 900 Mb/s, or less than 1 Gb/s. The reason is that there is no uploaded Ethernet packet from the hardware during a request of the computer, which decreases the usable bandwidth on a gigabit Ethernet network. In comparison with the data from the prototype, there is no error rate and missing packet within 10 h. The high-speed Ethernet interface has been utilized in our previous sTGC signal source [10], [11].

VI. Future Work

In the near future, a cosmic ray data acquisition system (DAQ) system for performance verification of sTGC prototype will be built. In the DAQ, there are two kinds of FEBs, pFEB, and sFEB. All FEBs are based on the structure of mini-FEB introduced earlier. The schematic block diagram of the cosmic ray DAQ system for the sTGC detector is shown in Fig. 12. The sTGC detector is sandwiched between two layers of scintillator arrays. For each layer of the scintillator array, there is a PMT array receiving scintillation light. Two layers of PMT signals are sent into a coincidence and trigger unit (CTU). The CTU will produce an external trigger signal (Trigger) when a cosmic ray muon goes through the sTGC detector. On the CTU, a fan-out module will output eight trigger signals of this kind to drive eight FEBs, four pFEBs, and four sFEBs. The fan-out module also sends eight 40-MHz

clocks originating from a phase-locked loop to synchronize eight FEBs. A reset signal is used for resetting parameters of the FEB. When a cosmic ray muon event crosses the sTGC detector, pFEBs and sFEBs receive the charge signal of the sTGC detector. After processing of the VMM2 chip, digital signals are sent into FPGAs. The VMM2 data on each FEB are buffered in an FIFO, then uploaded to a computer via a 16-port commercial Ethernet switch.

VII. Conclusion

In this paper, a front-end electronics prototype based on a gigabit Ethernet interface has been built for the ATLAS small-sTGC Phase-I upgrade. The prototype consists of a VMM2, FPGA, and gigabit Ethernet transceiver. The VMM2 performance and the Ethernet performance are discussed in detail. In the early upgrade, the prototype will be used for the sTGC performance test.

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