The Electronic System for the Astro-E Hard X-Ray Detector

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ABSTRACT

The Hard X-ray Detector (HXD) is one of three instruments on the fifth Japanese X-ray astronomy satellite, *Astro-E*, scheduled for launch in 2000. The sensitivity of the *Astro-E* HXD will be higher by more than one order of magnitude than that of any previous instrument between 10 keV and several 100 keV. The electronic system is designed to handle many independent data channels from the HXD within the limitation of size and power consumption required in *Astro-E*. In this paper, we will present the design and the preliminary performance of the processing electronic system.

Keywords: hard X-ray detector, gamma-ray detector, phoswich counter, electronic system, *Astro-E*

1. ASTRO-E HARD X-RAY DETECTOR

The fifth Japanese X-ray astronomy satellite, *Astro-E*, following *Hakucho*, *Tenma*, *Ginga*, and *ASCA* is scheduled for launch in the year 2000 by the Institute of Space and Astronautical Science (ISAS) with an M-V rocket.[1–3] The satellite will be put into an approximately circular orbit with an altitude of ~550 km and an inclination of ~31°. *Astro-E* carries two focal-plane instruments for soft X-ray observations, and one collimated large-area counter array for hard X-rays. A micro-calorimeter array (X-ray Spectrometer – XRS) and four identical sets of X-ray CCDs (X-ray Imaging Spectrometers – XIS) cover the energy band from 0.5 keV to ~10keV with imaging capability. The Hard X-ray Detector (HXD) is a combination of scintillation detectors and silicon PIN detectors. The HXD covers the energy range from 10 keV to 700 keV, which is essential to study non-thermal emission from celestial sources,

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such as supernova remnants, pulsars, blackhole candidates and AGN. All three instruments combined, *Astro-E* will become a spectrometer facility covering the wide energy band from 0.5 keV to 700 keV.

The HXD consists of a 4×4 = 16 modular assembly of identical units (the Well unit). The Well unit is a combination of GSO/BGO well-type phoswich counters and silicon PIN diodes.[4-6] The well-type phoswich counter differs from conventional phoswich counters in that it has a long protruding collimation part. This "well-shaped" shielding part made of BGO scintillator acts as an active collimator and an active shield. Silicon PIN diodes are an important addition which lower the energy coverage as well as improve the energy resolution in the lower-energy band (10–70 keV). Two layers of newly developed large (2 × 2 cm^2) 2mm-thick PIN detectors[7,8] are mounted at the bottom of the fine collimator and buried in the deep BGO well just above the GSO scintillator. Softer X-rays are absorbed in the PIN diodes; harder ones penetrate the diodes and are absorbed by the GSO. Since the detection part is surrounded over nearly in 4 π str by active shields, the detector background, which limits the sensitivity of the detector in the hard X-ray energy range, is reduced significantly.[9-12]

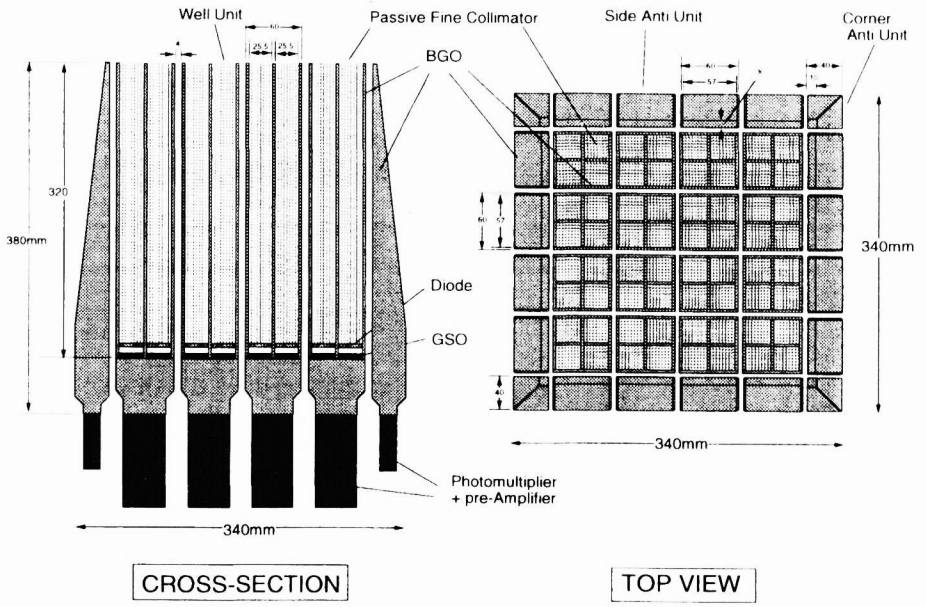

Figure 1. A schematic concept of HXD-S: Cross-section (left) and the top view (right). The housing and most of the electronic parts are not shown here.

Because of the simple structure of the Well unit, the effective area of the detector can be easily expanded. In the HXD, the 16 Well units are arranged into a compound eye configuration as shown in Fig. 1. For additional active shielding of the outermost units, 20 units of thick BGO anti-coincidence counters (Anti unit) surround the Well units. With 16 units, the geometrical area of the GSO scintillators (5 mm thick) is 330 cm^2 and that of the silicon PIN diodes (4 mm thick) is 230 cm^2. In addition to the concept of the well-type active shielding, the mutual anti-coincidence of the compound eye configuration further reduces the detector background. Furthermore, with the thick BGO scintillator wall of the Anti units (a thickness of 2.6 cm on average), the effective area at 1 MeV reaches 600 cm^2, and so the HXD will be capable of monitoring flares from transient γ-ray sources and γ-ray bursts. The baseline performance of the HXD is summarized in Table 1.

2. ELECTRONIC SYSTEM OF THE HXD

The electronic system of the HXD plays a crucial role in obtaining the best performance of the system. Although a modular configuration is the key to achieving the high sensitivity of the HXD, it requires the system to handle many components. The total number of signal channels extracted from the sensors of the HXD (HXD-S) to be processed is 116 (96 channels for the Well units and 20 channels for the Anti units). A robust and stable electronic system is required to process data from many channels under nominal constraints for a space experiment. Furthermore, the

real time performance of the system is critical to minimize the dead time caused by triggers issued randomly from these channels.

For this purpose, we have developed a new electronic system for the HXD. The system primary consists of the analog electronic system (AE) and the digital electronic system (DE). A schematic diagram of the HXD electronics is shown in Fig. 1. Front electronics such as preamplifiers are mounted in the detector housing. The AE processes analog signals from the HXD-S. The DE receives event data from the AE, formats the data into packets, and sends these packets to the DP. The AE consists of one control board (ACU) and eight signal-processing boards. The latter are broken into the following two types: Well Processing Unit (WPU; four modules) for the WPU unit, and Transient Processing Unit (TPU; four modules) for the Anti units. The ACU controls the power lines and the high voltages of the HXD-S. The temperature of the scintillators and photomultiplier tubes (PMTs) and high voltages are monitored by the ACU. Communication between modules in the AE is made via a series of parallel wires running along the backplane of the AE crate (AE backplane). The DE comprises CPU modules and I/O adaptor boards for communicating with the AE and the satellite data processing system (DP). The data packets sent to the ground station are classified into two categories: the event data of the Well unit received asynchronously from the AE, and the monitor data. The monitor data includes the count rates taken by scalars and the house keeping information of the HXD collected in the AE and the DE.

Table 1. Baseline performance of the HXD.

Energy range	10–700 keV
Energy resolution	~9% (FWHM) @ 662 keV, ~3 keV (FWHM) @ 10 keV
Effective area	230cm^2 (< 40 keV), 330 cm^2 (> 40 keV)
Field of view	0°.56 × 0°.56 (< 100 keV), 4°.6 × 4°.6 (> 200 keV)
Background rate	$\sim (2-5) \times 10^{-5}$ c sec^{-1} cm^{-2} keV^{-1}
Time resolution	normally 61 μsec (minimum 15.3 μsec)

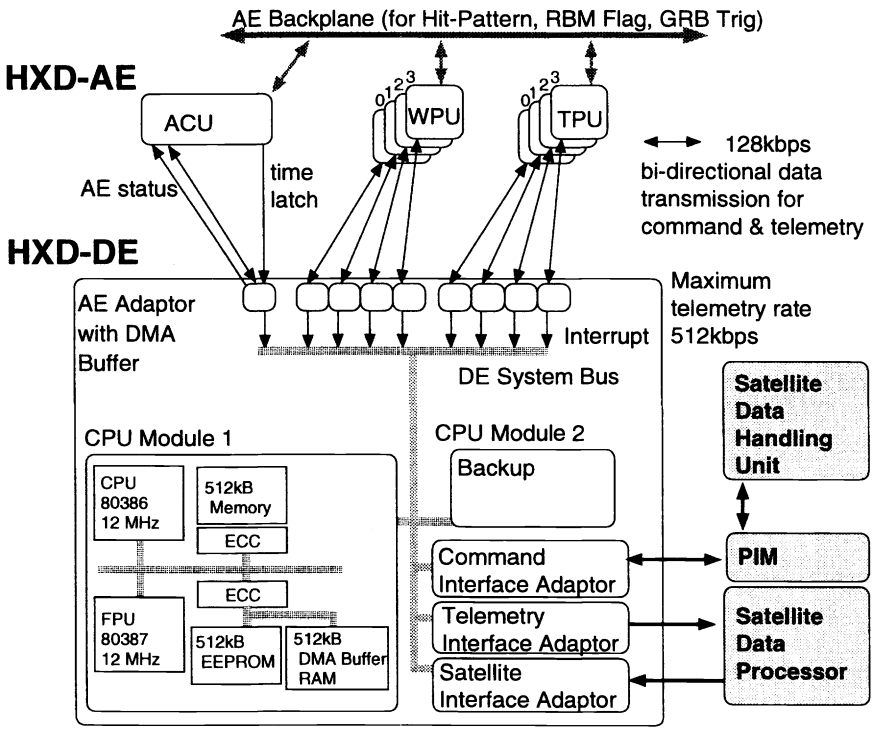

Figure 2. Block diagram of the electronics system. The data flow between the Analog Electronics (AE) and the Digital Electronics (DE) is shown.

The master clock which is used to synchronize the clock system in the electronic system is supplied from the DP to the DE and then distributed to the AE. The commands to the HXD system are transmitted from the Data Handling Unit (DHU) of the satellite to the HXD-DE through the Peripheral Interface Module (PIM). The AE related commands are sent to each of AE boards from the DE independently and decoded by the command decoder in the board. The electric power is supplied from the Power Supply Unit (PSU) dedicated for the HXD. The outputs of the PSU are ± 5V and ± 12V for the analog circuitry, and +5V for digital circuitry.

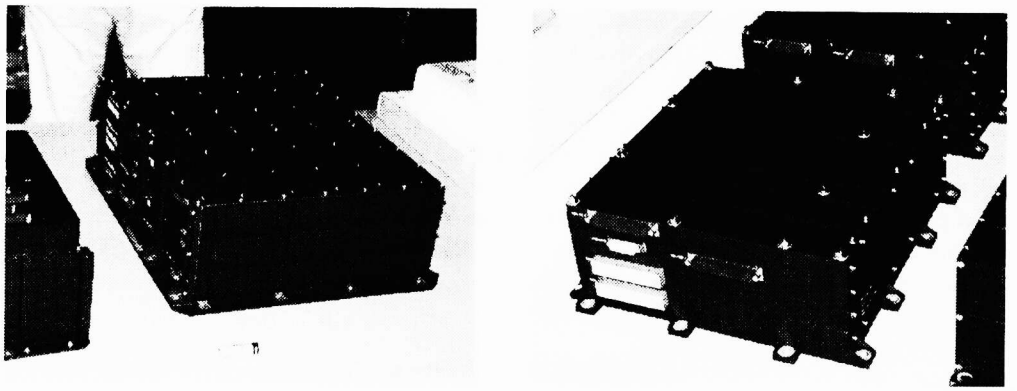

Figure 3. Outlook of the AE Box (Left) and the DE Box (Right)

In order to achieve the high reliability of the system, all parts used in the AE and the DE are carefully selected from qualified parts: ICs are screened by MIL-883 class B specification, transistors are selected from JANTXV, and passive elements such as resistors and capacitors are selected from ER-MIL. The CPU and the interface ICs, which are the most critical elements in the DE, are screened by the MIL-883 class S specification. Special care has be taken to design the circuits with low power consumption. Since the size of the electronic boards has to be minimized, we utilize FPGA with a capacity of 2000 gates (A1020B-1PG84B; from ACTEL), which is one of a few FPGAs that is qualified for use in satellite experiments. The size and power consumptions of the HXD-S, HXD-AE, and HXD-DE are listed in Table 2. The total power consumption of the AE is 25 W and that of the DE is 5 W, respectively. The outlook of the HXD-AE and the HXD-DE are shown in Fig.3.

Table 2. Parameters of HXD-AE and HXD-DE

	AE	DE
dimension	460 × 370 × 142 mm^3	317 × 297 × 118.8 mm^3
weight	18 kg	5 kg
power consumption		
+5 V (Digital)	880 mA	1020 m A
+5 V (Analog)	1034 mA	0 mA
−5 V	1514 mA	0 mA
+12 V	1003 mA	3 mA
−12 V	237 mA	0 mA

3. ANALOG ELECTRONICS

3.1. DATA PROCESSING OF THE WELL UNIT

3.1.1. OVERVIEW

The analog outputs from the Well unit are processed by the front electronics mounted in the housing of the HXD-S and the WPU modules. One WPU module handles four Well units. The last dynode signal of the PMT (Hamamatsu

R6231-07) of the well-type phoswich counter is first fed into the charge sensitive amplifier (CSA) and then fed to the WPU module. The anode signal of the PMT is used as a fast pretrigger that generates gate signals for the pulse shape discrimination (PSD) circuit and the Analog to Digital Converter (ADC) in the WPU. Signals from two layers of PIN diodes are passively summed and extracted from a hole drilled in the well made by BGO and fed into the low noise CSA mounted on the back of the PMT. Since there are four sets of PIN diodes in the Well unit, four outputs from the CSAs are transmitted to the WPU module and subjected to the further pulse processing.

3.1.2. WELL PROCESSING UNIT (WPU)

The functional block diagram of the WPU module is shown in Fig. 4. The WPU consists of the analog processing block, the scalar block, the data transmission block, and the command decoder. In order to minimize the complexity of the circuit, especially for the trigger logic, the analog processing block is functionally divided into four identical blocks, each corresponding to one Well unit. It consists of the pulse processing chain for the well-type phoswich counter and PIN diodes, the trigger logic handling part, and ADCs. The scalar block comprises twenty 16 bit-scalars by FPGAs, for counting the outputs of various discriminators and the dead time of the system. When a trigger is selected as a "Good event" in the trigger handling part from pre-trigger signals, the trigger status flag is set after the completion of the digitization of analog signals by ADCs. The sequencer in the data transmission block polls the trigger status flag in the analog processing blocks, collects the event data and transmits it to the DE through the 9-bit FIFO with a depth of 1 KByte (IDT7202; from IDT) . In order to implement these circuits in the limited space, 28 FPGAs (A1020B) are used to implement components such as sequencers, latches, and scalars in one WPU board.

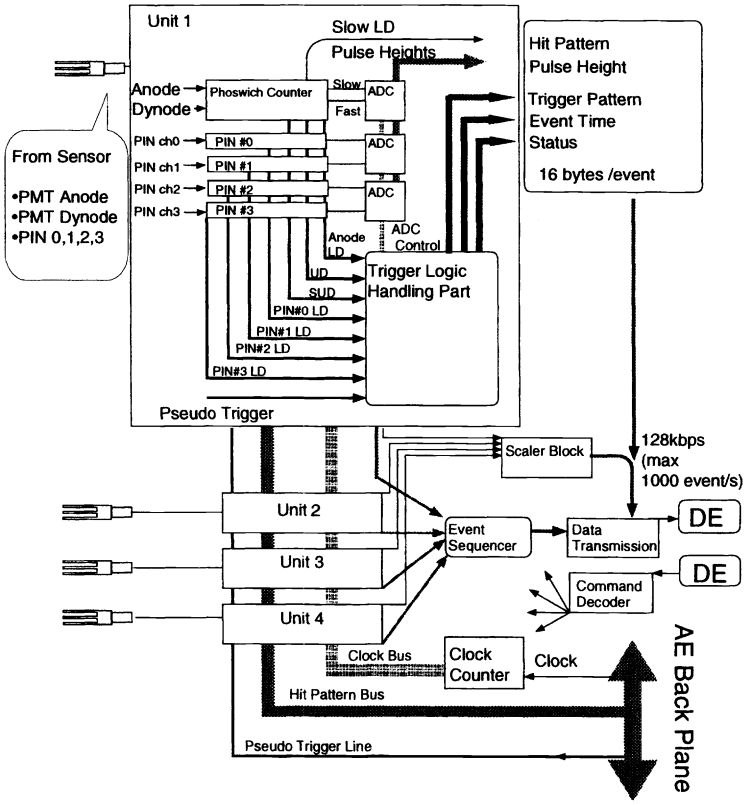

Figure 4. Functional block diagram of the WPU module

3.1.3. FAST CHARGE SENSITIVE AMPLIFIER FOR THE PMT

In order to assure the proper operation of the GSO/BGO phoswich counter and to obtain high energy resolution in the energy range from 40 keV to 700 keV, a preamplifier to handle the fast signal from the GSO scintillator[13] (τ =

86 ns at 20 °C and τ = 122 ns at −20 °C) is required. We have developed a CSA that has a high frequency response and a good linearity as well as a low power consumption. Fig. 5 shows the circuit diagram of the CSA. The CSA is based on an input FET stage cascoded with a bipolar transistor. A J-FET 2SK322, which has high transconductance (g_m) of ∼ 25m siemens, is used as the first stage and a bipolar transistor 2SA1226 is used as the second stage. The drain voltage of 2SK322 is fixed by the base of 2SA1226 to minimize the mirror effect. In order to obtain the high frequency response, as well as the good linearity over a wide dynamic range, a large open loop gain is required. In the CSA, the output stage consists of a emitter follower, which feeds the boot strap loop. Since the open loop gain is proportional to the product of the g_m and the load resistance, the large g_m value of the 2SK322 and the large dynamic load by the boot strap technique provides us the fast response which is sufficient for the spectroscopy by using the GSO scintillator. When we use a feedback capacitance of 100 pF (decay time constant τ=4 μs), the GSO signal of the Well unit by 662 keV γ-lines becomes 0.8 V for the PMT gain of 5×10^5. The power consumption of the CSA is 42.5mW.

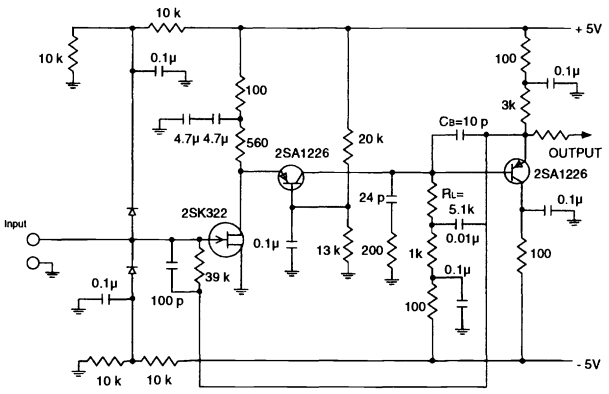

Figure 5. Circuit diagram of the Charge Sensitive Amplifier for the dynode signal of the PMT

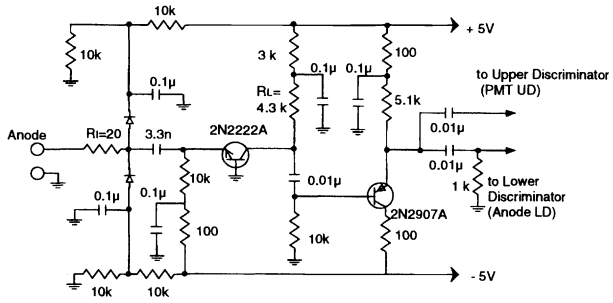

Figure 6. Circuit diagram of the fast amplifier for the anode signal of the PMT. The gain of the amplifier is calculated from thr ratio between R_L and the sum of R_I (20 Ω) and the emitter ohmic resistance (70 ∼ 80 Ω).

3.1.4. PULSE SHAPE DISCRIMINATOR

In the well-type phoswich counter, events that deposit all their energy in the detection part (here, GSO) are selected from events in which X-rays partially/totally lose their energy in the large BGO scintillator. The PSD selects signals with time profiles that are consistent with those of the GSO and rejects those contaminated with slow-decaying BGO scintillation light (τ = 353 ns at 20 °C and τ = 706 ns at −20 °C). Because of the large volume of the shielding scintillator of the Well unit, the counting rate from each unit is anticipated to be on the order of several 100 Hz to several kHz. Most of these events are background events to be rejected. The counting rate of real X-ray and gamma-ray events, which come from the Field of View (FOV) of the detector and deposit their energy only in the detection part (Good event), is as small as a few Hz per unit.

The PSD, employed in the HXD, compares the outputs of two shaping amplifiers with different time constants. With these time constants, the event that hits on the GSO scintillator generates the same pulse heights for two outputs and that of BGO scintillator generates the lower pulse height for the fast shaping amplifier than that for the slow shaping amplifier. The PSD has been developed as a semi-customized LSI to reduce the circuit size and power consumption.[14,15] It comprises two sets of amplifiers and peak hold circuits. The comparator in the LSI compares the output of the peak hold circuits and generates the status flag (PSD_OUT) as an indicator of the events that are contaminated by the signal from the BGO scintillator. The PSD contains a comparator connected from the slow shaping amplifier (SLOW_LD). The power consumption of the PSD LSI is 250 mW.[15,8]

3.1.5. SIGNAL PROCESSING OF THE WELL-TYPE PHOSWICH COUNTER

The signal processing of the well-type phoswich counter is shown in Fig. 7. In the WPU, the output from the CSA is split into two paths : one goes to the slow (τ=1000ns) shaping amplifier and the other to the fast (τ=150 ns) shaping amplifier in the PSD. A simple gain amplifier which utilizes a Digital to Analog Converter (DAC) is used

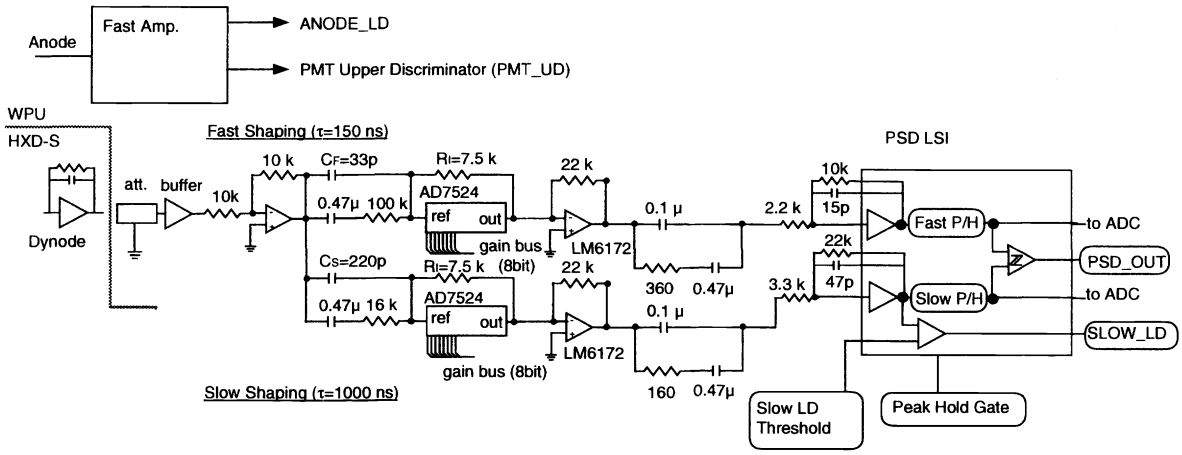

Figure 7. The signal processing of the well-type phoswich counter. We utilize the register ladder in the Digital-to-Analog converter (DAC: AD7524) for the gain amplifier. The gain of the amplifier is controlled by setting 8 bits data of the DAC through the gain bus by a command.

for the pulse-height adjustment. As shown in Fig. 7, we change the gain of the inverting amplifier by selecting the combination of the resistors in the register ladder of the DAC chip. A combination of C_F (or C_S for the slow shaping amplifier), R_I, and the total internal resistivity of the DAC chip (10 kΩ) forms a RC filter in the shaping chain. The gate signals and the reset signals for the peak hold circuits and the reset signal for the comparator are provided from the sequencer (PSD_CNTL) designed in the trigger handling part. The SLOW_LD from the PSD is distributed to the hit pattern bus in the AE back plane to serve as "hit pattern" information for other Well units.

Since the Well unit is operated in the self-trigger mode, the gate signal for the PSD and ADCs has to be generated as quickly as possible. In the HXD, the anode signal is transmitted to the HXD-AE via long coaxial cable (3-4 m). In order to keep fast rise time of the signal from the GSO scintillator, a fast amplifier with low input impedance is necessary before the comparators for the low energy discriminator (ANODE_LD). In addition, the amplifier has to have sufficiently high gain to generate the fast pre-trigger signal stably even for low energy X-ray events of ∼ 40keV. Fig. 6 shows the circuit of the simple amplifier designed for this experiment. The amplifier is a combination of common-base and emitter-follower amplifiers with separate current and voltage amplification. The input impedance of the common-base amplifier is determined by the emitter ohmic resistance of 70 – 80 Ω. By adding the emitter-follower amplifier, a low output impedance, which is sufficient to load the subsequent components of the circuit, is obtained. The gain of the amplifier is measured to be ∼ 40. Despite the simple circuit and low power consumption (12.8mW), a feature of the amplifier is its fast response with a rise time of 15 ns.

One important issue for the design of analog system is robustness against the saturation. When charged particles penetrate through the BGO scintillator, often energy higher than the saturation point of the amplifying system is deposited and may potentially cause some erroneous response in the system. Fig. 8 shows the preamplifier output for a proton of ∼1 GeV/c and that for a 122 keV γ-ray event. In addition to the saturation in the same polarity of the signal, the output of amplifier goes to the opposite polarity before the amplifier baseline is restored to a certain level. Since a new trigger is inhibited during these saturation periods, the PSD output has a possibility to misbehave. As shown in Fig. 7, we install a Super Upper Discriminator (SUD) to detect the saturation and protect the analog system from the mis-operation. As described later, the trigger is inhibited while the SUD is active (see Fig.8).

3.1.6. SIGNAL PROCESSING OF THE PIN DIODES

The energy resolution of the PIN diodes is mostly determined by the electric noise due to the leakage current and the input capacitance. The total input capacitance is the sum of the junction capacitance of two PIN diodes (∼2 × 20 pF) and the capacitance of the cables connecting the diodes to the CSA (∼ 30 pF). Whiles, the leakage current of the PIN diode is ∼ 1 nA each at −20 °C with a bias voltage of 500 V. The CSA for the PIN diode is designed

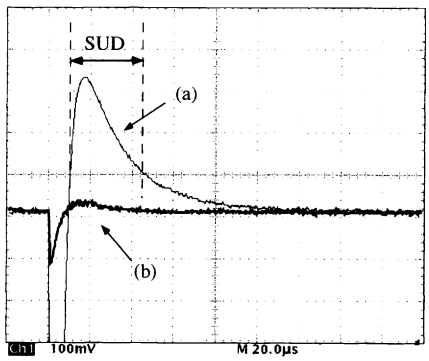

Figure 8. Pulse profiles at the output of a charge sensitive amplifier for the PMT. The pulses by the passage of (a) 1 GeV proton from the accelerator beam and (b) 122 keV line from ^{57}Co are shown. The SUD signal from the Super Upper Discriminator is activated until the baseline of the amplifier is restored. The duration of the SUD is monitored by the dead time counter.

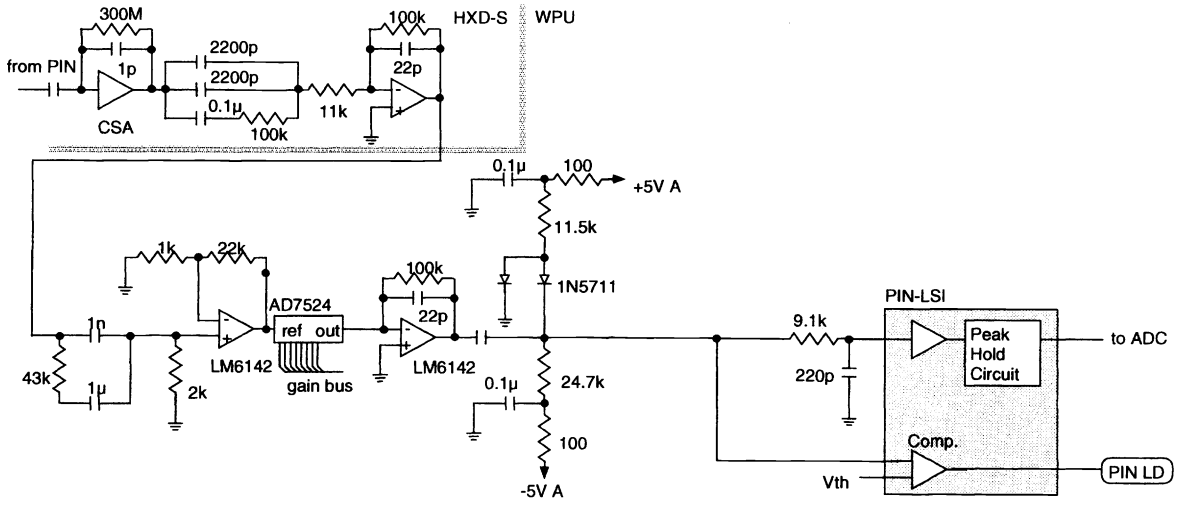

Figure 9. The signal processing of the PIN diode.

for use with a large input capacitance near 70pF by selecting JFET with a large g_m. With use of 2SK322, which has $g_m \sim 25$m siemens, the energy resolution of the PIN diodes is 3~4 keV (FWHM) at -20 °C .

The output from the CSA is passed through a buffer amplifier with a *CR-RC* filter (τ=2μs) and then further shaped by two stages of amplifiers that have *RC* filters with τ=2μs (See Fig.9). A pretrigger signal from the PIN diodes is generated from the discriminator connected to the intermediate stage of the shaping chain. Since as many as 64 channels of PIN diodes need to be processed, the reduction of the size and the power consumption is very important in the AE electronics. We integrated the last step of the amplification, the peak-circuit and the lower discriminator into the PIN LSI.[8] The power consumption of the PIN LSI is 47 mW. As shown in the figure, the simple base line restorer is placed in front of the PIN LSI, to recover the base line after the large signal due to the passage of charged particles in the PIN diode.

3.1.7. TRIGGER LOGIC

The logic diagram of the trigger handling part implemented in the sequencer is shown in Fig.10. It handles pre-trigger signals generated from seven trigger sources: the anode signal of the well-type phoswich counter, the low-energy discriminators for four PIN-diodes, the pseudo event pulse, and the upper discriminators that sense the saturation of the CSA signal of the PMT.

When a pre-trigger is issued from trigger sources, the TRIG signal is activated and the sequencer is inhibited from accepting a new trigger. At the leading edge timing of the TRIG signal, the peak hold gate for the PSD and PIN LSIs are generated. The TRIG signal is then synchronized to the clock for a master sequence of the PSD_CNTL to produce the DELAYED_TRIG signal, which is delayed 4 μs by couting the clock. At the DELAYED_TRIG timing, the output from the PSD is verified. If the PSD_OUT signal indicates that the event is contaminated with the signal from the BGO scintillator, the event is rejected as a background event and the sequencer goes back to the initial state. Fig. 11 shows the results of the event selection by the PSD. As shown in Fig. 10, the upper discriminator of the anode signal and the super upper discriminators are also used for the selection of events.

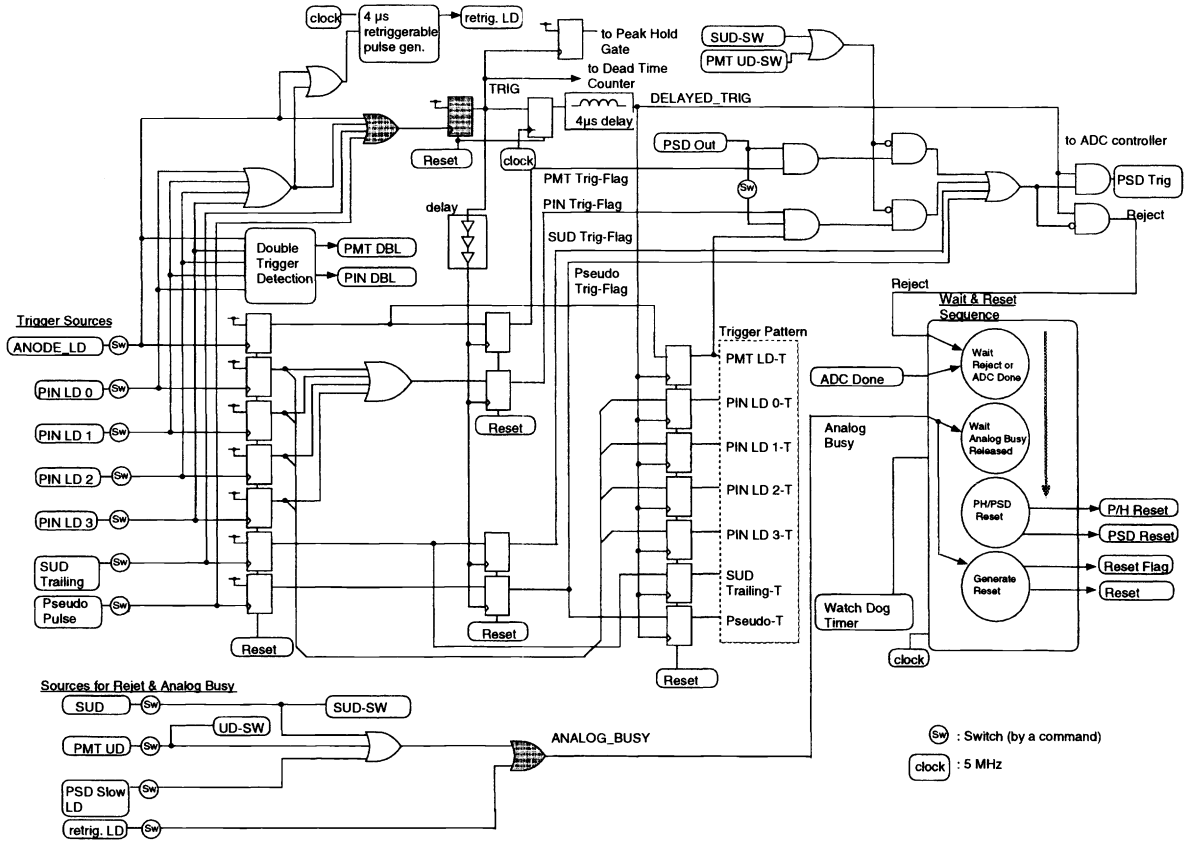

Figure 10. Logic diagram of the sequencer PSD_CNTL, which handles the trigger logic for the Well Unit.

When the trigger conditions are satisfied, all analog outputs from the corresponding Well unit (those of the slow shaper, the fast shaper, and the four diode shapers) are digitized by 12 bit ADCs (ADC12062 MW/883; from National Semiconductor). For the signal of the PIN diodes, the upper 8 bits are used, because the dynamic range of the PIN diode is small (10 – 80 keV). Also recorded are the existence of any hits in the seven trigger sources in the Well unit (trigger pattern) and any hits in the 16 Well units and 20 anti-counters (hit pattern). Because of the high counting rate of pre-triggers, the rejection of pile up events is important. The implementation of the pile-up detection circuit and its performance is presented in the accompanying paper.[16] The output of the PSD, flags to monitor the pile-up events, and the upper discriminator outputs are also recorded. Event arrival times are recorded with a resolution of 61 μs in the normal operation mode. The higher resolution of 15.3 μs can be selected by a command (Fast mode) but this requires the high telemetry rate for the HXD. The data format which is sent to the DE on an event-by-event basis is listed in Table 3.

The sequencer starts accepting a new event after the event data is sent to the FIFO. The outputs from the SUD, the PMT UD, the SLOW_LD, and the ANODE_LD are ORed to form the ANALOG_BUSY signal. Before the

Table 3. WPU Event Data. 16 bytes of data is sent to the DE on an event-by-event basis.

Channel ID	2 bit
Event Time	19 bit
Phoswich Counter Slow Pulse Height	12 bit
Phoswich Counter Fast Pulse Height	12 bit
PIN detector 0 Pulse Height	8 bit
PIN detector 1 Pulse Height	8 bit
PIN detector 2 Pulse Height	8 bit
PIN detector 3 Pulse Height	8 bit
Trigger Pattern	7 bit
PIN LD Trig	1 bit
Hit Pattern	36 bit
PSD Out	1 bit
PMT UD	1 bit
PIN UD	1 bit
PMT Pile-up Flag	1 bit
PIN Pile-up Flag	1 bit
Reset Flag	1 bit

sequencer generates the RESET signal, it polls the ANALOG_BUSY signal to make sure that the baseline of the amplifiers are restored. The minimum processing time of the event is 11.2 μs for the accepted events and 6 μs for the rejected event.

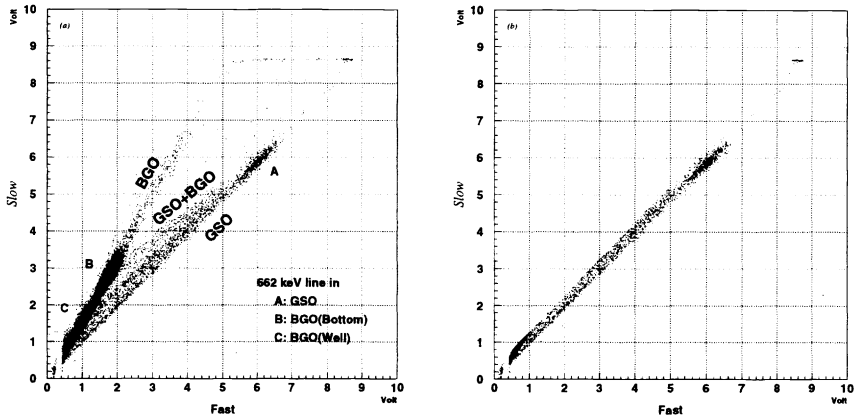

Figure 11. Correlation between the fast and slower shaper outputs (τ = 150 ns and 1000 ns) obtained by the Well unit at -20 °C with the pre-flight model of the WPU module: (a) without and (b) with the selection by the PSD_OUT signal of the PSD LSI. In (b), one can see that GSO events are selected out cleanly.

Measuring the deadtime is one of the most important tasks of the electronic system, because the spectrum from a celestial objects is obtained by subtracting the back ground spectrum from the observed spectrum. The precise value on the observation time is required for the proper subtraction, especially for faint source observations, in which the signal to noise ratio is very low. The deadtime measurement is done individually for each Well unit by sampling the inhibit signal at a frequency of 10 MHz (selectable by a command); a dead time counter is incremented for each sample which indicates that the trigger is inhibited. The deadtime counters are filled in the monitor data and sent to the DE every second.

Another means to estimate the dead time is the pseudo event pulse. The pseudo event pulse is generated periodically with a selectable period in the ACU module. As shown in Figs.4 and 10, the pseudo event pulse is fed

into the trigger handling block and activates the trigger logic in the same way as other trigger sources, but with a specific mark in the trigger pattern. When we compare the total number of the injected pseudo pulses and number of recorded events, we can estimate the fraction of the dead time.

3.2. DATA PROCESSING OF THE ANTI UNIT

3.2.1. OVERVIEW

The anode signal of the PMT (Hamamatsu R3998-01) of the Anti unit made by BGO scintillator is fed into the emitter follower (EF) circuit mounted directly on the back of the PMTs in the HXD-S housing. It is then processed by the TPU module. One TPU board processes five Anti units. Primary function of the Anti units and the TPU are to provide signals for the lateral anticoincidence shielding for the Well unit. In addition to this, the HXD has a capability to measure the summed energy spectrum from the Anti units.

3.2.2. TRANSIENT PROCESSING UNIT (TPU)

Figure 12 shows the schematic diagram of the TPU module. In the TPU, the signal from the EF circuit is fed into a C-R filter and then to the gain amplifier to adjust the pulse height. Its output is divided into two: one goes to the discriminator (MAX913; from Maxim) and the other goes to the summing amplifiers (LM6172; from National Semiconductor) with a R-C filter ($\tau = 1\mu$s), via analog switches. Whiles the outputs of discriminators are distributed to the WPU modules via the "hit pattern" bus in the AE backplane. The output of the summing amplifier signals is sent to a pulse height analyzer (PHA) block.

In the PHA block, gamma-ray events from 100 keV to 2 MeV are accumulated into 54-channel spectra (PH Data) at selectable time interval in the range between 512ms to 4s (in the normal operation, it is set at 512ms). The PHA block consists of a 6-bit FADC (CA3306; from Halis), a peak detection circuit and FPGAs that handles triggers and controls the accumulation of the spectrum into memory. The conversion of the pulse and the accumulation of the pulse height information into a histogram takes 10 μs. This corresponds to the maximum count rate of 100 kHz. As similar to the WPU, the pseudo event trigger is injected in the trigger control circuit in the PHA block. By measuring the live rate of the pseudo events, the deadtime can be estimated.

In order to monitor the background environment of the HXD, the discriminator outputs distributed on the hit pattern bus are counted in the TPU. Nine 16 bit scalars are implemented in the TPU modules; five scalars count pulses from the Anti units and four scalars count pulses from the Well units. 144 bytes of the transient data, which primary consists of the spectrum acquired in the PHA block and the scaler outputs, is transmitted to the DE every second.

3.2.3. GAMMA-RAY BURST MONITOR

In addition to the PH data, the PHA block produces high time resolution rate samples in each of the four energy band. The highest sample rate provides a resolution of 1/64 s (TH data). Both the TH and the PH data are recorded in the circular buffer with a size of 64 KByte in the TPU module. When the GRB Monitor detects the significant increase of the event rates, it sends the GRB trigger signals to all TPU modules via the AE back plane. If the multiplicity of the GRB triggers from four TPU modules exceeds the selected value, the GRB flag handling block waits 112 s after the trigger (for the normal operation) and stops the recording into memory. The memory preserves the TH data and the PH data prior to the trigger for 16 s. The burst data is transmitted to the DE on request.

3.2.4. RBM MONITOR

In order to prevent damage to the photomultipliers, the high voltages (HVs) of PMTs in the HXD-s are turned off, before the satellite goes into the South Atlantic Anomaly (SAA) region, where the fluxes of charged particles are high. Although this operation will be done by a command prepared for the daily operation, the automatic shutdown procedure have to be prepared for the emergency, such as mis-operation. An alarm signal is generated form a Radiation Belt Monitor (RBM) circuit in the TPU. In the RBM, the event rates of the Anti unit located at the corner of the HXD-S are monitored by the scalar in the RBM. When the count rate exceeds the selectable threshold level, the RBM flag is set and the information is sent to the ACU module, via the AE back plane. When the ACU receives the alarm signals from one of the TPU modules, it automatically shuts down the high voltages for the PMTs.

4. DIGITAL ELECTRONICS (HXD-DE)

4.1. OVERVIEW

The base line requirement of the HXD electronic system is to acquire data without loss from sources with brightnesses of several times of that of the Crab Nebula. For the DE, this corresponds to an acquisition rate of 4,000 events per second. In order to achieve this high acquisition rate with limited hardware resources, we use a fast real time operating system, specially designed for this experiment, in conjunction with a circuit capable of receiving data by the Direct Memory Access (DMA) mode. In the DMA mode, the I/O adaptor accesses the DMA buffer directly, without communicating with the CPU, when it sends or receives data.

The DE is designed to provide: (1) the primary interface with the satellite data processor for command and telemetry, (2) control to the acquisition and formatting of the data from the AE, and (3) reaction to events such as γ-ray bursts. As shown in Fig. 2, the DE is based on a CPU 80C386 running at 12 MHz. There are two CPU boards in the DE, with one board allocated for backup purposes. Mounted on the board are 512 KB of SRAM for the work area of the program, 512 KB of SRAM for the DMA buffer, and 512 KB of EEPROM for the storage of the program.

Communication between AE and DE is made through bi-directional data transmission lines with a band width of 128 Kbps using a 4050 LSI. The maximum data transmission from the AE is thus limited by this band width and corresponds to the rate of 1,024 events per WPU board. When the I/O adaptor for the Well board receives data, the DMA transfer is invoked, on an event by event basis. The data is then stored in a circular buffers with 1,024 bytes. Two circular buffers, A and B, are prepared for each WPU module to form a double buffer system. When the buffer is filled with event data, the write pointer moves to the other buffer and the interrupt signal to the CPU is issued. The CPU load due to the frequent interrupts is significantly reduced by this method. In the normal operation, the data for 64 events are blocked for each WPU board.

The DE is connected to the DP via a bi-directional serial transmission line with a speed of 512 Kbps using a combination of 26C31 and 26C32 interface ICs for the RS422 data transmission. The DP notifies the maximum data

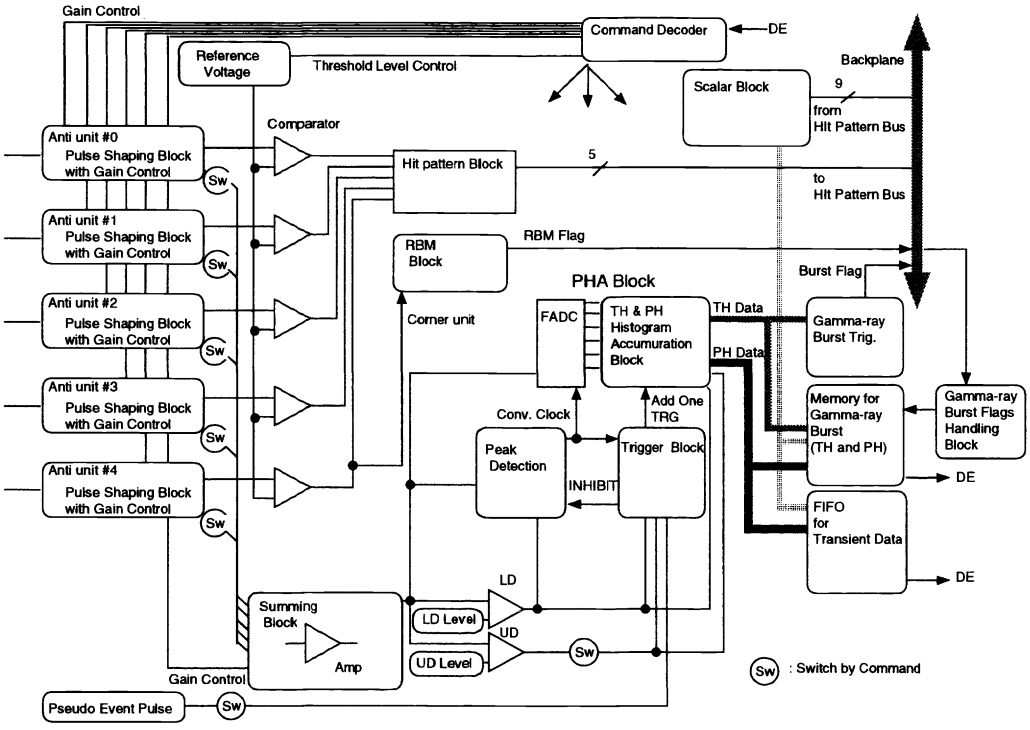

Figure 12. Schematic functional diagram of the TPU module

size to be sent in certain periods. Data transmission speed for the HXD is 6-12 KB/s for contact orbits and 3 – 6 KB/s for remote orbits.

4.2. CONTROL

The software of the DE is organized into 15 processes running concurrently under the real time OS. These processes perform various tasks such as receiving commands, accumulating house keeping information, formatting packets, and sending packets to the DP. Among them, the process called CONTROL_TASK and the interrupt handlers are the central part that control the data processing in the DE. The CONTROL_TASK is activated automatically every 31.25ms. It checks the time table by using the internal clock counter and activates the corresponding processes. The interrupt handlers are activated by interrupt signals from I/O adaptors. When it receives the interrupt signals, it activates the processes such as a process that copies data from the DMA buffer. The communication between tasks are based on the shared memory. When the process is activated, it reads information from the corresponding area in the the shared memory and performs its task. The processes go into the sleep mode, when the task is done.

In order to prevent the malfunction of the DE system due to the bit errors by the irradiation of charged particles in the space, the process called Memory-Patrol is always running to verify the contents of memory byte by byte.

Table 4. Correspondence between AE data and telemetry packet

board	AE data name	output(VCID:APID)	transfer period (SH/H/M/L)
ACU	ACU data	HK Status (2:520H)	2/4/8/32 s
		ACU HK data (5:123H)	1/2/4/16 s
WPU	Monitor data	HK Status (2:520H)	2/4/8/32 s
		Scalar (5:124H)	1/2/4/16 s
	Well Event data	Well Event(5:130–133H)	depends on DMA setup
		Histogram (5:129–12EH)	depends on PI program setup
TPU	Transient data	HK Status (2:520H)	2/4/8/32 s
		Transient (5:122H)	1/2/4/16 s
	Gamma Burst data	Gamma Burst (5:126H)	1/2/4/16 s at maximum

4.3. PI PROGRAM

The process called "PI program" is an important addition to the HXD electronic system to realize the high throughput while keeping the low background capability. It is software to filter out the background events that leak through the selection in the WPU and to condense the transient data sent from the TPU. It is particularly important when the telemetry band width is limited (during remote orbits) during the observation of a bright source. Additional tasks are to collect calibration data and to notify the gamma-ray burst trigger to the TPU. The PI program is activated when the data arrives from the DMA buffer with the type of the data as input. According to the type of data, the main routine of the PI program calls the corresponding function that handles the data.

Although the selection by means of the PSD in the WPU is very powerful, the PI program features very flexible ways in selecting events.The PI program does the event selection in several different algorithms. The methods of the selection can be chosen by commands. The information and the algorithms used in the PI program include:

hit pattern The program selects events by using hit pattern information of the surrounding units, rejecting Compton scattered events and particle interaction events.

pulse shape In the AE, the pulse shape discrimination is performed by comparing the pulse height of the slow and fast shaping amplifiers of the phoswich counter. In the DE, the selection can be done more flexibly by the formula implemented in the program.

delta-t It is reported that some in-organic scintillator, such as CsI(Tl),[10,17] a train of pulses with random shapes during 400μs - a few ms occur when there is a large energy deposit (at least E$\geq$60 MeV) in the crystal. This leads to a number of fake triggers in a very short time. In the case for this kind of events occur in the HXD, the PI program has a capability to remove pairs of events that arrive within the very short time intervals.

5. SUMMARY

The electronic system of the HXD is the key to extract the best performance of the *Astro-E* HXD. We have developed a robust, fast and stable electric system. The sensitivity of the HXD for point sources, calculated from these background levels, is substantially higher than any other past mission in energy band from 10keV to several 100keV.[5] We therefore expect to detect and study many new cosmic hard X-ray point sources. The first end-to-end test of the satellite is underway at the time of writing, leading to a launch in early 2000.

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