NUCLEAR SCIENCE AND TECHNIQUES

Test system of the front-end readout ASIC for the WCDA in LHAASO*

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The Water Cherenkov Detector Array (WCDA) is an important part of the Large High Altitude Air Shower Observatory (LHAASO), which is in the R&D phase. The central scientific goal of LHAASO is to explore the origin of high energy cosmic rays of the universe, and to push forward the frontier of new physics. To simplify the readout electronics of WCDA, a prototype of the front-end readout ASIC is designed based on the Time-Over-Threshold (TOT) method to achieve Charge-to-Time Conversion. High precision time measurement and charge measurement is necessary over a full dynamic range (1∼4000 photo electrons (P.E.)). To evaluate the performance of this ASIC, a test system is designed. This system consists of the front-end ASIC test module, digitization module and the test software, the first module needs to be customized for different versions of the ASIC, while the digitization module and the test software are general purpose. In the digitization module, a Field Programmable Gate Array (FPGA) based Time-to-Digital Converter (TDC) is designed with a bin size of 333 ps, which also integrates Inter-Integrated Circuit (I^2C) for configuration of the ASIC test module, as well as the Universal Serial Bus (USB) interface to transfer data to the remote computer. The test results indicate that the time resolution is better than 0.5 ns; while the charge resolution is better than 30% RMS @ 1P.E. and 3% RMS @ 4000 P.E., which is beyond the application requirement.

Keywords: Time and Charge measurement, Photomultipliers tube (PMT), WCDA, I^2C, ASIC, test system

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I. INTRODUCTION

A. Background & Physical objective

The Large High Altitude Air Shower Observatory (LHAASO) oriented to study and observation of the high energy cosmic rays of the universe. It consists of several detector systems: a 1 km^2 complex array (KM2A); a Wide FOV Cherenkov Telescope Array (WFCTA); a 100 m^2 high threshold core-detector array (SCDA) and a 90000 m^2 Water Cerenkov Detector Array (WCDA)[1].WCDA is one of major components of the LHAASO project[2, 3], which consists of four 150 m $\times$ 150 m water ponds. As shown in Fig. 1, each pond is subdivided into 30 $\times$ 30 cells, each cell with one photomultiplier tube (PMT) looking up at the bottom center to collect the Cherenkov light produced by the shower particles in water[4].

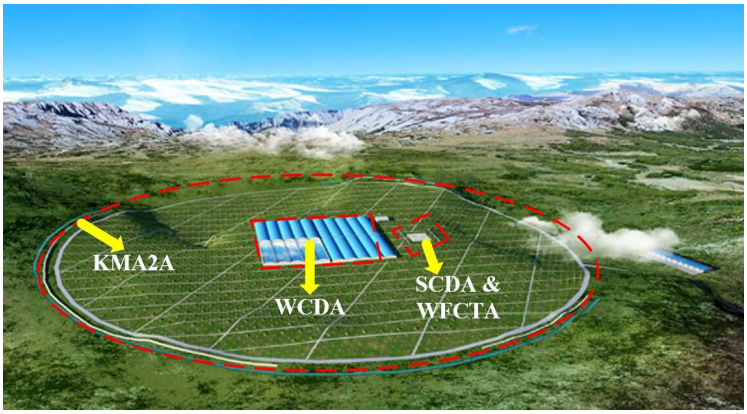


Fig. 1. WCDA in LHAASO project

Fig. 2 illustrates an air shower detected by the PMTs in the WCDA. The kernel task of the WCDA includes two parts: through the time measurement of secondary particles, the incidence direction of the air shower can be determined; though charge measurement, particle identification (PID) and energy information can be obtained.

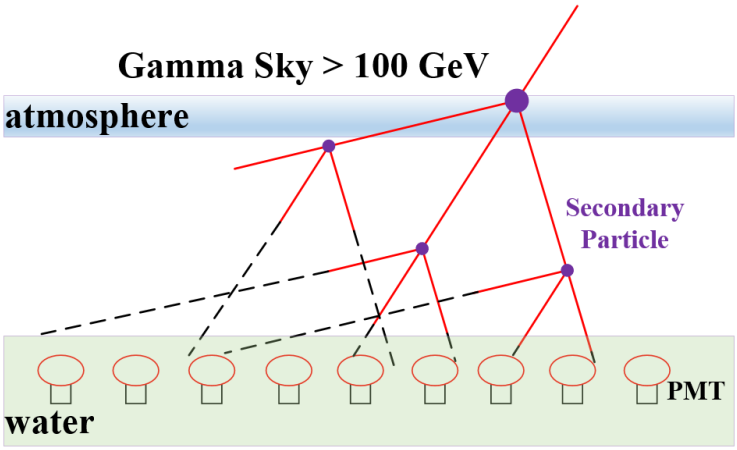


Fig. 2. Block diagram of the Gamma ray detected by the PMT

B. Requirements

According to the physics requirement and the performance of the detectors, the performance of the readout electronics is required in table 1. To target the research purpose, both the amount of the Cherenkov light (corresponding to the charge information of the PMT output signal) and its arrival time on the PMTs need to be efficiently measured. The amplitude of the smallest signal (1 P.E. (photo electron)) is as low as 60 μA, with a leading edge of 4 ns, and a trailing edge of 16 ns. And a large dynamic range from 1 P.E. to 4000 P.E. (0.75 pC to 3000 pC) is required.The detailed requirements of the readout electronics

for WCDA are listed in table 1.As for charge measurement requirement, it is equivalent to an ENOB of around 13.3 bit of ADCs.

Table 1. Measurement requirement of the WCDA readout electronics

item	requirement
channel number	3600
bin size of time measurement	< 1 ns
RMS of time measurement	< 500 ps
dynamic range of charge measurement	S.P.E. $\sim$ 4000 P.E.
charge measurement (relative resolution)	3% RMS @4000 P.E., 30% RMS @ S.P.E.

To simplify the structure of the FEE, a front-end readout Application Specific Integrated Circuit (ASIC) is designed. The PMT signal is imported to the leading-edge discrimination circuit for time measurement, and meanwhile converted to a pulse width for Charge-to-Time Conversion based on the Time-Over-Threshold (TOT) method. To evaluate the performance of this ASIC, a test system is designed, which will presented in the following sections.

II. ARCHITECTURE OF THE TEST SYSTEM

Shown in Fig. 3 is the structure of the WCDA readout electronics. To achieve a large dynamic range, signals are read out from the Anode and Dynode of PMT. The anode channel in the ASIC covers range from 1 P.E. to 100 P.E., while the Dynode channel covers a range from 40 P.E. to 4000 P.E. The signal is input to the discriminator of the ASIC for time measurement, and converted to a pulse width through Charge-to-Time Converters (QTC) based on current mode linear discharging method. With the FPGA based TDC, time and charge information can be digitized simultaneously. The measurement results are packaged based on the TCP/IP (Transmission Control Protocol / Internet Protocol) standard and then sent through the GTX (GTX Transceiver) and optical transceiver to CDTM (Clock & Data Transfer Module) for data accumulation, and finally transferred to the DAQ (Data Acquisition) for data analysis.

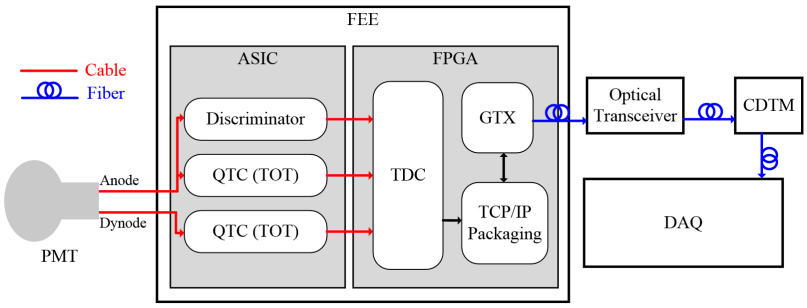


Fig. 3. Block diagram of the WCDA readout electronics (one channel)

Shown in Fig. 4 is the block diagram of one channel of the prototype ASIC. In the ASIC, the signals from the Anode and Dynode are converted to a pulse width ("Q_puse" in Fig. 4 and Fig. 5, which corresponds to the input signal charge information; the Anode signal is also fed to the discriminator in the ASIC for time measurement, the output is marked as "T_pulse" in Fig. 4 and Fig. 5. In the current version, a total of two channels are integrated in a 3 mm $\times$ 3 mm block with 0.35 μm CMOS technology. After confirming the basic functionality and performance through the current version, more channels will be integrated in the following versions of the ASIC.

To evaluate whether the performance of the chip can achieve the target of the experiment, systematic tests must be conducted. To accommodate the test of different versions the ASIC[5] designed, a test system is designed.

As shown in Fig. 5, the whole system consists of three parts: the front-end module, digitization module and the test software. The ASIC under test is placed on the front-end module with power supplies and I/O connectors. This module should be accustomed for different ASIC versions, while the digitization module can be designed for general purpose, which import signals from the ASIC module and integrates the Time-to-Digital Converter (TDC) in one Field Programmable Gate Array (FPGA) for time digitization, as well as the Inter-Integrated Circuit (I^2C) interface logic for the configuration of the ASIC, Universal Serial Bus (USB) interface for data readout, etc. The test software is designed based on Visual C++ for data readout and hardware configuration. Considering the simple structure of the ASIC module, this paper focuses on the digitization module and the test software, which will be presented in the following sections.

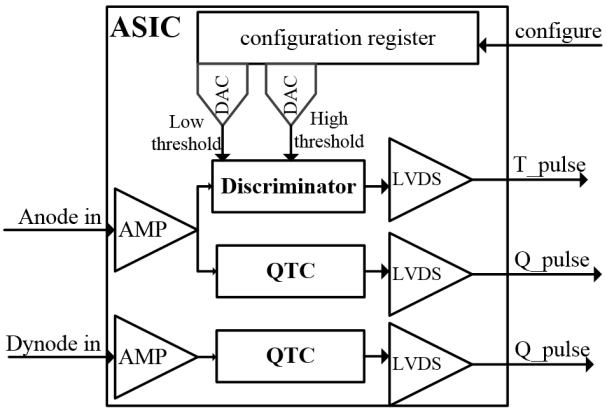


Fig. 4. Block diagram of the ASIC (each channel)[5]

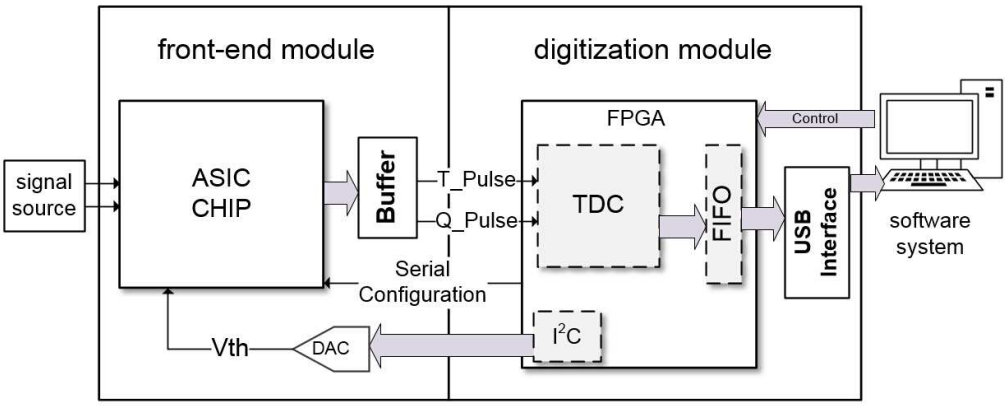


Fig. 5. Block diagram of the test system. Mainly consists of front-end module, digitization module, and the test software.

III. STRUCTURE OF THE TEST MODULE

A. Serial interface logic design for ASIC configuration

The I^2C protocol is widely used in ASIC configuration, considering its following advantages: validity of data transfer is guaranteed by the acknowledgement process; different registers can be accessed by addresses, and all I^2C devices are designed to be able to communicate together on the shared two-wire bus, i.e. featuring a simple structure[6].

We designed an I^2C interface logic to configure the ASIC chip and other peripheral devices on the front-end module. The structure of the Algorithmic State Machine (ASM) figure is shown in Fig. 6. The logic is designed with Verilog HDL (Hardware Description Language) on Quartus II 13.1, and running in an ALTERA FPGA (EP3C55F780).

To confirm the logic functionality, we conducted simulations. Shown in Fig. 7 are the functional simulation results of the three wire signals, including the serial data (SDA, containing addresses and data), serial clock (SCL), and the write start (WR) signal, which concord with the expected. As shown in Fig. 7, A HIGH to LOW transition on the SDA line while SCL is HIGH acts as a START signal, while a LOW to HIGH transition on the SDA line while SCL is HIGH acts as a STOP signal. The receiver is obliged to generate an acknowledge ("Ack1, 2, 3, 4" in Fig. 7) after each byte is received. In Fig. 7, a total of four bytes are successfully transferred in the simulation. The first byte contains the address of the receiver, while the following three bytes include the user command and data information.

B. Time-to-Digital Converter integrated in the FPGA

To digitize the output signals from the ASIC chip, we designed TDC which is based on a FPGA and time interpolation method[7]. Compared with ASIC based TDC, the FPGA based TDC reduces the system complexity while providing a good flexibility[8], since the TDC and the control logic, as well as the data transferring interface can be integrated within one single

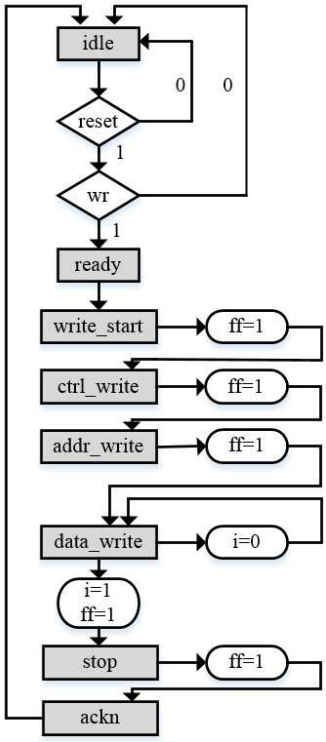


Fig. 6. ASM figure of I^2C interface

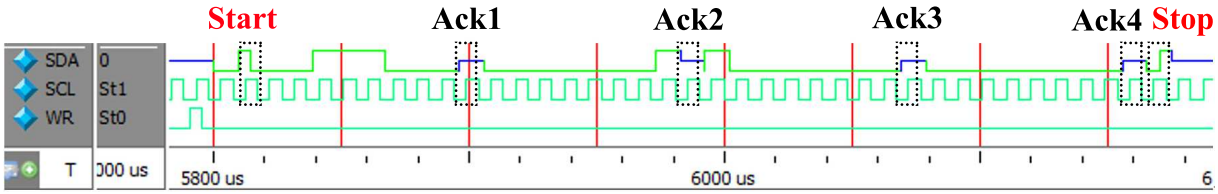


Fig. 7. Simulation result of I^2C timing diagram. SCL (serial clock), WR (write start), SDA (serial data containing addresses and data). The SCL and SDA is the shared two-wire bus

FPGA device. The designed logic about TDC is implemented in an ALTERA FPGA (EP3C55F780), while the synthesis result of the logic (one channel of TDC) shows that only 469 LEs (logic elements) are used.

Fig. 8 shows the block diagram of this TDC. It consists of a coarse-time counter and a fine-time measurement stage. The coarse counter is used to record the high bits of the time measurement result, with a clock (CLK_SYS) frequency of 62.5 MHz. The fine-time measurement is used to obtain the low bits, with 8 clock (fanned out by interval PLL with a 45°phase interval) a frequency of 375 MHz, which is equivalent to 3 GHz. The 26-bit coarse counter achieves a measurement range of 1.0737 second, while the 6-bit fine measurement corresponds to the TDC bin size of 333 ps. The encoded 6-bit fine-time measurement result and 26-bit coarse counter output constitutes a final 32-bit time measurement result, which is read out by a FIFO.

Tests were conducted to evaluate the TDC performance, as shown in Fig. 9. The “cable delay test” method was used[9, 10]. A signal source Tektronix AFG3252 generates two synchronized output signals (3.3 V CMOS level standard, 10 kHz frequency), which are imported two TDC channels in the FPGA[11]. By analyzing statistically the time interval of the two TDC channels’ output, the time resolution of single channel can be obtained by dividing the RMS of the time interval by $2^{1/2}$.

A typical histogram of time measurement result is shown in Fig. 10, with a RMS of 85 ps.

In fact, the RMS test results consists of two parts: one comes from the noise of the circuits, and the other is contributed by the quantization error. When the time interval between the two input signals in Fig. 9 changes, the RMS contributed the quantization error varies in a certain pattern, which is well described in Eq. (1).

$$\sigma = T_o\sqrt{c/T_o(1-c/T_o)} \tag{1}$$

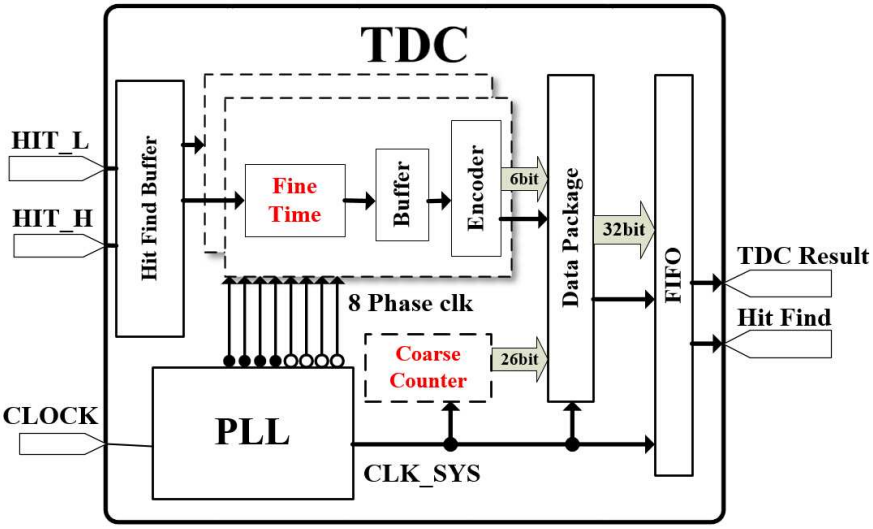


Fig. 8. TDC design in the FPGA. 6-bit 'Fine Time' and 26-bit 'Coarse Counter' constitutes a final 32-bit time measurement result (with a 1.0737 second dynamic range and 333 ps bin size)

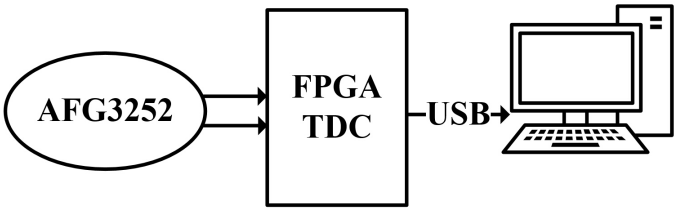


Fig. 9. TDC test platform setup based on the "cable delay test" method.

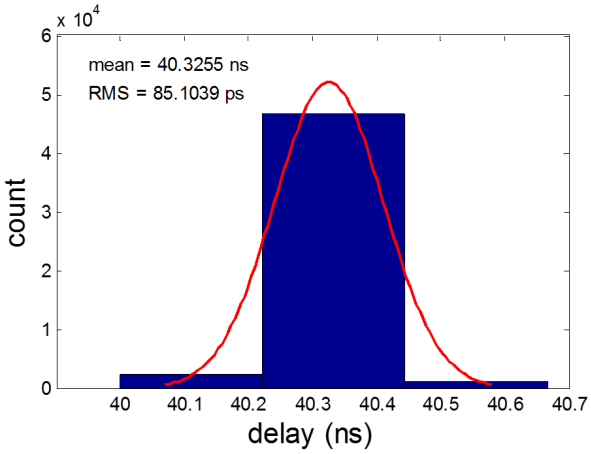


Fig. 10. Normal curve fitting of the test data

T_o is the bin size of the TDC, c is the remainder of T_o from time interval, and σ refers to the RMS result. To accurately evaluate the TDC performance, we changed the time interval and conducted a series of tests, with the results shown in Fig. 11. A characteristic relationship can be clearly observed[13], which agrees well with the expected (marked with dotted line in Fig. 11) and a time resolution (RMS) no worse than 0.5 LSB (166 ps) is obtained[14].

Characterization of the differential non-linearity (DNL) and integral non-linearity (INL) was performed based on the "code density test" method[15]. The code density is the number of times that every individual code has occurred[8]. When the input signal is uncorrelated with the TDC clock, with a big amount of data statistics, the count on each code corresponds to the bin width of that code, and then the DNL and INL can be calculated. Because there are 48 bins in each cycle of the CLK_SYS,

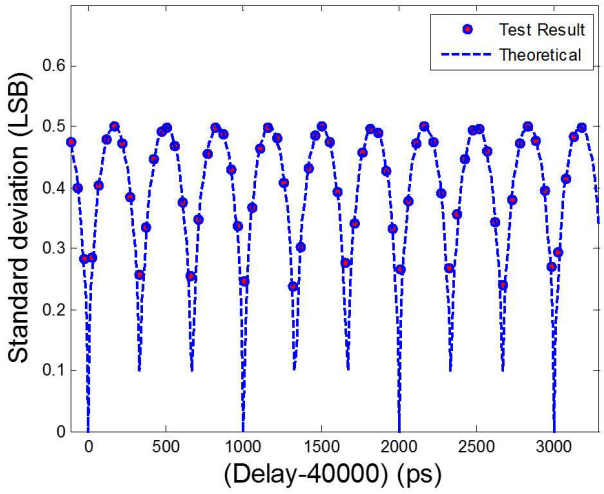


Fig. 11. 8 Phase 6 Frequency doubling of 62.5 MHz FPGA based TDC result. Plots of the relationship between RMS and the mean values of the time interval.

the nonlinearity is periodic corresponding to a repeating pattern of every 48 bins. The DNL and INL test results are shown in Fig. 12, which indicate that the DNL and INL are both better than $\pm$ 0.2 LSB.

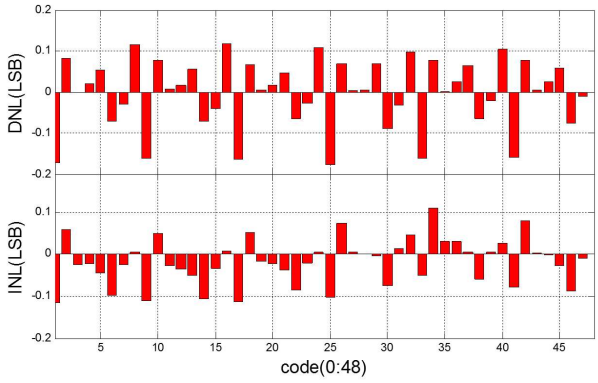


Fig. 12. DNL and INL under 333 ps FPGA based TDC. The DNL is in the range of -0.2 to +0.15 LSB. while the INL is in the range of -0.15 to +0.15 LSB.

C. USB interface for data readout

A standard USB 2.0 interface is integrated in the test system to transfer the test data to a remote computer. As shown in Fig. 13, single-chip integrated USB 2.0 transceiver (CY7C68013A) is used. In this work, the chip was programed as 16-bit data interface, and end-point 2 (EP2) was programed to transfer the command form PC to FPGA, while the EP6 was programmed to transfer the test data from FPGA to PC[16]. A FIFO (1024 words depth, 32-bit input width and 16-bit output width) was integrated in the FPGA to communicate with USB. To read out the data through this USB interface, we also designed a test software based on Visual C++ (details will be presented in the following sub-section), with the USB driver embedded in it.

D. Test software

Frame of the software is shown in Fig. 14, which contains there independent threads. The “control thread” sends commands to FPGA in the Digitization Module, while the “status display thread” monitors system status in real-time, and the “data interface thread” stores the data to the hard disk.

The GUI (Graphical User Interface) of this software is shown in Fig. 15, which contains all necessary functionalities.

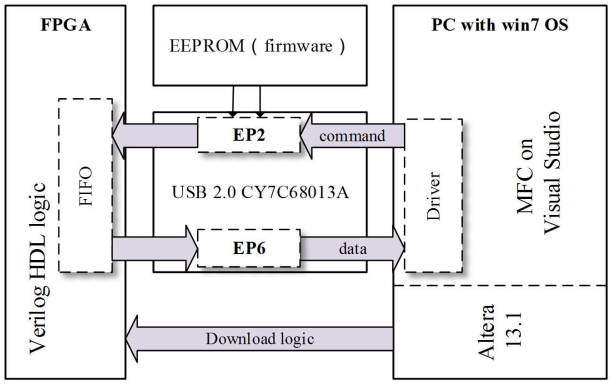


Fig. 13. USB 2.0 based data acquisition. CY7C68013A is used to connect the FPGA and remote PC with a data rate of 240 Mbps.

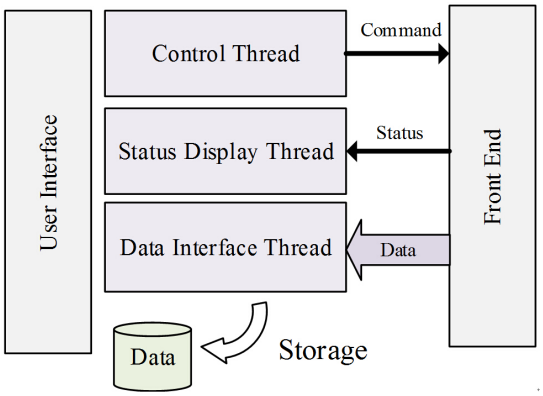


Fig. 14. Software frame. Three threads are running parallel. To achieve the data acquisition.

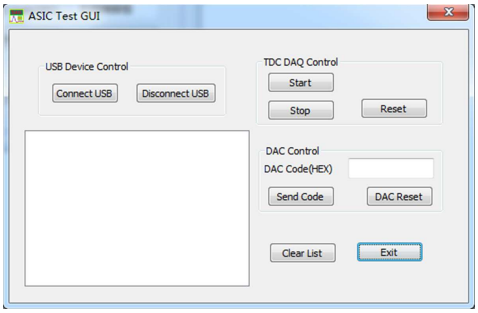


Fig. 15. Graphical user interface of the test system

IV. TEST RESULTS

To confirm the functionality of this test system, we conducted tests on real ASICs in the laboratory. The test system is set up as shown in Fig. 16, which consists of a power supply, a signal source (Tektronix AFG3252), an oscilloscope (LeCroy 104 MXi), and the front-end module & the digitization module presented in previous sections.

A. Functionality test

The ASIC functionality test was conducted by observing the transient waveforms of the critical points of the ASIC with the oscilloscope, as shown in Fig. 17. These waveforms concord well the simulation results of the ASIC, which indicate the ASIC functions well.

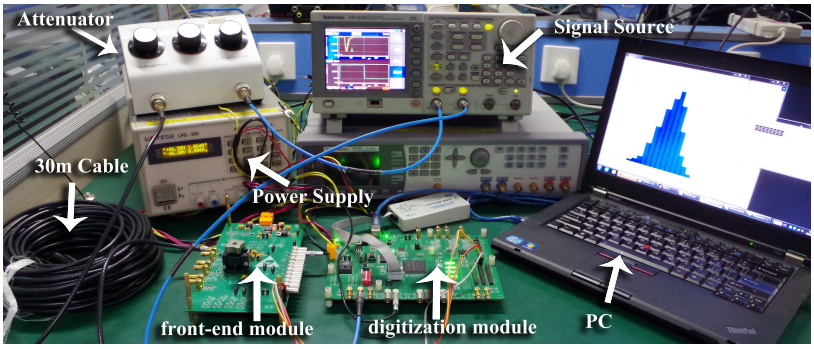


Fig. 16. Test platform of the test system. Mainly consists of front-end module, digitization module, PC, power supply, attenuator, 30 m cable and signal source.

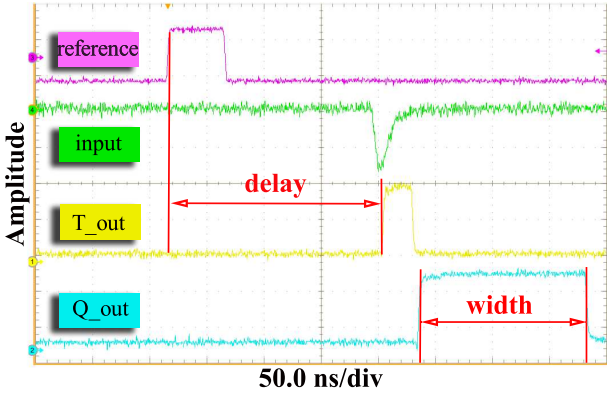


Fig. 17. Waveforms of the ASIC output signals. The "reference" and "input" signals are generated by the signal source (AFG3252). The "T_out" and "Q_out" signals are the output of the ASIC. The amplitude scale is 700mV/div, 50mV/div, 100mV/div, and 100mV/div from top-down.

In the test, the signal generator output two signals. One is created based on the waveform of the PMT output signal, and it is the "input" (in Fig. 17) after passing through a 30-meter cable. The other is a synchronization signal from the signal generator (i.e. "reference" in Fig. 17), and there exists a predetermined time interval between "input" and "reference" signal. The signal "T_out" is the output of discriminator in the ASIC, while the signal "Q_out" is the output of QTC. By analyzing the time measurement results between the "reference" and "T_out" signal (i.e. "delay" in Fig. 17), the time measurement performance can be estimated; by analyzing the width of the "Q_out" signal, the charge performance can be obtained. Then we conducted a series of tests to evaluate the performance of this ASIC with this test system.

B. Time measurement result

The time performance test results of the ASIC are shown in in table 2 & Fig. 18[17].

As shown in Fig. 18, the time walk is round 10 ns, and the time resolution is better than 300 ps, beyond the application requirement. The "low V_{th}" and "high V_{th}" refer to test results with the low (1/4 P.E.) and high (3 P.E. in the test, user controlled) threshold of the discriminator in Fig. 4. The reason for employing this two-threshold is to avoid deterioration of time measurement resolution which would be caused by noise or interference in the baseline of the large input signal.

C. Charge measurement result

The charge information of the PMT signals (related to the amount of Cherenkov light) is converted to the width of a pulse signal in the QTC ASIC. By analyzing the digitation output of the FPGA based TDC, the charge measurement performance can be evaluated.

As shown in Fig. 19, by combination the anode and dynode channel, a dynamic range of 1 $\sim$ 4000 P.E. is covered and the

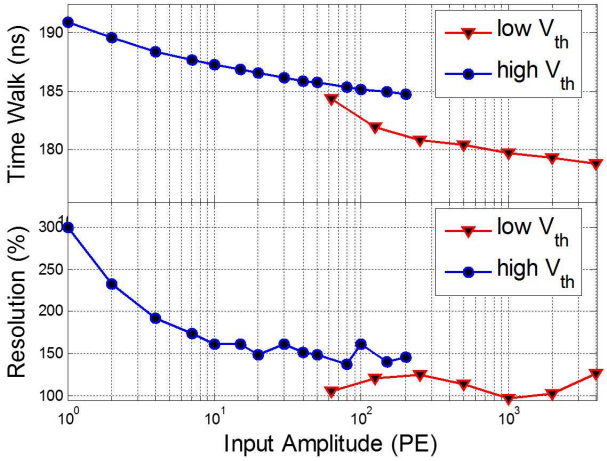
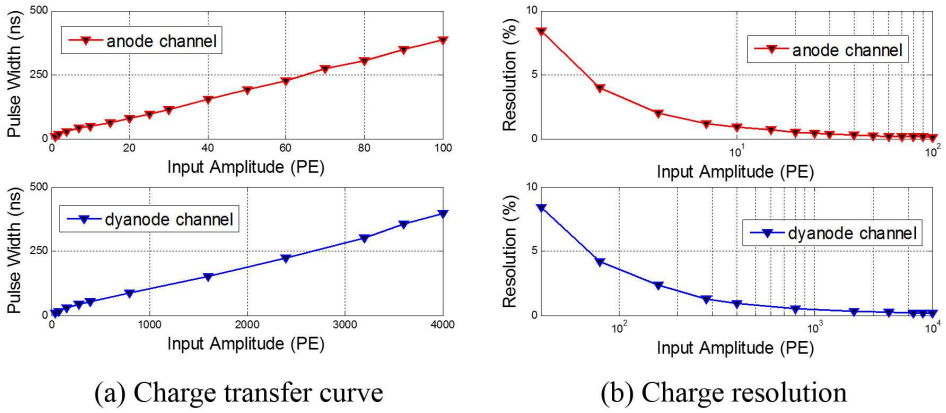


Fig. 18. Time measurement with FPGA based TDC. Data are listed in table 2.

Table 2. Time measurement results of anode and dynode

Input Amplitude (PE)	low V_{th}		Input Amplitude (PE)	high V_{th}	
	delay(ns)	resolution (ps)		delay(ns)	resolution (ps)
1	190.96	299.4	62.5	184.31	106.0
2	189.58	232.8	125	181.9	125.6
4	188.43	192.3	250	180.81	130.5
7	187.74	174.7	500	180.37	113.4
10	187.32	161.1	1000	179.69	97.4
15	186.91	161.2	2000	179.30	102.1
20	186.61	149.1	4000	178.83	136.7
30	186.21	161.6			
40	185.92	152.2			
50	185.74	149.2			
80	185.38	137.6			
100	185.21	161.6			
150	184.94	140.2			
200	184.75	145.9			



(a) Charge transfer curve (b) Charge resolution

Fig. 19. Charge measurement with FPGA based TDC. Data are listed in table 3.

charge resolution is better than 10% RMS @ 1 P.E., 1% RMS @ 4000 P.E., also beyond the requirement. With the test system presented in this paper, the ASIC chip designed for the WCDA in LHAASO was successfully tested, with the performance good enough for the application. With the modular structure of this test system and the design of a general purpose digitization module, this test system can accommodate the test of different versions of the ASICs designed in future. In the bulk test of the final 3600 ASICs, multiple front end modules will be designed, with sockets to amount the ASIC on the PCB without soldering,

Table 3. Charge measurement results of anode and dynode

Input Amplitude (PE)	anode		Input Amplitude (PE)	dynode	
	width(ns)	resolution (%)		width(ns)	resolution (%)
1	9.27	8.4228	40	8.27	8.3761
2	18.54	3.9687	80	16.54	4.2086
4	30.52	1.9810	160	30.16	2.3203
7	41.09	1.2054	280	42.83	1.2727
10	50.13	0.9212	400	53.94	0.9282
15	63.73	0.6965	800	85.50	0.5185
20	78.60	0.5367	1600	150.29	0.2883
25	95.93	0.4244	2400	222.08	0.2106
30	115.76	0.3550	3200	300.83	0.1711
40	155.76	0.2835	3600	354.64	0.1548
50	193.39	0.2279	4000	397.76	0.1411
60	225.75	0.1985			
70	272.88	0.1724			
80	305.27	0.1510			

and each digitization module can be used repeatedly.

D. Performance comparison

We also investigated the typical readout ASICs for PMT with a large signal dynamic range, and list their performances in table 4. Compared with these ASICs, the performance test results of our ASIC indicates a larger dynamic range with a good time and charge measurement resolution.

Table 4. Other PMT readout electronic requirements

	Dynamic range (P.E.)	RMS of time measurement	resolution of charge measurement (RMS@1P.E.)	quantity of charge (@1P.E.)
PARISROC[18, 19]	600	1 ns	30%	150 fC
SPIROC[20]	2000	1.25 ns	30%	80 fC
SCOTT[21]	60	600 ps	40%	8 pC
CLC101[22]	2500	300 ps	10%	2 pC
ASIC for WCDA	4000	300 ps	10%	750 fC

V. CONCLUSIONS

To evaluate the performance of a large dynamic range PMT readout ASIC designed for the WCDA in LHAASO, a test system is designed. This test system employs a modular structure, and can accommodate test of a series of ASICs with different versions, with a general purpose digitization module. Kernel parts in the digitization module, including I^2C interface, FPGA based TDC (333ps bin size) and USB data interface, as well as the test software were presented. Tests were conducted with this test system to evaluate the performance the real ASICs. The test results indicate that the time resolution is better than 0.5 ns; the charge resolution is better than 30% RMS @ 1P.E. and 3% RMS @ 4000 P.E., which is well beyond the application requirement.

VI. BIBLIOGRAPHY

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