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SKIROC2, front end chip designed to readout the Electromagnetic CALorimeter at the ILC

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ABSTRACT: SKIROC (Silicon Kalorimeter Integrated ReadOut Chip) is the front end chip designed for the readout of the Silicon PIN diodes foreseen for the Electromagnetic CALorimeter (ECAL) at the future International Linear Collider.

The fine granularity of the ILC calorimeters implies an extremely large number of electronics channels (82 millions) which is a new feature of "imaging" calorimetry.

Moreover, for compactness, the chips must be embedded inside the detector without any external component making essential the reduction of the power consumption to 25 μWatt per channel. This is achieved using power pulsing, made possible by the ILC bunch pattern (1 ms of acquisition data for 199 ms of dead time).

KEYWORDS: VLSI circuits; Analogue electronic circuits; Electronic detector readout concepts (solid-state); Front-end electronics for detector readout

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1 ROC chips for ILC prototypes

SKIROC [1] is one of the ROC chips designed within the CALICE collaboration [2] by the microelectronics group OMEGA to equip the technological prototypes built to check the feasibility of large scale modules and to address the integration issues (figure 1).

The design and the technological prototypes were funded by the EUDET European program and next generations of chips will be funded by the AIDA European programs [3, 4].

The requirements for the electronics are quite stringent. A hundred million channels have to be read out with a calorimetric performance (High precision, large dynamic range) and a power consumption which is four orders of magnitude lower than the corresponding LHC readout.

1.1 ECAL detector

To perform imaging calorimetry which consists of reconstructing each particle individually using the Particle Flow Algorithm (PFA), the detector has to be highly granular and segmented.

There will be 100 million channels to be readout in the ECAL and to avoid cracks and to ensure compactness, the ASICS have to be embedded inside the detector with no external components.

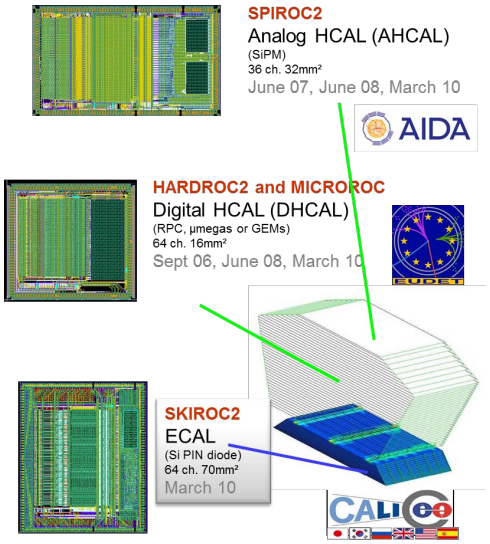

Figure 1. ROC chips for Technological prototypes.

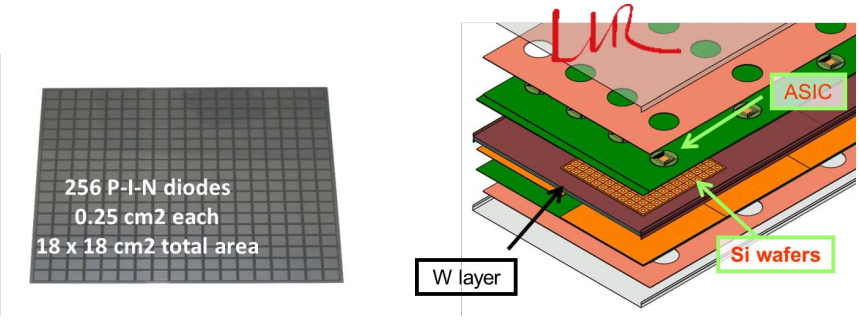

Figure 2. Si Pin diodes Wafer and Active Sensor Unit.

A SiW technology for the Electromagnetic Calorimeter [5] has been chosen: Tungsten for the absorber to ensure the compactness of the detector and Silicon Pin diodes of 5.5 mm $\times$ 5.5 mm for the active medium to ensure the granularity (figure 2).

The design of the ASICs has to be all the more cautious as these ASICs are System on Chip with a lot of digital activity near the sensitive analog Front End.

1.2 Common readout

The large number of channels requires minimizing the data lines and the power. The readout is therefore common to all the calorimeters and designed to be daisy chained using a token ring mode, without any external components [6].

This readout matches the ILC beam structure where collisions take place during 1 ms and with a 199 ms interbunch during which the readout is performed and the electronics switched off (figure 3).

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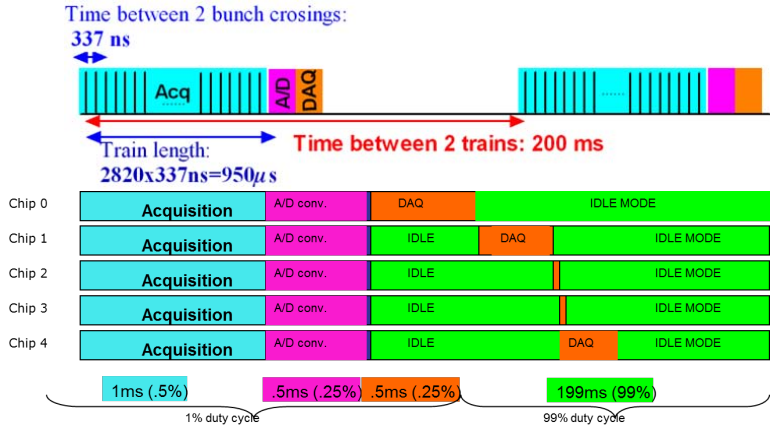

Figure 3. Common Readout.

2 SKIROC2

2.1 Requirements

SKIROC2 (Silicon Kalorimeter Integrated ReadOut Chip) has been designed in AMS SiGe 0.35μm technology and integrates 64 identical channels.

Each channel has been designed to handle a large dynamic range, from 1/2 MIP (about 2 fC for a 325 μm thick wafer) up to 2500 MIPs (10 pC). The detector capacitance has been estimated to be 20pF taking into account the 25 mm^2 pin diode and the printed board on which the ASIC is embedded. The chip allows auto triggering on 1/2 MIP and integrates the analogue storage and the digitization.

2.2 Features

Each of the 64 channels has an input charge preamplifier. A common gain for all channels can be set by changing the feedback capacitor Cf using the Slow Control parameters.

Each preamplifier is followed by a slow channel for the charge measurement and by a fast channel for trigger generation (figure 4).

The fast channel is made of a high gain variable CRRC shaper (peaking time tuneable between 50 ns and 100 ns via the Slow Control parameters) and is followed by a low offset discriminator to auto trig down to 0.5 MIP. The threshold of the 64 discriminators is supplied by a common 10-bit DAC and additionally by a 4-bit DAC per discriminator. Each discriminator output is sent to an 8-bit delay cell (delay time tuneable between 100 ns and 300 ns using the Slow Control) to provide the Hold signal for the slow channel. A wired OR of the 64 triggers is available (trig_outb).

The slow channel is made of two low gain and high gain CRRC shapers to handle the large dynamic range for the charge measurement. Each one is followed by a Track and Hold. As soon as there is a HOLD signal, the charge is stored in a 15 deep bank of capacitors (Switched Capacitors Array) and the time of each event is stored as well. The time tagging is performed by a 12-bit TDC ramp.

The time and charges stored in the SCA cells are then converted by a 12-bit Wilkinson ADC and sent to an integrated 4 Kbytes memory.

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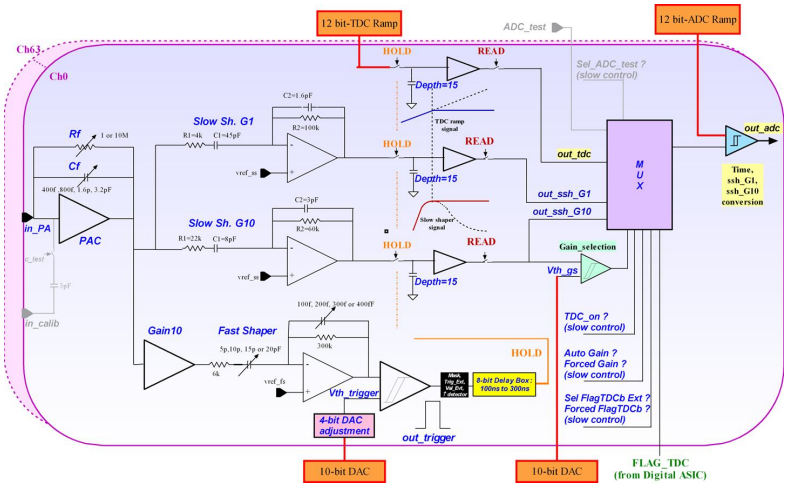

Figure 4. Schematics diagram.

The power consumption has been optimized to reach an ultra-low consumption: about 1.5 mW/channel. This chip can be power pulsed and each stage can be individually shut down when not used.

The digital part is very complex and performs the management of the acquisition, the conversion, the control of the 15 Switched Capacitors Arrays and of the Inputs/Outputs.

The size of the die is about 70 mm^2.

3 Measurements

The chip was submitted in March 10 and received in September 10. A few dies have been packaged to allow characterization.

3.1 10-bit DAC

A 10-bit DAC is used to set the threshold of the discriminators. Its linearity has been measured: the slope is 2.2 mV/ DAC Unit with a DNL= $\pm$1LSB and an INL=$\pm$1.7 LSB.

3.2 Fast shaper

The gain of the Fast Shaper is 50 mV/MIP and its noise is 5.3 mV, providing a MIP to Noise ratio of 10. This allows triggering down to 0.5 MIP.

Trigger efficiency measurements have been performed on the 64 channels. The non-uniformity between channels is quite good: within $\pm$1.5 DAC Units. This non uniformity can be further improved by using the 4bit-DAC per channel.

The trigger efficiency measurements as a function of the injected charge have been performed and show a minimum threshold level of 0.5 Mip (2fC) corresponding to the expected 5σ noise limit (figure 5).

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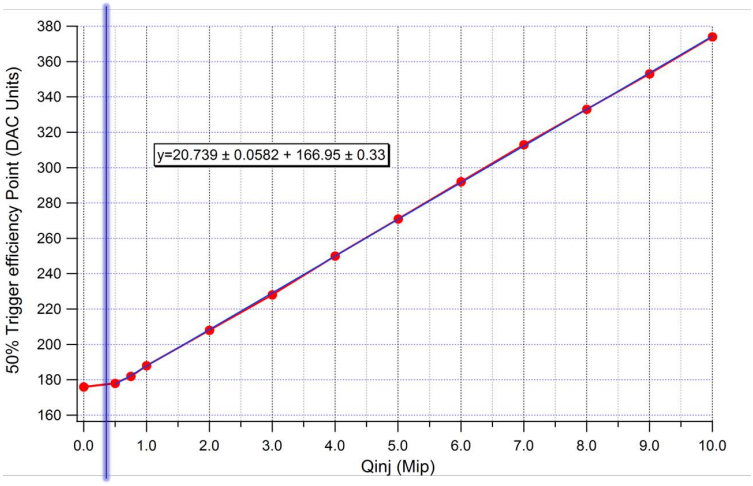

Figure 5. 50% trigger efficiency vs injected charge.

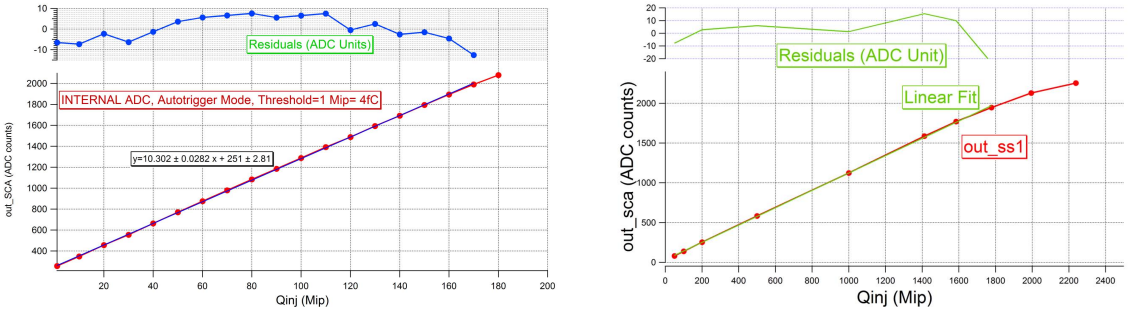

Figure 6. Linearity of Gain 10 and Gain 1 slow shapers.

3.3 Slow shaper

The linearity of the low gain slow shaper (Gain=1) and the high gain slow shaper (Gain=10) has been measured in the auto-trigger mode with a threshold set to 1 MIP and using the Switched Capacitors Arrays and the 12-bit ADC.

The linearity is good with an Integral Non Linearity better than 0.5% up to 2000 MIP. The dispersion of the measurement is within 1.2 ADC Unit or 600 μV (figure 6).

3.4 Power consumption

The power consumption requirement is 25 μW/ch with a 0.5% duty cycle which means 500 μA for the entire chip.

The chip is therefore power pulsed taking into account the ILC beam structure which allows shutting down the bias currents during the 199 ms between bunches.

The table in figure 7 summarizes the power consumption with and without power pulsing during the acquisition, conversion and readout phases. Hence skiroc2 power consumption is 1.7 mW or 27 μW/channel when it is fully power pulsed.

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Acquisition	88 mA , 290 mW	Duty Cycle =0.5%, 1.45 mW
Conversion	27.3 mA, 90 mW	Duty Cycle =0.25%, 0.225 mW
Readout	8.0 mA, 26.4 mW	Duty Cycle =0.25%, 0.066 mW

Figure 7. Power consumption with and without power pulsing.

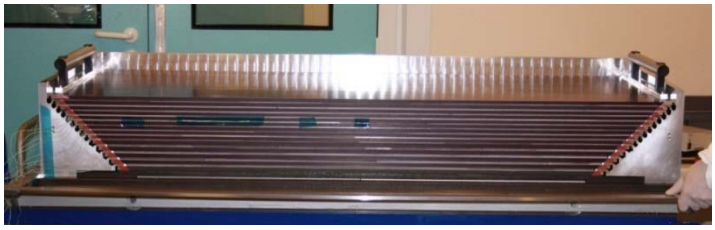

Figure 8. ECAL module (@LLR Palaiseau).

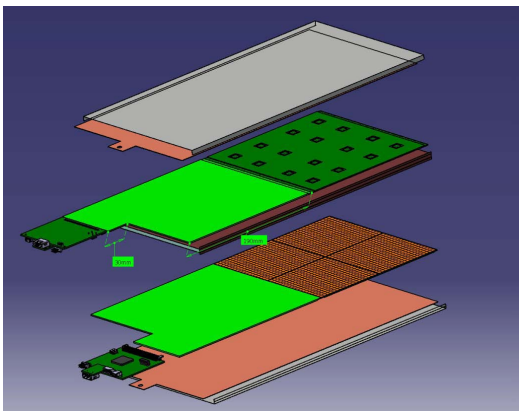

Figure 9. ASU layers.

4 ECAL technological prototype

Technological prototypes must be built to check the integration issues. The mechanical structure made of 15 tungsten plates wrapped into carbon fibre (figure 8) has been built by the mechanics group of the LLR Lab (Palaiseau) [7].

A detector slab made of one tungsten core, two detector layers (Active Sensor Unit) with electronics embedded on a printed circuit board must be inserted inside the 7 mm alveolar.

4.1 Active Sensor Unit (ASU)

Each ASU (figure 9) is made of a kapton layer to provide the HV bias of the pin diodes, one layer of pin diodes, one printed board with embedded SKIROC2 and one copper layer for the heat dissipation.

Up to seven ASUs will be interconnected to form a complete slab to be inserted in the alveolar of the module.

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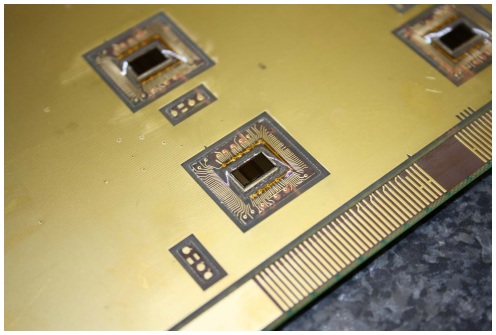

Figure 10. FEV board with embedded ASICs (bonding by CERN).

4.2 Printed circuit board

The design of this printed board is difficult as its thickness must be smaller than 1.1 mm including the embedded SKIROC2 chip.

This is a 9 layers PCB with five drilling sequences. Several versions have been realized since three years and have raised fabrication issues and difficulties to bond the ASICs. Eventually a Front End board (FEV board) with a thickness below 1.2 mm was realized with chips embedded inside cavities and without any external components (figure 10).

The first measurements using the DAQ system [8] have been performed and are encouraging.

5 Summary

SKIROC2 exhibits good performance and handles a large dynamic range from 1/2 MIP (2 fC) up to 2000 MIPs (8 pC). The low noise of the fast shaper (0.1 MIP = 0.4 fC = 2 500 electrons) allows setting the threshold down to 0.5 MIP.

Measurements have been performed using the auto trigger mode with a threshold set to 1 MIP.

Tests at system level with the Front End boards equipped with sensors and with embedded chips are ongoing.

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