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ROC chips for imaging calorimetry at the International Linear Collider

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Imaging calorimetry at the International Linear Collider requires new detectors with one hundred million channels that will be read-out with calorimetric performance, that is percent accuracy over 16-bit dynamic range. The readout electronics must be highly integrated and ultra-low power (μW per channel) to be embedded inside the detectors.
To tackle these challenges, R&D started in 2000 under the CALICE collaboration framework and FP6 EUDET, FP7 AIDA EU programs. Several detector technologies have been proposed and tested: Tungsten/Silicon for the Electromagnetic Calorimeter (ECAL), scintillating tiles read-out by Silicon PhotoMultipliers (SiPM) for an Analog Hadronic Calorimeter (AHCAL) and RPC/Micromegas/GEM for a Semi Digital Hadronic Calorimeter (SDHCAL).
Detector prototypes have been built and readout by ReadOut Chips (ROC chips) named SKIROC, SPIROC and HARDROC and designed in SiGe 350 nm technology by the IN2P3 OMEGA group. Different front-end architectures have been integrated for the various sensors and, to optimize the commonalities between the various detector proposals, the chips share a common backend and readout scheme. In order to address the numerous challenges, three generations of chips have been foreseen. The first generation consisted in analog readout ASICs that allowed characterizing the detector concepts in testbeam, referred to as CALICE physics prototypes. The second generation addresses the integration issues with embedded electronics and performs analog amplification, shaping, internal triggering, digitization and local storage of the data in memory. Thousands were produced in 2010 to equip CALICE technological prototypes and are being tested by IN2P3, DESY, CERN, and KEK groups. Zero suppression will be added in the 3rd generation chips, which is a major modification as it increases the complexity of the digital part.
The performance of these chips on testbench and at the system level will be detailed in this presentation.

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1. ILC challenges

Imaging calorimetry at the International Linear Collider requires highly granular and segmented detectors with one hundred million channels. The readout electronics must be highly integrated and ultra-low power to be embedded inside the detectors. Four dedicated integrated circuits were therefore designed by the OMEGA group in AMS Silicon Germanium 0.35 μm technology to equip detector prototypes [1]. The requirements are quite challenging in terms of electronics as the dynamic range is large and the noise must be small enough to allow auto triggering down to half a MIP. The challenges are also strong in terms of integration. The large number of channels and the compactness needed to avoid cracks mean that the FE asics must be embedded inside the detectors. These stringent requirements imply ultra low power as there is no much room for cooling. To tackle these challenges, R&D started in 2000 under the CALICE collaboration framework and EU programs [2][3]. Several detector technologies were proposed: Tungsten/Silicon for the Electromagnetic Calorimeter (ECAL), scintillating tiles readout by SiPM for an Analog Hadronic Calorimeter (AHCAL) and RPC/Micromegas/GEM for a Semi Digital Hadronic Calorimeter (SDHCAL). Physics prototypes were designed and tested under test beam between 2003-2005 to validate simulation models and PFA concept and check the performance of the various detectors. The dedicated electronics is therefore referred as "1st generation" electronics. In 2003, the design of ROC chips (ReadOut Chips) started to equip technological prototypes which had to be built to assess the feasibility of large scale, industrializable modules and to address power pulsing and integration issues.

This "2nd generation" electronics integrates auto-trigger mode, analog storage, internal digitization. The large number of channels requires minimizing the data lines and the power. The readout is therefore common to all the calorimeters and designed to be daisy chained using a token ring mode, without any external component. This readout matches the ILC beam structure where collisions take place during 1 ms and with a 199 ms interbunch during which the readout is performed and the electronics can be switched off allowing power pulsing. 3rd generation ASICS with completely independent channels started 2 years ago within the AIDA program [4].

2. SKIROC2 readout chip for the Electromagnetic CALorimeter (ECAL)

2.1 Electromagnetic calorimeter (ECAL)

The Electromagnetic Calorimeter [5] combines tungsten for the absorber to ensure the compactness of the detector and Silicon Pin diodes of 5 mm$\times$5 mm for the active medium to ensure the granularity. The extremely large number of channels (100 million channels) of the final design implies integration issues. Each detector slab is made of one tungsten core, two detector layers (referred as Active Sensor Unit) with electronics embedded on a printed circuit board. The slab is inserted inside a 7 mm alveolar.

2.2 SKIROC2 main features

SKIROC2 (Silikon Kalorimeter Integrated ReadOut Chip) is the 64 channel FE chip designed to readout the Si pin diodes of the ECAL. It handles a very large dynamic range from 0.5 MIP up to 2500 MIP (Figure 1).

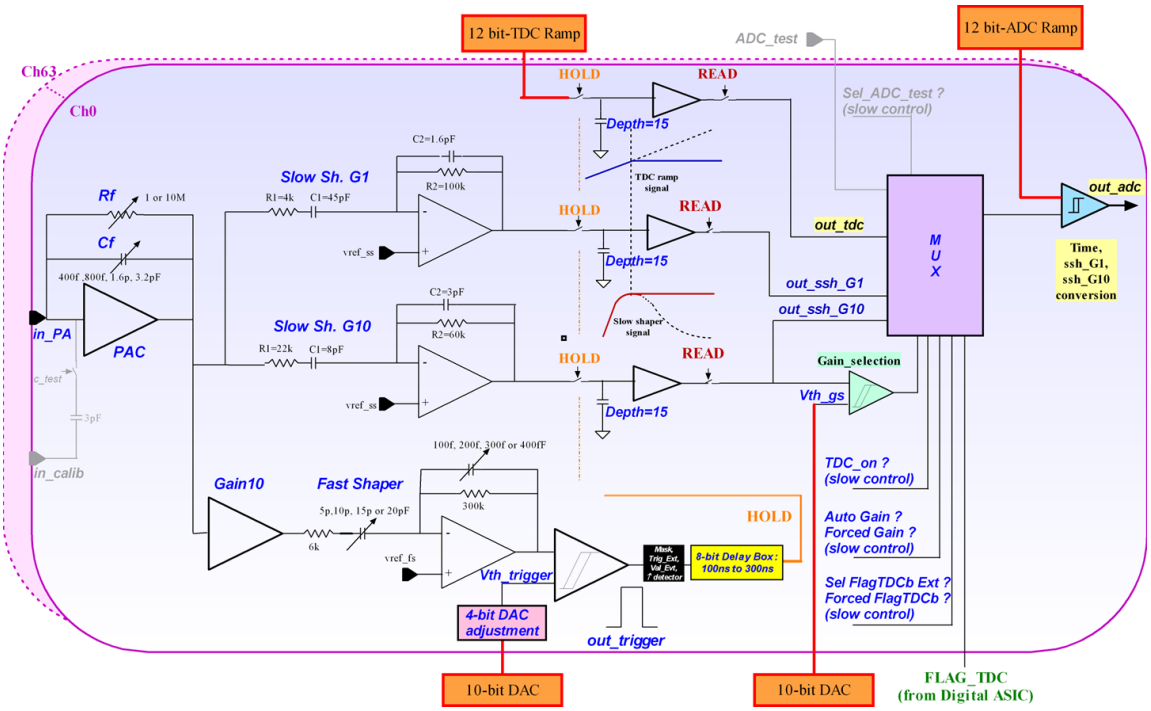

Figure 1: SKIROC2 schematics diagram

Each of the 64 channels integrates a charge preamplifier, the gain of which can be set by changing the feedback capacitor using the Slow Control parameters. Each preamplifier is followed by a slow channel for the charge measurement and by a fast channel for trigger generation. The fast channel is made of a high gain variable shaper with a peaking time tunable between 50 ns and 100 ns. It is followed by a low offset discriminator to auto trigger down to 0.5 MIP. The threshold of the 64 discriminators is supplied by a common 10-bit DAC and additionally by a 4-bit DAC per discriminator. Each discriminator output is sent to an 8-bit delay cell tune able between 100 ns and 300 ns to provide the Hold signal for the slow channel.

The slow channel is made of a low gain (Gain = 1) and a high gain (Gain = 10) CRRC shapers to handle the large dynamic range for the charge measurement. Each one is followed by a Track and Hold buffer. As soon as there is a HOLD signal, the charge is stored in a 15 deep bank of capacitors (Switched Capacitors Array). The charges contained in the SCA are then converted by a 12-bit Wilkinson ADC and sent to an integrated 4 Kbytes memory. The power consumption has been optimized to reach an ultra-low power consumption and is around 1.5 mW/channel. This chip can be power pulsed and each stage can be individually shut down when not used. The digital part is very complex and performs the management of the acquisition, the conversion, the control of the 15 Switched Capacitors Arrays and of the Inputs/Outputs.

2.3 SKIROC2 performance

The gain of the Fast Shaper is around 50 mV/MIP and its noise is 5.3 mV, providing a MIP to Noise ratio of 10. This allows triggering down to 0.5 MIP. Trigger efficiency measurements have been performed on the 64 channels. The non-uniformity between channels is quite good: within

$\pm$ 1.5 DAC Units. This non uniformity can be further improved by using the 4bit-DAC per channel. The trigger efficiency measurements as a function of the injected charge have been performed and show a minimum threshold level of 0.5 MIP (2 fC) corresponding to the expected 5 σ noise limit (Figure 2).

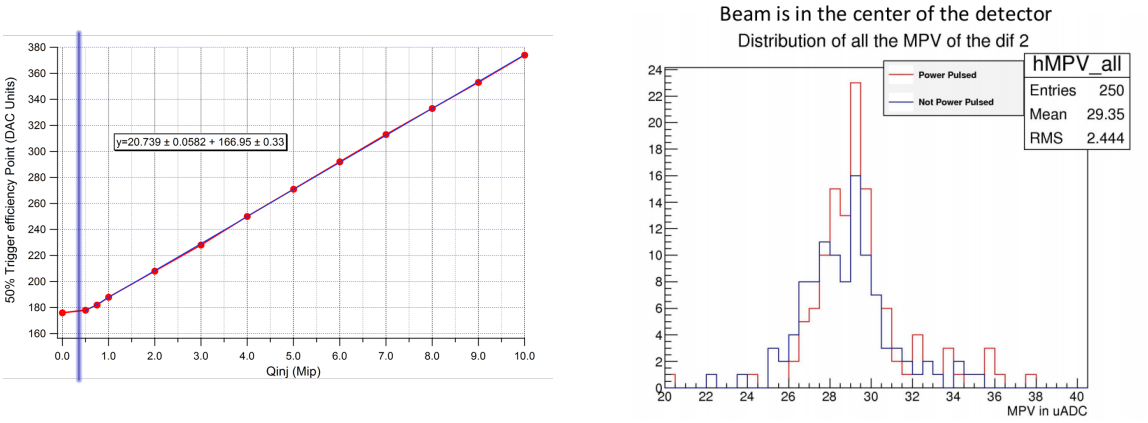

Figure 2: Left: 50% trigger efficiency vs injected charge. Right: MIP signal with and without power pulsing.

The linearity of the low gain slow shaper (Gain=1) and the high gain slow shaper (Gain=10) has been measured in the auto-trigger mode with a threshold set to 1 MIP and using the Switched Capacitors Arrays and the 12-bit ADC. The linearity is good with an Integral Non Linearity better than 0.5% up to 2000 MIP. The dispersion of the measurement is within 1.2 ADC Unit or 600 μV.

The power consumption requirement is 25 μW/ch with a 0.5% duty cycle which means 500 μA for the entire chip. The chip is therefore power pulsed taking into account the ILC beam structure which allows shutting down the bias currents during the 199 ms between bunches.

The power consumption of SKIROC2 has been measured to be 1.7 mW corresponding to 27 μW/channel with a power pulsing duty cycle of 0.5%. The settling time has been measured less than 100 μs at chip level. Successful testbeams took place at DESY with up to 8 layers in 2012 and 2013. The chips were used with the autotrigger and power pulsing modes. The signal over noise ratio is larger than 10 allowing nice events displays as shown in Figure 2 where a MIP signal is reconstructed with and without power pulsing.

The stability and the coherent noise of the electronics when power pulsed and located inside a magnetic field of 1 T were also successfully checked using a simplified detection element. These studies are funded by the French ANR program CALIIMAX [6].

3. HARDROC2, readout chip for the Semi Digital Hadronic CALorimeter

3.1 Semi Digital Hadronic CALorimeter (SDHCAL)

One option for the hadronic calorimeters proposed for the future ILC experiments is the so-called semi-digital hadronic calorimeter (SDHCAL) [7]. It consists of using Resistive Plates Chambers (GRPC) with 1 cm$\times$1 cm readout pads for the active medium with a semi digital readout based on 3 thresholds in order to perform both good tracking and coarse energy measurement. The 1 m^2 chambers consist of the elements shown in Figure 3.

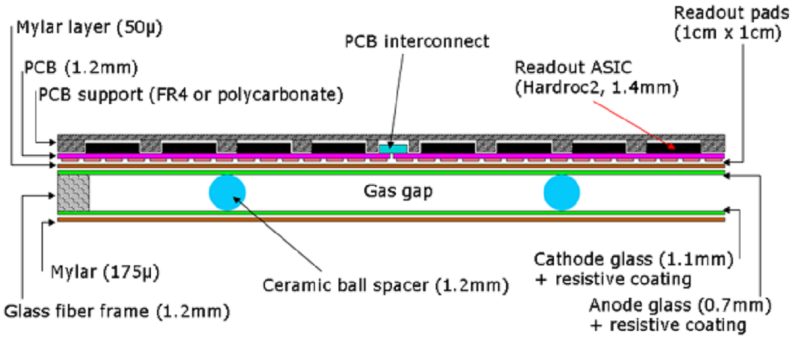

Figure 3: Cross-section through a 1 m^2 chamber

3.2 HARDROC2 main features

HARDROC (HAdronic Rpc Detector ReadOut Chip) is the very front end chip designed for the semi digital readout of the 1×1 cm^2 cells of the GRPC chambers.

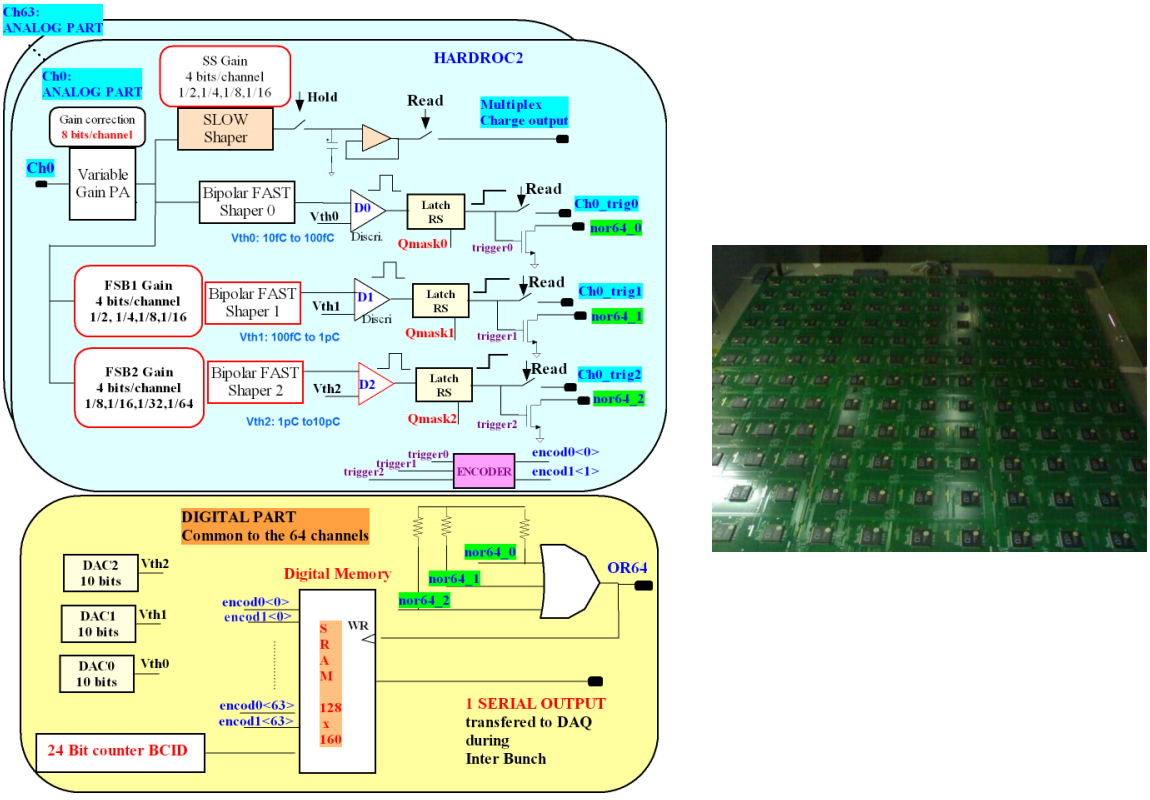

Figure 4: Left: HARDROC2 schematic diagram. Right: 144 chips per GRPC chamber.

The 64 channels of HARDROC2 (Figure 4) are made of a fast low impedance preamplifier with a variable gain over 8 bits per channel. A variable slow shaper (50-150 ns) and a Track and Hold buffer provide a multiplexed analog charge output up to 10 pC. The trigger path is made of three variable gain fast shapers followed by 3 low offset discriminators to auto-trigger down to 10 fC up to 10 pC. The thresholds are in a ratio of 1-10-100 for better physics performance of the

semi digital and are set by 3 internal 10 bit-DACs. The 3 discriminator outputs are encoded in 2 bits. A 128 deep digital memory is integrated to store the 2*64 encoded discriminator outputs and the bunch crossing identification. The chip is fully power pulsed and a Power On Digital module has been integrated to manage the 5 MHz and 40 Mhz clocks during the readout, to reach 10 μW/channel.

3.3 HARDROC2 performance

The performance has been measured on testbench since 2009. In particular, trigger efficiency measurements before and after gain correction show that the uniformity between channels can be corrected from $\pm$ 25 fC down to $\pm$ 5 fC. The 50% trigger efficiency point as a function of the injected charge shows that the threshold can be set down to 5 fC which corresponds to the 5 σ limit.

The performance in testbeam conditions was also measured. A technological prototype with up to 50 layers each equipped with HARDROC2 chips was built between 2010 and 2011 by IPNL lab.

This complete system with 360 000 channels was successfully tested at CERN (Figure 5), using the auto trigger mode and the power pulsing mode [8]. The power consumption of the chip has been measured to be 1.5 mW/channel when running continuously and 10 μW/channel with a 0.5% duty cycle which allows 24 hour running of a full slab with a 2AAA battery.

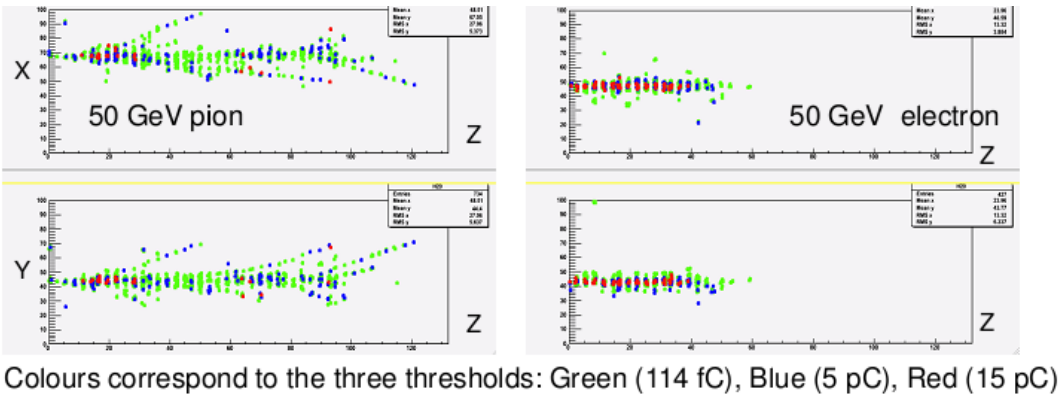

Figure 5: Testbeam results with 360000 power pulsed channels

A 3rd generation of ROC chip is necessary for ILD detectors. HARDROC3 is the first 3rd generation chip to have been designed and submitted within the european AIDA program. The channels are handled independently to perform zero suppression on chip. This is a major modification, especially for the digital part, as it implies a complex management of the readout. Besides, a I2C link with triple voting for radiation tolerance has been integrated for the control of the ASIC. HARDROC3 was submitted at the end of February 2013 and dies will be delivered at the end of June 2013.

3.4 MICROROC

MICROROC (MICRO Megas Readout Chip) [9] is a variant of HARDROC for a Digital Hadronic Calorimeter made of micromegas chambers. This 64-channel chip integrates a very low

noise charge preamplifier (0.2 fC) designed in collaboration with the LAPP lab. This low noise allows auto triggering down to 1 fC. Four micromegas chambers were built in 2011-2012 and tested in particle beams inside the SDHCAL steel structure described previously. The electronics and the detector exhibit a very good performance with the autotrigger mode and thresholds set down to 1 fC.

4. SPIROC, readout chip for the AnalogHadronic CALorimeter (AHCAL)

4.1 Analog Hadronic Calorimeter (AHCAL)

One option for the hadronic calorimeters is an Analog Hadronic Calorimeter [10] made of 40 layers of steel plates interleaved with cassettes of scintillating tiles readout by Silicon Photomultipliers (SiPM). The integration issues are also strong as the mother boards must be sandwiched between two absorber plates and the chips embedded inside the detector slabs.

4.2 SPIROC2 main features

SPIROC2 (SiPm Integrated ReadOut Chip) is the chip designed to readout the SiPM. The main features of SPIROC2 are quite similar to those of SKIROC2. A 8-bit input DAC is integrated for each of the 36 channels to tune the HV of the SiPM and so the gain, which is an important feature to compensate for the non uniformity between SiPM. Two voltage amplifiers with a gain of 1 and 10 are integrated for each input to perform the large dynamic range energy measurement (from 0.5 pe- up to 2000 pe-, or 80 fC to 320 pC with a SiPM gain of 10^6). The energy and the time are stored in an analog memory and converted by an internal 12 bit-ADC. The trigger path is made of a fast shaper followed by a discriminator to generate a signal to hold the maximum value of the two slow shaper outputs. The time measurement is performed by a Time to Amplitude Converter. The charge and time measurements are stored in a 16 depth analog memory. The conversion is performed by a 12-bit Wilkinson ADC and the converted data are stored in an internal memory.

4.3 SPIROC2 performance

The performance of SPIROC2 has been evaluated on testbench. The 50% trigger efficiency point as a function of the injected charge shows that the threshold can be easily set down to 1/3 of photo-electon, allowing nice spectrums performed with LED and using the auto trigger mode (Figure 6).

A 576 channel AHCAL prototype was equipped with 16 SPIROC2 chips and successfully tested under testbeam conditions at CERN and DESY in 2012 (Figure 7).

5. Summary

Imaging calorimetry is possible thanks to readout chips. These asics are complex but the integration issues are also stringent and were successfully addressed. Complete systems were built and ran under testbeam conditions, in auto-trigger mode and with power pulsing, with up to 400 000 channels in the case of the SDHCAL. It is an important step for the feasibilty of imaging calorimeters at the ILC.

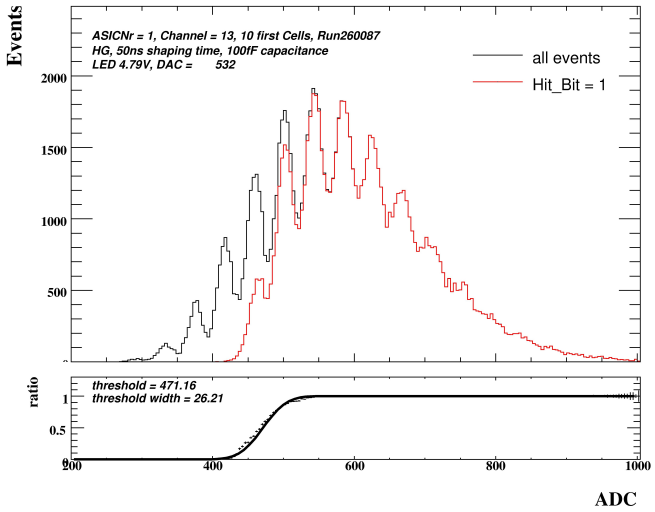

Figure 6: SiPM spectrum obtained with SPIROC2 and LEDs (@DESY)

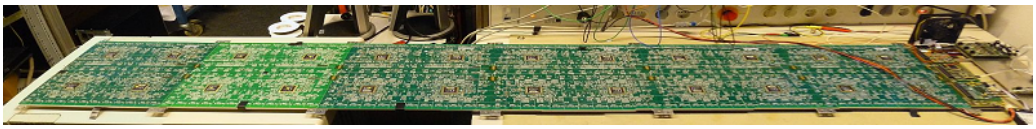

Figure 7: Slab equipped with 24 SPIROC2 chips

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