A Fully Fledged TDC Implemented in Field-Programmable Gate Arrays

Jinhong Wang, Shubin Liu, Qi Shen, Hao Li, and Qi An

***Abstract*—The motivation of this paper is to implement a fully fledged time-to-digital converter (TDC) in a field-programmable gate array from Xilinx Virtex 4 family with self-test and temperature variation compensation features. The TDC resolution is temperature and supply voltage dependent which, to a large part, is compensated. A self-test procedure, which covers a temperature range of 30 °C to 60 °C is used to determine the compensation constants. After compensation and integral nonlinearity (INL) calibration, the TDC presents a timing resolution of 25 ps RMS or 50 ps per LSB. A total of 9 channels TDCs are implemented in a single FPGA.**

***Index Terms*—Compensation, field-programmable gate arrays (FPGAs), time measurement, time-to-digital converter.**

I. Introduction

BASED on the principle of time interpolation, various time-to-digital-converter designs have been implemented in field-programmable gate arrays (FPGAs) [1]–[10], using the basic or auxiliary resources of the FPGA. It is a good choice to implement TDC in an FPGA due to its low cost, fast development cycle, and flexibility of reconfiguration. Previous research on TDCs in an FPGA has been carried out in our laboratory, using the dedicated carry-lines to perform time interpolation and obtaining a timing resolution of 50 ps root mean square (RMS) [9].

This paper describes a fully fledged TDC implemented in a single Xilinx FPGA. Some techniques for Self-Test and temperature variation compensation are introduced. This paper is organized as follows. In Section II, we first explain the methodology used to optimize the performance of the TDC. Then we cover the techniques of automatic placement of cells in a delay chain and Self-Test mode of the TDC, as well as the method for temperature compensation. In Section III, bench-top test results are shown and the corresponding discussion is given in Section IV. Finally, in Section V, we conclude this paper and summarize what has been achieved.

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The authors are with the Department of Modern Physics, University of Science and Technology of China and the Key Laboratory of Technologies of Particle Detection and Electronics, Chinese Academy of Sciences, Hefei, Anhui 230026, China (e-mail: wangjinh@mail.ustc.edu.cn; liushb@ustc.edu.cn; shenqi@mail.ustc.edu.cn; lihao01@mail.ustc.edu.cn; anqi@ustc.edu.cn).

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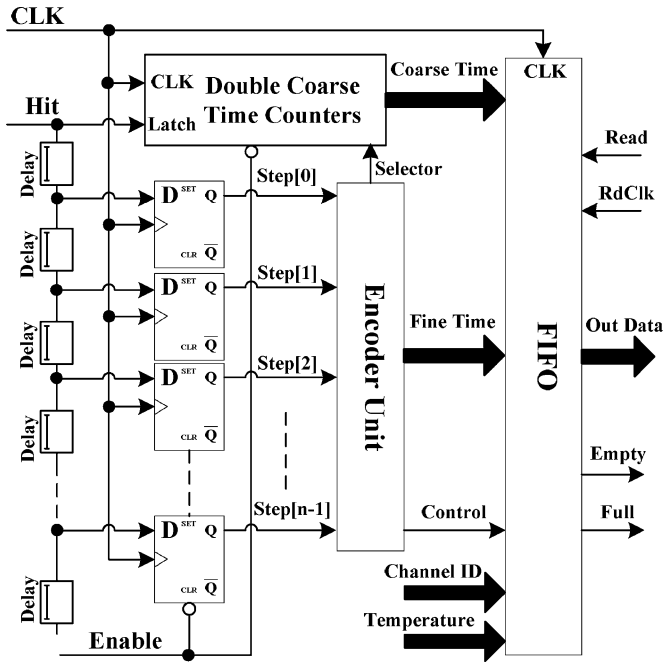

Fig. 1. Block diagram of the time-to-digital converter implemented in a single FPGA device.

II. Methodology

A. Placement of Delay Cells of TDC

The TDC is based on a counter and an interpolator method. A simplified block diagram is shown in Fig. 1, in which two crucial parts, the time delay chain (Fine Time measurements) and the coarse time counter are shown. The n-element delay cells (Delay) perform a tapped delay line time interpolation. The total delay of the n-element cells must cover the fine time measurement range (i.e., the clock cycle of the system clock CLK ($\mathrm{T_{CLK}}$)). CLK samples the state of delay cells when a hit arrives. By determining in which sample the rising edge of input signal comes out of a delay cell, the arrival time of the input signal can be deduced with a resolution equal to the tap delay. The bin width of these subdivisions is about $\mathrm{T_{CLK}}/n$. The system clock drives coarse counters to track the number of multiplied clock periods elapsed since the TDC was enabled. Since the hit signal (Hit) is asynchronous to CLK, the coarse counter may be in the middle of changing its value when the hit arrives. To circumvent this problem, two coarse counter values, half a clock cycle out of phase, are sampled when the hit arrives. One of the two counter values will be selected as the correct coarse time according to the fine time measurement from the delay line. The detailed description on the construction of

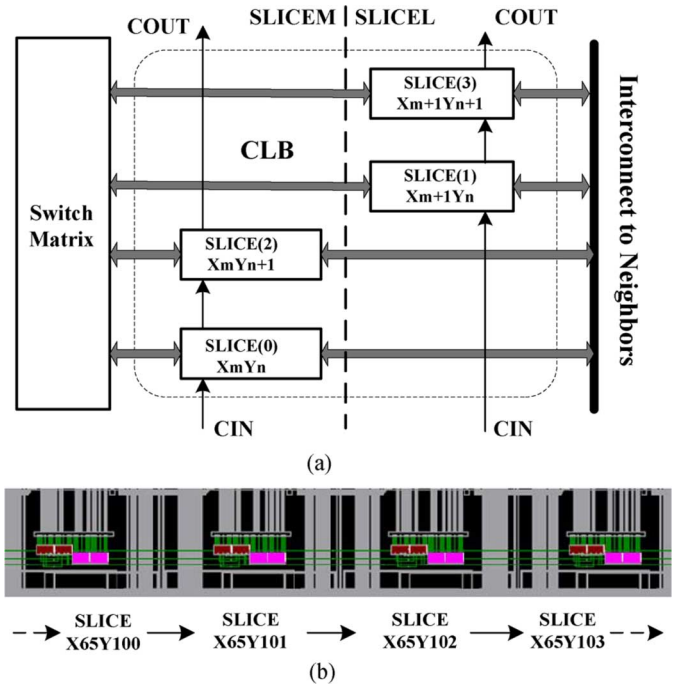

Fig. 2. Logic element arrangement in a CLB and the floor layout of the delay chain, where (a) shows a simplified diagram of the logic elements in the CLB and (b) is a part of the floor layout for the delay chain.

TDC is given in [9]; this section focuses on the method applied to optimize the placement of cells in the delay chain.

The block diagram of a configurable logic block (CLB) of a Xilinx Virtex 4 device is shown in Fig. 2(a) [11]. The carry-in line, as shown from CIN to COUT, is utilized as the basic delay cell and connected consecutively to the adjacent ones in the same column to form a time delay line.

It is essential that the delay cells form a uniform time-delay. Manual routing can, of course, achieve equal delay up to a certain point, but the placement work will be very time consuming. The method applied here is to insert a series of library primitives and placement constraints in the design [12], [13]. Using library primitives guarantee that each delay cell is mapped to a well defined CLB with an identified entry and exit point. The placements constraints, called LOC and RLOC, are then applied by the place and route software to obtain an adequate time delay chain. The LOC constraint locates the first delay cell to a specific position, such as $\mathrm{SLICE\_X_mY_n}$, while RLOC keeps on placing all the other cells of the delay chain in a pre-assigned sequence. For example, when LOC locates the first delay cell at $\mathrm{SLICE\_X_{65}Y_{100}}$, RLOC can keep on placing adjacent ones in the column $\mathrm{SLICE\_X_{65}}$ one by one. The delay cell in each CLB is identical and, thus, the time delay will be very uniform. Fig. 2(b) shows a part of the floor layout of the delay chain implemented in a Xilinx XC4VFX60FFG1152I device.

B. Self-Test Mode

Statistical methods based on a large number of measurements [14], [15] were used to estimate the cell delay at different temperatures and to execute the Self-Test mode. Test signals can be obtained from an external signal source or generated by a digital clock manager (DCM) block inside the FPGA. In both cases, the test signals have no correlation to the system clock.

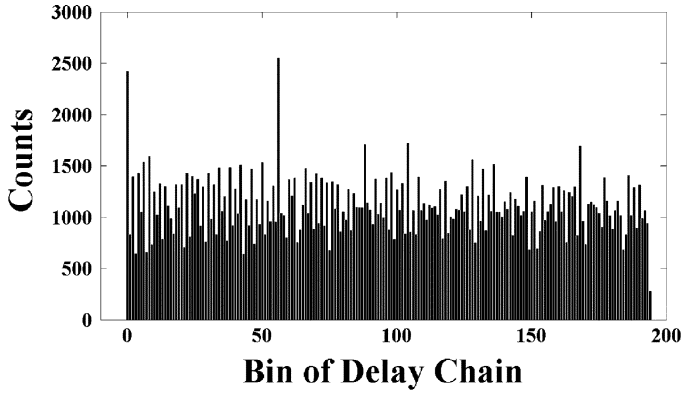

Fig. 3. Statistical analysis of the TDC bins.

The self-test mode is used to estimate the speed of the delay chain for the current temperature and power supply voltage. The principle of this method is to distribute a signal uncorrelated to the system clock uniformly within the assumed measurement range of the delay chain $(\mathrm{T_{CLK}})$. Test signals are considered to have identical distribution probability over these taps, thus, by averaging active segment (n) obtained from thousands of test results, the propagation delay of each cell or the bin size can be calculated by $\mathrm{T_{CLK}}/n$. Here, n may have a fractional part since $\mathrm{T_{CLK}}$ is not always a multiple integer number of the unit tap delay. n can be expressed as follows:

$$n = N + \frac{C_N}{C_{\mathrm{mean}}}. \tag{1}$$

In (1), N represents the maximum number of active segments and $\mathrm{C_{mean}}$ is the averaged count number per tap of the prior $0 \sim (N-1)$ taps. The last tap N causes the fractional part of n, and C_N is the corresponding counts at tap N.

Tests were performed at a temperature of 38 °C with the internal supply voltage $(\mathrm{V_{CCINT}})$ of FPGA set to 1.2 V. The statistical analysis results of the active segments for more than 200 000 trials are shown in Fig. 3. In Fig. 3, the counts of the last bin (bin 194) is 169, whereas the mean of the bins 0–193 is 618, thus n is equal to 194.3 according to (1), which is the equivalent total taps actually used. Therefore, the real tap delay (LSB) is 51.5 ps ($\mathrm{T_{CLK}} = 10$ ns).

C. Temperature Variation Compensation

Since the temperature of the FPGA influences the cell propagation delay from CIN to COUT, tests were performed with the aid of the self-test mode with the ambient temperature being changed from 28 °C to 60 °C. This corresponds to a temperature inside the FPGA of 31 °C to 63 °C. The temperature inside the FPGA was measured with a dedicated device (MAX6627) directly connected to the temperature sensing diode embedded in the FPGA [11], [16]. Part of the results is shown in Fig. 4. From the results in Fig. 4, we observe that cell delays vary almost linearly versus temperature. An experimental law can be established to estimate the LSB dependence on temperature, as in

$$\mathrm{LSB} = 51\,\mathrm{ps} + 0.047\ \mathrm{ps/^\circ C} \times (T - 31^\circ\mathrm{C}). \tag{2}$$

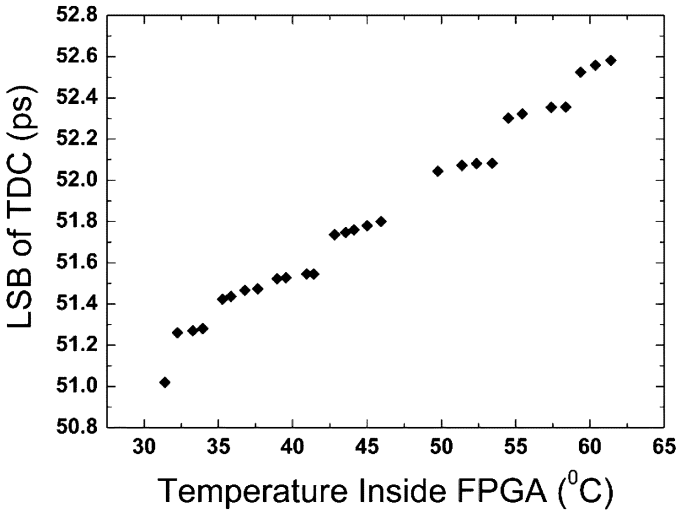

Fig. 4. Drift of LSB from 31 °C to 63 °C is illustrated.

For a temperature change inside the FPGA of 31 °C to 61 °C, the LSB increases from 51 ps to 52.6 ps. The LSB of the TDC increases by about 0.047 ps/°C. The temperature compensation mechanism is needed to determine the exact tap delay at the given operating temperature.

III. Test Results

An evaluation board with readout via the universal serial bus (USB) was designed to test the performance of the TDC and to verify the effectiveness of the methodology applied. We chose Xilinx Virtex 4 XC4VFX60FFG1152I for the implementation.

Characterization of the differential and integral nonlinearities was performed using the statistical code density test [14]. Measurements of cable delays were used to evaluate the overall precision [2], [17]. The tap delay of the delay chain or the LSB can be obtained from the self-test mode for a given temperature and the temperature variation of the LSB can be derived from (2) for compensation.

The coarse time counters work circularly at the system clock. To get the coarse time, the counter value is sampled at the moment when a hit arrives. The coarse counter value is a relative value, rather than an absolute one. Furthermore, the stability of the driven clock of the coarse counter can reach ± 0.5 ppm in the dynamic range. Therefore, the tests are focused on the fine time measurements.

A. Characterization of Nonlinearity

Typical results from the characterization of the differential and integral non-linearity are shown in Fig. 5(a), and (b), respectively. The obtained differential nonlinearity (DNL) is within $-0.4/+0.6$ LSB except for one bin (bin 56), which is about 1.4 LSB. The obtained integral nonlinearity (INL) is in the range $-1.3/+1.7$ LSB.

The nonlinearity is mainly caused by the architecture of Xilinx FPGA. The different clock distribution delays and the unequal bin widths in the delay chain contribute to most of the nonlinearity [9], but the very large value of DNL, such as DNL

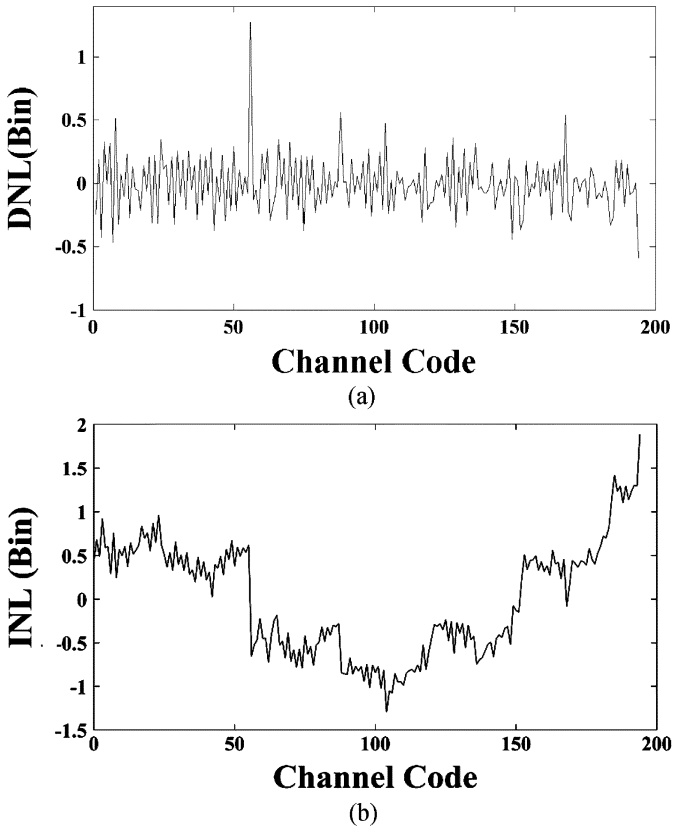

Fig. 5. Performance of the fine time measurement of the TDC, where (a) is the differential nonlinearity and (b) is the integral nonlinearity.

at bin 56 in Fig. 5(a), is attributed to the ultra wide cell of the delay chain of the TDC. The ultra large bin can be seen from the distribution of the TDC bins, as shown in Fig. 3. In Fig. 3, bin 56 exhibits a much larger hit count compared to other bins.

The integral nonlinearity here is systematic and inherent to the architecture of the FPGA being used. We can partly compensate the deviations and perform calibration (INL calibration) to obtain a higher precision in the time measurements [17], [18]. In our design, INL data are stored in a look-up table (LUT) in the FPGA, as an array of correcting vectors. The correcting mechanism implemented in the FPGA can perform INL error correction automatically.

B. Overall Performance of Time Measurement

The resolution of TDC, which is the most important parameter for a time measuring system, is usually reported as a single-shot precision (i.e., the standard deviation of the distribution of the time measurement results around the mean value when a single time interval is repeatedly measured for the statistical analysis). We used the measurement of the delay introduced by a cable of a given length to evaluate the overall precision. A Hit signal from a pulse generator, which is free running with respect to the TDC clock, is connected to two TDC channels with a fixed cable delay between the channels. The delay varies from 0 ns to 10 ns with about 1 ns per step to cover the whole measurement range of the delay chain, which is the fine time measurement range or the TDC system clock period (10 ns). Tests were performed for all the nine channels, and typical results are shown

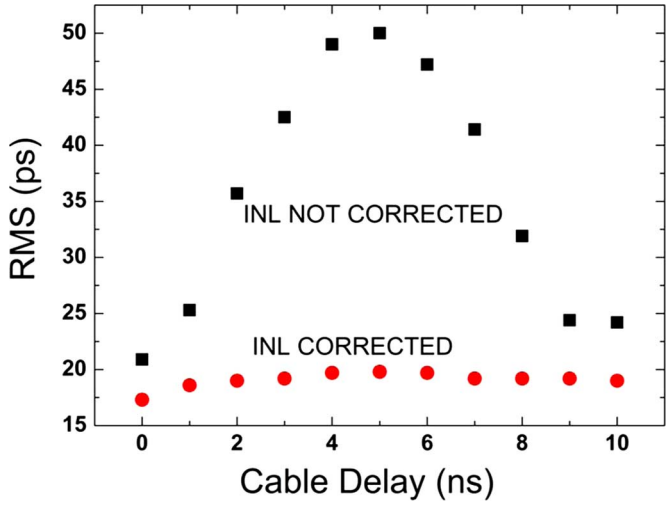

Fig. 6. Dependence of the timing resolution in RMS on the cable delay within the whole fine time measurement range from 0–10 ns, with and without INL calibration, respectively, is illustrated.

in Fig. 6. The RMS timing measurements of a single channel remain below 20 ps throughout the fine time measurement range after INL calibration and temperature compensation. The tests mentioned above were performed at an internal FPGA temperature of 36 °C and with a nominal supply voltage V_{CCINT} of 1.2 V.

C. Effectiveness of Temperature Compensation Strategy

A constant cable delay of about 5 ns was measured at different temperatures and the RMS timing measurements was calculated to verify the effectiveness of the temperature compensation scheme. The results at the temperature of 61°C are shown in Fig. 7(a) and (b), with and without compensation, respectively. For the case with compensation, the appropriate cell delay (LSB = 52.6 ps) at 61 °C is used. Whereas for the case without compensation, the LSB at 31°C (51 ps) is used instead. The compensation results in lowering the maximum value of the random error from 102 ps to 20 ps in this case. The tests mentioned here were performed with the nominal voltage supply and the results in Fig. 7(a) and (b) include the effect of the related INL calibration.

IV. Discussion

A. Minimum Number of the Delay Cells Required

In our TDC design, the total delay time of all active carry lines is equal to one clock period (T_{CLK}). The self-test mode gives the actual tap delay (LSB) and, thus, the minimum number of delay cells can be easily calculated by T_{CLK}/LSB. However, the delay time of cells in the delay chain is dependent on temperature. It varies with the temperature of the FPGA; thus, the minimum number of the delay cells changes (we assume T_{CLK} is a constant value). In Fig. 4, $T_{CLK} = 10$ ns, as the temperature of FPGA falls from 61 °C to 31 °C, the LSB decreases from 52.6 ps to 51 ps, the corresponding number of active delay cells used increases from 190 to 196. From this point of view, extra bins should be added to the number of T_{CLK}/LSB in the worst case.

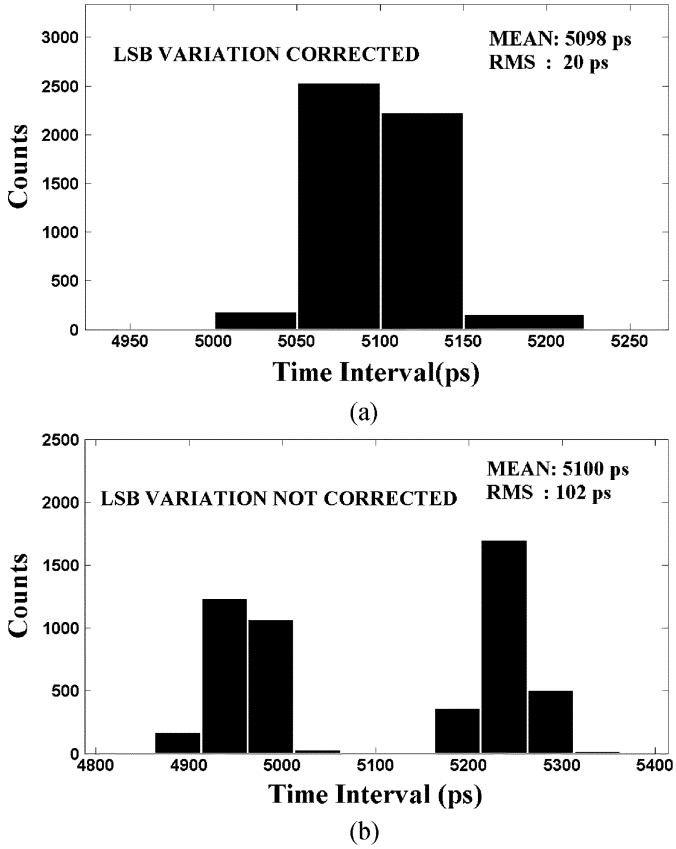

Fig. 7. Statistical spread of the cable delay measurements at 61 °C, showing a significant reduction of RMS after the correction of the LSB variation. (a) With LSB variation correction and (b) without LSB variation correction.

A higher rate of system clock can reduce the total number of delay cells required. The reduction of the length of the delay chain can lower the distribution of clock delays and the overall non-uniformity of the delay chain [9], [11]. However, it increases the difficulty in system design.

In the evaluation board, the TDC works at 100 MHz and the LSB is around 50 ps. The total number of delay cells finally chosen was 210.

B. Voltage Dependency of LSB

The LSB of the TDC changes not only with the temperature, but also with the internal supply voltage. Self-Test mode can give the effective bin size (LSB) at different voltages and, thus, it is necessary to perform voltage compensation.

In our evaluation board, we changed the internal power supply of the FPGA (V_{CCINT}) from 1.2 V to 1.0 V at a temperature of 28 °C. The self-test was performed and the results indicate that the LSB varies from 50.8 ps to 76.8 ps.

Actually, the LSB given by the self-test mode depends on the temperature and the supply voltage. The compensation for temperature and power supply variations is essential to improve the TDC timing performance (RMS and LSB).

C. Dead Time

The dead time of the TDC can be reduced to one cycle of the system clock by using pipeline techniques. The dead time of the

TDC on our evaluation board is 10 ns. TDCs with short dead time can be implemented to meet the various needs of multi-hit situations.

D. Trigger Matching

In high accuracy timing measurement applications, where rare events are searched in a dominating background, a high interaction rate is needed to achieve adequate sensitivity in a reasonable amount of observation time. Trigger matching can be performed to reject background noise data that may not be of interest to the experiment and to maximize the use of the DAQ data bandwidth.

In our TDC design, we integrated trigger matching utilizing content-addressable memory (CAM) embedded in the FPGA. Generally, a programmable trigger latency up to 2.3 ms and a maximal matching window of about 640 ns are achieved.

V. Conclusion

A 9-channel fully fledged TDC is implemented on a Xilinx XC4VFX60FFG1152I device. Some techniques were developed for the automatic placement of the delay cells and a method for the compensation of temperature variations is also applied. The LSB of each TDC channel is about 50 ps and the standard deviation of time measurement is below 25 ps after temperature variation compensation and INL calibration.

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