Design of a Test Platform for Screening Procedures of VA160 and VATA160 ASICs in DAMPE Mission

Di Jiang, Changqing Feng, Chi Zhang, Shanshan Gao, Deliang Zhang, Zhongtao Shen, Shubin Liu, Qi An

***Abstract*–The Dark Matter Particle Explorer (DAMPE) is a scientific satellite designed to search for the clue of dark matter particles for a mission period of at least 3 years. Two types of readout ASICs, named VA160 and VATA160, are adopted for the front-end electronics (FEE) to meet the design specification. Total lot screening of VA160 and VATA160 is utilized to assist in achieving levels of quality and reliability commensurate with the aerospace application. A test platform has been designed and built to provide comprehensive electric parameters acquisition during screening process of VA160 and VATA160. The system consists of a master board, a DUT board, a host PC, a DC supply power and necessary cables. The tester measures supply current, gets dynamic range and linearity of charge measurement, checks the 165-bit configuration register and verifies trigger signal output. With the test platform, the task of five rounds of electric test of over 200 chips has been finished in time, which ensured the progress of the qualification model of DAMPE mission.**

***Index Terms*–ASIC, DAMPE, front-end readout, screening, test platform, VA160, VATA160**

I. Introduction

The DAMPE is a scientific satellite designed for cosmic ray study with a primary scientific goal of the indirect search of dark matter [1], [2]. The satellite will be launched into sun-synchronous orbit with the altitude of 500 km and the inclination of 97 degrees in 2015 for a mission period of at least 3 years, which makes stringent requirements on the quality and reliability of the electronics components used on the satellite. The DAMPE payload consists of four sub-detectors from top to bottom: the Plastic Scintillation Detector (PSD), the Silicon-Tungsten Tracker (STK), the Bismuth Germanium Oxide (BGO) calorimeter, and the Neutron detector. The BGO calorimeter takes charge of the measurement of the primary cosmic ray spectrum from 5GeV to 10TeV and the generation of the fast trigger signal for the trigger system. To accomplish this goal, two types of front-end readout ASICs, named VA160 and VATA160, are adopted for the front-end electronics (FEE) of PSD and BGO calorimeter.

Manuscript received May 22, 2014. This work was supported in part by the Strategic Priority Research Program on Space Science, the Chinese Academy of Sciences (Grant No. XDA04040202-4), and the National Basic Research Program (973 Program) of China (Grant No. 2010CB833002).

All Authors are with State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, No.96, Jinzhai Road, Hefei, Anhui, China. (telephone: +86-0551-63600408, e-mail: jiangdi@mail.ustc.edu.cn, fengcq@ustc.edu.cn, legendzc@mail.ustc.edu.cn, shawn@mail.ustc.edu.cn, dlzhang@mail.ustc.edu.cn, henzt@mail.ustc.edu.cn, liushb@ustc.edu.cn, anqi@ustc.edu.cn)

Total lot screening of VA160 and VATA160 must be utilized to assist in achieving levels of quality and reliability commensurate with the aerospace application according to the appendix A of GJB-548B-2005. Part of the procedures related to the electric test is shown in Fig. 1. Five rounds of electric test are required during the screening process [3]. Concerning the fact that there are over 200 chips to be tested, we have designed a test platform that can quickly and easily obtain the key electric parameters of the chips to help complete the task in time. The tester has also been used in irradiation tests to evaluate the radiation tolerance of VA160 and VATA160.

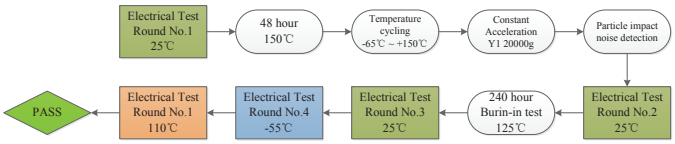

Fig. 1 VA160 and VATA160 screening procedures

II. Overview of VA160 And VATA160

VA160 and VATA160 are designed for the front-end readout of photomultiplier tubes (PMT) coupled to scintillators by a company named IDEAS in Norway [4], [5]. They are manufactured with the 0.35um CMOS technology processed on epitaxial silicon wafer and bounded in CQFP-128 package. Fig. 2 shows an unformed chip and a DUT board with the IC socket.

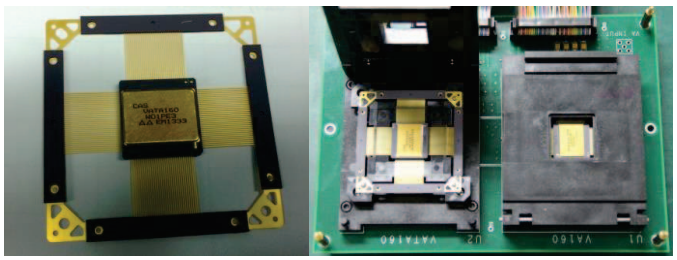

Fig. 2 Left: VATA160, unformed. Right: IC socket with VATA160

VATA160 is a combination of VA160 and TA160 on one chip and the VA160 part is exactly the same with VA160 ASIC. The chip has 32 charge sensitive pre-amplifiers (CSA) inputs, a multiplexed output for the pulse heights, and a trigger output [5]. Fig. 3 shows the simplified block diagram of VATA160.

978-1-4799-3659-5/14/$31.00 ©2014 IEEE

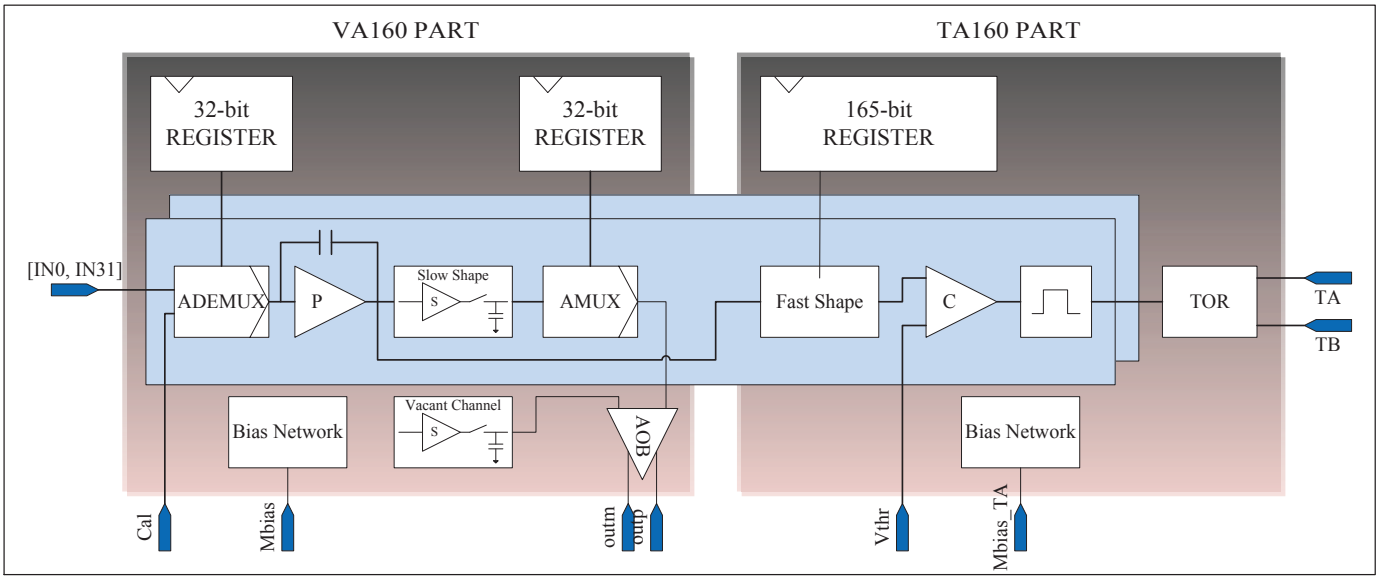

Fig. 3 Simplified lock diagram of VATA160

Each pre-amplifiers output, whose pulse height is proportional to the input charge, is connected to a slow shaper of VA160 part as well as a fast shaper of TA160 part. The pulse height from all channels can be sampled simultaneously and switched via an analogue multiplexer (AMUX) to one differential analogue current output buffer (AOB). Each pre-amplifier input can be tested using a calibrated charge, which must be applied to Cal by the external system [4].

TA160 has 32 pulse height discriminators, which provide a trigger (TA and TB) if the pulse height in a channel exceeds the common threshold (Vthr). This trigger signal can be used to sample and read out the signal charge from all channel inputs. TA160 has a 165-bit configuration register that allows one to program various features of the chip. VATA160 has a bias generation network that generates all bias currents and voltages needed for its operation. The bias network requires Mbias and Mbias_TA input current supplied by the external system [5].

III. System Overview

A. Components

The VA160 and VATA160 test platform, which consists of a master board, a DUT board, a host PC, a DC supply power and necessary cables, has been conceived and built to meet all the testing requirements. The system architecture is presented in Fig. 4. A photograph of a test platform in use is shown in Fig. 5. A DUT boards contains a VA160 and VATA160. They can be tested simultaneously to improve the efficiency, but the tester also works with only one chip.

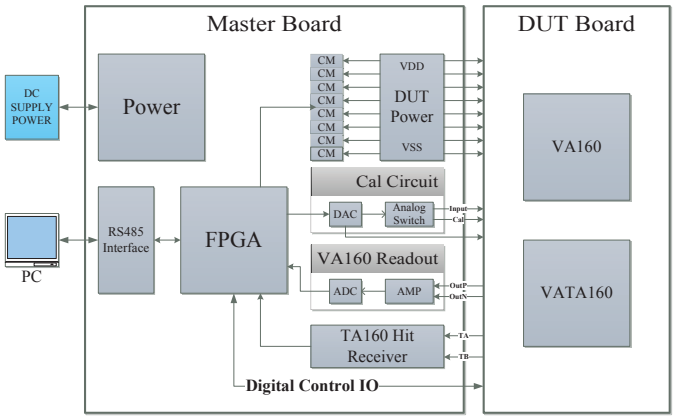

Fig. 4 Block diagram of VA160 and VATA160 test platform

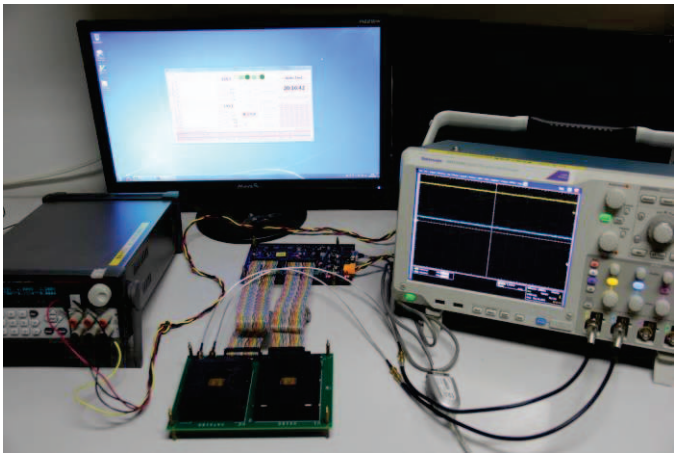

Fig. 5 A test platform deployed at FELab, USTC

B. Design Consideration

Master-slave board structure is adopted to simplify the design and facilitate the test [6].

The DUT board only includes some passive components and IC socket for VA160 and VATA160, which can minimize the impact of other components on the results When DUT board is tested in high and low temperature. To avoid possible electrostatic discharge (ESD) during operation, clamp diodes are used in front of 32 channel analog inputs.

The master board, as the core part of the platform, communicates with the host PC through RS485 interface on one hand and controls the chip on the DUT board through two 34-pin flat ribbon cables on the other hand. To run VA160 and VATA160 testing, it has a DUT power supply and current monitoring module, a calibration charge generator module, an analog readout and analog-to-digital conversion module, a trigger differential line receiver and a control module.

The DUT power provides positive and negative voltage (+2.5V, -2.5V) which can be power down by FPGA. They are both divided to 4 independent channels with current monitoring to obtain more detailed current information.

The charge pulse is generated through injecting step voltage into a 10 pF capacitor. The capacitor is placed as closely as possible to the pin of VA160 while the step voltage is generated by a DAC and an analog switch of the calibration module. The height of the charge pulse corresponds with the step voltage.

The system is controlled by a GUI written in LabVIEW running on a Windows PC, as shown in Fig. 6. It can achieve real-time monitoring of the supply current and calculate the power dissipation. Pedestal test and calibration test can be performed to check VA160, after which the test data will be analyzed and the results will be displayed immediately. Register test and hit test can be performed to verify TA160. Taking into account that the task is heavy and the time is emergency, the automation of the software is the direct way to help improve the efficiency of the whole testing process. Actually a set of test of every chip can be completed in less than 5 minutes with only a few clicks.

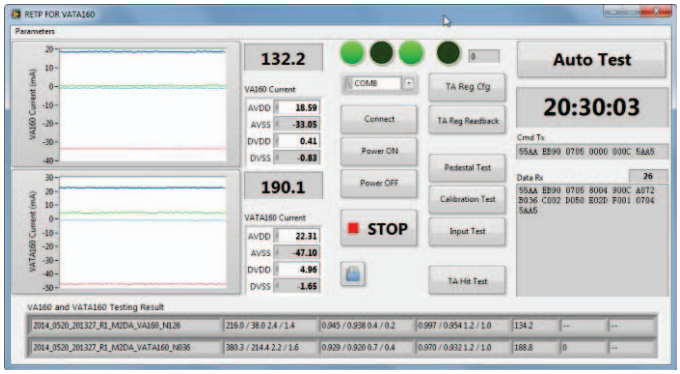

Fig. 6 GUI software based on LabVIEW

IV. Testing Procedures

VA160 No. 126 and VATA160 No. 26 was tested as samples using the test platform at room temperature.

A. Supply Power

VA160 and VATA160 require positive and negative supply voltage (-2.5V, +2.5V). For VA160 and VATA160, 4 types of supply current (AVDD, AVSS, DVDD, DVSS) will be monitored respectively to obtain detailed current information. The typical current value is shown in TABLE I.

TABLE I. Supply current of VA160 and VATA160

	AVDD (mA)	AVSS (mA)	DVDD (mA)	DVSS (mA)	POWER (mW)
VA160	19.01	-33.05	1.24	0	133.24
VATA160	23.14	-45.86	4.13	-0.83	184.89

B. VA160 Part

Pedestal test, calibration test and input test are performed to check the performance of VA160. Since VATA160 covers VA160, we just present the results of VATA160 as an example.

Pedestal test is to measure the pedestal and RMS noise when VA160 works in normal mode with the inputs floating. The maximum RMS noise is less than 3 bit, equivalent to 3.3 fC, as shown in Fig. 7.

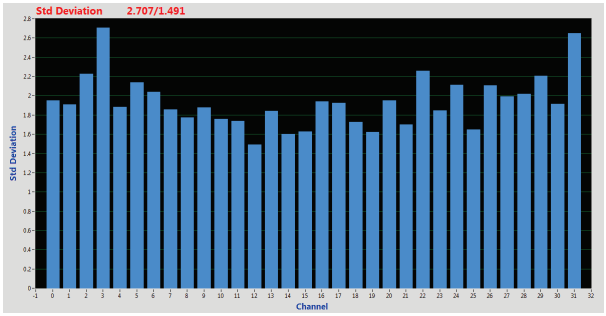

Fig. 7 RMS noise of pedestal test, less than 3 bit

Calibration test is to obtain the linearity and dynamic range through measuring the input charge to the Cal pin when the chip works in calibration mode. Input charge ranges from about -4 pC to 18 pC with interval of 720 fC and the fitting range is from 0 to 12 pC.

As all channels share the same input charge, the result shows very good consistency between channels, as shown in Fig. 8 and Fig. 9. The coefficients of input charge versus ADC code distribute within a very narrow range from 0.907 to 0.916 and the maximum non-linearity error is less than 0.6%.

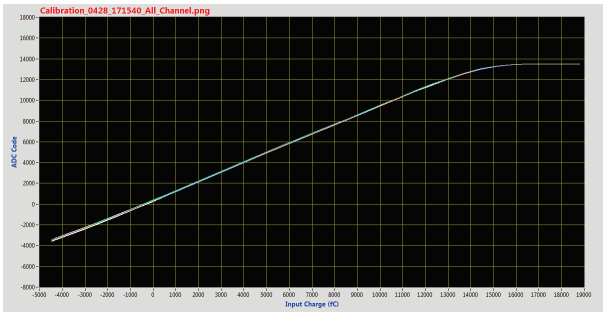

Fig. 8 Calibration result of 32 channels

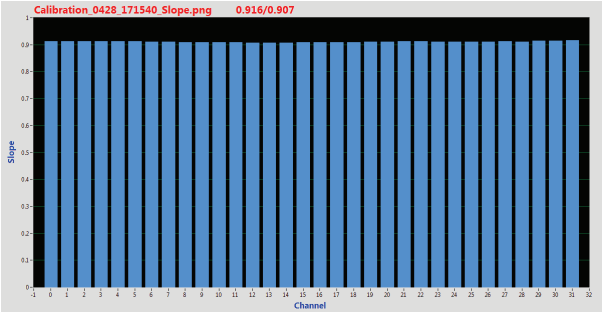

Fig. 9 Slope of linear fit of 32 channels, the max/min is 0.916/0.907.

Input test is to measure the input charge to the IN0 to IN31 pin when the chip works in normal mode. The input charge range and fitting range are the same with calibration test. However, because of the difference between the capacitors as well as the distribution of PCB traces, the results is not that perfect as calibration test. The coefficients of input charge versus ADC code distribute from 0.941 to 0.971 and the maximum non-linearity error is about 1.2%. Input test is performed to check the input stage as a complement to calibration test.

C. *TA160 Part*

When it comes to TA160, register test and hit test are required to check the chip.

Since the working status of the triggering chip is completely controlled by its 165-bit register, it is important to assure that it functions well. Register test is to write into and read back from the 165-bit register and then compare.

Hit test is to check if each channel can generate trigger signal properly, which will be monitored with the oscilloscope. This is a rough test without acquire the precise curve between Vthr voltage and charge threshold. The Vthr voltage is set to 400 mV and the input charge is set to 1 pC from IN0 to IN31 pin. Under such conditions, TA160 is expected to generate the trigger signal shown in Fig. 10 for each channel [7].

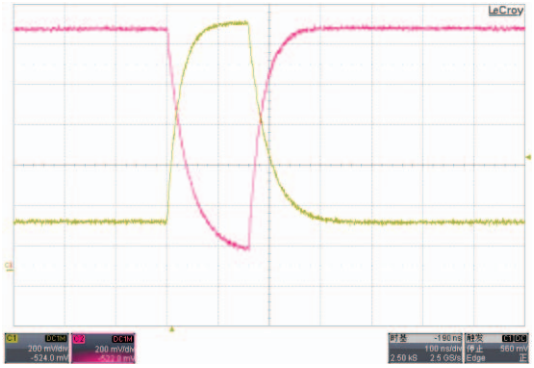

Fig. 10 TA160 trigger signal output

V. Acceptance Criteria

Referring to the test results of some chips using the VA160 and VATA160 test platform, we set the acceptance criteria that is listed in TABLE II.

TABLE II Acceptance criteria of VA160 and VATA160

Test	Parameter	Typical	Max / Criteria	Unit
Power Dissipation	VA160	130	150	mW
	VATA160	180	200	mW
Pedesta Test	Pedestal	--	Max-Min<500	bit
	RMS	3	4	bit
Calibration Test	Slope	0.9	Max-Min<0.01	--
	Non-linearity Error	1%	1%	--
Register Test	--	--	No Error	--
Hit Test	--	--	Each channel functions well	--

VI. Concluding Remarks

Using the test platform, we have successfully completed the VA160 and VATA160 screening procedures of over 200 chips. From the qualified chips that satisfies the acceptance criteria, 68 VA160 chips and 32 VATA160 chips were picked up and used for the mass production of BGO and PSD FEE boards. All the FEEs mounted with the ASICs operated steadily during functional and environmental tests and the following integrating tests, which ensured the progress of the Qualification Model of DAMPE mission.

References

[1] Chang, J., et al. "An excess of cosmic ray electrons at energies of 300–800 GeV," Nature 456.7220 (2008): 362-365.

[2] J. Chang, "Dark Matter Particles Detection in Space," Journal of Engineering Studies. vol.2(2), pp. 95-99, June 2010.

[3] GJB 548B-2005, *Test methods and procedures for microelectronic device,* Chinese PLA General Armament Department, 2005

[4] IDEAS Inc. Norway, *VA160 Datasheet,* http://ideas.no.

[5] IDEAS Inc. Norway, *VATA160 Datasheet,* http://ideas.no.

[6] Gao Shanshan, Feng Changqing, Jiang Di, et al. "Radiation tolerance studies on the VA32 ASIC for DAMPE BGO calorimeter," Nuclear Science and Techniques, 25(1), 10402-010402.

[7] Shanshan Gao, Changqing Feng, Yunlong Zhang, et al. "The BGO Electromagnetic Calorimeter Sub-trigger Electronics for DAMPE," Real Time Conference (RT), 2014 19th IEEE-NPSS. to be published.