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Beam test performance of the SKIROC2 ASIC

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ABSTRACT

Beam tests of the first layers of CALICE silicon tungsten ECAL technological prototype were performed in April and July 2012 using 1–6 GeV electron beam at DESY. This paper presents an analysis of the SKIROC2 readout ASIC performance under test beam conditions.

1. Introduction

The next particle accelerator at the energy frontier after the LHC will be a linear electron positron collider at the TeV scale. This machine will allow high precision measurements to extend the scientific results of the LHC. Currently the most advanced proposal is the International Linear Collider (ILC) with a centre-of-mass energy of up to 1 TeV [1]. An alternative at higher centre-of-mass energies than the ILC is the Compact Linear Collider (CLIC).

Relevant physics processes at the future linear collider mostly lead to multijet final states. The reconstruction of the final state will be based on the Particle Flow Algorithm (PFA), which aim to reconstruct every particle of the final state [2]. Particle flow techniques require highly granular calorimeters with a huge number of electronics channels. The front end ASICs will be embedded inside the detector.

The CALICE collaboration is preparing large scale prototypes for highly granular calorimeters for detectors to be operated at a future linear electron positron collider. A silicon–tungsten ECAL physics prototype to demonstrate the principle of highly granular electromagnetic calorimeters has been operated successfully in beam test campaigns at DESY, CERN and FNAL [3,4]. The next, so-called "technological", prototype addresses the engineering challenges associated with the realisation of highly granular calorimeters. This prototype has entered its construction phase.

We present the test beam results of the first layers of the technological prototype. The data collected in April and July 2012 at DESY using an electron beam up to 6 GeV were analysed. The main

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goal of these tests was to study the readout electronics, especially the SKIROC2 ASIC. A calibration procedure for a larger number of cells was established. The homogeneity of the response was studied and the signal to noise ratio of the detector was determined.

2. Very front end electronics – SKIROC2 ASIC

The SKIROC ASIC (Silicon pin Kalorimeter Integrated Read-Out Chip) is a 64-channel very front end ASIC designed for the readout of silicon PIN diodes [5,6]. Amplification, trigger decision, digitisation and readout are integrated into the ASIC. The measured signals are first stored in an analogue memory and then converted into digital words by an ADC. These digital values are stored in an integrated RAM to be readout at the end of the acquisition cycle.

The analogue part has been designed to handle a dynamic range of charge depositions between 0.4 fC and 10 pC. The charge deposition expected for a Minimum Ionising Particle is 3.7 fC, hereafter referred to as a MIP. Each channel is made of a variable-gain low-noise charge preamplifier. The gain can be set by changing the feedback capacitor C_f. Each preamplifier is followed by a slow channel for the charge measurement and by a fast channel for the trigger decision. Indeed, since LC detectors will not provide a central global trigger signal, the ASICs require a self-triggering capability (auto-triggering). If one channel of an ASIC triggered, the levels of all the channels are recorded. A bandgap ensures the stability with respect to supply voltage and temperature for all the requested references in the analogue core. An internal slow clock is used for the time stamping of the events. The slow clock frequency can be as high as 5 MHz. This timestamp number is referred to as a Bunch Crossing Identifier (BCID).

The fast channel consists of a high gain variable CRRC shaper. The integration time is set to 30 ns, but can be adjusted. The peaking time is 50 ns due to the limited gain-bandwidth product of the preamplifier. The fast shaper is followed by a low offset discriminator to trigger down to 0.4 fC. The gain is 125 mV/fC. The noise of the fast shaper is about 0.4 fC ($\simeq$ 2600 electrons). The threshold of the 64 discriminators is supplied by a common 10-bit DAC. A supplementary 4-bit DAC is implemented for the fine adjustment of the individual channel trigger thresholds. The goal is to calibrate each channel to trigger down to 0.185 fC. Each discriminator output is sent to an 8-bit delay cell to provide the hold signal for the slow channel. The delay time can be varied between 100 ns and 300 ns.

The slow channel is made of a low gain and a high gain CRRC shapers to handle the large dynamic range. For C_f=6 pF, the high gain is 14.25 mV/fC and the low gain is 1.425 mV/fC. A track and hold cell is used to save the signal at its peaking time. The measured signal from the two slow shapers are stored in a 15 cell deep buffer. In a buffer, each cell is powered using one low consumption amplifier. The reference level depends on the cell number. The Switched Capacitor Array (SCA) write command is issued at the first rising edge of the internal ASIC slow clock after the logical disjunction of the 64 channel triggers (OR64 signal). For all channels without hits, the hold signal is sent at this rising edge of the slow clock. This information is used to determine the position and width of the pedestal. The charges stored in the SCA cells are then converted by a 12-bit Wilkinson ADC and sent to an integrated 4 kbyte memory.

The ASIC can be power-pulsed in order to reduce the power consumption to 25 μW per channel by taking advantage of the ILC spill structure. During these test beams, the electronics was operated with continuous power supply. The power consumption was 2.7 mW per channel.

3. Experimental set-up and trigger adjustment

The prototype tested in beam was composed of six layers. The sensitive part of the detector was an array of PIN diodes made of 320 μm thick high resistivity silicon. The size of the sensor was around 9 × 9 cm^2, and the pixels size was around 5 × 5 mm^2 [7]. The sensors were mounted on Printed Circuit Boards (PCBs) which channelled the signals to the ASICs. The sensors were glued to the PCBs using a robotic system. The thickness of the PCB was 1.45 mm. Each PCB was equipped with 4 SKIROC2 ASICs, corresponding to 256 readout channels. All the channels worked in self-triggering mode. The mapping of the pixels of the sensor to the ASICs M1–M4 within a layer is illustrated in Fig. 1. Some ASIC channels were linked to several pixels resulting in higher capacitive noise. The preamplifiers of these channels were disabled for the data taking.

Each layer was mounted in a U-shaped carbon composite mechanical housing. The top of the U was closed with a 300 μm−thick aluminium cover. The overall thickness of each layer was 7 mm. Fig. 2 shows a photograph of one layer without the aluminium cover. The layers were inserted into a Polyvinyl Chloride (PVC) supporting structure designed to house up to 10 layers. The distance between successive layer positions was 15 mm. A 2.1 mm-thick tungsten plate could be inserted in front of each layer. During this test beam, the layers were at the positions 1, 3, 5, 7, 9 and 10. A picture of the detector

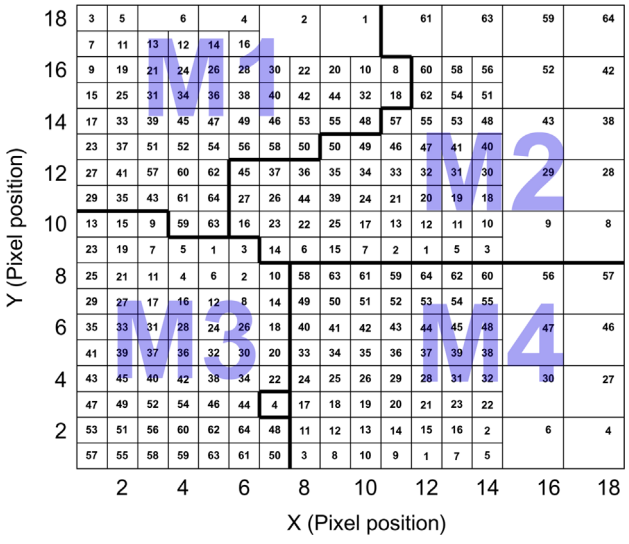

Fig. 1. Mapping of the channels of one layer. The ASIC channels connected to sensor pixels are shown as a function of the pixel position. The broad lines represent the ASIC borders. Some ASIC channels are linked to several pixels (large boxes). The isolated channel 4 between M3 and M4 belonged to M2.

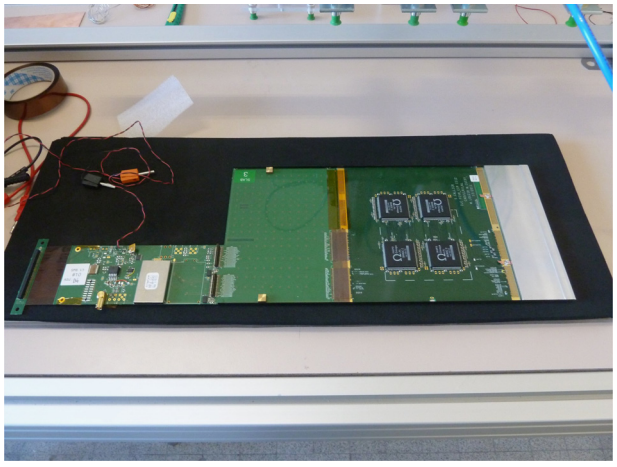

Fig. 2. Picture of one layer without aluminium cover.

is shown in Fig. 3. The detector was mounted on a movable stage, with the layers arranged perpendicularly to the beam direction.

Each layer was equipped with a Detector InterFace (DIF) card which connected to the DAQ system [8,9].

3.1. Setting of the trigger threshold and trigger delay

The threshold of the auto-trigger was adjusted in order to optimise the efficiency for measuring a MIP for a given maximum noise rate. To define the trigger threshold, a threshold scan was performed without beam. The maximum number of events that the ASIC can record during a spill is limited by the size of the memory (15 events). During the data taking, to avoid the saturation of the memory by the noise, a goal of only one noise event per spill was set. For one channel, this rate is 0.016 event per spill which corresponds to 0.1% of the maximum trigger rate. The non-uniformity of the effective trigger threshold between channels was measured to be within ± 0.4 fC on a test bench. However, the design of the PCB was not optimal: some lines between silicon pads and ASICs were too long and some digital lines or clock were too close to several analogue lines. This non-optimal PCB routing implied an increase of the noise in some channels and an increase of the spread of the effective trigger threshold. Taking into account these effects, the non-uniformity was within ± 2 fC. It turned out that the range of the individual threshold adjustment was too small to be used in this beam test. Therefore the same trigger threshold was set for all channels of an ASIC, which constituted a compromise between the optimal trigger threshold of each channel.

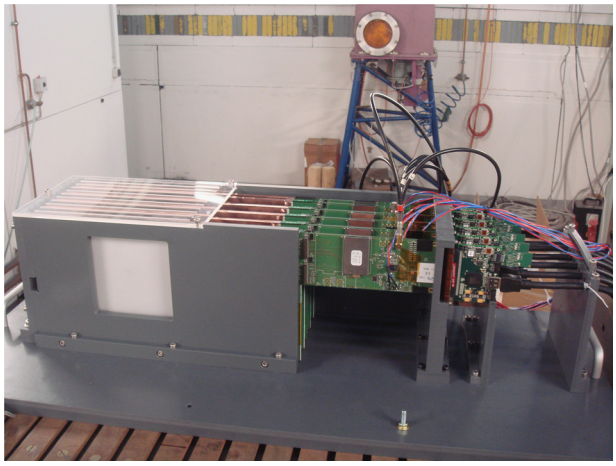

Fig. 3. Picture of the experimental set-up with six layers.

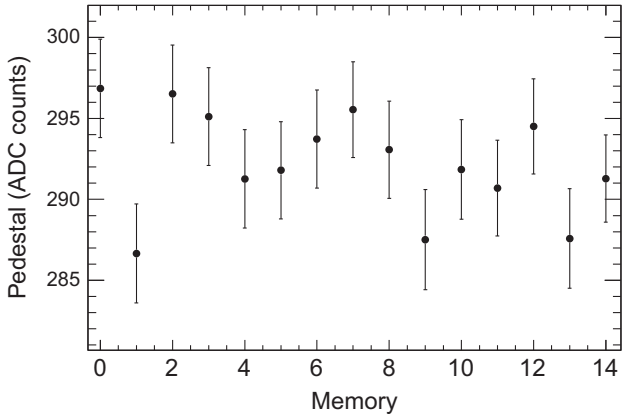

Fig. 4. Pedestal as a function of the cell number for one channel. The noise of an individual channel is given by the error bar. The noise is defined by the width of the Gaussian fit to the non-triggered event distribution of a given channel.

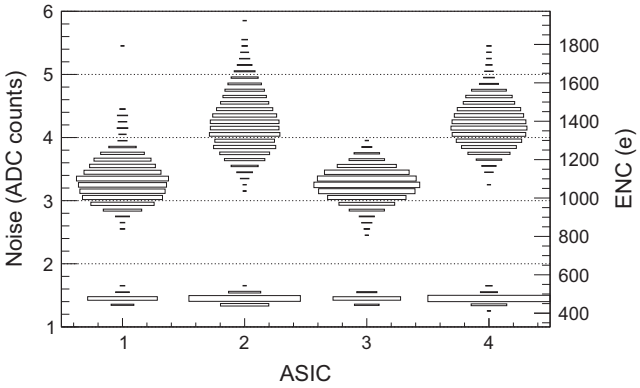

Fig. 5. Noise distribution as a function of the ASIC number for all layers. The left y-axis is the noise in ADC counts. The right y-axis is the equivalent noise charge.

The preamplifiers of channels with too high trigger rate were disabled. Around 9.5% of channels had high trigger rates due to the mapping of several silicon pads to one ASIC channel. Noise due to non-optimal PCB routing resulted in high trigger rates for an additional 9.5% of channels.

The trigger signal is delayed to select the measurement time of the signal from the slow shaper. This optimal delay depends on the trigger threshold. A scan of delay values was performed during the test beam with the feedback capacitance set at 1.2 pF. The maxima of all channels were in the range 200–230 ns. During the test beam, the delay was set at 220 ns for all ASICs.

4. Noise study

4.1. Pedestals measurements

For each channel, pedestals were extracted simultaneously to the recording of test beam data using non-triggered events. These distributions were fitted to a Gaussian distribution, whose mean was taken to be the pedestal, and width the noise.

As explained in Section 2, the reference level depends on the cell number. Therefore, pedestals have to be subtracted individually for each cell number as illustrated by Fig. 4 which shows the pedestal and noise as a function of the cell number for one channel.

Fig. 5 shows the distribution of the noise as a function of the ASIC number for all layers. The noise of the channels with disabled preamplifiers is around 1.5 ADC counts, the Equivalent Noise Charge (ENC) is 493.2 e. For other channels, we clearly see two patterns. Two ASICs (M1 and M3) have a noise distributed around 3.2 ADC counts (1052.1 e) and the other two ASICs (M2 and M4) have a noise around 4.2 ADC counts (1380.8 e). The only difference between the ASICs is the routing of the PCB. The lines between the ASICs M2/M4 and their pixels are longer than the lines between the ASICs M1/M3 and their pixels. In Fig. 6, the measured noise is plotted against the line length, demonstrating the strong influence of PCB line length on the observed noise level.

The noise as a function of the gain[2] was studied to investigate the evolution of the noise pattern. The noise as a function of the gain is plotted in Fig. 7 for two channels of one layer, with long and short lines, respectively. As expected, the noise increases linearly with the gain. The two graphs were fitted with linear functions. The gain tends to zero at the y-intercept. For all channels of all layers, the y-intercept of the fit converges to the same value, as shown in Fig. 8.

[2] Inverse of the feedback capacitance C_f (see Section 2).

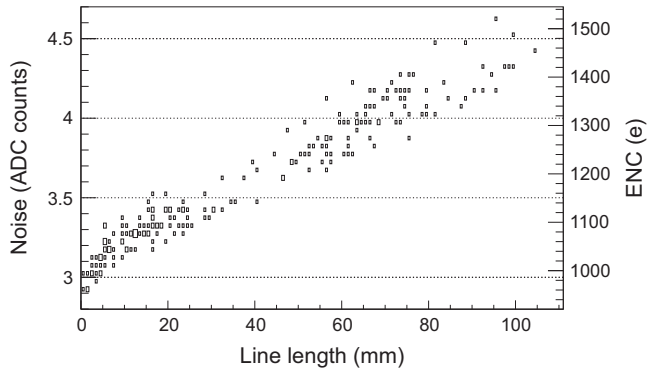

Fig. 6. Noise as a function of the line length in the PCB for one layer. The left *y*-axis is the noise in ADC counts. The right *y*-axis is the equivalent noise charge.

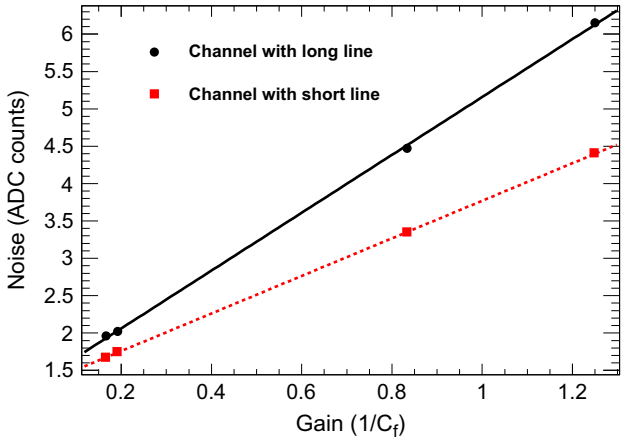

Fig. 7. The noise as a function of the feedback capacitance C_f for two channels of one layer, with long and short lines. The lines are linear fits.

This value corresponds to the noise which is not injected through the pre-amplifiers. On the other hand, the distribution of the slopes, shown in Fig. 9, shows two peaks corresponding to channels with short and long lines. These results confirm the noise pattern shown in Fig. 5. The varying line length provokes different capacitance on the inputs of the ASICs. At the same time, the internal noise of the ASICs is the same for all channels of all ASICs.

4.2. Coherent noise

A detailed analysis of coherent noise was carried out for the physics prototype to study the perturbation of the noise induced by high-energy showers [10]. In the present analysis, we apply the algorithm described in [11].

We consider that each channel i is affected by an incoherent noise source Inc_i and N_c coherent noise source ($Coh_{1,2,\ldots Nc}$). The total noise in channel i is given by

$$\sigma^2_{tot_i} = \sigma^2_{Inc_i} + \sum_{j=1}^{N_c} \sigma^2_{Coh^j_i}. \quad (1)$$

Coherent and incoherent noise sources are identified comparing the covariance matrix calculated from this expression and the measured covariance matrix.

For all ASICs, two sources of coherent noise were identified. Fig. 10 shows the noise of the first coherent source as a function of the channel number for one ASIC. This source affects only channels with an enabled preamplifier. Since the 64 preamplifiers have the same power supply, it could be the source of this coherent noise. The mean noise is between 2.2 and 2.7 ADC counts (723.3 and 887.7 e), depending on the ASIC. Fig. 11 shows the contribution of the second coherent source as a function of the channel number for one ASIC. This source affects all channels. The analogue signals of the 64 channels are converted at the same time in the ADC. Thus, the ADC could be the source of this coherent noise. The mean noise is between 0.7 ADC counts and 1 ADC counts (230.1 and 328.8 e) depending on the ASIC.

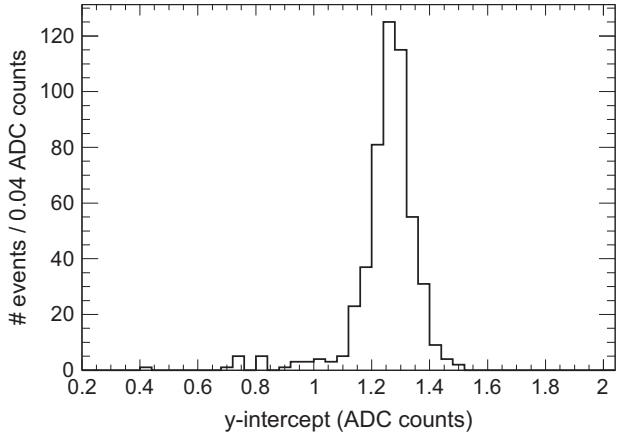

Fig. 8. The *y*-intercept of the linear fit introduced in Fig. 7 for all channels of all layers.

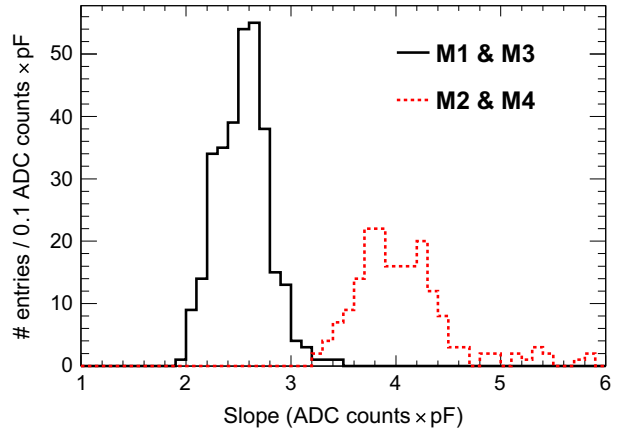

Fig. 9. The slope of the linear fit introduced in Fig. 7 for all channels of all layers. The solid black line corresponds to the M1 and M3 ASICs. The dashed red line corresponds to the M2 and M4 ASICs. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.)

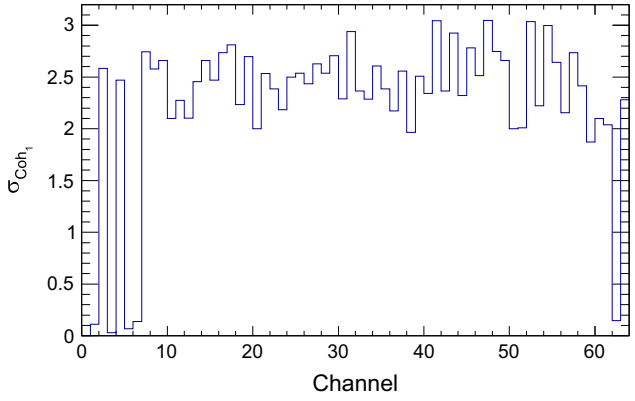

Fig. 10. Noise of the first coherent source as a function of the channel number for ASIC M1 (layer 3).

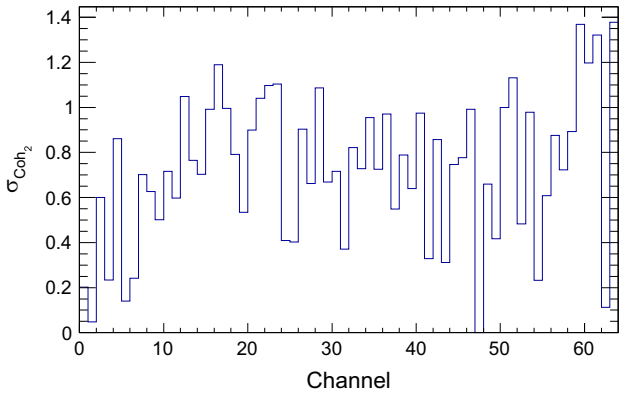

Fig. 11. Noise of the second coherent source as a function of the channel number for ASIC M1 (layer 3).

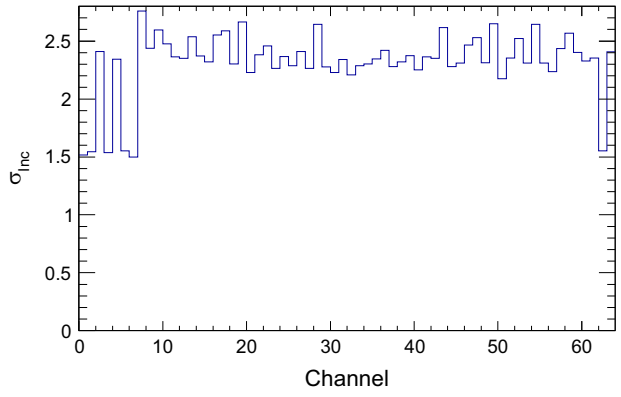

Fig. 12. Noise of the incoherent source as a function of the channel number for ASIC M1 (layer 3).

As shown in Fig. 12, the noise due to the incoherent sources is around 2.4 ADC counts (1.5 ADC counts) for channels with an enabled (disabled) preamplifier. The contribution of the coherent noise sources to the total noise (R_{Coh_1} and R_{Coh_2}) can be expressed as

$$R_{Coh_1} = 1 - \sqrt{\langle\sigma_{Inc}\rangle^2 + \langle\sigma_{Coh_2}\rangle^2} / \sqrt{\langle\sigma_{tot}\rangle^2} \approx 0.25 \quad (2)$$

$$R_{Coh_2} = 1 - \sqrt{\langle\sigma_{Inc}\rangle^2 + \langle\sigma_{Coh_1}\rangle^2} / \sqrt{\langle\sigma_{tot}\rangle^2} \approx 0.05. \quad (3)$$

The suppression of these sources of coherent noise may reduce the total noise by about 30%.

5. Response to Minimum Ionising Particles

The MIP detection efficiency was determined using beam electrons. For the detector without absorber, the 3 GeV electrons provided by DESY II can be considered as MIPs.

5.1. Reconstruction

During data taking, two types of fake events due to the ASIC design were observed: the first was due to the preamplifiers' sensitivity to the power supply, and the second was an artefact of the event validation logical sequence of the ASIC. These fake events were removed offline using timing information. Then, in each layer, adjacent hits were grouped into clusters. Clusters from the six layers were grouped using their time stamp, allowing for a tolerance on the BCID of +1. Since the detector was operated in self-triggering mode, events produced by the electron beam were separated from those induced by cosmic rays or electronic noise. The mean cluster position, the so-called barycentre, was calculated in the transverse plane. Clusters more than 3 cm from this barycentre were excluded. Events containing less that three layers with clusters were rejected. Finally, tracks were reconstructed using a 3D linear fit.

5.2. Simulation

The set-up described above was simulated using the GATE software [12] based on Geant4 [13]. The inter-pixel dead zones and the channels with disabled preamplifiers were taken into account. We developed a digitisation procedure to simulate charge collection in the silicon sensor, taking into account the generation of electron–hole pairs, drift in the electric field, diffusion, and a detailed description of the noise.

5.3. MIP calibration

The cell-by-cell energy calibration was carried out using beam electrons considered as MIPs. The pedestal and the noise were determined from the same data sets. For each channel, the pedestal was subtracted from the triggered hit energies. The distribution of triggered hit energy was fitted to a Landau function convoluted with a Gaussian if the distribution had more than 2000 events. The width of the Gaussian was fixed to the noise. The MIP position was determined from the Most Probable Value (MPV) of the Landau. An example for one cell is shown in Fig. 13.

The homogeneity of the detector response was checked by scanning the beam over the detector, using a feedback capacitance equal to 1.2 pF. Fig. 14 shows the MPV of all active channels. The MPVs are distributed normally with a RMS of 2.2 ADC counts, consistent with the results of the previous prototype [14]. The spread could be due to the channel by channel gain dispersion. As the trigger threshold and the trigger delay were a compromise between all channels of one ASIC, the delay time was not optimal for all channels. We expect to obtain an improved homogeneity by the individual adjustment of channels' trigger thresholds. The average width of the Landau is 5.1 ADC counts, consistent with the prediction of simulation.

The MPV as a function of the gain is plotted in Fig. 15 for one channel of one layer. The graph is fitted with a logarithmic function. As expected the amplitude of the MIP signal increases with increasing gain. The non-linear response is due to the fact that the trigger and timing settings were optimised only at the gain of 1/1.2 (1/pF).

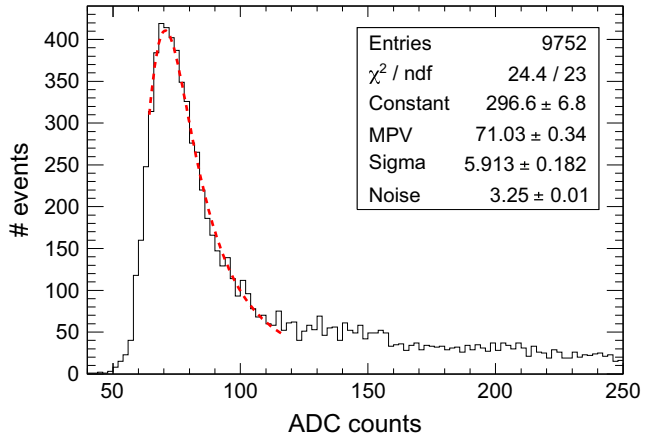

Fig. 13. MIP distribution in one channel after pedestal subtraction. The distribution is fitted using a Landau function convoluted with a Gaussian (dashed red line). (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.)

In the simulation, the most probable MIP energy deposition is 0.095 MeV. The energy calibration factor was defined as the ratio between the MIP MPV measured in the detector and the most probable MIP energy deposit predicted by simulation.

5.4. MIP detection efficiency

To measure the detection efficiency in a particular layer, events were required to have at least three additional hit layers. The efficiency was defined as the fraction of events with a cluster at a distance $d < 1$ cm from the track. The efficiency as a function of layer is shown in Fig. 16. The beam was normal to the detector and the angular spread was small, so geometrical effects due to the sensor borders and disabled channels were small, estimated using simulation to be less than 2%. The main effect on the detection efficiency was the trigger threshold. As explained in Section 3.1, the non-optimal PCB routing increased the spread of the effective trigger threshold. The detection efficiency was reduced due to the compromises necessary in the setting of trigger thresholds. The trigger threshold in the simulation was adjusted using the detection efficiency. Using simulations, the trigger threshold was estimated to be between 85% and 95% of the MIP MPV.

6. Signal to noise ratio

A typical single-channel signal distribution is shown in Fig. 17. The signal to noise ratio (S/N) was defined as the ratio between the MIP MPV and the noise. Fig. 18 shows S/N for several feedback capacitances, and for all active channels with sufficient statistics (2000 events). These distributions have a double peak structure, due to the noise pattern explained in Section 4.1. The measured S/N was found to be better than for the physics prototype (~7.5) for all the gain settings provided by the SKIROC2 ASIC.

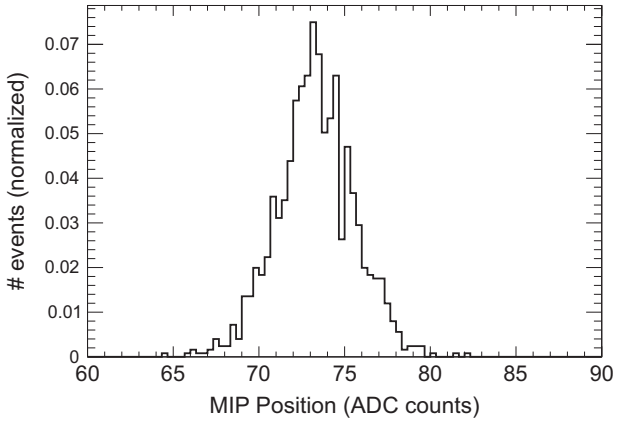

Fig. 14. MPV of the Landau fit for all active channels.

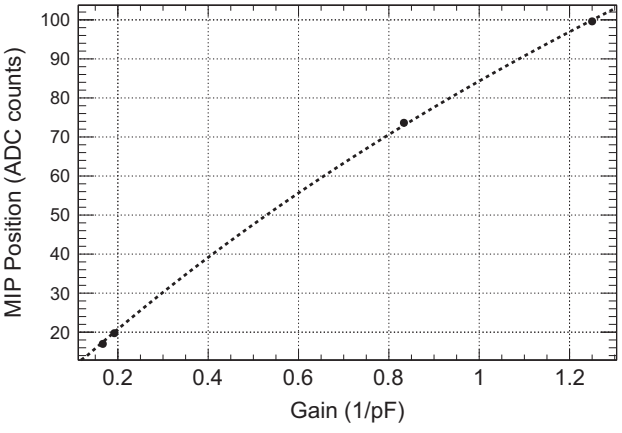

Fig. 15. The MPV as a function of the gain for one channel of one layer. The line is the result of a logarithmic fit.

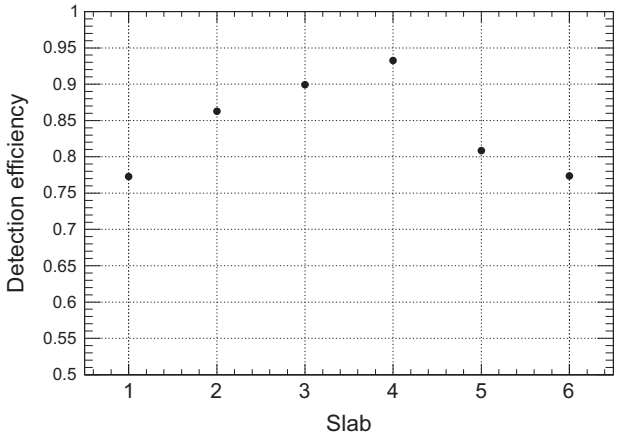

Fig. 16. Detection efficiency as a function of the layer number.

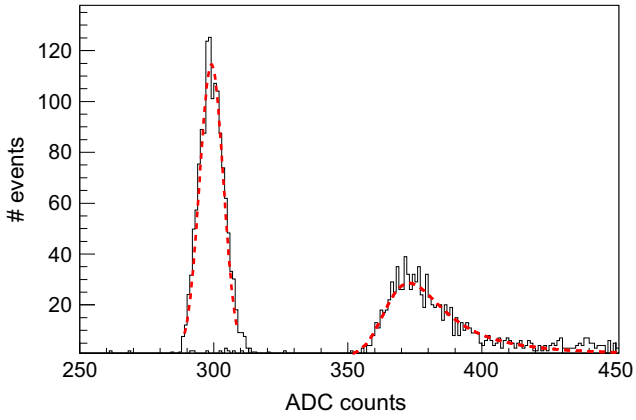

Fig. 17. Pedestal and MIP distribution for one channel. The feedback capacitance is 1.2 pF.

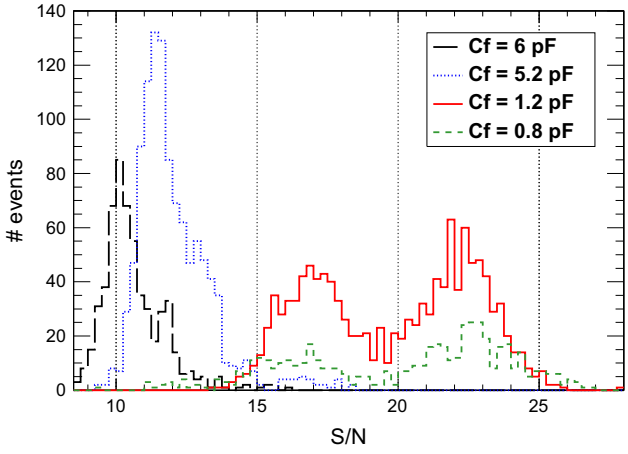

Fig. 18. Signal to noise ratio for all active channels for several feedback capacitances. Long dashed black line corresponds to C_f=6 pF. Dotted blue line corresponds to C_f=5.2 pF. Solid red line corresponds to C_f=1.2 pF. Dashed green line corresponds to C_f=0.8 pF. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.)

7. Conclusion

The R&D for a highly granular silicon–tungsten calorimeter is ongoing. After the proof-of-principle with a physics prototype, the technological prototype addresses the engineering challenges of the project. A central element of the detector is the embedded front end electronics, the SKIROC2 ASIC. This paper presents an analysis of the ASIC performance under test beam conditions.

The results were promising, observed shortcomings are instructive for improving the system. The signal to noise ratio was above 10:1 for all pre-amplifier gains of the ASIC, except for few channels using the lowest gain. This value is to be compared with the R&D goal of 10:1, and also with the value of 7.5:1 achieved by the physics prototype under similar operation conditions. A further improvement of about 30% can be expected after the suppression of sources of coherent noise. For the prototype described here, the excellent signal to noise ratio was compromised by too long connection lines on the interface card, a shortcoming that will be addressed in future versions of this card. A flaw of the current version of the SKIROC2 ASICs was the non-operational fine adjustment of the trigger thresholds. The individual channel trigger threshold adjustment and the improvement of the PCB routing are needed to reach 50% of the MIP position for all channels as required for the ECAL design.

The next step will be to study the performance of the SKIROC2 ASIC in power pulsed mode and to test the response of the ASIC over the entire dynamic range of 2500 MIPs. In order to make progress towards the final detector design, detection units with 16 ASICs and 4 sensors will soon be fabricated.

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