Readout Electronics of Silicon PIN Diode Arrays for CEPC ECAL – A Preliminary Study on Prototype System

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ABSTRACT: A readout system, based on SKIROC2 application-specific integrated circuit (ASIC), for silicon PIN diode array detectors, has been developed. The system, which is intended to explore the design concept of the Si-W electromagnetic calorimeter (ECAL) at Circular Electron Positron Collider (CEPC), consists of three kinds of electronics modules: the Front-end Board (FEB) modules, the data-interface (DIF) modules and a data collection module (DCM). The FEB, which carries the SKIROC2 ASIC and the silicon PIN diode arrays (S5980 from HAMAMATSU), is in charge of particle detection and analog to digital signal conversion. The DIF is designed to control the FEB and transfer data to DCM via optical fiber. The DCM gathers data from all DIFs and transmits data to the computer through gigabit ethernet interface. The equivalent noise levels of all the channels are below 0.4 fC, while most of them are below 0.2 fC. The dynamic range is up to +3000 fC with an integral non-liearity (INL) of 0.2 % and gain uniformity higher than 5%. The X-rays from a radioactive source (^{241}Am) and cosmic rays have been applied to assess the performance. The energy resolution with X-rays, at 59 keV, reaches up to 13.3 % (in RMS). The signal-to-noise ratio (SNR) is about 10.9 for minimum ionizing particle (MIP) signal, which satisfies the design requirements. The details of the readout system, together with preliminary results, are presented in this paper.

KEYWORDS: ECAL; CEPC; Prototype; Silicon PIN diode; Readout system; Data-acquisition, Modular electronics; Front-end electronics.

Contents

1. Introduction

The circular electron positron collider (CEPC) is a promising next-generation electron-positron collider [1] to produce Higgs boson, whose separation depends on the success of the particle flow concept [2], and making precise measurements of it. The CEPC calorimeters, such as electromagnetic calorimeter (ECAL) and hadron calorimeter (HCAL), are widely utilized for precise energy measurements of electrons, photons, taus and hadronic jets. In order to obtain the high energy resolution, the particles inside the jets should be separated and the tracks should be assigned to calorimeter clusters one by one. The high-granularity plays a critical role in determining the maximum capability of particle separation and silicon-tungsten-based ECAL (Si-W ECAL) is considered as a promising candidate for this type of applications.

According to the preliminary conceptual design report (Pre-CDR), the requirements towards the ECAL are an energy resolution of $16\%/\sqrt{E(GeV)}$ and an energy range up to 100 GeV [1]. The Si-W ECAL is a sampling calorimeter with tungsten absorber and highly segmented readout layers which are made of pixelated silicon PIN diode arrays. According to the simulated predictions for CEPC [3] and test results of CALICE ECAL physics prototype [4,5] for international linear collider (ILC) [6], the Si-W ECAL for CEPC requires dozens of layers of silicon PIN diode pad arrays , where the size of each pad of silicon PIN should be about 1×1 cm^2 or even smaller, which leads to a total number of tens of millions electronic channels.
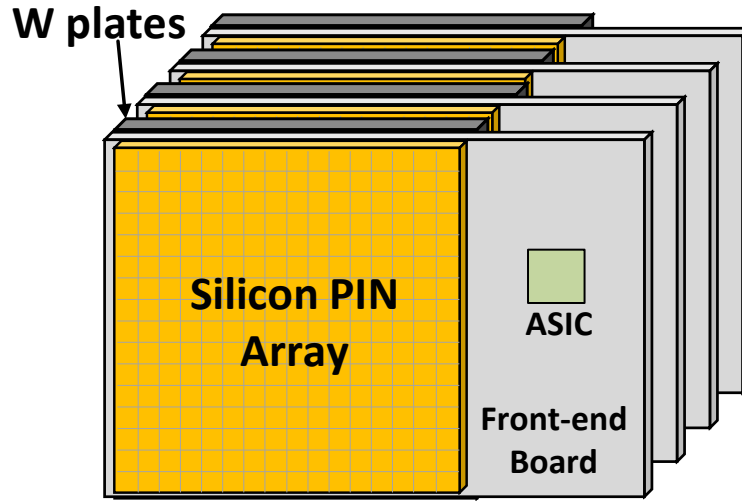
Figure 1. The cascading relationship of ECAL prototype.

We aimed to design a small prototype to study the principle and verify the key techniques of Si-W ECAL for CEPC. The cascading relationship outline of the prototype is shown in Figure 1. This prototype has dozens of layers with pixelated silicon PIN arrays and a readout system with multi-channels and scalable features. The readout channel of each silicon PIN pad should have enough signal-to-noise ratio (SNR) and energy range for at least 500 MIPs. To meet these requirements, the readout electronics are expected to have an equivalent noise level of better than 1 fC and a linear range up to at least +2000 fC, considering the equivalent charge of MIP is about 4 fC [5]. In addition, the high-level integration should be carried out with minimal power consumption (< 10 mW / channel).

Based on the requirements mentioned above, a multi-channel and scalable readout system is currently being developed to test the performance of silicon PIN diodes and pre-design the prototype. Details of the readout system and preliminary test results are presented below.

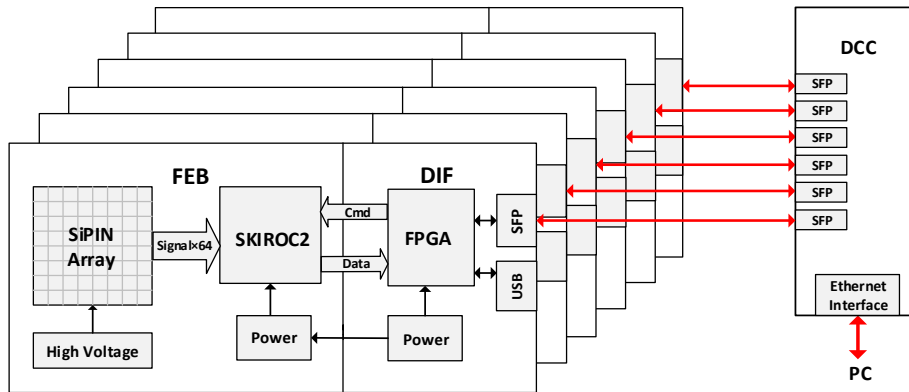## 2. System implement

2.1 Architecture

Figure 2. The architecture of the readout electronics system

The architecture of the designed system is shown in Figure 2. It consists of three kinds of modules, the detector and ASIC module called front-end board module (FEB), the data interface module (DIF) and the data concentration module (DCM). The FEB receives and digitizes the signal from the detectors and supplies high voltage. It is configured by the DIF and drives data to the latter, which then are transferred to the DCM via optical fiber after packing process. Each DIF and FEB pair is responsible for a single layer. The DCM is in charge of sending commands to DIFs, collecting data from different DIFs, making compression and transferring data to PC. In this study, a prototype based on the architecture mentioned above, with up to six layers of detector arrays, is implemented.

2.2 ASIC

The core of the FEB is the SKIROC2 (**S**ilicon **K**alorimeter **I**ntegrated **R**ead**O**ut **C**hip **2**) chip designed by the IN2P3/OMEGA group from France. The SKIROC2 is an ASIC for the **I**nternational **L**arge **D**etector (ILD) [8] Si-W ECAL. Figure 3 presents the schematic illustration of SKIROC2, where 64 channels are integrated on one chip. Each channel is composed of a charge-sensitive amplifier (CSA), two slow shapers with different gains, one fast shaper with a discriminator, a time-to-digital convertor (TDC) for time measurement, three switched capacitor arrays (SCA) of 15 depth to store analog signal and an ADC to convert signal from analog to digital.
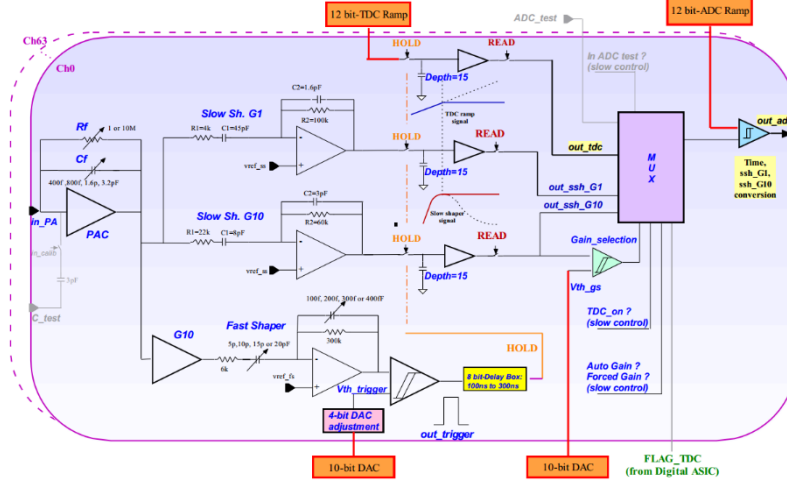

Figure 3. The schematic illustration of the analog part of the SKIROC2

The input signal passes through the CSA with the variable gain set by switchable feedback capacitance (C_f) array. The output of CSA is fed to the fast and slow shapers. By comparing fast shaper's output with a threshold, the discriminator generates a trigger signal to hold the voltages at two slow shaper outputs, which are optimized for low-noise charge measurement, on the SCAs. The signals on the SCAs are read out and converted by a 12-bit Wilkinson ADC and a multiplexer, with a bunch ID tagged on a 10 MHz clock, then saved in the on-chip memory.

Benefited from the two different-gain slow shapers and the adjustable gain CSA, the SKIROC2 has a wide dynamic range, ensuring a linear response for 1–1500 MIP signals. The peak time is tuneable between 50 ns and 100 ns and the power consumption is about 6 mW per channel. These features meet the requirements of the Si-W prototype. As a result, the SKIROC2 is chosen as readout chip of the system.

2.3 Front-end Board

In the current phase, the FEB accommodates one SKIROC2 chip to read 64 detector signals. The silicon PIN detector S5980 from HAMAMATSU, which has four outputs from the anode of the diode and one common cathode, is one of the ideal candidate detectors for the prototype [9]. The total active area is 5×5 mm^2 and the thickness of depletion layer is 460 μm. Moreover, its dark current and terminal capacitance meet the input requirements of SKIROC2. According to the Geant4 simulation results, the cosmic MIP signal of the S5980 is about 7.5 fC. The schematic illustration of detector, assembled with ASIC, is presented in Figure 4. To make the best use of SKIROC2 inputs, the detectors are assembled in form an 8×8 array, which implies that the total active area of detector is 1600 mm^2. The S5980 claims a high-voltage of 13 V. Since output noise is very sensitive to the high voltage ripples, a well-designed low-dropout regulator (LDO, TPS7A4700) [10], from Texas Instruments company (TI), is employed with the low power supply ripple rejection (82 dB) and output noise (4 μVrms). The SKIROC2's input supplies a reference voltage about 1 V to ensure the correct working status of the detector.
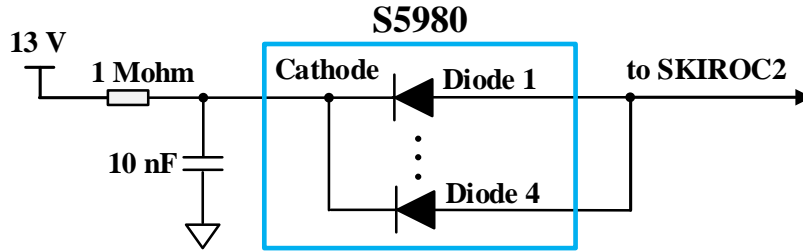

Figure 4. A schematic illustration of connection of silicon PIN S5980

After acquisition and convertion phase, the signals from the silicon PIN diode array are converted, from analog to digital, by SKIROC2 and stored in memory on chip, waiting to be readout. The SKIROC2 is controlled by field-programmable gate array (FPGA) on DIF. There are two kinds of control data bus, depending on the speed; fast control and slow control. The fast control buses, which work through low voltage differential signal (LVDS) pairs, are in charge of SKIROC2's clock, trigger and reset or valid the SCA. On the other hand, the slow control is in a daisy chain cascade and configures 616-bits registers on chip to store many configurations such as C_f and trigger mode. The DIF controls the ASIC on FEB to readout memory data and transmit them to DIF over open collector (OC) gate. Considering the OC gate and daisy chain cascade, it is very convenient to expend FEB for more detectors and ASICs without changing the interface definition to DIF. The DIF also supplies an initial voltage of 5 V to FEB.
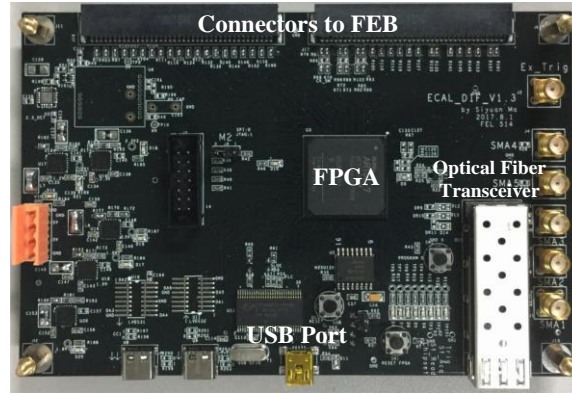
2.4 Data Interface

Figure 5. Picture of DIF

The digital photograph of the DIF is shown in Figure 5. The DIF consists of four main parts; FPGA, connector, power supply and interface.

The FPGA is composed of an FPGA (ARTIX7, Xilinx) and a flash programmable read only memory (PROM, N25Q128). The function of FPGA is to implement the required logic to control FEB and to communicate with DCM board or PC directly. The logic diagram is presented in Figure 6. The acquisition module controls the ASIC to work in the normal mode and get data saved in SKIROC2. The data transferred into FPGA is stored in the first-in-first-out (FIFO) memory and transferred to DCM or PC. The trigger module is in charge of generating a trigger when working in calibration mode or ex-trigger mode. The calibration module and S-curve module are used to control the ASIC during calibration or testing, which discussed below. The optical module transmits data from FIFO to DCM and gets a command from DCM via optical fiber. The transmission is based on the high-speed transceiver GTP on FPGA. However, the USB module is used to communicate with PC, when debugging a single DIF.
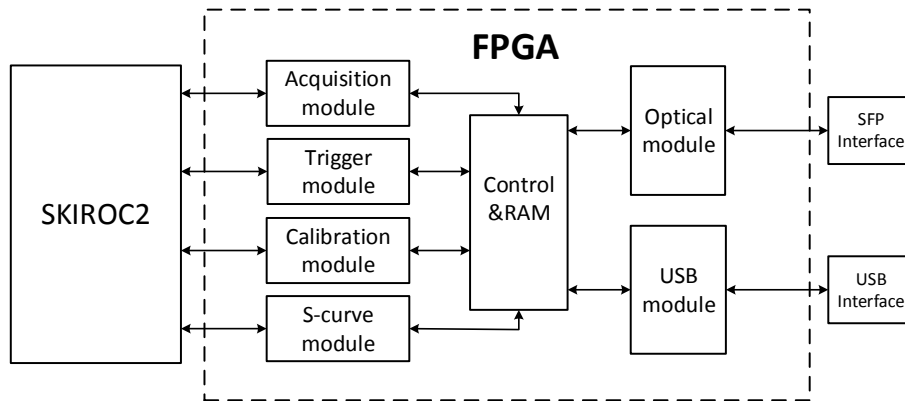

Figure 6. Block diagram of logic implemented in the FPGA

The communication with FEB is via two ERNI-154744 connectors [11]. All control and reply signals, as well as initial power supply for FEB, pass through these two connectors. The interface part is composed of a 1 Gbps bidirectional small form-factor pluggable (SFP) optical transceiver and a USB interface realized by a USB chip CY7C68013 and a Mini-USB port. The

supply part is implemented with a DC input (5 V) from outside and several LDO regulators (TPS74401, TI). From this DC supply rail, the analog power supplies are generated for DIF.
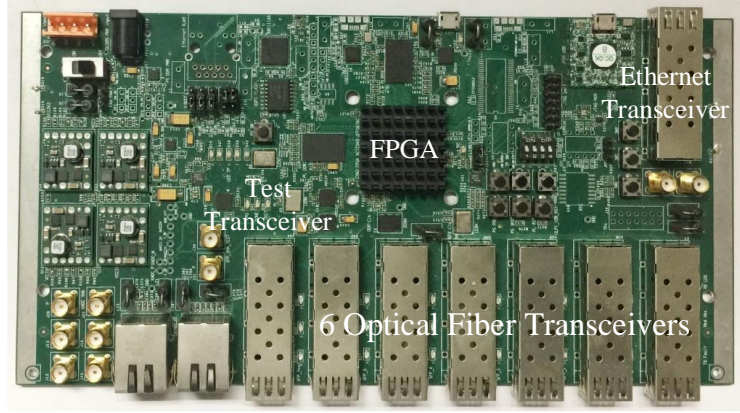
2.5 Data Concentration Module

Figure 7. The digital photograph of DCM

The function of DCM board is to gather data from DIFs via optical fibers and to transmit the received data to the PC server via a gigabit standard Ethernet network cable (RJ45). The current readout system is based on the DCM designed for PandaX-III prototype TPC [12]. The picture of DCM is shown in Figure 7. It contains an FPGA of Zynq-7, a 4 Gbits DDR3 SDRAM for data buffering, a SFP for Ethernet transmission and six SFPs for optical fibers, which means one DCM carries six DIFs. The SFPs are implemented with FPGA-based gigabit transceiver GTX to read DIF data and send commands to DIFs. This DCM has been used in the PandaX-III prototype readout system and showed sufficient data bandwidth and stable performance [13].

3. Characterization

We have carried out a number of characterizations to assess the performance of readout system. The results of baseline noise and calibration of SKIROC2, trigger efficiency, X-ray test and cosmic test are presented and discussed below.

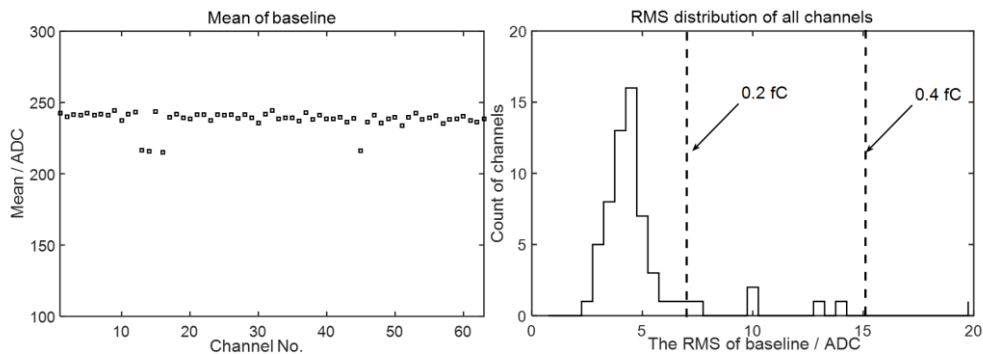### 3.1 Baseline and noise

Figure 8. The baseline and noise distribution of all 64 channels

In order to evaluate the noise level of the electronic system, the external trigger function of SKIROC2 was used to get the pedestal of the system without detectors. The DIF generated

triggers in a fixed time interval (10 ms) to FEB, controlling the acquisition of baseline. The time required by SKIROC2 for conversion phase and readout phase is 4 ms. SKIROC2 held the baselines of all 64 channels and converted them to digital signal when triggered. Figure 8 shows the average of baselines and sigma of noise from all channels. It worth nothing that not all channels exhibited excellent baseline and noise results, but most channels demonstrated the noise level lower than 0.2 fC equivalent input charge. The maximum noise level was less than 0.4 fC. As mentioned earlier, the S5980's MIP signal was about 7.5 fC and the obtained noise level satisfies the requirements.
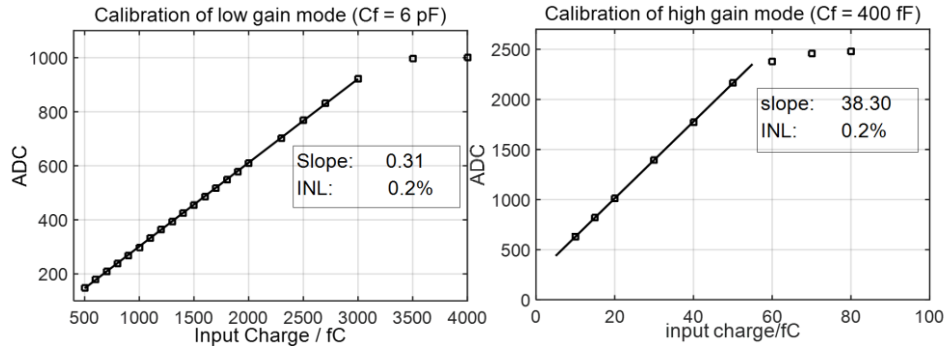
3.2 Calibration

Figure 9. The linear fit results of two gain modes of SKIROC2

The calibration assessment was carried out to obtain the linearity and dynamic range of SKIROC2. By taking advantaging of the SKIROC2's 3 pF calibration capacitors on each channel, the self-calibration was conducted by the procedure mentioned below. A waveform generator with attenuator was used to generate step pulses with different amplitudes. When the step pulses were applied to the on-chip capacitor, a certain amount of charge, which covered the full range, was injected into every channel of SKIROC2 from test pulse input for performance assessment. The SKIROC2 had many operation modes by tuning the C_f array. The measurement was carried out with the highest gain mode (C_f = 400 fF) and lowest gain mode (C_f = 6 pF). The gain uniformity between different channels was better than 5% and the typical linear curves of output ADC code versus input charge, of the two modes, are shown in Figure 9. Figure 9 shows that the linear range of the highest gain mode and the lowest gain mode were 50 fC and 3 pC, respectively. The Integral non-linearities (INL) of both modes reached up to 0.2%.
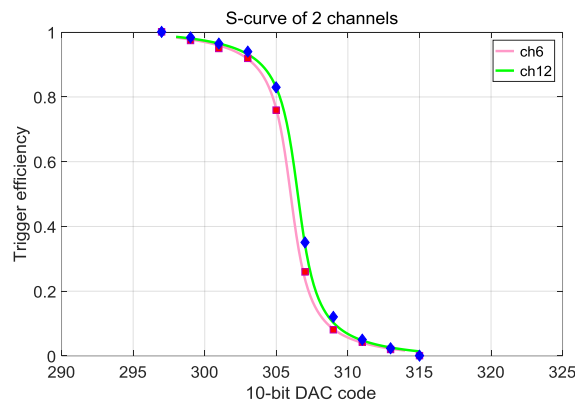
3.3 Trigger efficiency

Figure 10. The S-curve of 2 channels when input is 2 fC

The trigger efficiency was obtained via the "S-curve" and presented in Figure 10. The trigger threshold was set by two digital-to-analog conversion (DAC) settings; a global threshold with a 10-bit DAC and channel by channel adjustment with 4-bit DAC. To measure the trigger efficiency, a fixed amount of charge was introduced from the test pulse input. If the fast shaper pulse exceeded the threshold, the SKIROC2 would output trigger signal for counting. The S-curve was obtained by varying the trigger threshold 10-bit DAC and recording the efficiency at each DAC code. The curve was fitted by a complementary error function, where centre value corresponds to the threshold on the charge and the sigma represents the noise power. The 4-bit DAC adjustment for every channel should help to get a better threshold uniformity, but this function did not work properly in SKIROC2 due to a detected bug, which has been fixed in newer version of SKIROC2a.
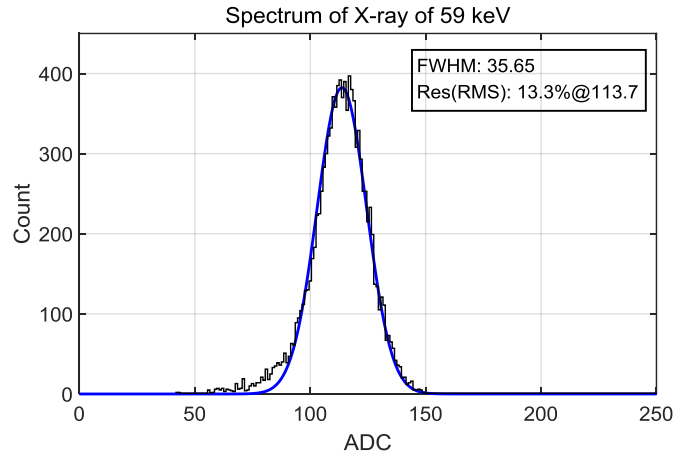
3.4 X-ray test

Figure 11. The spectrum of X-ray of ^{241}Am

The joint test with X-ray source of ^{241}Am was carried out. A bias voltage of 13 V was applied, as the high voltage, on the silicon PIN detectors S5980. The output signals were directly sent to SKIROC2, which was set to work in highest gain mode. In Figure 11, the spectrum of 59 keV X-ray is shown. According to the calibration results, the equivalent input charge was 2.89 fC and resolution was 13.3% (in RMS). Considering the fact that the total energy of X-ray was 59 keV and the charge of 2.89 fC indicated 18109 electron-hole pairs, the ionization energy of silicon PIN diode was 3.25 eV. It was lower than the theoretical value of 3.6 eV, which seems reasonable when Fano factor is considered. This test shows that the system had enough resolution to identify small signals such as X-rays and MIP.
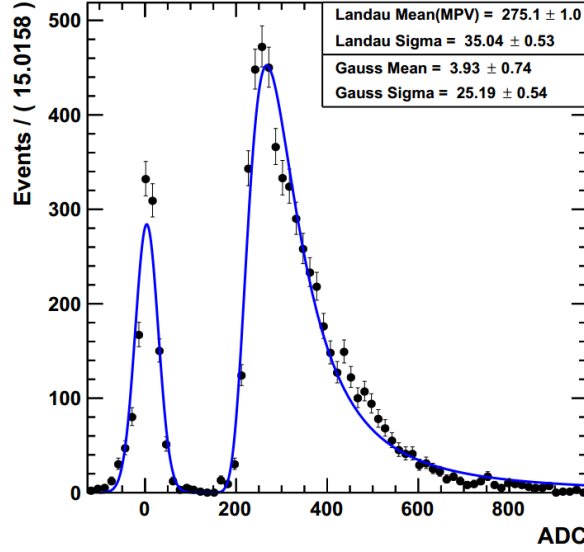
3.5 Cosmic ray test

Figure 12. The spectrum of cosmic ray

A simple cosmic test with one layer silicon PIN array was carried out. The 64 silicon PIN detectors of S5980 were installed to get cosmic muons. Figure 12 shows the first result obtained with this system. Since there was no coincidence to filter the cosmic ray, the input angle had a wide distribution from 0° to 90°. The spectrum of cosmic ray was Landau fitted and the pedestal was Gaussian fitted. The results of the fits show that the most probable value (MPV) of cosmic muon's equivalent input charge was 7.24 fC and the SNR was 10.9. The SNR is very close to the test result of CALICE ECAL physics prototype [5] and satisfies the requirement of the current phase, but considering the linear range of 3000 fC, the system didn't meet the required demand of 500 MIPs. This can be improved further by applying silicon PIN diodes with thinner depletion layer.

4. Conclusions

In this paper, a prototype readout electronics based on SKIROC2 for silicon PIN detectors has been presented. The system was intended to explore the design concept of the prototype of Si-W ECAL for CEPC and consisted of FEB, DIF and DCM modules. The system is scalable due to the modular structure and the characteristics of SKIROC2 ASIC. The performance assessment of the system is discussed in detail. The joint tests with X-ray and cosmic ray showed encouraging results of resolution. This study provides the basis for the implementation of a system with six layers of silicon PIN array and tungsten absorber in next step. In addition, a shower test will be carried out and system performance shall be optimized in future studies.

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