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2017 JINST 12 T04009

(http://iopscience.iop.org/1748-0221/12/04/T04009)

Published by IOP Publishing for Sissa Medialab

Received: *November 13, 2016*
Revised: *April 5, 2017*
Accepted: *April 10, 2017*
Published: *April 20, 2017*

TECHNICAL REPORT

2017 JINST 12 T04009

Transient waveform recording utilizing TARGET7 ASIC

J. Zhang, S. Liu,[1] Y. Wang, C. Yang, X. Zhu, C. Feng and Q. An

State Key Laboratory of Particle Detection and Electronics,
University of Science and Technology of China,
Jinzhai Road, Hefei, 230026, China
Department of Modern Physics, University of Science and Technology of China,
Jinzhai Road, Hefei, 230026, China

E-mail: liushb@ustc.edu.cn

Abstract: TARGET7, the 7th-generation TeV Array Readout with GSPS (Gigabit Samples Per Second) sampling and Experimental Trigger ASIC, has been initially designed to monolithically and inexpensively instrument large deployments of semiconductor photon detectors for large neutrino and muon detectors. It is a switched capacitor array (SCA) based transient waveform recorder with 3-dB bandwidth of 500 MHz; a large dynamic range of 1.8 V; high sampling rate (typically 1 GSPS); high channel density (16 channels per ASIC); low power consumption (< 10 mW/channel) and deep analog storage buffer (16,384 samples per channel). Moreover, each channel has an integrated Wilkinson ADC (Analog-to-Digital Convertor) for digitization. In this paper, a test board with the chip is described. Calibration methods, timing performance as well as its application possibility in charge measurement with a comparison to an oscilloscope are studied.

Keywords: Analogue electronic circuits; Data acquisition circuits; Front-end electronics for detector readout

[1]Corresponding author.

doi:10.1088/1748-0221/12/04/T04009

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1 Introduction

In many fields, especially in particle physics experiments, high speed waveform digitization is the most direct and effective method for extracting event information. Experiments demand new waveform digitizing methods to satisfy the increasing channel densities and low power consumption requirements at affordable cost. The employment of switched capacitor array (SCA) techniques in CMOS processes has been widely adopted in the area of waveform recording. For at least two decades, a number of SCA devices with sampling speeds in GSPS have been reported. With typical power consumptions of 10 mW per channel, these chips are excellent alternatives for commercial flash-ADCs. However, all the SCAs share the disadvantages that the analog storage depth is quite limited and the time required to read out the capacitor cells causes large dead time, which limit their fields of application.

For years SCAs have been successfully used in high energy physics. For instance, the ATWD was adopted in the AMANDA experiment [1, 2], the ARS0 and ARS1 were employed in the ANTARES experiment [3–5], the DRS was used in the MEG experiment [6, 8], and the LABRADOR was applied in the ANITA experiment [9, 10].

As a new version of the TARGET ASIC series [11], TARGET7 was designed by IDLab (Instrumentation Development Lab), University of Hawaii. Compared with those SCAs that sample, store, and readout analog signals in the same set of switched capacitors, signal sampling and storage processes are separate in TARGET7 in order to simultaneously achieve large analog bandwidth and a deep storage buffer of 16,384 cells for per channel. The total 256 k storage cells on one chip make it suitable for experiments which need a relatively long waveform record.

2 Design of the test board

2.1 Introduction to TARGET7

The functional block diagram is shown in figure 1. It is mainly composed of three parts: analog signal input, sampling & storage, and digitization.

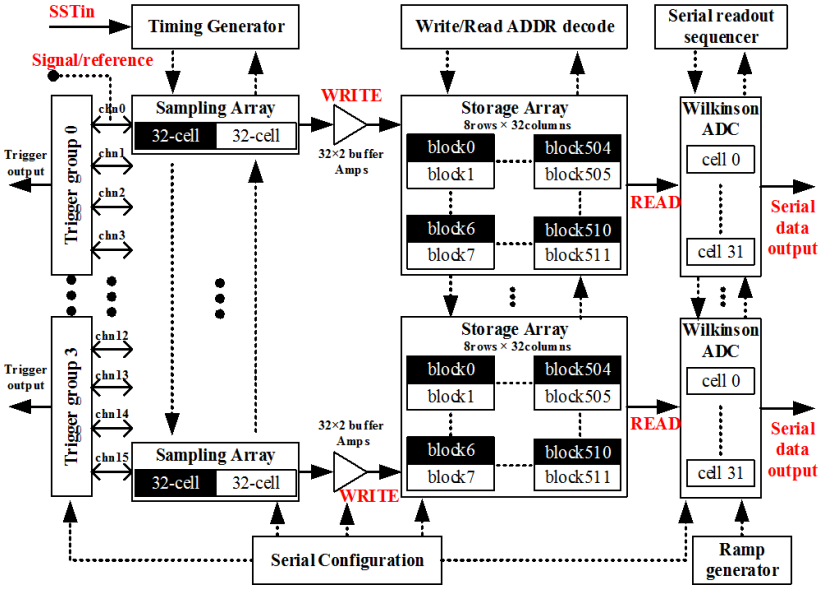

Figure 1. Functional block diagram of TARGET7.

2.1.1 Analog signal input

The TARGET7 chip implements 16 channels where both an input signal and its reference signal are connected to the ASIC. In order to provide a well-defined impedance into the Sampling Array on die, the reference input should be a DC level, while the input signal should be terminated to this voltage level. All channels are processed into 4 trigger groups with each triggering on the sum of four channels.

2.1.2 Sampling & storage

A Sampling Time-base generator uses inverter chains as delay lines to boost the sampling speed into GSPS, and controls the sampling of signals into dual groups of 32 sampling cells per channel. Using a ping-pong operation strategy, the samples are transferred from one group of 32 cells to storage while the other group is sampling, with the roles reversed in the next half sampling cycle. When acquisition occurs in one group of 32 cells of the Sampling Array, the other group are being amplified and buffered and then written into the Storage Array. The Storage Array contains 512 groups of 32 cells, which are arranged in 8 rows and 32 columns. In cooperation with an address decoder, groups of 32 cells are randomly accessed for digitization by integrated Wilkinson ADCs.

2.1.3 Digitization

Once one group of 32 cells is selected in the Storage Array, the 32 storage cells in all 16 channels are prepared for Wilkinson ADC conversion. A Wilkinson ramp generator block generates and broadcasts a ramp signal to all channels. Then a 12-bit ripple counter is activated for each channel. When the voltage ramp crosses the comparator threshold, the counter stops and the count value then represents the time corresponding to the voltage held in the storage cell. Address decoding and sequencing are performed by a serial readout sequencer block. Digitized samples are selected and then serially transferred in all 16 channels in parallel.

2.2 TARGET7 test board

With the benefits from integrated Wilkinson ADCs and a serial configuration block, the TARGET7 can be allowed to operate with a minimum number of external components required. As shown in figure 2, it features an ASIC and a Field-Programmable Gate Array (FPGA) as well as some ancillary components essential to support them. In the test board, a multi-channel DAC (LTC2614) followed by analog buffers is employed instead of a fixed DC level in order to make reference input signal flexible. AC-coupled input signals are terminated to the reference input by a 50 Ω resistor, with a pair of protection diodes followed to protect the chip from Electro-Static discharge (ESD). The desired sampling rate of the TARGET7 is adjusted by the period of 'SSTin' clock which is the reference clock signal of the Sampling Time-base generator. As there are 64 sample stages, the sampling rate for a given 'SSTin' clock can be easily derived as

$$f_{\text{sample}} = 64 \cdot f_{\text{SSTin}}, \tag{2.1}$$

where f_{sample} is the sampling rate and f_{SSTin} is the frequency of 'SSTin' clock generated by the FPGA. The ramping voltage for Wilkinson conversion is generated by using an internal charging current and an external 200 pF ramp capacitor. The counting clock 'WLCLK' of the Wilkinson conversion, which is also generated by the FPGA, drives a 12-bit ripple counter. Once the ramp threshold is crossed in a certain cell, the current count value is latched. Digitized results from all 16 channels are collected in parallel and then transferred to a host PC via a USB2.0 interface chip (CY7C68013A) which is controlled by the FPGA. The control and data acquisition are implemented by a custom designed graphic user interface (GUI) software based on windows presentation foundation (WPF).

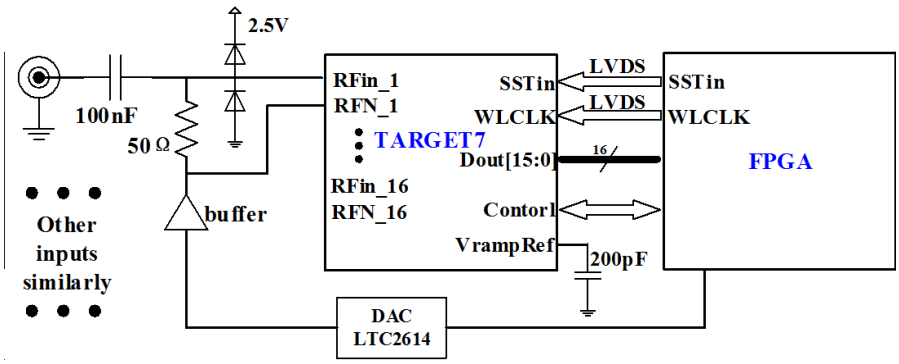

Figure 2. Block diagram of the TARGET7 test board.

2.3 Performance

2.3.1 DC transfer function

The TARGET7 is operating with a single power supply (+2.5 V). The sampling rate of the chip is set at a constant value of 1 GSPS. For a given internal charging current of Wilkinson ADC, a fast Wilkinson counting rate will result in a better resolution and a less dead time, but a limited dynamic range is also produced because of overflow of the 12-bit counter at large input voltages. Therefore, a tradeoff should be made between dynamic range, resolution and dead time [12]. Figure 3 shows the DC transfer function for a single channel of TARGET7 with an ideal Wilkinson counting rate found to be 95 MHz. It measures ADC counts as a function of input DC voltages. The dynamic range is found to be 1.8 V (spanning 0.5 to 2.3 V) which spans 552 to 3785 ADC counts, corresponding to 3233 counts (~ 11.6 bits) of resolution. After voltage calibration, the DC noise is measured to be 1.76 mV (~ 1.6 least-significant bits). The effective dynamic range is therefore about 10 bits.

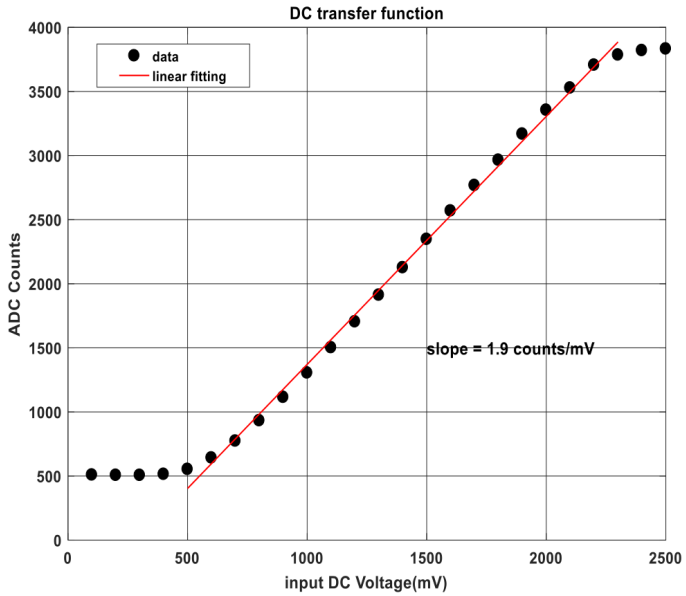

Figure 3. The DC transfer function for a single channel at a Wilkinson counting rate of 95 MHz. The mean data distributed in the figure are measured with the mean value of all 16,384 cells. The best linear fitting curve (spanning 0.5 to 2.3 V) has a slope of 1.9 counts/mV.

2.3.2 Voltage calibration

All 16,384 storage cells show different offsets to a DC input after digitization. In order to obtain a "clean" signal, these offsets must be measured with a zero input signal and then removed from every measurement, which we call "pedestal subtraction". Besides offsets, variations from cell to cell also cause voltage errors. Hence, calibration should be carried out for each cell individually. Polynomial parameterization (3rd order) is evaluated and applied to all the storage cells. Figure 4(a) depicts a DC response for a particular cell and the relationship between input and measured voltages after voltage calibration. Figure 4(b) shows a sinusoidal signal (20 MHz, 200 mVp-p) recorded by TARGET7 before and after voltage calibration. Obviously, the measurement waveform is efficiently improved after voltage calibration.

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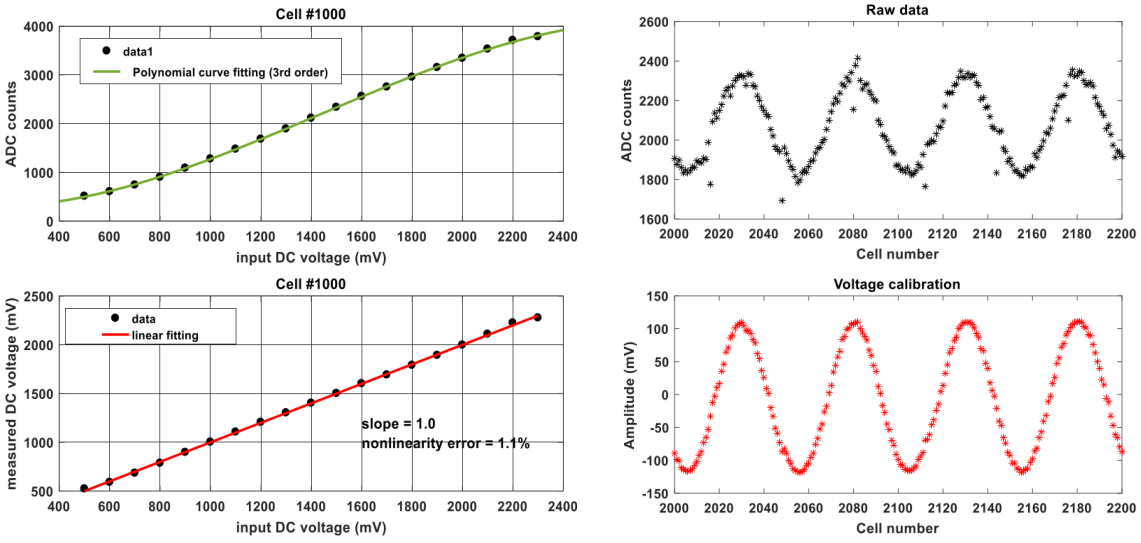

(a) (b)

Figure 4. (a) DC response for a particular cell (cell #1000) and the relationship between input and measured voltages after calibration. The linear fitting curve has a slope of 1.0 with a nonlinearity error of 1.1%. (b) A sinusoidal signal recorded by TARGET7 before and after voltage calibration. The raw data in the figure are recorded with ADC counts. After calibration, they are converted to amplitude.

2.3.3 AC saturation

The ASIC response is also evaluated using sinusoidal signals from a signal generator calibrated with the voltage calibration method. By scanning the input AC amplitude and comparing to the measured amplitude, the "AC transfer function" is shown in figure 5. As shown in the figure, for low amplitude (< 600 mV or 1.2 Vp-p) signals, gain loss due to the finite bandwidth becomes large as the frequency increases, which matches the previous results [13]. For signals of high amplitude (> 600 mV), AC saturation effect is observed. Compared with the finite bandwidth effect, AC saturation effect is negligible for high frequency signals.

2.3.4 Timing performance

We demonstrated timing resolution by measuring time difference, which is brought by different cables, at two different channels. Note that, timing resolution depends on different methods, especially for SCAs. If the delay introduced by different cables is larger enough that covers more cells, the non-linearity error due to non-uniform time base is more obvious, therefore, timing resolution becomes large [14].

Our procedure is as follows. Pulses with a pulse repetition frequency of 10 MHz from a function generator (AFG3252) are split into two branches, which are connected into two different channels (chn#5 and #6) of TARGET7 via two cables of different lengths (one is 1 m long, the other is 5 m) respectively. Thus, over 100 pulses distributed on 16,384 cells would be recorded at the same time. Time difference is measured sufficiently based on different cells. Triggers are also provided by the function generator for the on-chip complicated triggering scheme, which is based on the analog

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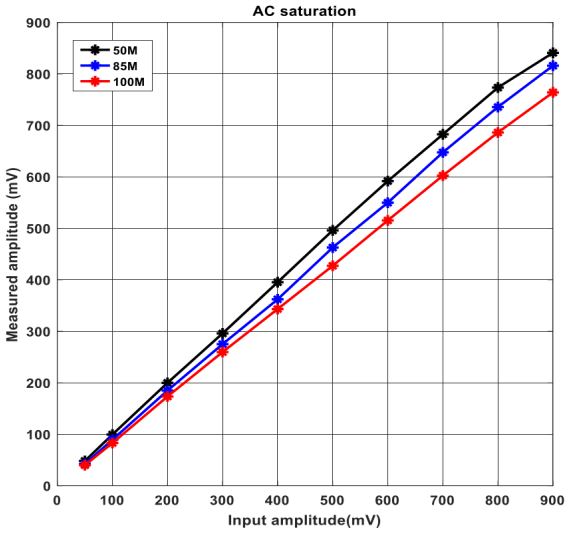

Figure 5. Measured sinusoid amplitude, as a function of input amplitude. Sinusoidal signals input with an on-board reference input set to 1.4 V. Measured amplitudes from fitted sinusoid are averaged over 20 times.

sum of signals in four adjacent channels and is specially designed for Cherenkov Telescope Array (CTA). Pulses of the two channels were recorded at the same time, and a typical merged waveform after voltage calibration is shown in figure 6(a). The pulse amplitude of chn#6 is less than chn#5 because of the attenuation caused by long cable. The time difference is determined at a constant fraction of the signal level (50% of the amplitude of chn#5), and the time difference between the two channels is calculated. As shown in figure 6(b), through nearly 5000 times of measurements, the cable delay is found to be 19.4 ns with a timing resolution of 152 ps in RMS. The cable delay is also measured on an oscilloscope with a timing resolution lower than 100 ps in RMS.

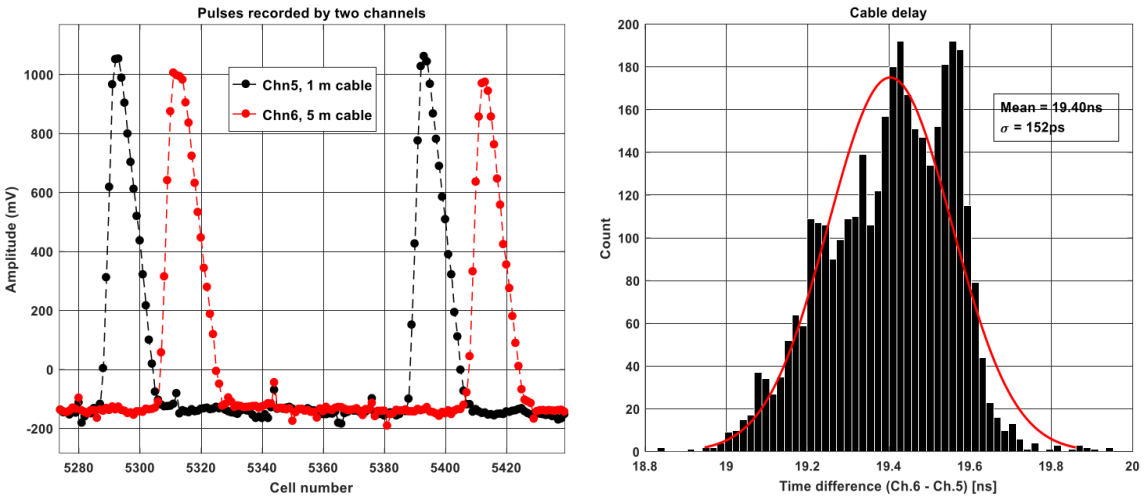

Figure 6. (a) Pulses recorded by two channels of TARGET7. (b) Time difference between two channels.

3 An application in charge measurement

An experiment is carried to demonstrate the performance of TARGET7 in charge measurement. Figure 7 shows the schematic diagram of the experiment. In order to simulate charge injection, negative voltage steps (leading: 2.5 ns, trailing: 6 μs) with a repetition frequency of 100 kHz from a function generator inject in a low noise charge-sensitive amplifier (CSA) through a 500 fF capacitor. A 50 Ω resistor is required for the cable adaptation. Thus, a 1mV-step in 500 fF simulates an injected charge of 0.5 fC. A following attenuator is necessary for low charge injection as the function generator can't be set to such a low voltage step. The output of the CSA is shaped through a CR-RC shaper with a gain of 4 and a peaking time of 100 ns, and then recorded by TARGET7 or an oscilloscope.

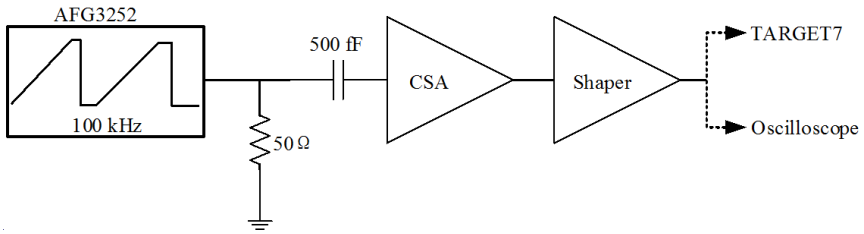

Figure 7. Schematic diagram of charge measurement experiment.

Figure 8(a) shows a typical output of the shaper recorded by TARGET7 versus an oscilloscope (Lecroy, WavePro715Zi) with a sampling rate of 1 GSPS when the injected charge is 50 fC. The 2 pulses shown in the figure are well matched with a peaking time of 100 ns. Compared with the oscilloscope, the result of TARGET7 has a lower noise level. In addition, a fine charge input scan (2 fC ~ 130 fC) is undertaken for sufficient comparison. As shown in figure 8(b), the measured amplitudes of the shaper output for both TARGET7 and the oscilloscope increase linearly with the input charge as expected. The drop due to limited dynamic range at 130 fC charge input for TARGET7 is observed as the reference input is 1.7 V. Linear fitting curves for both of them at a range of 2 fC ~ 120 fC have a same slope of 9.5 mV/fC but different nonlinearity errors. The result of TARGET7 has a nonlinearity error of 0.6% which is better than that of the oscilloscope.

4 Discussion

The separate sampling and storage in TARGET7 can be a new trend in SCA field, which needs a deep storage buffer without directly driving a large capacitance of the deep buffer on the input that will limit its bandwidth. In addition, the applications of TARGET7 are flexible. For some experiments which don't need an input dynamic range as large as 1.8 V, the Wilkinson counting rate could be set higher to achieve a better resolution by sacrificing the dynamic range. The maximum Wilkinson counting rate is capable of reaching as high as 208 MHz [15]. For positive or negative input signal, it is easy to fit the signal within the input dynamic range by adjusting the reference DC input. For using such SCAs, calibration methods are significant. A simplified calibration method which uses just a single average result as described in DC transfer function to calibrate all cells will cause large attenuation in voltage measurement. In next step, more efforts will be made for further calibration. New calibration methods are under investigation to make measurements more precise.

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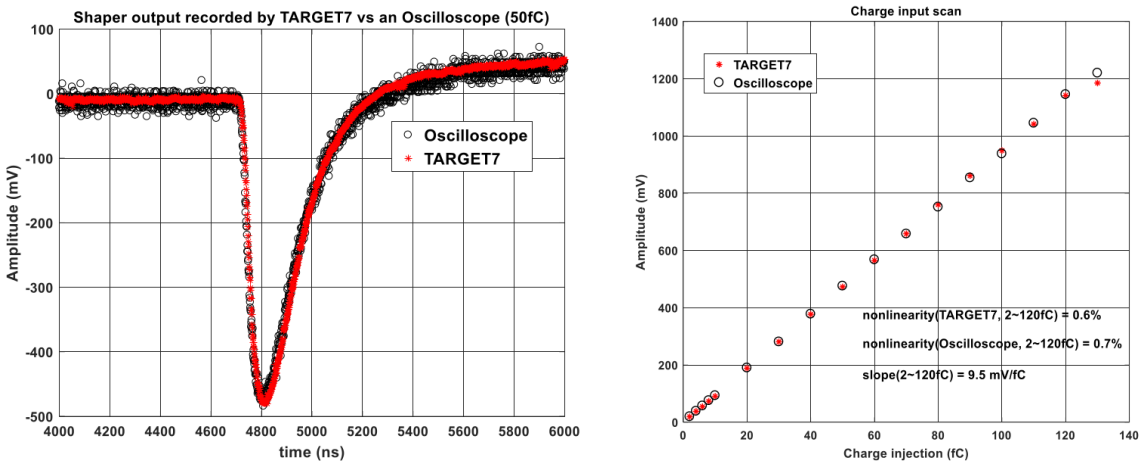

(a) **(b)**

Figure 8. (a) Shaper output recorded by TARGET7 vs WavePro715Zi. (b) Charge input scan using TARGET7 and WavePro715Zi. Measured amplitudes are averaged over 10 times.

5 Conclusion

We have designed a 16-channel 1 GSPS waveform digitizer with TARGET7 ASIC. The input dynamic range is 1.8 V with effective dynamic range of ~ 10 bits and DC noise of 1.76 mV. Voltage calibration, timing performance with a timing resolution of 152 ps in RMS are studied. In addition, an application in charge measurement is successfully carried out for TARGET7 and an oscilloscope. The results of them are well matched while TARGET7 shows a little bit better performance.

Acknowledgments

The author would like to thank Gary S.Varner and Isar Mostafanezhad for helpful discussions and useful suggestions. This work is supported by the National Science Natural Science Foundation of China (Grant No. 11505183 and 11205154).

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