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Title: Readout Electronics of Silicon PIN Diode Arrays for CEPC ECAL A Prelimin

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Referee report

Comments on the manuscript

Readout Electronics of Silicon PIN Diode Arrays for CEPC ECAL A Preliminary Study on Prototype System, S. Ma et al.

The paper reports on a readout system for an electromagnetic calorimeter based on PIN diodes. It is strongly based on prior work performed within the CALICE collaboration, using their ASIC and a wafer developed by Hamamatsu in the CALICE context. The CALICE publications are quoted, however the relationship should be made more transparent in the introductory part of the paper.

The hardware configuration, with electronics externally and next to instead of on top of the sensors, may be adequate for system tests, also with particle beams, but it is not really state of the art with respect to the design of detectors for collider experiments. Both the CALICE collaboration and the CMS collaboration are actively pursuing the development of silicon-based calorimeters with integrated read-out-boards interfaced to the silicon sensors within the volume of the detector, which brings considerable additional system challenges. This is not mentioned, either, and should also be discussed in the introduction, or in the conclusion, The claim made in the conclusion that the system is scalable is not valid without these further qualifications

A large fraction of the paper deals with the read-out chain, including the digital elements for control and data concentration. This hardware is not based on CALICE work but is taken from a different project. However, there are no performance characterizations for a multi-layer system given, only results for single channels or for a single chip at most. There is not even an evidence that the collection of data from several layers worked.

Given this, and the fact that there is other work on the characterization of the ASIC published, e.g.:

Beam test performance of the SKIROC2 ASIC
M.S. Amjad (Orsay, LAL) et al.. 2015. 7 pp.
Published in Nucl.Instrum.Meth. A778 (2015) 78-84
DOI: 10.1016/j.nima.2014.12.011

Performance study of SKIROC2/A ASIC for ILD Si-W ECAL
T. Suehara (Kyushu U., Fukuoka (main)) et al.. Jan 6, 2018. 6 pp.
Published in JINST 13 (2018) no.03, C03015
DOI: 10.1088/1748-0221/13/03/C03015

one may ask what the added scientific value of the presented article is. In any case these papers have to be referenced.

The paper draft should have been proof-read by a native speaker before submission, or before forwarding for review. There are many language-related comments. The more substantial ones are labelled by one or several asterisks.

Abstract

~~on THE SKIROC2~~
~~at THE Circular~~
~~through A gigabit~~

1. Introduction

~~Collider CONCEIVEED to produce~~
~~and making precise ->and to make precise~~
~~taus ->tau leptons~~
~~the high granularity plays ->the high granularity plays~~
~~critical role in determining the maximum capability of particle separation~~

->critical role in the capability of particle separation

*** At the end of the section, it should be mentioned that also experiments at other future electron positron colliders have studied a silicon-tungsten based ECAL, and the ILC TDR and CLIC CDR be quoted. This would also better explain why their results are being quoted in the paragraph below. A mentioning of and reference to the CMS endcap calorimeter upgrade would also be appropriate.

~~Results of THE CALICE ECAL~~
~~For THE international~~
~~Tens of millions OF electronic channels~~
~~Dozens of layers ->give exact number~~

*** Minimal power (<10mW per channel). This requirement is considered to be sufficient for linear colliders with their low duty cycle, because one can cycle the power, such that few 10s or micro-Watts per channel result. This is not possible at a circular collider, and it is the main difference in requirements for the calorimeter concept. So it should be discussed with a few sentences. It would be surprising if 10 mW per channel is sufficient to operate the detector without cooling.

2. System

~~data to A PC~~
earlier, there were dozens of layers, now it is 6. Is this the first stage of a larger prototype? Please clarify.
SKIROC2 was developed in the CALICE collaboration, as is stated in [7]; please mention.
CSA ->SCA, several times.
~~The total active area is 5x5mm2 ->the active area of one cell is 5x5mm2~~
~~Low power rejection (82 dB) >of 82 dB~~
~~Output noise (4 uV rms) -? Output noise rms of 4 uV~~

*** Fig 4: Actually one would like to see the entire powering scheme, including the depletion voltage and the input coupling to the pre-amp.

~~Convertion ->conversion~~
~~Memory on chip >on the chip~~
~~Controlled by field-programmable ->by a field-..~~
~~On DIF ->on the DIF~~

~~Valid the SCA ->validate the SCA~~
~~Configures 616 bits registers ->configures the 616 bit registers on the chips~~
~~Such as C_f and trigger mode ->such as the feed-back capacitance C_f and the trigger mode~~
~~ASIC on FEB ->ASIC on the FEB~~
~~Transmit them to DIF ->to the DIF~~
~~Expend FEB ->expand THE FEB~~
~~Interface definition to FEB ->to the FEB~~
~~5V to FEB ->to the FEB.~~
~~The FPGA Is composed of an FPGA ->the FPGA part is~~
~~Function of FPGA ->of the FPGA~~
~~Control FEB ->the FEB~~
~~With DCM ->with the DCM~~
~~Or PC ->or the PC~~
~~In the normal mode ->in normal mode~~
~~Into FPGA ->into the FPGA~~
~~To DCM or PC ->to the DCM or to the PC~~
~~Ex-trigger mode ->external trigger mode~~

*** here an explanation is missing that normally the chip is self-triggered

~~Which discussed below ->which is discussed below~~
~~From FIFO to DCM ->from the FIFO to the DCM~~
~~Gets a command from DCM ->receives commands from the DCM~~
~~GTP ->what is this?~~
~~On FPGA ->on the FPGA~~
* GTP is not explained
* Fig 6 SPP is not explained
~~With PC ->with the PC~~
~~As well as initial power supply to FEB ->As well as the initial power supply to the FEB~~
~~Generated for DOF~->for the DIF.~~
~~Data from DIFs ->data from one or several DIFs~~
~~Designed for PandaX ->for the PandaX~~
~~The picture of DCM ->a picture of the DCM~~
~~An FPGA of Zync 7 ->an FPGA of the Zync 7type~~
~~One DCM carries 6 DIFs ->serves 6 DIFs~~
* GTX is not explained

3. Characterisation

~~Performance of readout system ->the readout system~~
*** Fig 6: both plots have no axis labels
~~Acquisition of baseline ->of the baseline~~
~~Required by SKIROC2 ->by the SKIROC2 chip~~
~~SKIROC2 held ->The chip held~~
~~It worth noting ->it is worth noting~~
~~Demonstrated the noise level ->demonstrated a noise level~~
*** Fig 9 has no axis labels either
~~Range of SKIROC2 ->range of the SKIROC2 chip~~
~~By taking advantaging of ->advantage of~~
~~From test pulse input ->from the test pulse input~~
~~The SKIROC2 had many ->the SKIROC2 chips has many~~
~~* Fig 10 caption: The trigger efficiency for two channels as a function of threshold setting for an input charge of 2 fC~~.
~~Via the S curve and presented in Fig ->from an S curve as presented in Fig.~~
~~With 4-but DAC ->with a 4-bit DAC~~
~~Exceeded the threshold .. would output ->exceeds the threshold .. the SKIROC2 chip generates a trigger signal~~
~~Where center value ->the center value~~
~~the threshold on the charge and the sigma represents the noise power ->the charge threshold and the sigma parameter represents the noise induced width.~~
~~In newer version ->in a newer version~~
~~With X-ray source ->with an X-ray source~~

*** The bias voltage of 13 V appears to be too low for a full depletion of the wafer with 400 micron thickness. The CALICE prototype paper [5] reports 150V for a 500 micron wafer. Possibly a thin depletion layer is sufficient for the registration of X-ray signals, if irradiated from the right side. However, this raises the question how representative the S/N results are. This should be discussed.

*** Fig 11: The line shape is not Gaussian. Should be commented.

~~Total energy of X-ray ->energy of the X-ray photons~~
~~When Fano factor ->when the Fano factor~~

*** Fig 12: Cosmic ray test: Has an external trigger been used? Or has a selection (coincidence between layers) been applied? The origin of the 2 contributions in Fig.12 should be explained. In auto-trigger only signals above threshold should be seen. The SKIROC2 output contains the charges

of all channels if one has triggered, so it could be non-triggered channels in triggered events.
*** Moreover, it remains unclear whether the shown pulse height distribution is for a single channel or for several channels. (I assume not, since inter-calibration is not mentioned.

*** The entire characterization section is somewhat disappointing, since uniformity results are shown for a single chip only, and performance results are given for individual channels only. No statements are made on the entire 6-larer system.

4. Conclusion

Based on SKIROC2 ->based on the SKIROC2

*** System is scalable: This is over-selling the results. The system may be scalable to a test beam prototype like the one constructed by CALICE in 2005, but since the electronics is still external and next to instead of on top of the wafer, it is not scalable to a collider detector.

*** The performance assessment of the system is discussed in detail. It is discussed on the single channel level, and some results on chip level are given.
See also introductory remarks.