Response to the reviewers

(TNS-00233-2014)

Reviewer2:

1. The author is only concerned with single event effects. From personal experience I know that also dose effects should be considered when using flash based FPGAs. It might be that this is not a problem in the radiation environment of the DAMPE BGO Calorimeter, but i think at least it should be stated why dose is not relevant (if this is the case).

Answer:

Total ionizing dose (TID) test for the front end electronics (FEE) board with APA600 was conducted at National Institute of Metrology, China and University of Science and Technology of China (USTC). A ^{60}Co gamma source was used as in the TDI test. The whole FEE board was irradiated up to 10Krad (Si) with a dose rate of 2.61rad/s at the room temperature. Accelerated ageing with power-on at 100℃ for 60 hours was done after irradiation exposure. The experiment results showed that no evident degradation of FPGA was found. All function of FPGA worked well during the experiment. The supply current of FPGA was monitored and no abnormal value was found. After the experiment, the APA600 chip could be reconfigured with new logic, which meant the configuration part of the chip was not damaged either.
The information of the TID test and the results are stated as above. However, because that the main topic of this paper is to talk about the SEU mitigation in logic design, I have not added them to the paper.

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2. I have one question regarding the reset of the RAMs. Is this really needed? Does the content of the RAM really matter when it is not actually read? Normally, a reset of the RAM blocks should not be needed, and might actually lower the radiation tolerance. I would like to get a clearer motivation for why this reset is needed.

Answer:

Actually the content in the RAMs are useful all the time because they are used to set operating status of the system. Besides, all RAMs are belong to the status manager part instead of the control part or the scientific data acquisition part, so they will not be reset frequently. The RAMs will only be reset when powering on or receiving reset command, both of which happens seldom. To avoid misleading, this part of the paper has been rewritten as follows (second page line 63 to line 77):

"In the status manager part, there are some key registers and RAMs which are used to set the operating status of the system and need to be valid all the time. Other parts get operating settings from the status part. The monitor part provides some parameters describing the operating status for real-time monitoring.

When a command comes from the controlling computer, the control part begins to handle it. And when a trigger signal comes from the trigger board, it is handled by the scientific data acquisition part. There are many steps in both the command handling procedure and the scientific data acquisition handling procedure. When a command handling procedure or a scientific data acquisition procedure is finished, the part of the logic is under reset state until next command or trigger signal arrives."

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3. Irradiation tests (Section IV, B & C, Section V, A). This part should be extended. I would very much like to see some numbers here. What is the MTBF for the system with the radiation tolerance measures implemented? (DO you actually see NO errors at all? I guess you should see some CRC errors for example?) Could it be compared to the MTBF of the same system without radiation tolerance measures implemented? You use the Markov model to predict this difference, but it would be very nice to also have some beamtests results to compare against the Markov model

Answer:

Some calculation has been added to Section V. The model has been analyzed in detail and MTBF of the system with and without TMR has been calculated. This part of paper has been rewritten (forth page line 70 to fifth page line 39) as follows:

"Using Markov model in fault-tolerant computing, a system's reliability can be predicted [10]. According to the study of McMurtrey D, if defining reliability as the probability that the value in a single DFF register is still correct after a certain time, then

$$R_{DFF1}(t) = e^{(-\lambda t)} \quad (1)$$

Where λ *represents the rate that the value in a DFF transitions from correctness to error per unit time and t represents time.*

Concerning structure with TMR DFF, then

$$R_{DFF2}(t) = \frac{(\mu+5\lambda)\sinh\left(\frac{1}{2}t\sqrt{\mu^2+10\lambda\mu+\lambda^2}\right)e^{-\frac{1}{2}(\mu+5\lambda)t}}{\sqrt{\mu^2+10\lambda\mu+\lambda^2}} + \cosh\left(\frac{1}{2}t\sqrt{\mu^2+10\lambda\mu+\lambda^2}\right)e^{-\frac{1}{2}(\mu+5\lambda)t} \quad (2)$$

Where λ represents the rate that the value in a DFF transitions from correctness to error per unit time, μ represents the repair rate per unit time and t represents time.

Concerning there are 3000 key registers in the FPGA logic, if defining system reliability as the probability that all registers in the system are correct, then

$$R_{system}(t) = R_{DFF}{}^{3000} \quad (3)$$

As CREME96 predicts that the SEU probability for the APA chip is about 6.8×10^{-7} bit^{-1} day^{-1} at the altitude of 500km [6], [7], [8], λ is assumed to be 10^{-7} hour^{-1}. And because there is write-back line in the structure of TMR in the design, μ is very much closed to 1. Combining these two parameters with equations 1, 2 and 3, the system reliability changing with time can be derived and the results are shown in Fig. 8. Compared with the one of system without TMR, the reliability of system with TMR almost does not change with time and is still very close to 1 after 30000 hours. Therefore, the structure of TMR with write-back line can highly improve the reliability of a system.

Using the system reliability, Mean Time Between Failure (MTBF) of the system can be calculated. As shown in equation 4 and 5, the MTBF of the system can be improved by 10^6 times if using the structure of TMR with write-back line.

$$MTBF_{Without\ TMR} = \frac{\int_0^\infty \frac{d(1-R_{DFF1}{}^{3000})}{dt} * t dt}{\int_0^\infty \frac{d(1-R_{DFF1}{}^{3000}{}_1)}{dt} dt} := 3000 hours \quad (4)$$

$$MTBF_{With\ TMR} = \frac{\int_0^\infty \frac{d(1-R_{DFF2}{}^{3000})}{dt} * t dt}{\int_0^\infty \frac{d(1-R_{DFF2}{}^{3000})}{dt} dt} := 10^9 hours \quad (5)"$$

For the irradiation test, actually no errors including CRC errors was monitored.

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4. Section IV, C: APA300 Should be APA600?

Answer:

Actually, two kinds of FPGA is used in the BGO calorimeter and in the beam test. The introductions of these two chip have been added in the paper (first page line 48 to line 53).

"Two kinds of flash-based FPGA of Actel, ProASIC Plus APA300 (APA300) which has 300000 system gates and ProASIC Plus APA600 (APA600) which has 600000 system gates are chosen as the BGO FEE controlling chips. These two types of chips are same expect the number of resources."

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5. Section V, A: Fig.8 "Signle" DFF --> "single DFF"

Answer:

Fig. 8 has been modified in the paper (fifth page line 70).

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6. Section V, B: attitude --> altitude?

Answer:

English typos in the paper have been modified.