Harideep Nair

Mountain View, CA | 408-326-9548 | hpnair@andrew.cmu.edu | Personal Website: hpnair.github.io

Research: Neuromorphic algorithm/processor design for Machine Learning targeting brain-like capabilites and efficiency.

Education

- **Carnegie Mellon University** — Anticipated Graduation: Dec'23
  Ph.D. - Electrical and Computer Engineering | *GPA: 3.80/4.00* (Aug'18 - Present)
  Courses: *Computer Systems, Machine Learning, Deep Learning, Hardware Architectures for Machine Learning, Neural Computation*
- **Indian Institute of Technology (IIT) Bombay** — Mumbai, India
  Dual Degree (B.Tech+M.Tech) - Electrical Engineering | *GPA: 9.08/10.00* (Jul'13 - Jul'18)
  Courses: *Advanced Computer Architecture, VLSI Design, Computer Vision, Operating Systems, Computer/Network Security, Statistics*

Skills Summary

- **Programming**: C/C++/System C, Python, MATLAB, Verilog/Verilog-A, VHDL, Java, HTML
- **ML Frameworks**: PyTorch, TensorFlow, TensorFlow Lite, MLOps, Keras, Tensorboard, SNPE, NeuroPilot
- **Software Tools**: Gem5, Snipersim, Ramulator, Synopsys VCS/Design Compiler, Cadence Genus, Xilinx Vivado, HFSS

Key[1] Publications and Talks

- Harideep Nair, Prabhu Vellaisamy, Tsung-Han Lin, Perry Wang, Shawn Blanton, and John Paul Shen. "OzMAC: Energy-Efficient Sparsity-Exploiting Multiply-Accumulate-Unit Design for DL Inference". *Submitted to ISCA'23.*
- Harideep Nair, Prabhu Vellaisamy, Santha Bhasuthkar and John Paul Shen. "TNN7: A Custom Macro Suite for Implementing Highly Optimized Designs of Neuromorphic TNNs", *ISVLSI 2022.*
- Harideep Nair, John Paul Shen and James E. Smith. "A Microarchitecture Implementation Framework for Online Learning with Temporal Neural Networks", *ISVLSI 2021.*
- Shreyas Chaudhari, Harideep Nair, José M.F. Moura and John Paul Shen. "Unsupervised Clustering of Time Series Signals using Neuromorphic Energy-Efficient Temporal Neural Networks", *ICASSP 2021.*
- Harideep Nair, Cathy Tan, Ming Zeng, Ole J. Mengshoel, and John Paul Shen. "AttriNet: Learning Mid-Level Features for Human Activity Recognition with Deep Belief Networks", *UbiComp 2019.*
- "Building a Silicon Neocortex in CMOS", Alternative Computing Group, NIST, *Dec 2020 [Invited Talk].*

Professional and Teaching Experience

- **MediaTek Inc., San Jose** | **AI Computer Architecture Research Intern** (Summer'20, Jan'21 - Dec'22)
  - Worked on **architectural simulator** and ISA design for in-house AI accelerator in production mobile SoCs.
  - Designed and implemented novel **RTL**/microarchitectural blocks from scratch for **next-gen AI accelerator**.
  - Developed **Computer Vision** applications using MediaTek NeuroPilot for edge inferencing on Dimensity SoCs.
- **Carnegie Mellon University** | **Head TA** (Spring/Fall'19, Spring/Fall'20, Spring/Fall'21 & Spring/Fall'22)
  - Led 11 TAs over 7 offerings of 2 courses: 18-743 (Neuromorphic Comp. Arch.), 18-740 (Modern Comp. Arch.).
  - Played instrumental role in **creating** both courses at CMU and establishing **industry collaboration**.
  - Designed lab assignments exploring CPU/GPU/NPU cores inside Qualcomm/MediaTek's SOTA mobile SoCs.

Key[1] Projects

- **Facial Emotion Recognition using Efficient Deep Neural Networks** | **CMU** (Aug'19 - Dec'19)
  Mobile attention-based CNN design - top 10 in ICML'13 FER Challenge with 3x/8x less power/latency than VGG-19.
- **Hardware Aware Neural Network Architectures Using FBNets** | **CMU** (Jan'19 - May'19)
  NAS methodology with combined loss-latency-energy optimization - 3.8x/2.5x less energy/latency than MobileNetV2.
- **Energy-Efficient Microarchitecture with Dynamic Renaming** | **IIT Bombay** (May'17 - Jul'18)
  Freeflow frontend with inorder backend - 150% more energy-efficient than out-of-order for just 3.5% drop in IPC.
- **Hardware Acceleration of AES Decryption** | **National University of Singapore** (Aug'16 - Dec'16)
  AES decryption engine and TFT display controller on Xilinx FPGA - displayed decrypted image on an LCD monitor.
- **Electromagnetically Secure Integrated Circuits** | **Purdue University** (May'16 - Aug'16)
  EM side channel leakage analysis on IC stack model - successful AES key byte extraction using correlation analysis.

Selected[1] Honors and Awards

- **Exemplary Performance Award** for innovative contribution to the team during MediaTek internship.
- **Dean's Fellowship** for pursuing PhD in ECE at Carnegie Mellon University.
- **TF LEaRN Scholarship** (1/53 recipients all over Asia) for semester exchange at National University of Singapore.
- **Gold Medal** in National Chemistry Olympiad (top 40 students in India) and selected for the IChO Training Camp.
- **All India Rank 3** in All India Open Mathematics Scholarship Examination.
- Awarded prestigious **National Talent Search Examination (NTSE) scholarship** by the Government of India.

[1]Detailed list on my personal website mentioned at the top of the page