Advanced Computer Architecture (HPCA)

HW: GPU (CUDA) Histogram and Atomics

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[Item 1]:

Fill in the execution times using the event timers (T=32, H=64).

Array Size (N)	CPU Execution (us)	GPU Execution + CPU clean up: **histogram_kernel** (us)	GPU Speedup (us)
1000	17	280	0
10000	139	259	0
100000	1987	330	1657
1000000	12234	369	11865

[Item 2]:

T=32, H=64, N=10000, B=2

Block 1:

Start Time: 64475 us

Stop Time: 109518 us

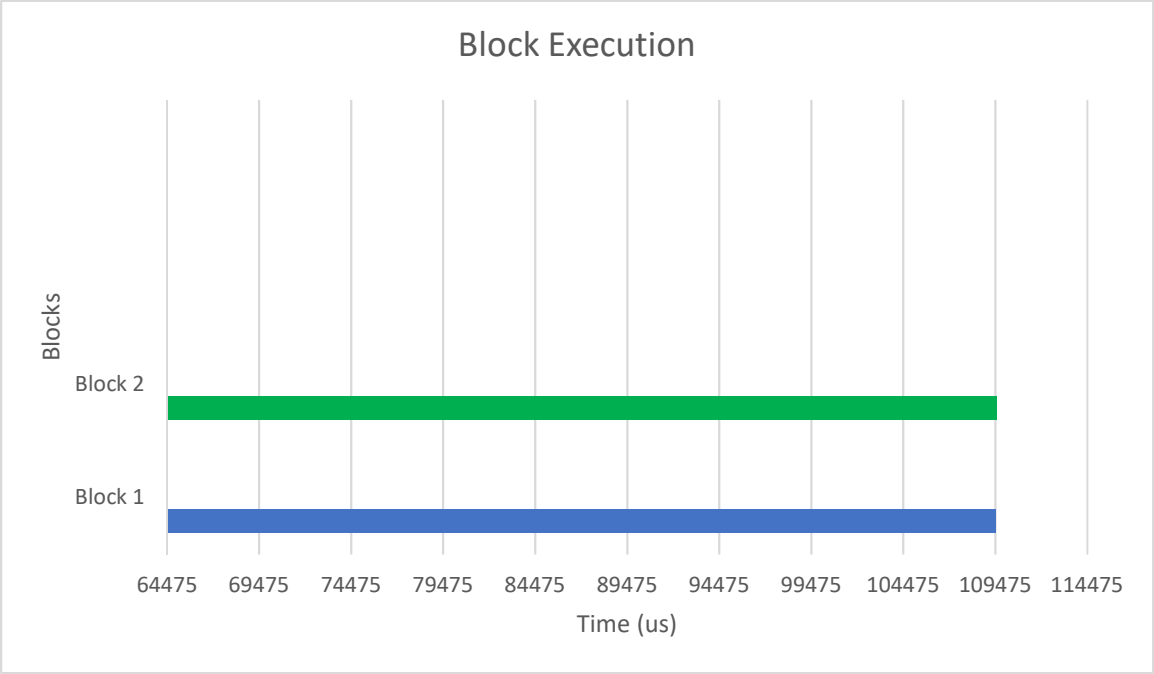
Execution Time: 45043 us

Block 2:

Start Time: 64479 us

Stop Time: 109520 us

Execution Time: 45041 us



T=32, H=64, N=10000, B=4

Block 1:

Start Time: 62962

Stop Time: 88605

Execution Time: 25643

Block 2:

Start Time: 62966

Stop Time: 88591

Execution Time: 25625

Block 3:

Start Time: 62967

Stop Time: 88611

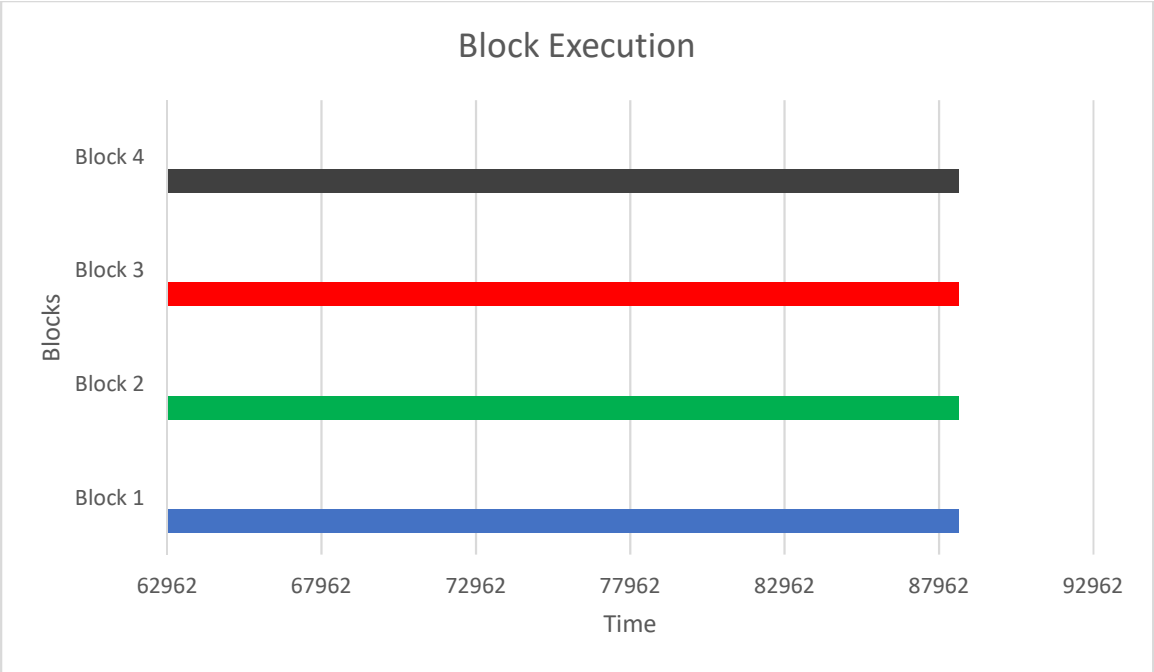
Execution Time: 25644

Block 4:

Start Time: 62967

Stop Time: 88597

Execution Time: 25630



[Item 3]:

You are to examine an optimization using an atomic instruction to enforce one thread at a time accessing to individual locations in the histogram array.

Array Size (N)	GPU Execution + CPU clean up: **histogram_kernel** (us)	GPU Execution + CPU clean up: **histogram_atomic_kernel** (us)	Speedup (us)
1000	280	222	58
10000	259	245	14
100000	330	276	54
1000000	369	323	46

[Item 4]:

T=32, H=64, N=10000, B=2

Time for Atomic Block 1: 45571 us

Time for Atomic Block 2: 45572 us

T=32, H=64, N=10000, B=4

Time for Atomic Block 1: 31466 us

Time for Atomic Block 2: 31470 us

Time for Atomic Block 3: 31462 us

Time for Atomic Block 4: 31464 us