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Digital logic design homework4: Project04: State Minimization

Case1(6 states)

```
Digital_homework3 > E case1.kiss
1 .start_kiss
2 .i 1
3 .o 1
4 .p 12
5 .s 6
6 .r a
7 0 a a 0
8 1 a b 0
9 0 b c 0
10 1 b d 0
11 0 c a 0
12 1 c f 0
13 0 d e 0
14 1 d f 1
15 0 e e 0
16 1 e f 1
17 0 f b 0
18 1 f a 1
19 .end_kiss
20
```

```
Digital_homework3 > E output1.kiss
1 |.start_kiss
2 .i 1
3 .o 1
4 .p 10
5 .s 5
6 .r a
7 0 a a 0
8 1 a b 0
9 0 b c 0
10 1 b d 0
11 0 c a 0
12 1 c f 0
13 0 d e 0
14 1 d f 1
15 0 f b 0
16 1 f a 1
17 .end_kiss
```

Case2(5 states)

```
Digital_homework3 > E case2.kiss
1 .start_kiss
2 .i 1
3 .o 1
4 .p 10
5 .s 5
6 .r a
7 0 a a 0
8 1 a c 0
9 0 b c 0
10 1 b a 0
11 0 c e 0
12 1 c b 0
13 0 d e 0
14 1 d b 0
15 0 e a 0
16 1 e c 1
17 .end_kiss
18 |
```

```
Digital_homework3 > ≡ output2.kiss
1 |.start_kiss
2 .i 1
3 .o 1
4 .p 8
5 .s 4
6 .r a
7 0 a a 0
8 1 a c 0
9 0 b c 0
10 1 b a 0
11 0 c e 0
12 1 c b 0
13 0 e a 0
14 1 e c 1
15 .end_kiss
```

Case3(4 state)

```
Digital_homework3 > ≡ output3.kiss
1 |.start_kiss
2 .i 1
3 .o 1
4 .p 6
5 .s 3
6 .r a
7 0 a a 0
8 1 a c 0
9 0 b a 0
10 1 b b 0
11 0 c d 0
12 1 c b 1
13 .end_kiss
```

```
Digital_homework3 > ≡ case3.kiss
1 .start_kiss
2 .i 1
3 .o 1
4 .p 8
5 .s 4
6 .r a
7 0 a a 0
8 1 a c 0
9 0 b a 0
10 1 b b 0
11 0 c d 0
12 1 c b 1
13 0 d a 0
14 1 d b 0
15 .end_kiss
16
```