QIJING JENNY HUANG

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RESEARCH INTERESTS

Hardware Acceleration, Compiler Optimizations, Design Methodology with High-Level Synthesis (HLS), Machine Learning for Design Automation

EDUCATION

University of California, Berkeley *Sep 2015 - Now*
PhD, Electrical Engineering and Computer Science

University of Toronto *Sep 2010 - May 2015*
Bachelor of Applied Science, Electrical & Computer Engineering
Graduated with High Honours

TECHNICAL SKILLS

Programming & Tools	C/C++, OpenCL, CUDA, Go, OpenMP/MPI, Python, Perl, Java, Scala, Verilog, Chisel, Tcl, Git, Tensorflow, Pytorch, Spark, Quartus, Vivado

PROFESSIONAL EXPERIENCE

Google, *Sunnyvale, CA* *Aug 2020 - Now*
· Student Researcher

Google, *Sunnyvale, CA* *May 2020 - Aug 2019*
· Hardware Engineer Intern

Facebook, *Menlo Park, CA* *May 2019 - Aug 2019*
· AI Infrastructure Research Intern

Intel Labs, *Santa Clara, CA* *June 2016 - Aug 2016*
· Parallel Computing Graduate Lab Technician

Altera (Intel FPGA), *Toronto, ON* *May 2013 - Aug 2014*
· Software Engineer

University of Toronto, *Toronto, ON* *Summer 2013*
· Research Assistant

University of Toronto, *Toronto, ON* *Summer 2012*
· Research Assistant

HONORS

University of Toronto Excellence Award

University of Toronto Scholar

PUBLICATIONS

1. Farshchi, F., Huang, Q., & Yun, H. (2020). Bru: Bandwidth regulation unit for real-time multicore processors. In *2020 ieee real-time and embedded technology and applications symposium (RTAS)* (pp. 364–375). (Paper)

2. Settaluri, K., Haj-Ali, A., Huang, Q., Hakhamaneshi, K., & Nikolic, B. (2020). Autockt: Deep reinforcement learning of analog circuit designs. In *Design, automation & test in europe conference & exhibition (DATE)* (pp. 1–6). (Paper)

3. Haj-Ali, A*, Huang, Q*, Xiang, J., Moses, W., Asanovic, K., Wawrzynek, J., & Stoica, I. (2020). Autophase: Juggling hls phase orderings in random forests with deep reinforcement learning. *Proceedings of Machine Learning and Systems*, *2*. (Paper, Slides, Github)

4. Huang, Q*, Wang, D*, Gao, Y., Cai, Y., Dong, Z., Wu, B., Keutzer, K., & Wawrzynek, J. (2019). Algorithm-hardware co-design for deformable convolution. In *The 5th workshop on energy efficient machine learning and cognitive computing co-located with the 33rd conference on neural information processing systems neurips 2019 (EMC^2).* (Paper)

5. Huang, Q., Yarp, C., Karandikar, S., Pemberton, N., Brock, B., Ma, L., . . . Wawrzynek, J. (2019). Centrifuge: Evaluating full-system HLS-generated heterogeneous-accelerator SoCs using FPGA-Acceleration. In *Proceedings of the 38th international conference on computer-aided design (IC-CAD).* (Paper, Slides, Github)

6. Huang, Q*, Haj-Ali, A*, Moses, W., Xiang, J., Stoica, I., Asanovic, K., & Wawrzynek, J. (2019). AutoPhase: Compiler Phase-Ordering for HLS with Deep Reinforcement Learning. In *2019 ieee 27th annual international symposium on field-programmable custom computing machines (FCCM)* (pp. 308–308). (Paper)

7. Yang, Y., Huang, Q., Wu, B., Zhang, T., Ma, L., Gambardella, G., . . . others (2019). Synetgy: Algorithm-hardware co-design for convnet accelerators on embedded FPGAs. In *Proceedings of the 2019 acm/sigda international symposium on field-programmable gate arrays (FPGA)* (pp. 23–32). (Paper, Slides)

8. Wu, L., Bruns-Smith, D., Nothaft, F. A., Huang, Q., Karandikar, S., Le, J., . . . others (2019). FPGA Accelerated INDEL Realignment in the Cloud. In *2019 ieee international symposium on high performance computer architecture (HPCA)* (pp. 277–290). (Paper)

9. Farshchi, F., Huang, Q., & Yun, H. (2019). Integrating nvidia deep learning accelerator (nvdla) with risc-v soc on firesim. In *2019 2nd workshop on energy efficient machine learning and cognitive computing for embedded applications (EMC^2)* (pp. 21–25). (Paper)

10. Karandikar, S., Mao, H., Kim, D., Biancolin, D., Amid, A., Lee, D., . . . others (2018). FireSim: FPGA-accelerated cycle-exact scale-out system simulation in the public cloud. In *Proceedings of the 45th annual international symposium on computer architecture (ISCA)* (pp. 29–42). (Paper)

11. Cheng, S., Huang, Q., & Wawrzynek, J. (2017). Synthesis of program binaries into FPGA accelerators with runtime dependence validation. In *2017 international conference on field programmable technology (FPT)* (pp. 96–103). (Paper, Slides, Best Paper Award)

12. Huang, Q., Lian, R., Canis, A., Choi, J., Xi, R., Calagar, N., . . . Anderson, J. (2015). The effect of compiler optimizations on high-level synthesis-generated hardware. *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, *8*(3), 14. (Paper)

13. Huang, Q., Lian, R., Canis, A., Choi, J., Xi, R., Brown, S., & Anderson, J. (2013). The effect of compiler optimizations on high-level synthesis for FPGAs. In *2013 ieee 21st annual international symposium on field-programmable custom computing machines (FCCM)* (pp. 89–96). (Paper)

14. Canis, A., Choi, J., Fort, B., Lian, R., Huang, Q., Calagar, N., . . . others (2013). From software to accelerators with LegUp high-level synthesis. In *Proceedings of the 2013 international conference on compilers, architectures and synthesis for embedded systems* (p. 18). (Paper)

OTHER RESEARCH PROJECTS

Golang HLS (Report)(Github) *2017*

JCGAN Car Image Synthesis with GAN (Report)(Github) *2017*

Spark Twitter Language Classifier on GPU (Report)(Github) *2016*

Reconfigurable Garp Coprocessor in Chisel (Report)(Github) *2016*

TEACHING ASSISTANTSHIPS

CS267 Applications of Parallel Computers

CS61C Great Ideas in Computer Architecture

INVITED TALKS AND LECTURES

ML for Computer Architecture and Systems Workshop at ISCA (MLArchSys) *2020*
· Algorithm-Hardware Co-Design for Edge DNN Deployment and ML for Hardware Design

Google (Slides) **Host: Phitchaya Mangpo Phothilimthana** *2020*
· AutoPhase: Juggling HLS Phase Orderings in Random Forests with Deep Reinforcement Learning

Xilinx (Slides) **Host: Kees Vissers** *2019*
· Synetgy: Algorithm-hardware Co-design for ConvNet Accelerators on Embedded FPGAs

EECS151/251 Introduction to Digital Design and Integrated Circuits (Slides) *2019, 2020*
· Deep Learning Accelerators and High-level Synthesis

PROFESSIONAL SERVICE

Conference Review
· 2020 FPGA
· 2019 FPGA, FPL
· 2018 FPGA, FCCM
· 2016 FPGA

Artifact Evaluation
· 2020 ASPLOS

Student Organization
· 2017 Women in Computer Science and Electrical Engineering (WICSE) Treasurer