QIJING JENNY HUANG

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RESEARCH INTERESTS

Hardware Acceleration, Compiler Optimizations, Design Methodology with High-Level Synthesis (HLS), Machine Learning for Design Automation

EDUCATION

University of California, Berkeley *Sep 2015 - Now*
PhD, Electrical Engineering and Computer Science

University of Toronto *Sep 2010 - May 2015*
Bachelor of Applied Science, Electrical & Computer Engineering
Graduated with High Honours

TECHNICAL SKILLS

Programming & Tools	C/C++, OpenCL, CUDA, Go, OpenMP/MPI, Python, Perl, Java, Scala, Verilog, Chisel, Tcl, Git, Tensorflow, Pytorch, Spark, Quartus, Vivado

PROFESSONAL EXPERIENCE

Google, Student Researcher, Sunnyvale, CA *Aug 2020 - Now*
Applies machine learning to improve hardware verification flow

Google, Hardware Engineer Intern, Sunnyvale, CA *May 2020 - Aug 2019*
Applies blackbox and heuristic-driven approaches to improve coverage for hardware verification

Facebook, AI Infrastructure Research Intern, Menlo Park, CA *May 2019 - Aug 2019*
Leverages reinforcement learning and optimization techniques for resource allocation and scheduling

Intel Labs, Graduate Lab Technician, Santa Clara, CA *June 2016 - Aug 2016*
Implements an HLS backend targeting FPGA accelerators for a deep learning DSL called Latte

Altera (Intel FPGA), Software Engineer, Toronto, ON *May 2013 - Aug 2014*
Develops a debugger for ARMv7 processor and creates tutorials for FPGA tools and IPs

University of Toronto, Research Assistant, Toronto, ON *May 2013 - Aug 2013*
Investigates the impact of compiler phase ordering on x86 processor

University of Toronto, Research Assistant, Toronto, ON *May 2012 - Aug 2012*
Works on an open-source HLS tool called LegUp and devises a beam search like algorithms to address the phase ordering problem for HLS

HONORS

2020 EECS Rising Stars

University of Toronto Excellence Award

University of Toronto Scholar

PUBLICATIONS

Conference Proceedings

1. CoDeNet: Efficient Deployment of Input-Adaptive Object Detection on FPGAs. (Paper)
   Qijing Huang*, Dequan Wang*, Zhen Dong*, Yizhao Gao, Yaohui Cai, Tian Li, Bichen Wu, Kurt Keutzer, John Wawrzynek
   To appear in 2021 Field-Programmable Gate Arrays (FPGA)

2. BRU: Bandwidth Regulation Unit for Real-time Multicoreprocessors. (Paper)
   Farzad Farshchi, **Qijing Huang**, Heechul Yun
   2020 Real-Time and Embedded Technology and Applications Symposium (RTAS)

3. AutoCkt: Deep Reinforcement Learning of Analog Circuit Designs. (Paper)
   Keertana Settaluri, Ameer Haj-Ali, **Qijing Huang**, Kourosh Hakhamaneshi, Borivoje Nikolic
   2020 Design, Automation & Test in Europe Conference & Exhibition (DATE),

4. AutoPhase: Juggling HLS Phase Orderings in Random Forests with Deep Reinforcement Learning. (Paper, Slides, Github)
   Ameer Haj-Ali*, **Qijing Huang***, John Xiang, William Moses, Krste Asanovic, John Wawrzynek, Ion Stoica
   2020 Machine Learning and Systems (MLSys)

5. Centrifuge: Evaluating Full-System HLS-Generated Heterogeneous-Accelerator SoCs using FPGA-Acceleration. (Paper, Slides, Github)
   Qijing Huang, Christopher Yarp, Sagar Karandikar, Nathan Pemberton, Benjamin Brock, Liang Ma, Guohao Dai, Robert Quitt, Krste Asanovic, John Wawrzynek
   2020 International Conference on Computer-Aided Design (ICCAD)

6. AutoPhase: Compiler Phase-Ordering for HLS with Deep Reinforcement Learning. (Paper)
   Qijing Huang*, Ameer Haj-Ali*, John Xiang, William Moses, Ion Stoica, Krste Asanovic, John Wawrzynek
   2019 Field-Programmable Custom Computing Machines (FCCM)

7. Synetgy: Algorithm-Hardware Co-Design for Convnet Accelerators on Embedded FPGAs. (Paper, Slides)
   Yifan Yang, **Qijing Huang**, Bichen Wu, Tianjun Zhang, Liang Ma, Giulio Gambardella, Michaela Blott, Luciano Lavagno, Kees Vissers, John Wawrzynek, Kurt Keutzer
   2019 Field-Programmable Gate Arrays (FPGA)

8. FPGA Accelerated INDEL Realignment in the Cloud. (Paper)
   Lisa Wu, David Bruns-Smith, Frank A. Nothaft, **Qijing Huang**, Sagar Karandikar, Johnny Le, Andrew Lin, Howard Mao, Brendan Sweeney, Krste Asanovic, David A. Patterson
   2019 High Performance Computer Architecture (HPCA)

9. FireSim: FPGA-Accelerated Cycle-Exact Scale-Out System Simulation in the Public Cloud. (Paper, 2018 MICRO Top Picks)
   Sagar Karandikar, Howard Mao, Donggyu Kim, David Biancolin, Alon Amid, Dayeol Lee, Nathan Pemberton, Emmanuel Amaro, Colin Schmidt, Aditya Chopra, **Qijing Huang**, Kyle Kovacs, Borivoje Nikolic, Randy Katz, Jonathan Bachrach, Krste Asanovic
   2018 International Symposium on Computer Architecture (ISCA)

10. Synthesis of Program Binaries into FPGA Accelerators with Runtime Dependence Validation. (Paper, Slides, Best Paper Award)
    Shaoyi Cheng, **Qijing Huang**, John Wawrzynek
    2017 Field Programmable Technology (FPT)

11. The Effect of Compiler Optimizations on High-Level Synthesis for FPGAs. (Paper)
Qijing Huang, Ruolong Lian, Andrew Canis, Jongsok Choi, Ryan Xi, Stephen Brown, Jason Anderson
2013 Field-Programmable Custom Computing Machines (FCCM)

12. From Software to Accelerators with LegUp High-Level Synthesis. (Paper)
Andrew Canis, Jongsok Choi, Blair Fort, Ruolong Lian, **Qijing Huang**, Nazanin Calagar, Marcel Gort, Jia Jun Qin, Mark Aldham, Tomasz Czajkowski, Stephen Brown, Jason Anderson
2013 Compilers, Architectures and Synthesis for Embedded Systems (CASES)

Journals

1. The Effect of Compiler Optimizations on High-Level Synthesis-Generated Hardware. (Paper)
Qijing Huang, Ruolong Lian, Andrew Canis, Jongsok Choi, Ryan Xi, Nazanin Calagar, Stephen Brown, Jason Anderson
2015 Transactions on Reconfigurable Technology and Systems (TRETS)

Workshop Papers

1. Algorithm-Hardware Co-design for Deformable Convolution. (Paper)
Qijing Huang*, Dequan Wang*, Yizhao Gao, Yaohui Cai, Zhen Dong, Bichen Wu, Kurt Keutzer, John Wawrzynek
2019 Energy Efficient Machine Learning and Cognitive Computing co-located with NeurIPS (EMC^2)

2. Integrating Nvidia Deep Learning Accelerator (NVDLA) with RISC-V SoC on FireSim. (Paper)
Farzad Farshchi, **Qijing Huang**, Heechul Yun
2019 Energy Efficient Machine Learning and Cognitive Computing co-located with HPCA (EMC^2)

Preprints

1. ProTuner: Tuning Programs with Monte Carlo Tree Search. (Paper)
Ameer Haj-Ali, Hasan Genc, **Qijing Huang**, William Moses, John Wawrzynek, Krste Asanovic, Ion Stoica

2. HAWQV3: DyadicNeural Network Quantization. (Paper)
Zhewei Yao*, Zhen Dong*, Zhangcheng Zheng*, Amir Gholami*, Jiali Yu, Eric Tan, Leyuan Wang, **Qijing Huang**, Yida Wang, Michael W. Mahoney, Kurt Keutzer

* for equal contribution

OTHER RESEARCH PROJECTS

Golang HLS (Report)(Github) *2017*
Implements an HLS flow for Golang to explicitly express parallelism via CSP abstraction

JCGAN Car Image Synthesis with GAN (Report)(Github) *2017*
Develops a generative deep learning model for synthesizing car images

Spark Twitter Language Classifier on GPU (Report)(Github) *2016*
Accelerates K-means classifier written in Spark on GPU

Reconfigurable Garp Coprocessor in Chisel (Report)(Github) *2016*
Implements a reconfigurable coprocessor in Chisel and synthesizes it with a hierarchical VLSI flow