# 1. Description

## 1.1. Project

| | |
|---|---|
| Project Name | Rear |
| Board Name | NUCLEO-F767ZI |
| Generated with: | STM32CubeMX 4.22.0 |
| Date | 09/04/2017 |

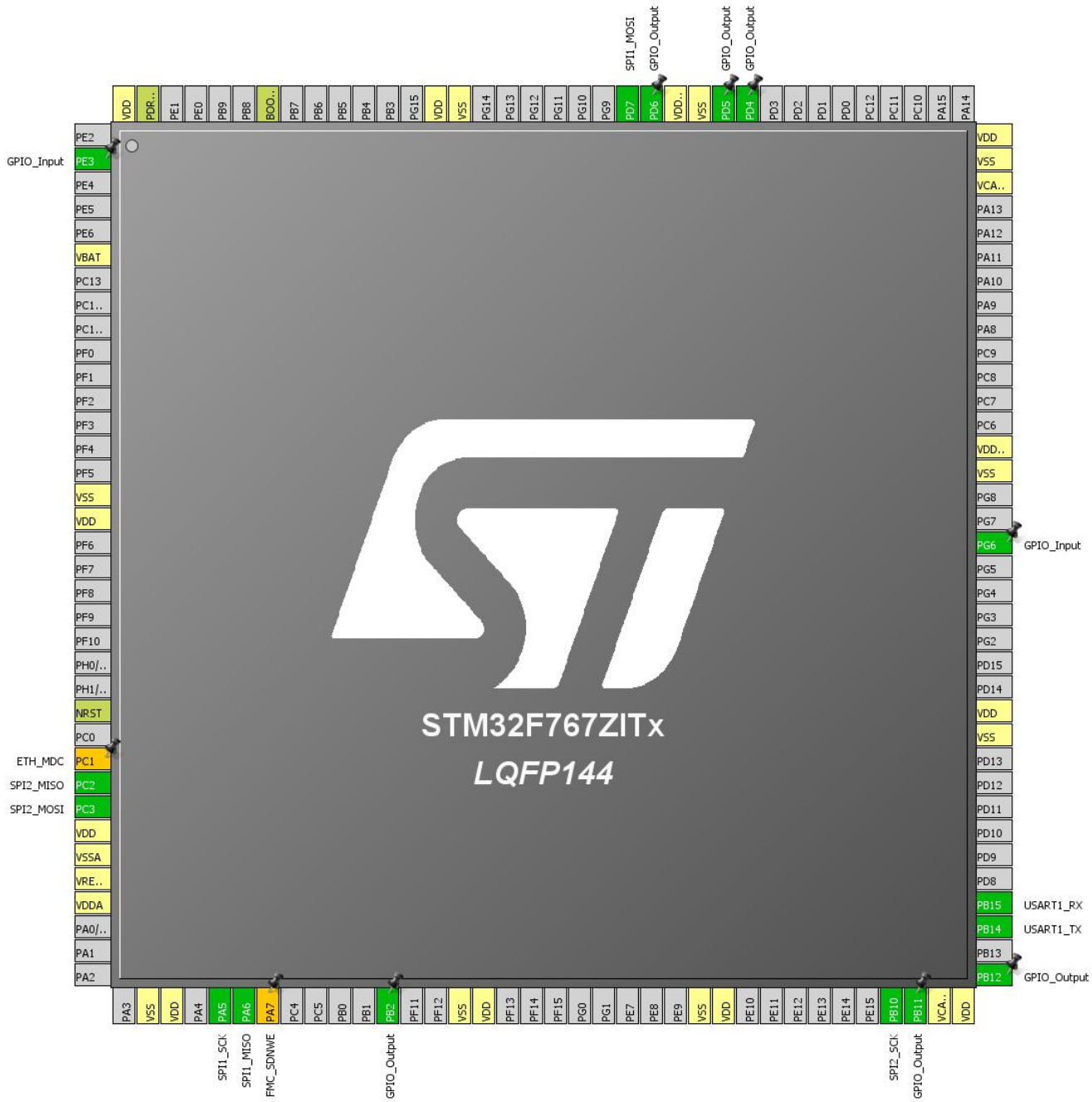
## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F7 |
| MCU Line | STM32F7x7 |
| MCU name | STM32F767ZITx |
| MCU Package | LQFP144 |
| MCU Pin number | 144 |

## 1.3. Caution

The report was generated although the configuration was in a modified state. It may be not accurate

# 2. Pinout Configuration



# 3. Pins Configuration

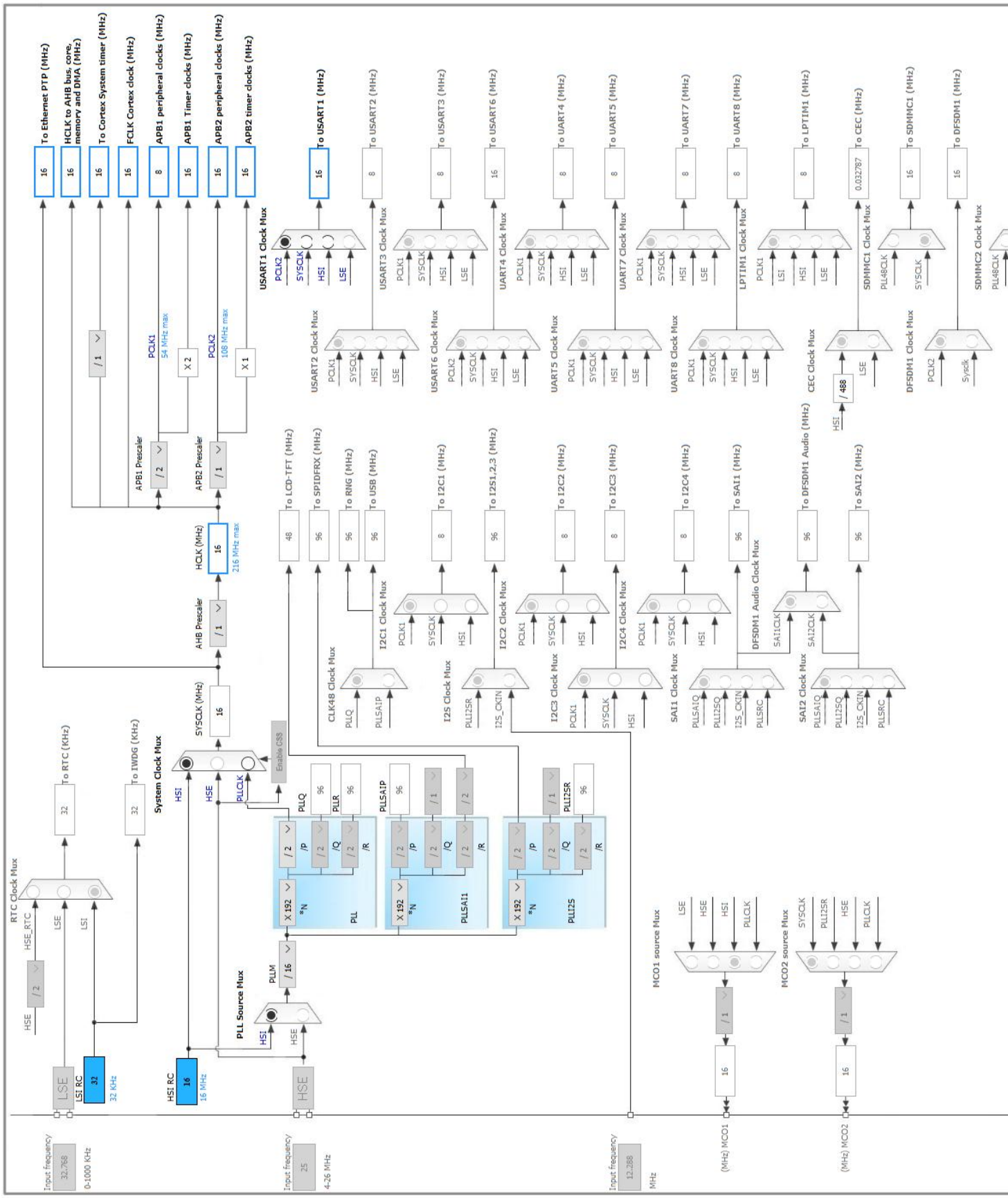
| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 2 | PE3 * | I/O | GPIO_Input | |
| 6 | VBAT | Power | | |
| 16 | VSS | Power | | |
| 17 | VDD | Power | | |
| 25 | NRST | Reset | | |
| 27 | PC1 ** | I/O | ETH_MDC | |
| 28 | PC2 | I/O | SPI2_MISO | |
| 29 | PC3 | I/O | SPI2_MOSI | |
| 30 | VDD | Power | | |
| 31 | VSSA | Power | | |
| 32 | VREF+ | Power | | |
| 33 | VDDA | Power | | |
| 38 | VSS | Power | | |
| 39 | VDD | Power | | |
| 41 | PA5 | I/O | SPI1_SCK | |
| 42 | PA6 | I/O | SPI1_MISO | |
| 43 | PA7 ** | I/O | FMC_SDNWE | |
| 48 | PB2 * | I/O | GPIO_Output | |
| 51 | VSS | Power | | |
| 52 | VDD | Power | | |
| 61 | VSS | Power | | |
| 62 | VDD | Power | | |
| 69 | PB10 | I/O | SPI2_SCK | |
| 70 | PB11 * | I/O | GPIO_Output | |
| 71 | VCAP_1 | Power | | |
| 72 | VDD | Power | | |
| 73 | PB12 * | I/O | GPIO_Output | |
| 75 | PB14 | I/O | USART1_TX | |
| 76 | PB15 | I/O | USART1_RX | |
| 83 | VSS | Power | | |
| 84 | VDD | Power | | |
| 91 | PG6 * | I/O | GPIO_Input | |
| 94 | VSS | Power | | |
| 95 | VDDUSB | Power | | |
| 106 | VCAP_2 | Power | | |
| 107 | VSS | Power | | |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 108 | VDD | Power | | |
| 118 | PD4 * | I/O | GPIO_Output | |
| 119 | PD5 * | I/O | GPIO_Output | |
| 120 | VSS | Power | | |
| 121 | VDDSDMMC | Power | | |
| 122 | PD6 * | I/O | GPIO_Output | |
| 123 | PD7 | I/O | SPI1_MOSI | |
| 130 | VSS | Power | | |
| 131 | VDD | Power | | |
| 138 | BOOT0 | Boot | | |
| 143 | PDR_ON | Reset | | |
| 144 | VDD | Power | | |

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

# 4. Clock Tree Configuration



# 5. IPs and Middleware Configuration

## 5.1. SPI1

**Mode: Full-Duplex Master**

### 5.1.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | **8 Bits *** |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | **4 *** |
| Baud Rate | **4.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | **Disabled *** |
| NSS Signal Type | Software |

## 5.2. SPI2

**Mode: Full-Duplex Master**

### 5.2.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | **8 Bits *** |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | **4.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | **Disabled *** |
| NSS Signal Type | Software |

## *5.3. SYS*

**Timebase Source: SysTick**

## *5.4. USART1*

**Mode: Asynchronous**

### 5.4.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | **9600 *** |
| Word Length | **8 Bits (including Parity) *** |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

*** User modified value**

# 6. System Configuration

## 6.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| SPI1 | PA5 | SPI1_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PA6 | SPI1_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PD7 | SPI1_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| SPI2 | PC2 | SPI2_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PC3 | SPI2_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PB10 | SPI2_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| USART1 | PB14 | USART1_TX | Alternate Function Push Pull | Pull-up | **Very High *** | |
| | PB15 | USART1_RX | Alternate Function Push Pull | Pull-up | **Very High *** | |
| Single Mapped Signals | PC1 | ETH_MDC | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PA7 | FMC_SDNWE | Alternate Function Push Pull | No pull-up and no pull-down | Very High | |
| GPIO | PE3 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | |
| | PB2 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **High *** | |
| | PB11 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **High *** | |
| | PB12 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **High *** | |
| | PG6 | GPIO_Input | Input mode | No pull-up and no pull-down | **n/a** | |
| | PD4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **High *** | |
| | PD5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **High *** | |
| | PD6 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | **High *** | |

## 6.2. DMA configuration

nothing configured in DMA service

## 6.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 0 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| SPI1 global interrupt | unused | | |
| SPI2 global interrupt | unused | | |
| USART1 global interrupt | unused | | |
| FPU global interrupt | unused | | |

*** User modified value**

# 7. Power Consumption Calculator report

7.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F7 |
| Line | STM32F7x7 |
| MCU | STM32F767ZITx |
| Datasheet | 029041_Rev3 |

7.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.6 |

# 8. Software Project

## 8.1. Project Settings

| Name | Value |
|---|---|
| Project Name | Rear |
| Project Folder | C:\Users\ljh70\Desktop\boardcar\Code\Rear |
| Toolchain / IDE | MDK-ARM V5 |
| Firmware Package Name and Version | STM32Cube FW_F7 V1.7.0 |

## 8.2. Code Generation Settings

| Name | Value |
|---|---|
| STM32Cube Firmware Library Package | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | No |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |