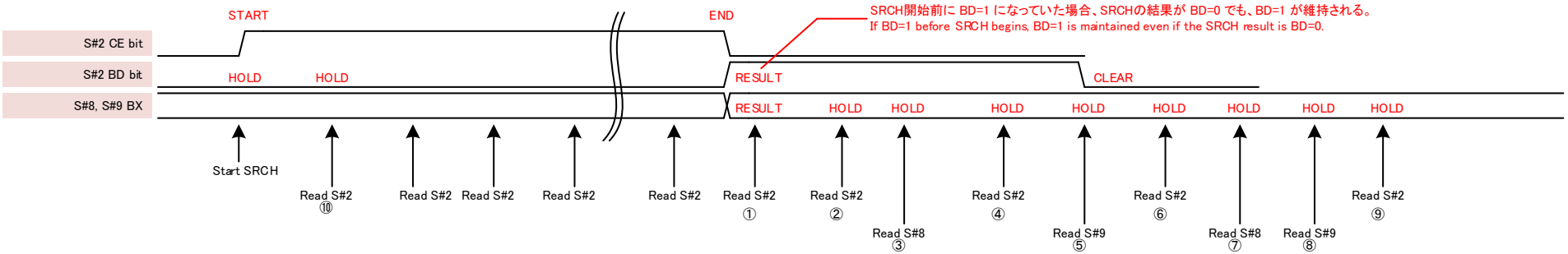
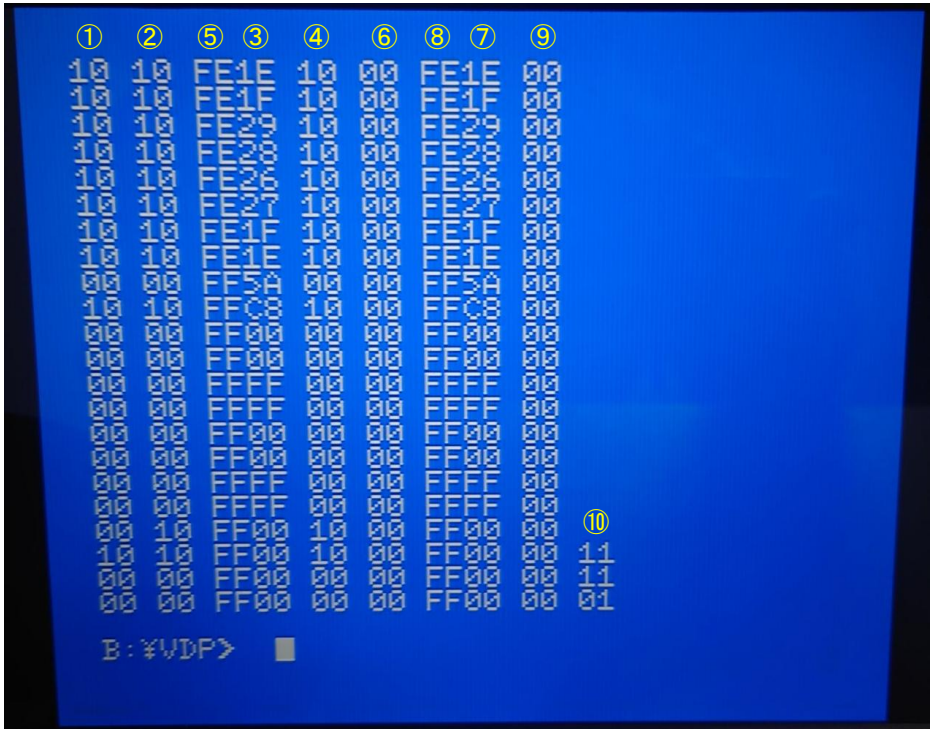

START
END
SRCH開始前に BD=1 になっていた場合、SRCHの結果が BD=0 でも、BD=1 が維持される。
If BD=1 before SRCH begins, BD=1 is maintained even if the SRCH result is BD=0.
S#2 CE bit
S#2 BD bit
S#8, S#9 BX
HOLD
HOLD
RESULT
CLEAR
RESULT
HOLD
HOLD
HOLD
HOLD
HOLD
HOLD
HOLD
HOLD
Start SRCH
Read S#2 ⑩
Read S#2
Read S#2
Read S#2
Read S#2
Read S#2 ①
Read S#2 ②
Read S#8 ③
Read S#2 ④
Read S#9 ⑤
Read S#2 ⑥
Read S#8 ⑦
Read S#9 ⑧
Read S#2 ⑨


① ② ⑤ ③ ④ ⑥ ⑧ ⑦ ⑨
10 10 FE1E 10 00 FE1E 00
10 10 FE1F 10 00 FE1F 00
10 10 FE29 10 00 FE29 00
10 10 FE28 10 00 FE28 00
10 10 FE26 10 00 FE26 00
10 10 FE27 10 00 FE27 00
10 10 FE1F 10 00 FE1F 00
10 10 FE1E 10 00 FE1E 00
00 00 FF5A 00 00 FF5A 00
10 10 FFC8 10 00 FFC8 00
00 00 FF00 00 00 FF00 00
00 00 FF00 00 00 FF00 00
00 00 FFFF 00 00 FFFF 00
00 00 FFFF 00 00 FFFF 00
00 00 FF00 00 00 FF00 00
00 00 FF00 00 00 FF00 00
00 00 FFFF 00 00 FFFF 00
00 00 FFFF 00 00 FFFF 00
00 10 FF00 10 00 FF00 00 ⑩
10 10 FF00 10 00 FF00 00 11
00 00 FF00 00 00 FF00 00 11
00 00 FF00 00 00 FF00 00 01
B:¥VDP>