



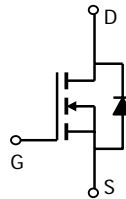
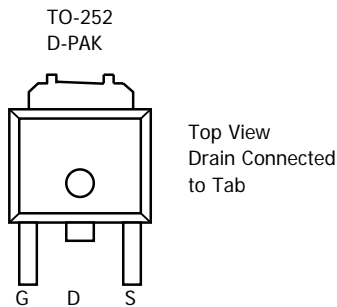
## AOD414, AOD414L( Green Product ) N-Channel Enhancement Mode Field Effect Transistor

### General Description

The AOD414 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , shoot-through immunity and body diode characteristics. This device is ideally suited for use as a low side switch in CPU core power conversion. AOD414L ( Green Product ) is offered in a lead-free package.

### Features

$V_{DS}$  (V) = 30V  
 $I_D$  = 85A  
 $R_{DS(ON)} < 5.2m\Omega$  ( $V_{GS} = 10V$ )  
 $R_{DS(ON)} < 7.0m\Omega$  ( $V_{GS} = 4.5V$ )



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		$V_{DS}$	30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>B,G</sup>	$T_C=25^\circ\text{C}$ <sup>G</sup>	$I_D$	85	A
	$T_C=100^\circ\text{C}$ <sup>B</sup>		73	
Pulsed Drain Current		$I_{DM}$	200	
Avalanche Current <sup>C</sup>		$I_{AR}$	30	A
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>		$E_{AR}$	140	mJ
Power Dissipation <sup>B</sup>	$T_C=25^\circ\text{C}$	$P_D$	100	W
	$T_C=100^\circ\text{C}$		50	
Power Dissipation <sup>A</sup>	$T_A=25^\circ\text{C}$	$P_{DSM}$	2.5	W
	$T_A=70^\circ\text{C}$		1.6	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$t \leq 10\text{s}$	$R_{\theta JA}$	14.2	20	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>	Steady-State		40	50	$^\circ\text{C/W}$
Maximum Junction-to-Lead <sup>C</sup>	Steady-State	$R_{\theta JL}$	0.56	1.5	$^\circ\text{C/W}$

Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C		0.005	1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±20V			100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> I <sub>D</sub> =250μA	1.2	1.8	2.4	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =5V	110			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A T <sub>J</sub> =125°C		4.2 6	5.2 7.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A		5.6	7	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		85		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current				85	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =15V, f=1MHz		6060	7000	pF
C <sub>oss</sub>	Output Capacitance			638		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			355		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		0.45	0.6	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub> (10V)	Total Gate Charge	V <sub>GS</sub> =4.5V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A		96.4	115	nC
Q <sub>g</sub> (4.5V)	Total Gate Charge			46.4	55	nC
Q <sub>gs</sub>	Gate Source Charge			13.6		nC
Q <sub>gd</sub>	Gate Drain Charge			15.6		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, R <sub>L</sub> =0.75Ω, R <sub>GEN</sub> =3Ω		15.7	21	ns
t <sub>r</sub>	Turn-On Rise Time			14.2	21	ns
t <sub>D(off)</sub>	Turn-Off DelayTime			55.5	75	ns
t <sub>f</sub>	Turn-Off Fall Time			14	21	ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=100A/μs		31	38	ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=100A/μs		24	29	nC

A: The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The Power dissipation P<sub>DSM</sub> is based on steady-state R<sub>θJA</sub> and the maximum allowed junction temperature of 150°C. The value in any a given application depends on the user's specific board design, and the maximum temperature fo 175°C may be used if the PCB or heatsink allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

C: Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

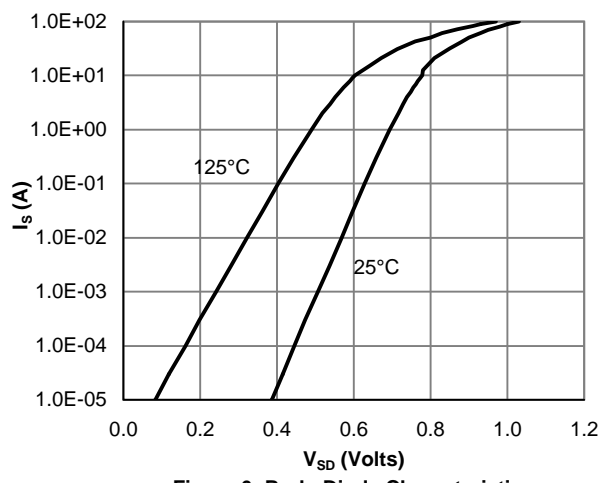
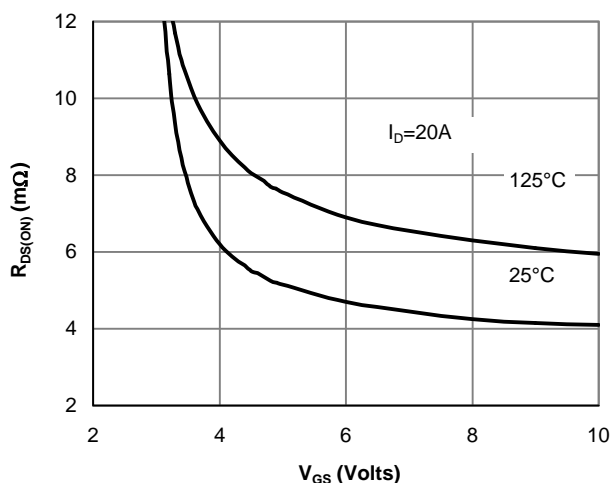
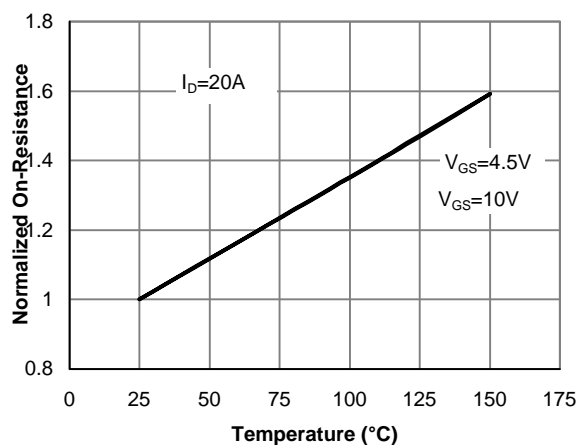
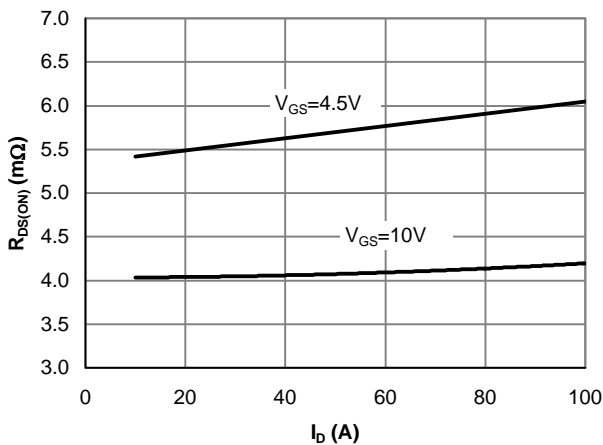
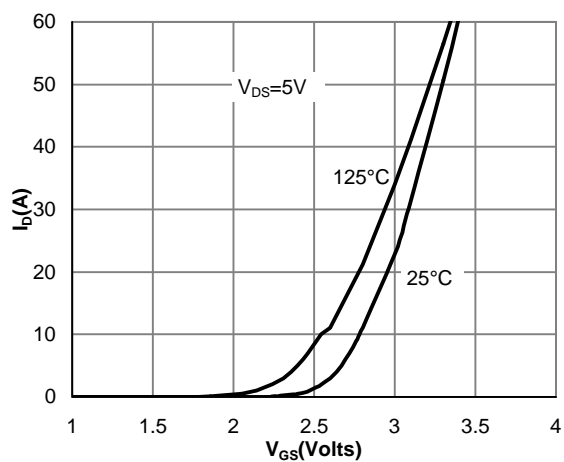
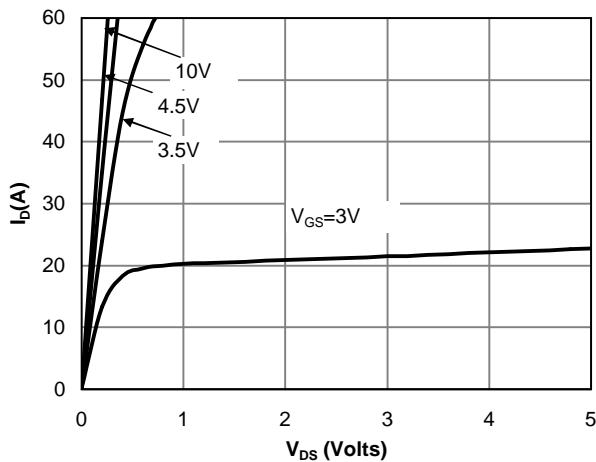
E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by the package current capability.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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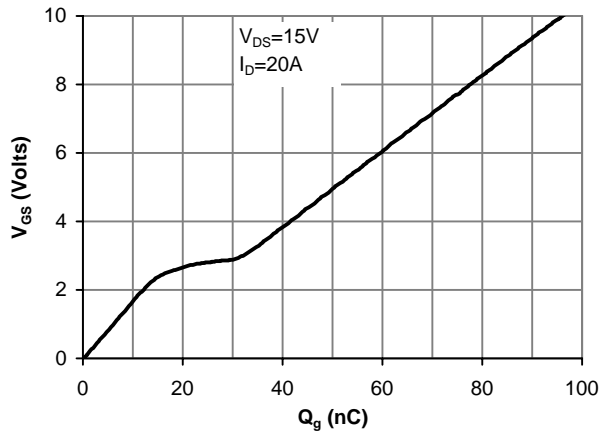


Figure 7: Gate-Charge Characteristics

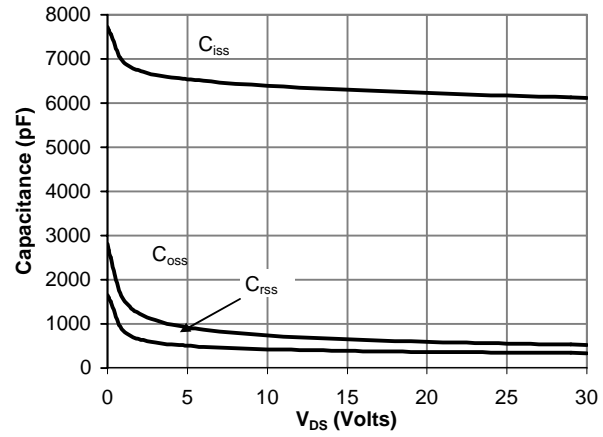


Figure 8: Capacitance Characteristics

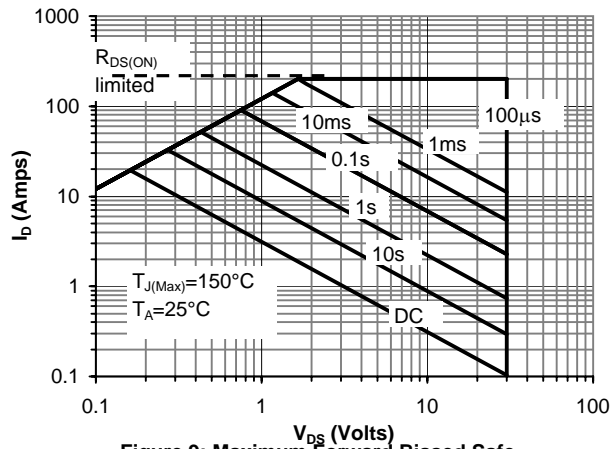


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

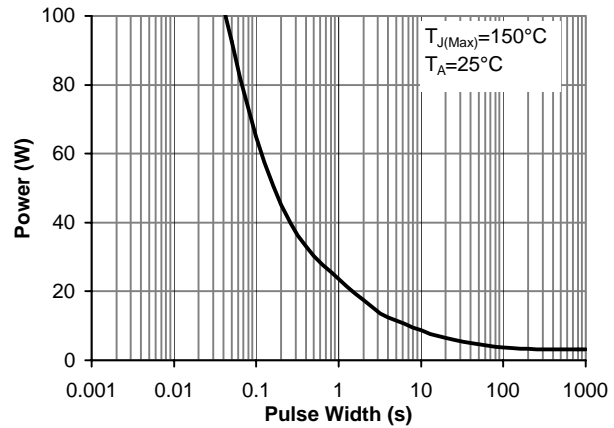


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

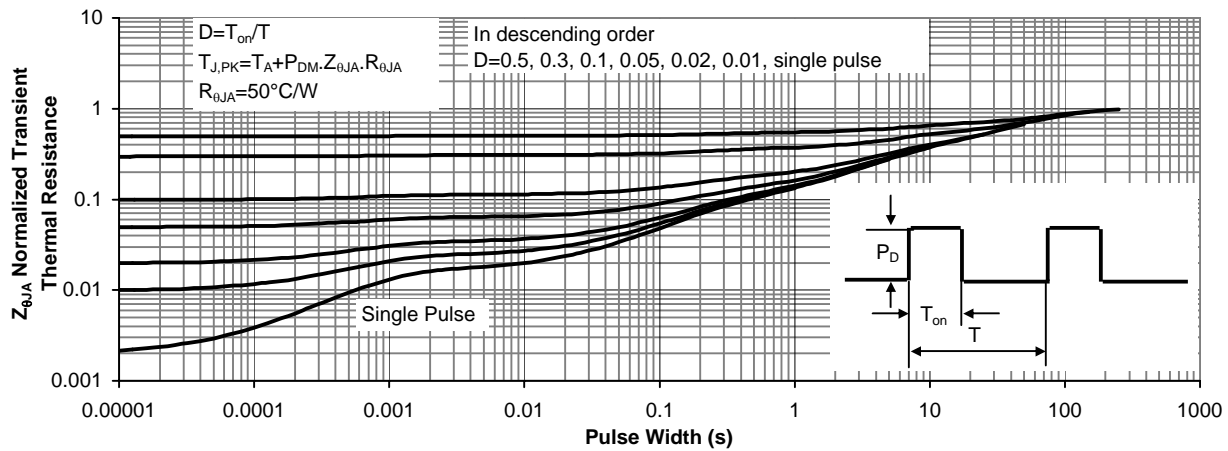


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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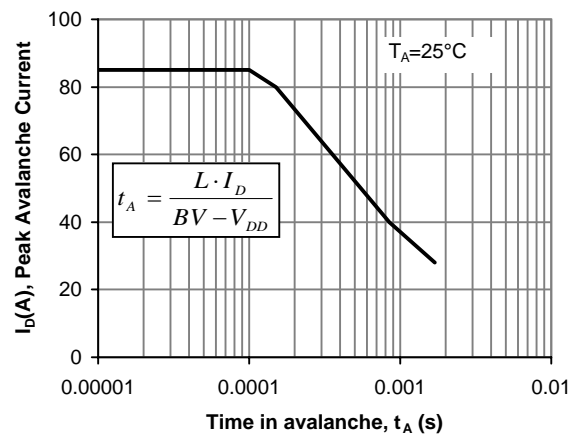


Figure 12: Single Pulse Avalanche capability

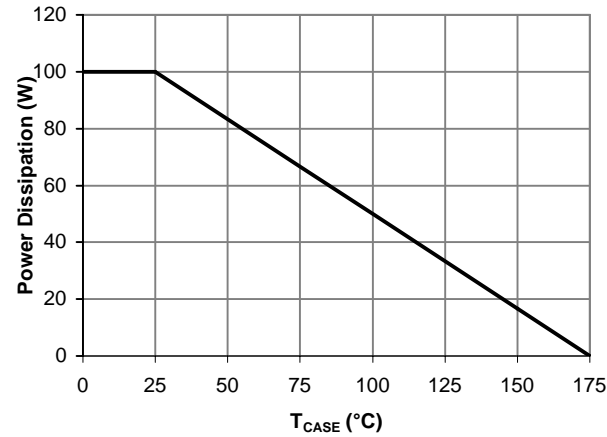


Figure 13: Power De-rating (Note B)

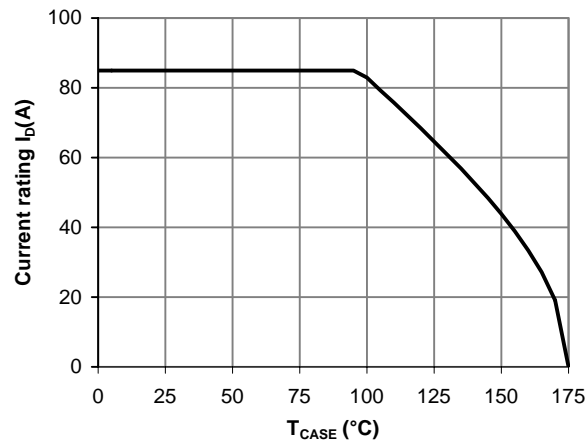


Figure 14: Current De-rating (Note B)