A5.1 ARM instruction set encoding

The ARM instruction stream is a sequence of word-aligned words. Each ARM instruction is a single 32-bit word in that stream. The encoding of an ARM instruction is:

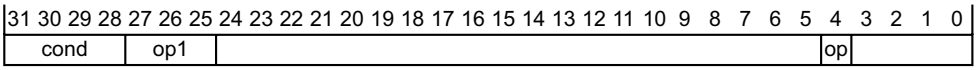


Table A5-1 shows the major subdivisions of the ARM instruction set, determined by bits[31:25, 4].

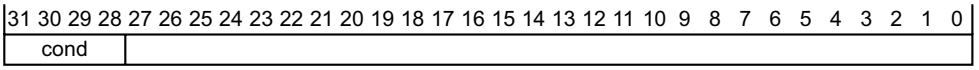
Most ARM instructions can be conditional, with a condition determined by bits[31:28] of the instruction, the `cond` field. For more information see *The condition code field*. This applies to all instructions except those with the cond field equal to `0b1111`.

Table A5-1 ARM instruction encoding

cond	op1	op	Instruction classes
not 1111	00x	-	*Data-processing and miscellaneous instructions* on page A5-196.
	010	-	*Load/store word and unsigned byte* on page A5-208.
	011	0	*Load/store word and unsigned byte* on page A5-208.
		1	*Media instructions* on page A5-209.
	10x	-	*Branch, branch with link, and block data transfer* on page A5-214.
	11x	-	*Coprocessor instructions, and Supervisor Call* on page A5-215. Includes Floating-point instructions and Advanced SIMD data transfers, see Chapter A7 *Advanced SIMD and Floating-point Instruction Encoding*.
1111	-	-	If the cond field is `0b1111`, the instruction can only be executed unconditionally, see *Unconditional instructions* on page A5-216. Includes Advanced SIMD instructions, see Chapter A7 *Advanced SIMD and Floating-point Instruction Encoding*.

A5.1.1 The condition code field

Every conditional instruction contains a 4-bit condition code field, the `cond` field, in bits 31 to 28:



This field contains one of the values `0b0000`-`0b1110`, as shown in Table A8-1 on page A8-288. Most instruction mnemonics can be extended with the letters defined in the *mnemonic extension* column of this table.

If the *always* (`AL`) condition is specified, the instruction is executed irrespective of the value of the condition flags. The absence of a condition code on an instruction mnemonic implies the `AL` condition code.