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Technical Reference

Surge Arrester

StaSua, StaSuabi

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POWER SYSTEM SOLUTIONS

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Contents

1 General Description

This document describes the models of the surge arrester *StaSua* and the surge arrester with two terminals *StaSuabi*.

In general, the surge arrester model in *PowerFactory* defines a highly nonlinear voltage-current (V-I) characteristic using peak values. This nonlinear characteristic represents the requirement that the surge arrester should have a very high resistance during normal system operation and a low resistance during transient disturbances. The peak voltage-current values are input using the surge arrester element (*StaSua*) via the *Characteristic* table on the *Basic Data* tab of the dialogue.

Values lying between those specifed are interpolated according to the user-selected *Interpolation* mode. For *spline* interpolation, the values are obtained according to the derivative of the first/last point. For *piecewise linear* interpolation, the values are obtained according to the derivative of the first/last inner interval. The interpolated V-I characteristic is then depicted graphically on the *Diagram* tab in the dialogue, as shown in Figure 1.1.

The characteristic represents the full range of the surge arrester, including its ”normal” condition (i.e. leakage current for the rated voltage). It should be noted that this graphical representation uses a logarithmic scale on the x-axis, and therefore cannot display zero current values entered into the *Characteristic* table. In *PowerFactory* , the surge arrester element is only considered by the EMT simulation.

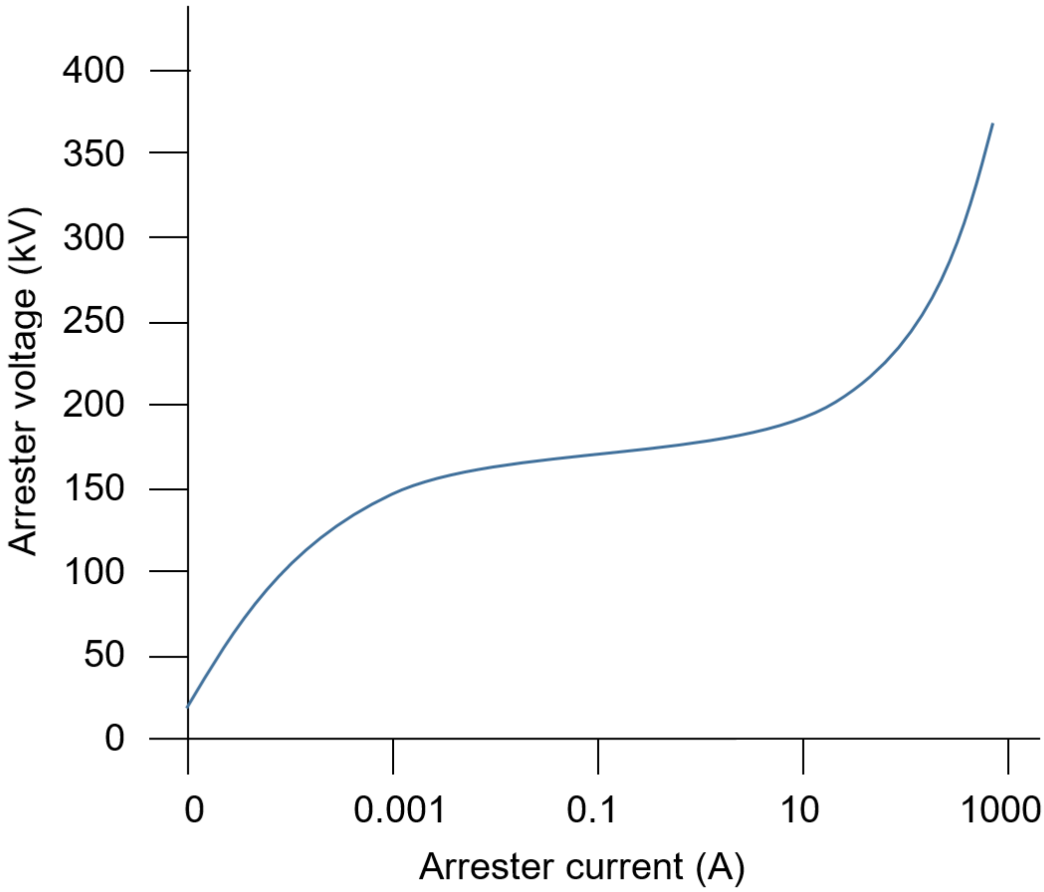

Figure 1.1: Surge arrester element plot

2 Surge Arrester

The surge arrester model circuit diagram is shown in Figure 2.1. The capacitor $C0$ represents the stray capacitance of the arrester to ground, $L0$ represents the stray inductance, while $R0$ represents the grounding resistance. These values can be estimated based on the physical dimensions of the arrester (which are commonly provided in manufacturers' datasheets), using formulae such as those used in [1].

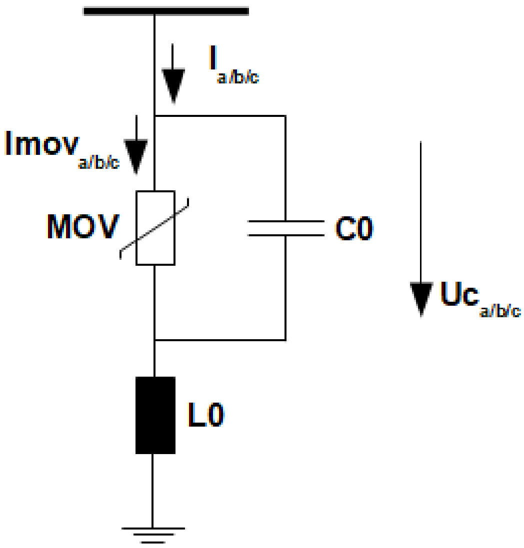

Figure 2.1: 1-Terminal surge arrester model circuit diagram

2.1 EMT Simulation

In the EMT simulation, the surge arrester is represented as a nonlinear resistance where the peak values of the current (I_{mov}) are interpolated from the current values of the residual voltage (U_{mov}).

The surge arrester model has a capacitor, $C0$, in parallel with the MOV, leading to the following expression for the phase current, I_a:

$$I_a = I_{mov_a} + C0 \cdot dU_{c_a} \tag{1}$$

where dU_{c_a} is the derivative of the phase-A voltage.

The calculation of the voltage at the terminal considers the inductance $L0$ and the resistance $R0$ which are in series with the MOV:

$$U_a = U_{c_a} + L0 \cdot dI_a + R0 \cdot I_a \tag{2}$$

where U_a is the voltage at the terminal in the case of the 1-terminal surge arrester and between terminals for the 2-terminals surge arrester, U_{c_a} is the voltage across the MOV and the capacitor, and dI_a is the derivative of the phase-A current.

The instantaneous power is expressed as:

$$P_{mov_a} = I_a \cdot U_a \tag{3}$$

and the MOV energy, E_{mov}, is calculated from the instantaneous power, P_{mov}:

$$E_{mov_a} = \int P_{mov_a} \tag{4}$$

2.1.1 Spark Gap

The surge arrester model for EMT simulations allows the definition of a protection spark gap, via the selection of the *Spark Gap* option. Once this option is selected, the resistance and reactance of the damping circuit can be defined. The spark gap model is shown in Figure 2.2.

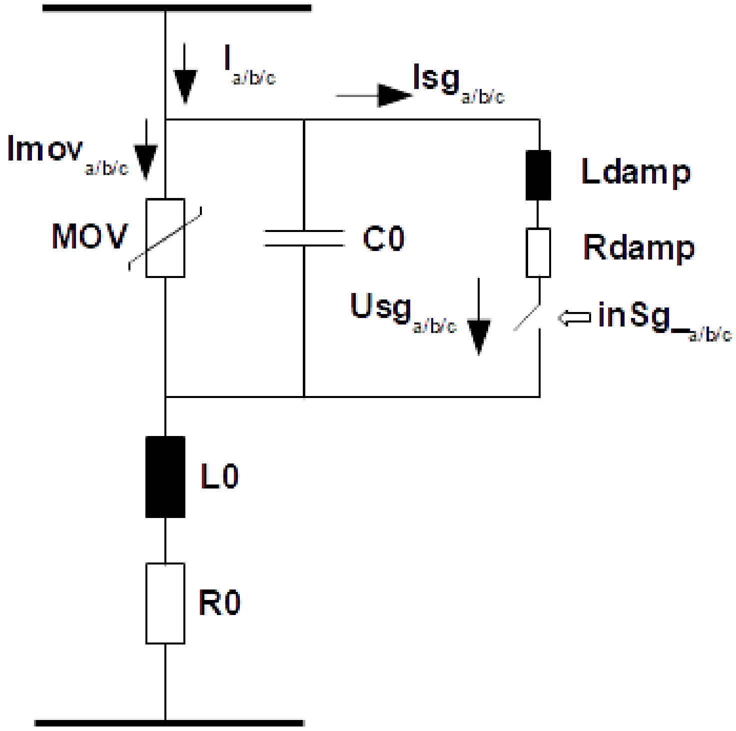

Figure 2.2: Spark gap model

External Tripping When the option *Built-In Tripping Unit* is deactivated, the spark gap can be triggered via the use of input signals *inSg_A*, *inSg_B* and *inSg_C* (defined in Table A.1) using either a parameter event (*EvtParam*) defined for the EMT simulation, or via an external DSL controller.

Built-In Tripping Unit By activating the option *Built-In Tripping Unit*, it is possible to specify the voltage value at which the spark gap will trigger.

3 Surge Arrester with Two Terminals

The surge arrester with two-terminals (*StaSuabi*) model circuit diagram is shown in Figure 3.1. The capacitor $C0$ represents the stray capacitance of the arrester. $L0$ represents the stray inductance, while $R0$ represents the series resistance. These values can be estimated based on the physical dimensions of the arrester (which are commonly provided in manufacturers' datasheets), using formulae such as those used in [1].

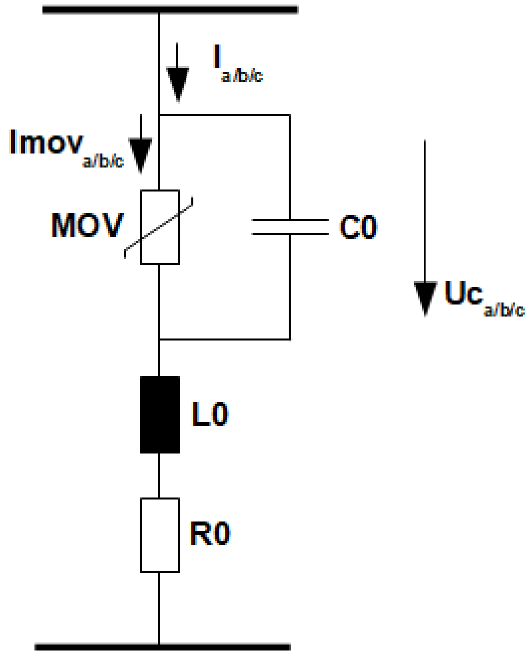

Figure 3.1: 2-Terminals surge arrester model circuit diagram

Where

$$U_{c_a} = U_{c_a(T1)} - U_{c_a(T2)} \tag{5}$$
$$U_{c_b} = U_{c_b(T1)} - U_{c_b(T2)} \tag{6}$$
$$U_{c_c} = U_{c_c(T1)} - U_{c_c(T2)} \tag{7}$$

3.1 EMT Simulation

The model described in Section 2.1 is also valid for the two-terminal model, considering the voltage differential given by equations 5 to 7.

3.1.1 Spark Gap

The model described in Section 2.1.1 is also valid for the two-terminal model.

A Input Parameters

A.1 Internal Signals

Parameter	Unit	I/O	Description	Symbol
Emov_a	MWs	STATE	MOV absorbed energy	E_{mov_a}
Emov_b	MWs	STATE	MOV absorbed energy	E_{mov_b}
Emov_c	MWs	STATE	MOV absorbed energy	E_{mov_c}
Uc_a	kV	STATE	Capacitor voltage	Uc_a
Uc_b	kV	STATE	Capacitor voltage	Uc_b
Uc_c	kV	STATE	Capacitor voltage	Uc_c
inRs	Ohm	IN	Series resistance	
inSg_A		IN	Spark gap trigger	$inSg_a$
inSg_B		IN	Spark gap trigger	$inSg_b$
inSg_C		IN	Spark gap trigger	$inSg_c$

Table A.1: Internal signals (EMT simulation)

B Parameter Definitions

Parameter	Unit	Default Value	Description	Range	Symbol
loc_name			Name		
bus1			Terminal (StaCubic)		
bus1_bar			Terminal		
cpZone			Zone		
cpArea			Area		
outserv		0	Out of Service	x≥0 and x≤1	
nphase		3	No. of Phases	1:3	
pbusbar			Location (StaBar,ElmTerm, StaCubic)		
cbusbar			Location		
Im	kA	0,	Current		$Imov$
Vm	kV	0,	Voltage		Uc
iInterPol		0	Interpolation	spline:- piecewise linear	
smoothfac	%	10,	Smoothing Factor	x≥0.0 and x≤100.0	
Cp	uF	0,	Stray Capacitance	x≥0	$C0$
Ls	mH	0,	Series Inductance	x≥0	$L0$
Rs	Ohm	0,	Series Resistance	x≥0	$R0$
iSparkGap		0,	Consider spark gap	x≥0 and x≤1	
Rdamp	Ohm	0,	Damping Resistance	x≥0	$R0$
Xdamp	Ohm	0,	Damping Inductance	x≥0	$R0$
iBuiltIn		0,	Use built-in tripping	x≥0 and x≤1	
Uthr	kV	0,	Voltage threshold	x≥0	$R0$
gnrl_modif		01.01.1970 01:00:00	Object modified		
gnrl_modby			Object modified by		
chr_name			Characteristic Name		
for_name			Foreign Key		
dat_src		MAN	Data source		
desc			Description		
appr_status		Not Approved	Approval Information: Status		
appr_modif		01.01.1970 01:00:00	Approval Information: Modified		
appr_modby			Approval Information: Modified by		
cimRdfId			RDF ID		

Table B.1: Input parameters for surge arrester (StaSua)

C References

[1] IEEE Working Group 3.4.11. Modeling of Metal Oxide Surge Arresters. *IEEE Transactions on Power Delivery*, 7, 1992.

List of Figures

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