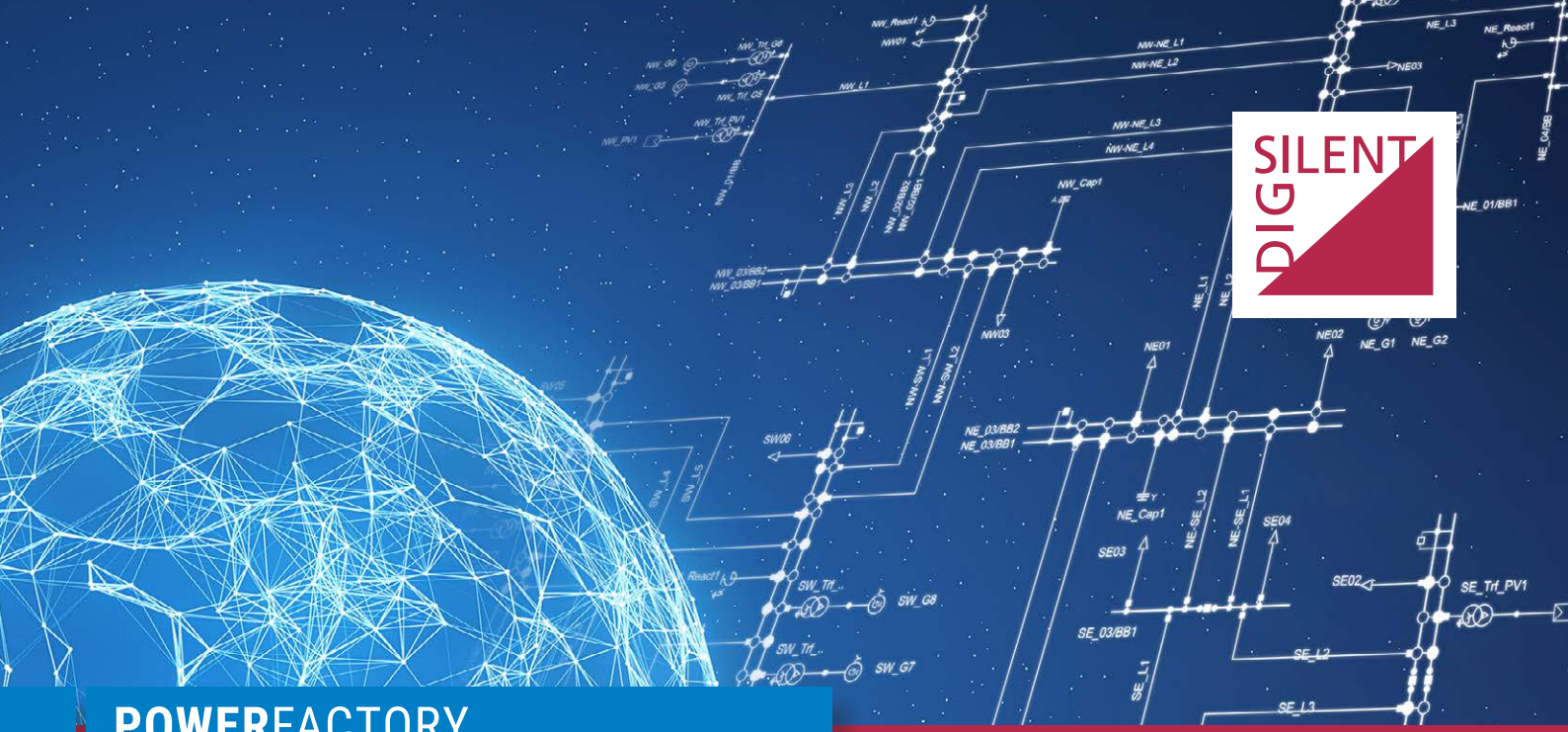

POWERFACTORY

PowerFactory 2021

Technical Reference

Sample and Hold

ElmSamp

PF2021

POWER SYSTEM SOLUTIONS

MADE IN GERMANY

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December 1, 2020
PowerFactory 2021
Revision 1

Contents

1 General Description

Analog signals can not be connected to digital signal processing modules directly. The analog signal must be sampled first. Usually a sample and hold module is setting the output at the rising edge of the clock signal. The output value is constant up to the next clock pulse. The *Sample and Hold* model of *PowerFactory* is providing exactly this functionality. In the following S&H denotes *Sample and Hold*.

In *PowerFactory* the S&H model will produce the following output.

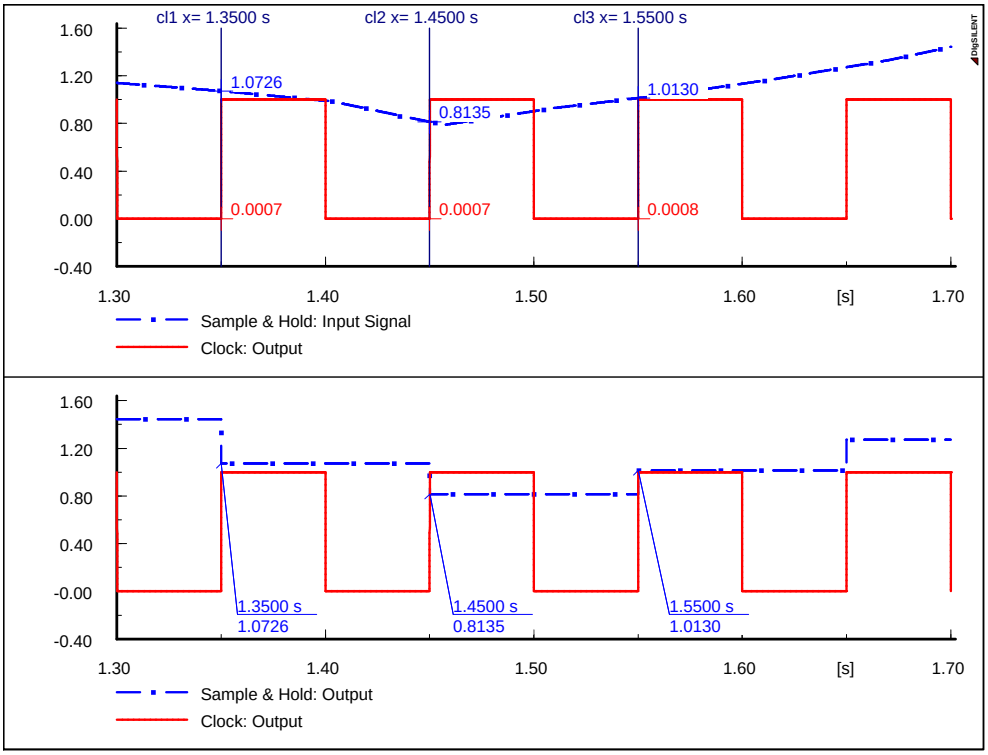

Figure 1.1: Plot Sample & Hold Output

In the example given in 1.1 the clock period is 100 ms. The upper plot shows the input signal of the clock. The plot on the bottom shows the output signal. At every rising edge of the clock pulse the input of the S&H model is read and written to the output. The intersection point between the vertical bars in the upper plot and the curve show the sampled value. The output of the S&H model is constant up to the next rising edge of the clock.

2 Dynamic Simulation

The input signals *input* and *cl* must always be connected for using the model in the simulation. *input_A*, *input_B* and *input_C* need not to be connected. Input values not connected are set to 0.

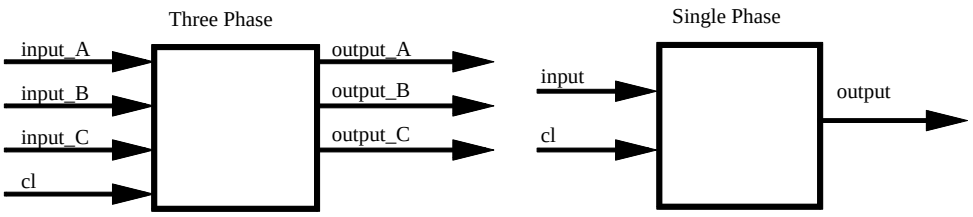

Figure 2.1: Input/Output Definitions

3 Example Configuration

Figure 3.1 shows a typical configuration for the use of the S&H model. An analog signal is connected to the input of the S&H model. The output of the S&H is the connected to the input of a register (*ElmReg*). The size of the register is one. Both, the register and the S&H model are connected to the same clock source. The plots show input and output of the S&H model and the output of the register.

Due to the register size of one there is a delay of one clock period between the input and the output of the register.

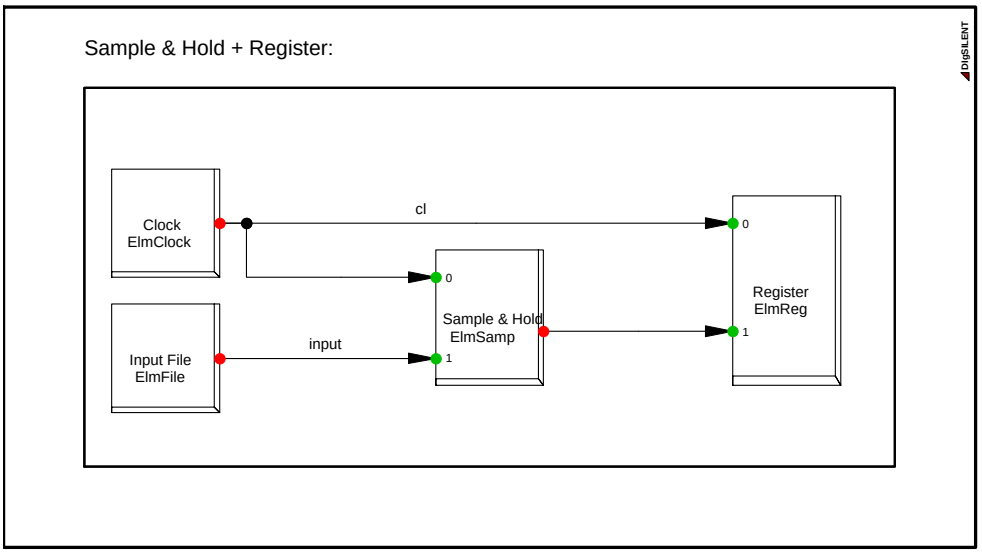

Figure 3.1: Block Diagram

Table 3.1: Example settings

Element	Classname	Variable	Value
Initial Conditions	*ComInc*	iopt_sim iopt_net dtgrd and dtout tstart	RMS values (Electromechanical Transients) Balanced, Positive Sequence 0.05 ms 0.05 ms
Clock	*ElmClock*	cFreq Tp tonTp	0.01 kHz 100 ms 0.5
Sample & Hold	*ElmSamp*	nphase	1
Register	*ElmReg*	nphase nsamp iopt_mod	1 1 Register

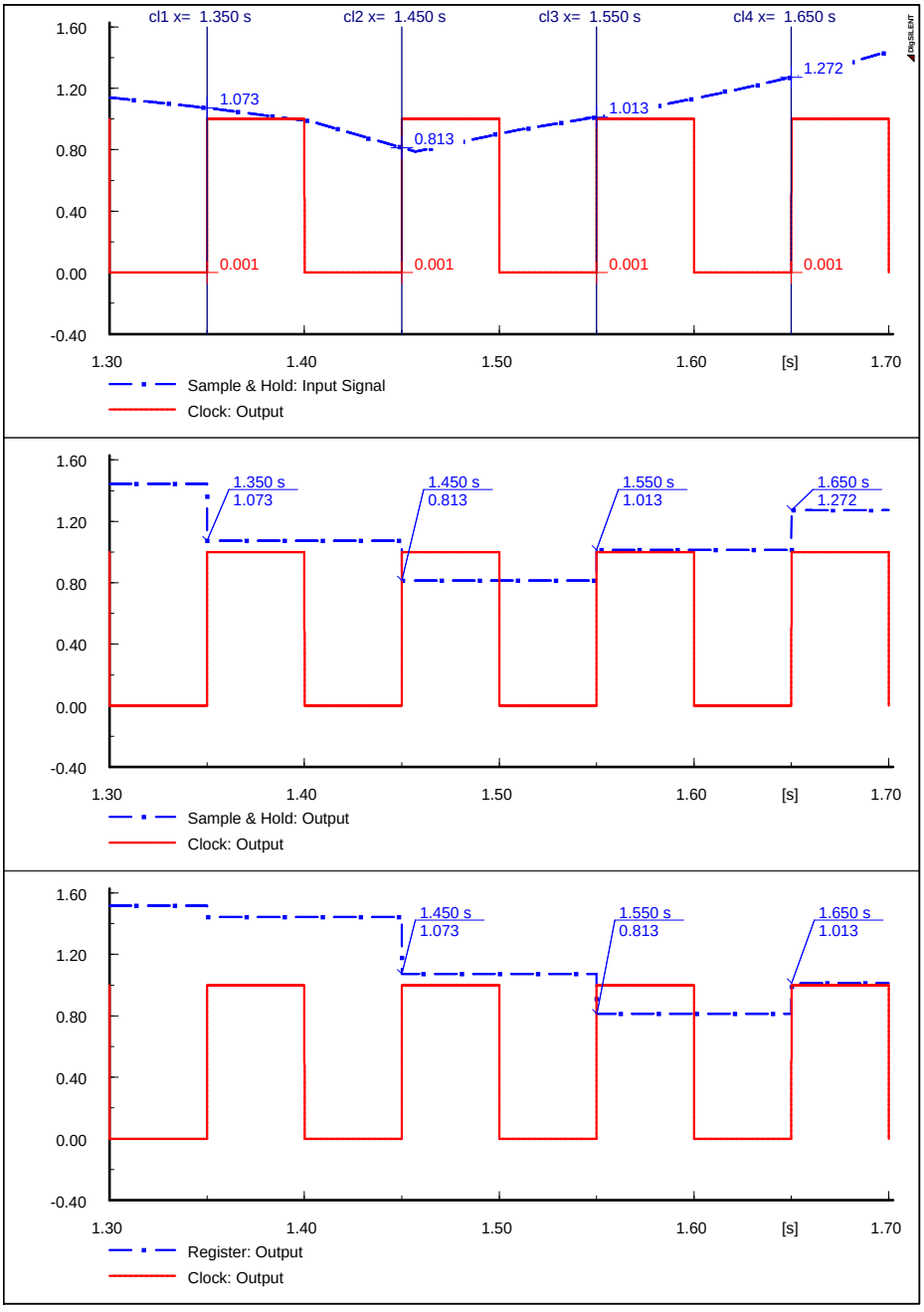

Figure 3.2: Example plots

A Parameter Definitions

Table A.1: Sample and Hold Parameters

Parameter	Description	Unit
loc_name	Name	
outserv	Out of service	
nphase	Number of phases	

B Signal Definitions

Table B.1: Input/Output signals

Name	Description	Unit	Type	Model
input_A	Input		IN	RMS, EMT
input_B	Input		IN	RMS, EMT
input_C	Input		IN	RMS, EMT
input	Input signal		IN	RMS, EMT
cl	Clock signal		IN	RMS, EMT
output_A	Output		OUT	RMS, EMT
output_B	Output		OUT	RMS, EMT
output_C	Output		OUT	RMS, EMT
output	Output signal		OUT	RMS, EMT

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