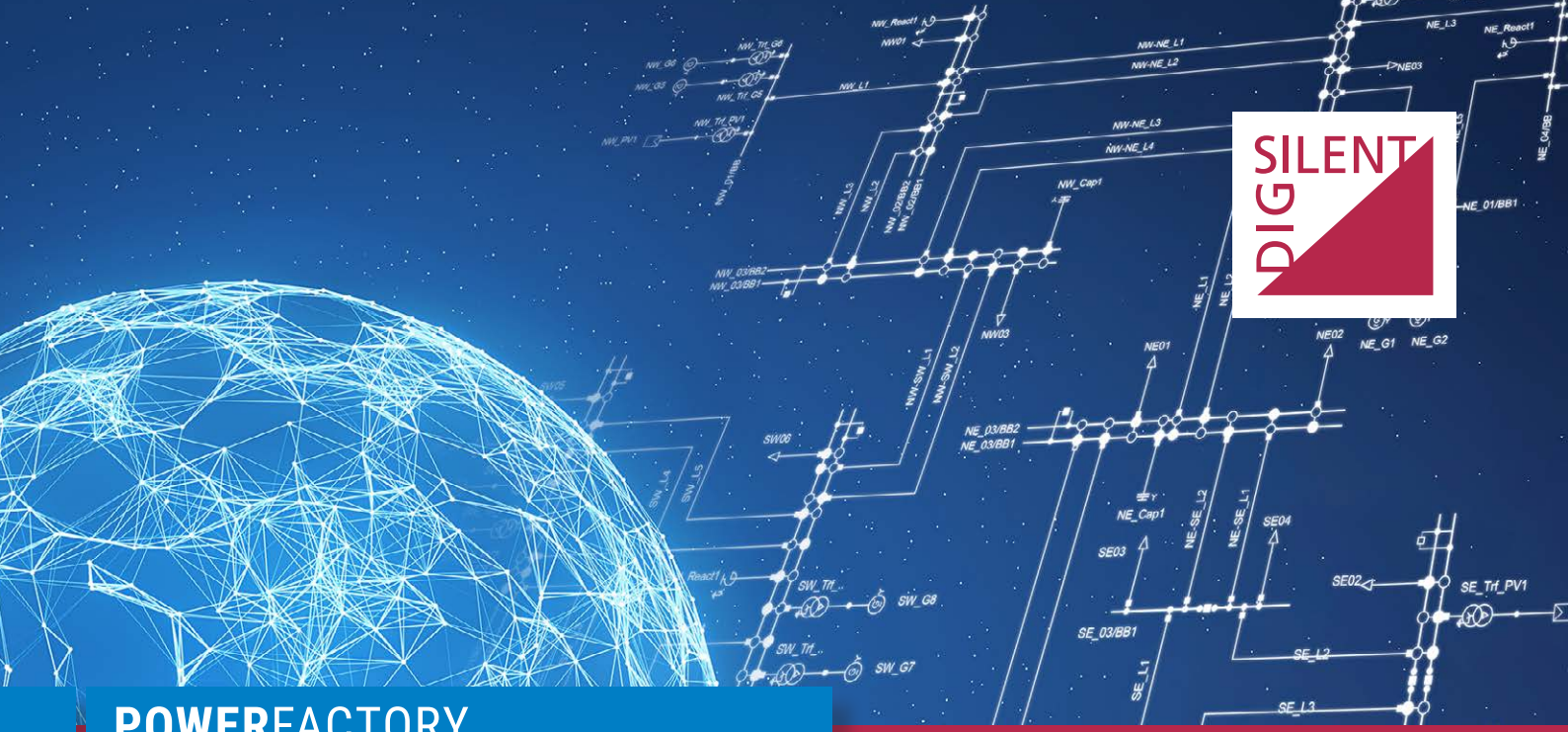

PowerFactory 2021

Technical Reference

DIgSILENT F78V Vector jump Generic Relay

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POWER SYSTEM SOLUTIONS

MADE IN GERMANY

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Contents

1 F78V Vector jump

1.1 Intent

To simulate the ability to detects the step change in frequency that occurs when a generator and local load is suddenly disconnected, or islanded, from the rest of the power system.

1.2 Functionality

The *F78V Vector jump* generic relay operates only running a RMS or an EMT simulation when a voltage angular discontinuity is detected. The algorithm compares the voltage phasor with the voltage phasor measured an half cycle and cycle before. The relay can operate in

- 1-phase mode.
- 3-phase mode.

In the *1-phase mode* the tripping takes place as soon as a measured voltage angular discontinuity greater than an user configurable parameter is detected on one of the three phase voltages. In the *3-phase mode* as soon that the discontinuity is detected on all the three phases at the same time. The *Operation mode* is set in the *DIP Settings* tab page of the ”Operation mode” block.
An undervoltage element blocks the ”Vector Jump”function if the voltage drops below an user configurable threshold.
An relay input signal can be used to block the *Vector jump* trip. The reset of the input signal can be delayed (”Input block delayed reset” block).

1.3 Inputs

- One 3 phase VT (”Phase Vt” block, *StaVt* class).
- One blocking signals (*iblock_1*).

1.4 Available Units

Measurement

- One 3phase measurement element (”Measurement” block, *RMS Calculation* enabled, *Filter* disabled [RelMeasure class]).

Protective elements

- One voltage element set with *Function* equal to *Vector shift* (”Vector jump” block, [*RelUlim* class]).
- One 3phase under voltage element (”Minimum voltage” block, [*RelUlim* class])).
- One timer (”Input block delayed reset” block, [*RelTimer* class]).
- One logic block (”Operation mode” block, [*RelLogdip* class]).

Output logic

- One relay trip element (”Output logic” block, [*RelLogdip* class]).

1.5 Outputs

- *yout* associated by default to the *Vector jump* trip.

The output logic can be configured in the ”Logic” tab page of the ”Output Logic” block.