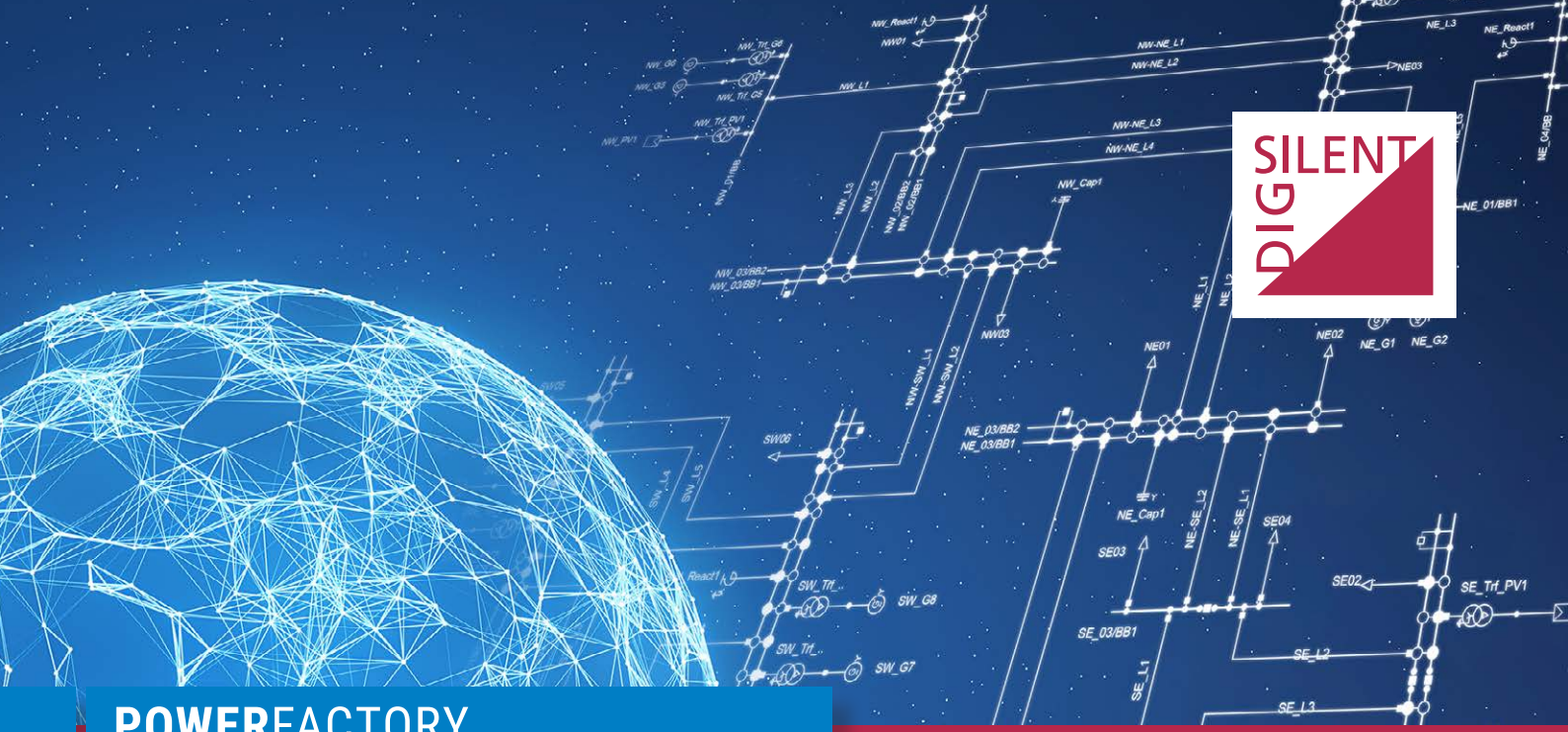

POWERFACTORY

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Technical Reference

DIgSILENT Motor protection Generic Relay

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POWER SYSTEM SOLUTIONS

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Contents

1 Motor protection

1.1 Intent

To model the most common protective functions used to protect (small/medium size) asynchronous motors which can be simulated with a short circuit calculation. To protect large motor it can be integrated with a differential generic relay model. Protective functions which needs a simulation to be reproduced (like the *Time between 2 start-ups*) are modeled in the ”Motor protection Sim” model [see **??**].

1.2 Functionality

The *Motor_protection* relay model simulates the following protective features:

- Thermal image protection with negative sequence current contribution(F49).
- Inverse/definite time phase overcurrent protection (F50/51).
- Inverse/definite time neutral/ground overcurrent protection (F50N/51N).
- Phase undercurrent protection(F37).
- Inverse/definite time current unbalance protection (F46).
- Loss of phase protection (F46).
- Phase-ground overvoltage protection(F59).
- Phase-ground undervoltage protection(F27).
- Definite time unbalance overvoltage (F47).
- Zero sequence overvoltage protection(F64/F59N).
- Definite time over/under frequency protection (F81).

The following inverse time trip and reset characteristics can be used in the phase (”I>”), ground (”I0>”), and negative sequence (”I2>”) inverse time elements:

Trip characteristic	**Reset characteristic**
IEC Class A (Standard Inverse)	IEC Class A(Standard Inverse) reset
IEC Class B (Very Inverse)	IEC Class B(Very Inverse)reset
IEC Class C (Extremely Inverse)	IEC Class C(Extremely Inverse)reset
IEC Long Time Inverse	IEC Long Time Inverse reset
IEC Short Time Inverse	IEC Short Time Inverse reset
IEEE Moderately Inverse	IEEE Moderately Inverse reset
IEEE Inverse	IEEE Inverse reset
IEEE Very Inverse	IEEE Very Inverse reset
IEEE Extremely Inverse	IEEE Extremely Inverse reset
IEEE Short Time Inverse	IEEE Short Time Inverse reset
RD (Logarithmic) inverse	
RI inverse	

Trip characteristic	Reset characteristic
I2t	I2t reset
IAC Extremely Inverse	
IAC Inverse	
IAC Short Inverse	
IAC Very Inverse	
CO2 Short time inverse	
CO8 Long time inverse	

The reset characteristic can be enable or disabled by the user. The reset time delay can be set with a separated relay model parameter.
Each characteristic can be set with an user configurable minimum and a maximum trip time.

Four relay input signals can be used to block the protective elements. The overcurrent protective element can be set to ignore the blocking input or to ignore the blocking input after that a user's definable time has expired after the element trip ("Blocking" tab page).
Two additional relay input signals can be used to energize the motor:

- *wBreakerClose* is processed by the user's configurable "Output Logic" block logic and then sued to trigger the motor energization.
- *wForceBreakerClose* forces the motor energization without any other interposed logic.

The thermal image element considerate the effect of the negative sequence current contribution using a *K* factor which is multiplied to the negative sequence current; the obtained value is then added to the phase current before the motor thermal status evaluation. The *K* factor can be set in the "Logic" tab page of the "Thermal K" block.

The loss of phase element uses in the "Loss of phase detector" block a 2% I_n current threshold to detect the open phase condition. The "Loss of phase Logic" block, when at least one phase current is smaller than 2% I_n , sends a trip command to the "Loss of phase" block which acts as time delay.

1.3 Inputs

- One 3 phase CT ("Phase Ct" block, [*StaCt* class]).
- One single phase CT ("Core Ct" block, [*StaCt* class]).
- One 3 phase VT ("Phase Vt" block, [*StaVt* class]).
- Four blocking signals (*iblock_1* blocking the "Ith", "I>", "I>>", and the "I>>>" element, *iblock_2* blocking the "I<" element, *iblock_3* blocking the "U>", "U<","U0>",and the "U2>" element and *block_4* blocking the "f1><", and the "f1><" element).
- Two motor start input signals

1.4 Available Units

Measurement

- One 3phase measurement element (”Measurement” block, *RMS Calculation* enabled, *Filter* disabled [RelMeasure class]).
- One 3phase sequence measurement element (”Measurement seq” block, *RMS Calculation* enabled, *Filter* disabled [RelMeasure class]).
- One frequency measurement element (”Measurement Freq” block, [RelFmeas class]].

Protective elements

- One thermal image element with negative sequence current contribution (”Ith>” block [*RelToc* class] and ”Thermal K” block [*RelLogdip* class]).
- One inverse time phase overcurrent element (”I>” block, [*RelToc* class]).
- Two definite time phase overcurrent elements (”I>>” and ”I>>>” block [*RelIoc* class]).
- One definite time phase undercurrent element (”I<” block [*RelIoc* class]).
- One inverse time ground overcurrent element (”I0>” block, [*RelToc* class]).
- One definite time ground overcurrent element (”I0>>” block [*RelIoc* class]).
- One inverse time negative sequence overcurrent element (”I2>” block [*RelToc* class]).
- One definite time negative sequence overcurrent element (”I2>>” block [*RelIoc* class]).
- One loss of phase element (”Loss of phase”block [*RelTimer* class], ”Loss of phase detector” block[*RelIoc* class] and ”Loss of phase Logic” block *RelLogdip* class).
- One definite time phase-ground overvoltage element (”U>” block [*RelUlim* class]).
- One definite time phase-ground undervoltage element (”U<” block [*RelUlim* class]).
- One definite time neutral overvoltage element (”U0>” block, *RelUlim* class).
- One definite time negative sequence overvoltage element (”U2>” block, *RelUlim* class).
- Two definite time over/underfrequency elements (”f1><”, and ”f2><” block, *RelFrq* class).

Output logic

- One relay trip element (”Output logic” block, *RelLogdip* class).
- One relay close element (”Closing logic” block, *RelLogic* class).

1.5 Outputs

- *yout* associated by default to any element trip.
- *yClose* associated to the ”Closing logic” block trip.

The output logic can be configured in the ”Logic” tab page of the ”Output Logic” block.