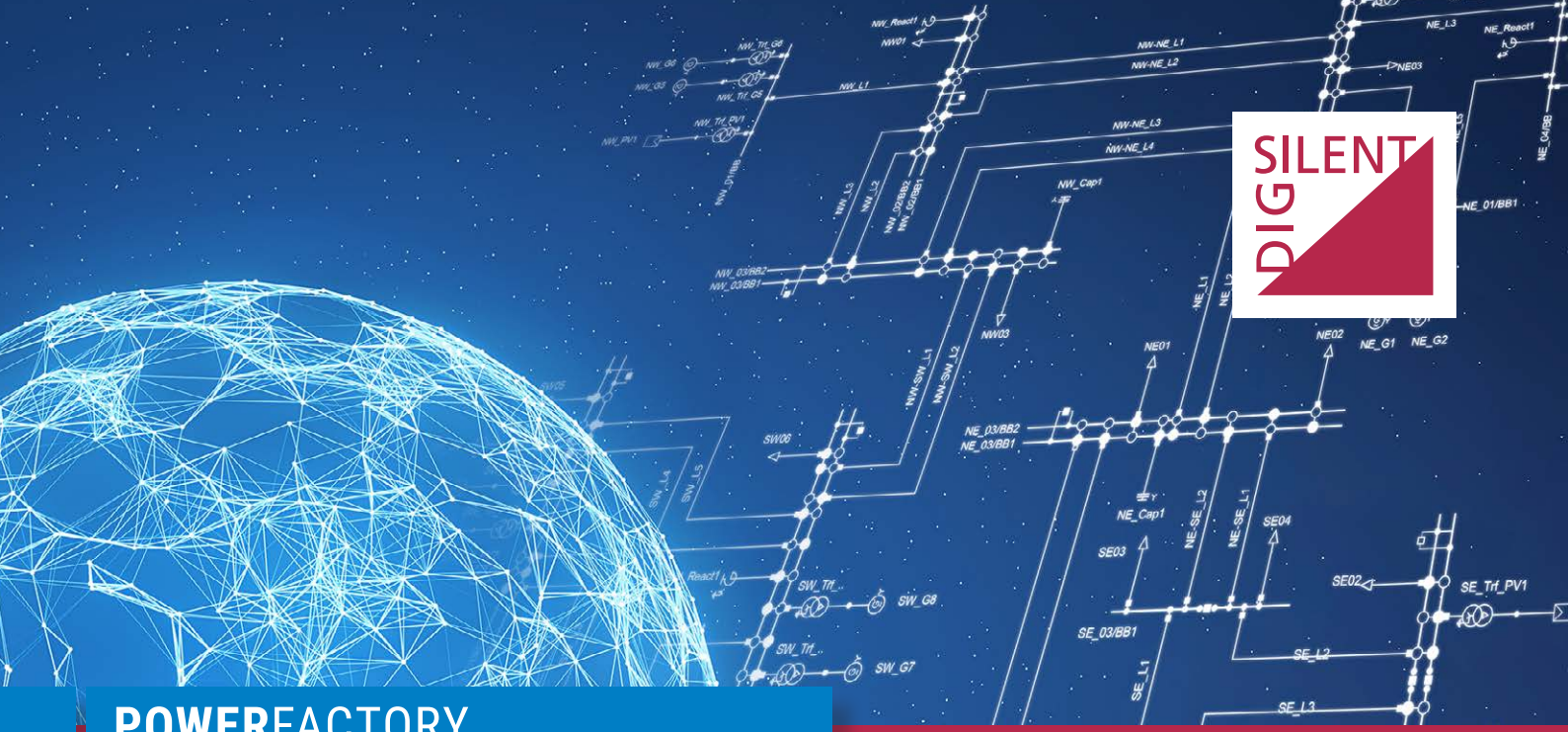

POWERFACTORY

PowerFactory 2021

Technical Reference

Register

ElmReg

PF2021

POWER SYSTEM SOLUTIONS

MADE IN GERMANY

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Contents

1 General Description

The *Register* model in *PowerFactory* is a digital shifting register. With every rising edge of the clock signal the values are shifted by one, then the output is set and the input is read and stored in the register. Therefore there is a delay of at least one clock pulse at the output. The output of the register depends on the setting *Type of Model* (*iopt_mod*). The possible settings are listed in the following:

Register The input value is written to the output with a delay of n pulses.

Moving Average Filter The output value is the average of the last n values read.

Maximum The output is the maximum of the values in the register.

Minimum The output is the minimum of the values in the register.

where n equals the size of the register.

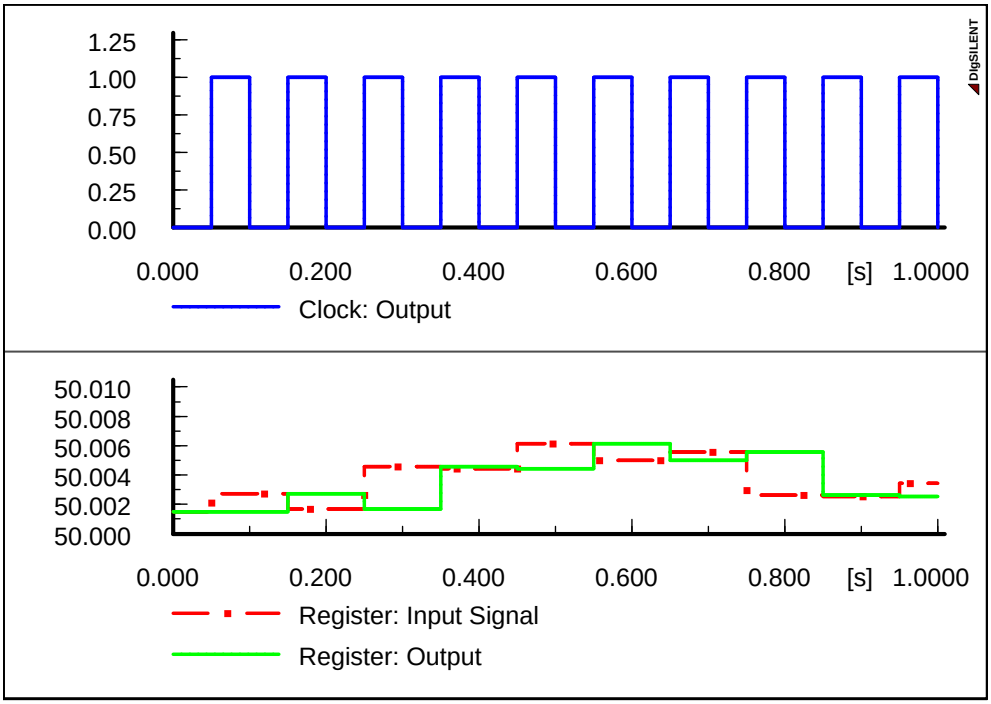

Figure 1.1: Plot register size 1

Note: For a register size of one the output is the input delayed by one pulse. This applies for all types of models.

Like for digital hardware the input of digital models must be digitized first. Therefore the register is working fine for signals already digitized. An analog value should not be input to the register directly. There is no error message if the input signal of a register was not digitized before but the register might not work properly. The *Sample and Hold* (S & H) model is to be used for sampling the analog signal first. The input of the S & H block is the analog signal, the output is connected to the input of the register. It is recommended to use the same clock source for the S & H and the register. Apart from the parameter *Number of Phases (nphase)* there is no input parameter to be specified in the S & H.

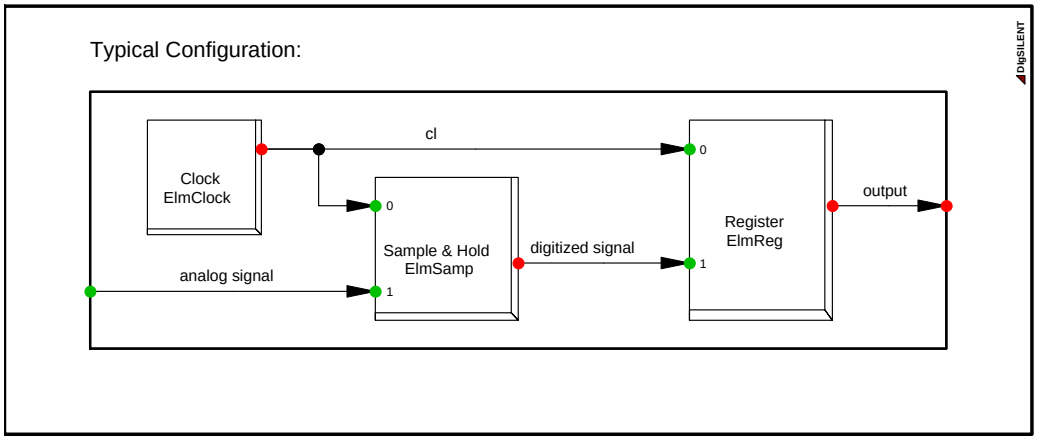

Figure 1.2: Typical block diagram

2 Dynamic Simulation

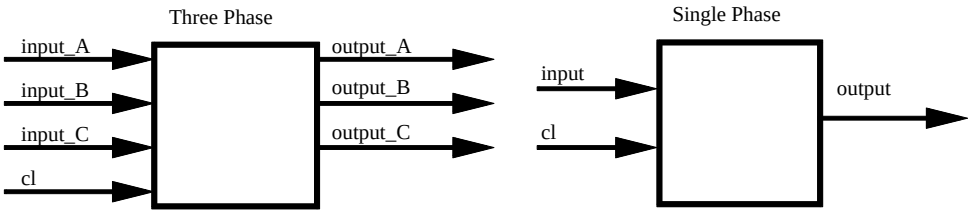

Figure 2.1: Input/Output Definitions

The input signals *input* and *cl* must always be connected for using the model in the simulation.

input_A, input_B and *input_C* need not to be connected. Input values not connected are set to 0.

3 Example Configuration

There are four registers in the example configuration. Each of the registers is set to a different model type. The clock and input signal are identical for every register. All plots, one for every register, display the input and output of the register model.

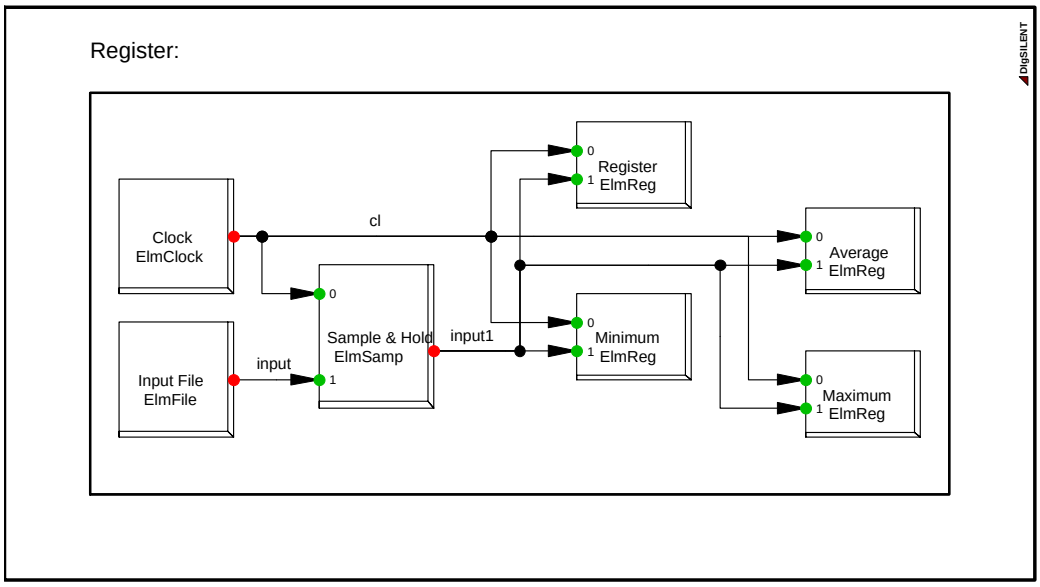

Figure 3.1: Block Diagram

Table 3.1: Example Settings

Element	Class name	Variable	Value
Initial Conditions	*ComInc*	*iopt_sim* *iopt_net* *dtgrd* and *dtout* *tstart*	RMS values (Electromechanical Transients) Balanced, Positive Sequence 0.01 s 0 s
Clock	*ElmClock*	*cFreq* *Tp* *tonTp*	0.01 kHz 0.1 s 0.5
Register	*ElmFft*	*iopt_mod* *nphase* *nsamp*	Register 1 8
Average	*ElmFft*	*iopt_mod* *nphase* *nsamp*	Moving Average Filter 1 8
Minimum	*ElmFft*	*iopt_mod* *nphase* *nsamp*	Minimum 1 8
Maximum	*ElmFft*	*iopt_mod* *nphase* *nsamp*	Maximum 1 8

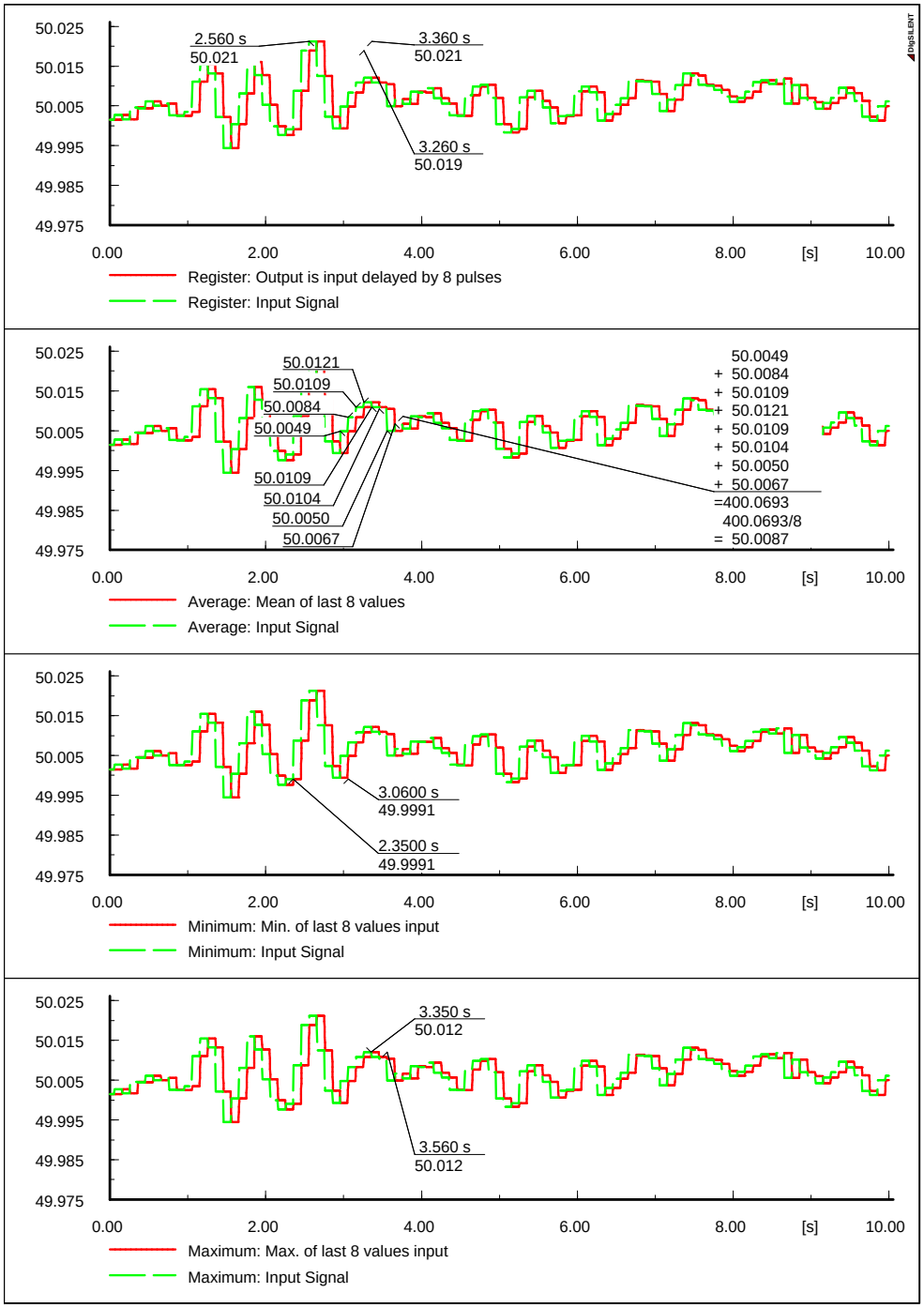

Figure 3.2: Plots of different register models

A Parameter Definitions

Table A.1: Trigger Parameters

Parameter	Description	Unit
loc_name	Name	
outserv	Out of service	
iopt_mod	Type of model	
nphase	Number of phases	
nsamp	Buffer size	

B Signal Definitions

Table B.1: Input/Output signals

Name	Description	Unit	Type	Model
input	Input signal		IN	RMS, EMT
cl	Clock signal		IN	RMS, EMT
output	Output		OUT	RMS, EMT

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