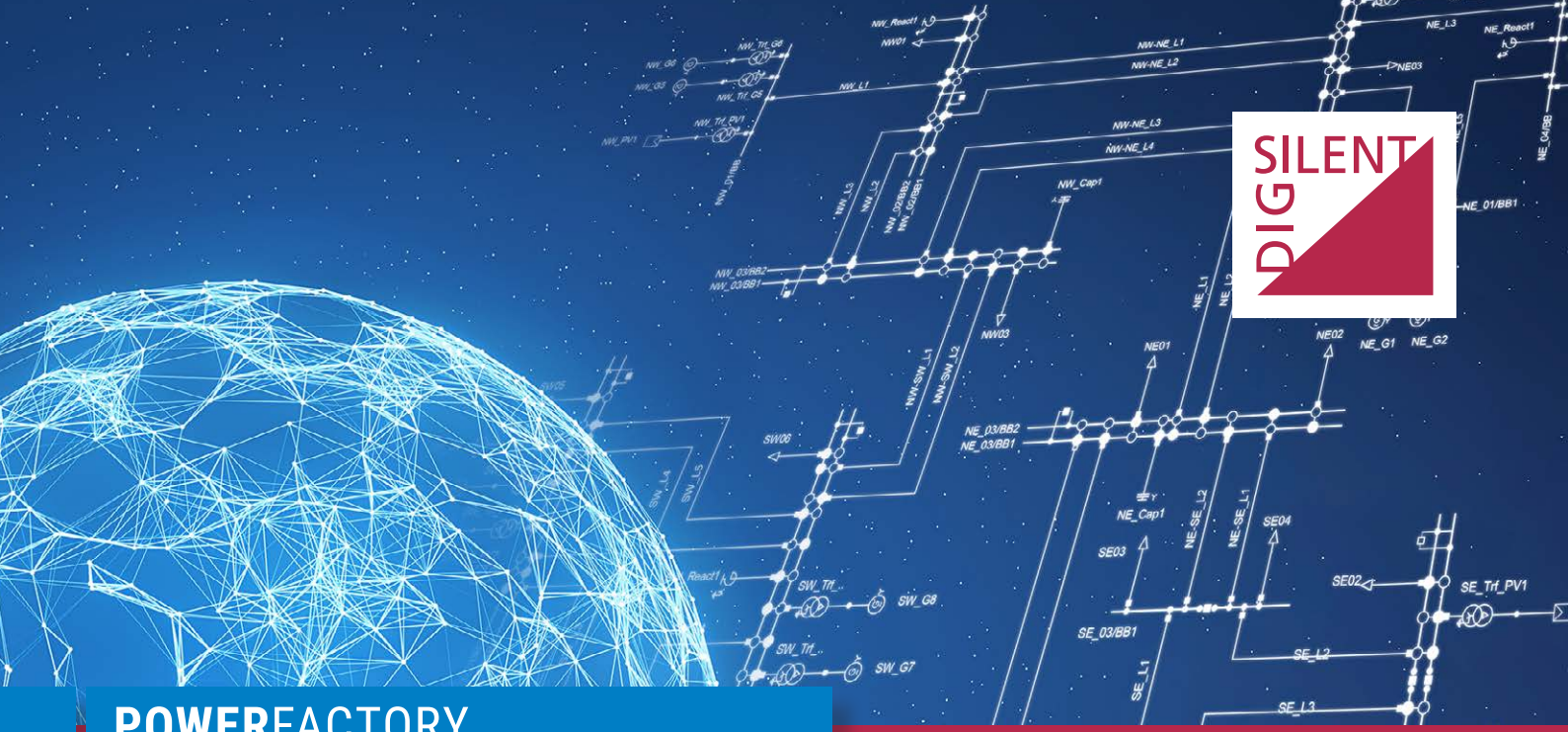

PowerFactory 2021

Technical Reference

DIgSILENT F27D Positive sequence under voltage Ger

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POWER SYSTEM SOLUTIONS

MADE IN GERMANY

Publisher:
DIgSILENT GmbH
Heinrich-Hertz-Straße 9
72810 Gomaringen / Germany
Tel.: +49 (0) 7072-9168-0
Fax: +49 (0) 7072-9168-88
info@digsilent.de

Please visit our homepage at:
https://www.digsilent.de

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1 F27D Positive sequence under voltage

1.1 Intent

To simulate a set of positive sequence under voltage protective elements.

1.2 Functionality

The *F27D Positive sequence under voltage* relay model simulates a set of positive sequence under voltage elements. One inverse/definite time and 3 definite time elements are available.

1.3 Inputs

- One 3 phase VT (”Phase Vt” block, *StaVt* class).

The following blocking signals are available:

- *iblock_1* blocking ”U1<”.
- *iblock_2* blocking ”U1<< ”.
- *iblock_3* blocking ”U1<<<”.
- *iblock_4* blocking ”U1<<<<”.

1.4 Available Units

Measurement

- One 3phase sequence measurement element (”Measurement seq” block, *RMS Calculation* enabled, *Filter* disabled [RelMeasure class]).

Protective elements

- One inverse/definite time positive sequence undervoltage element (”U1<” block, *RelChar* class).
- Three definite time positive sequence undervoltage elements (”U1<< ”, ”U1<<<” and ”U1<<<<” block, *RelUlim* class).

Output logic

- One relay trip element (”Output logic” block, *RelLogdip* class).

1.5 Outputs

- *yout* associated by default to any protective element trip.
- *inv_trip* associated by default to the inverse/definite time positive sequence undervoltage element trip (”U1<” block).
- *def_trip* associated by default to the definite time positive sequence undervoltage element trip(”U1<< ”, ”U1<<<” and ”U1<<<<” block).

The output logic can be configured in the ”Logic” tab page of the ”Output Logic” block.