POWERFACTORY

PowerFactory 2021

Technical Reference

Timer

RelTimer, TypTimer

PF2021

POWER SYSTEM SOLUTIONS
MADE IN GERMANY

Publisher:
DIgSILENT GmbH
Heinrich-Hertz-Straße 9
72810 Gomaringen / Germany
Tel.: +49 (0) 7072-9168-0
Fax: +49 (0) 7072-9168-88
info@digsilent.de

Please visit our homepage at:
https://www.digsilent.de

December 1, 2020
PowerFactory 2021
Revision 1

Contents

1 General Description 1

2 Features & User interface 1

2.1 Timer (RelTimer) 1

2.1.1 Basic data 1

2.1.2 Description 1

2.2 Timer Type(TypTimer) 2

3 Integration in the relay scheme 4

4 Logic 5

4.1 Simple timer 5

4.1.1 Single phase 5

4.1.2 Three phase 5

4.2 Timer with OR Logic 6

4.2.1 Single phase 6

4.2.2 Three phase 6

4.3 Timer with AND Logic 7

4.3.1 Single phase 7

4.3.2 Three phase 7

4.4 Timer with AND and OR logic 8

4.4.1 Single phase 8

4.4.2 Three phase 8

4.5 Timer as a Flip-Flop 9

4.5.1 Single phase 9

4.5.2 Three phase 9

A Parameter Definitions 10

A.1 Timer Type (TypTimer) 10

A.2 Timer Element (RelTimer) 10

B Signal Definitions 10

B.1 Single phase 10
B.2 Three phase 10

List of Figures **12**

List of Tables **13**

1 General Description

The *Timer* “RelTimer” block implements one of the following logic:

- A timer applied to a single input signal.
- A timer applied to the output of an OR logic or of an AND logic combining two input signals.
- A *flip-flop*.

The *Timer* “RelTimer” block is operational during short circuit, load flow and RMS/EMT simulations.

2 Features & User interface

2.1 Timer (RelTimer)

The user can change the block settings using the “Timer” dialogue (“RelTimer” class). The dialogue consists of two tab pages: *Basic Data*, and *Description*. The main settings are located in the *Basic Data* tab page.

2.1.1 Basic data

The “Basic Data” dialogue contains the following controls:

- An editbox which allows to insert a name to identify the *Timer*.
- A pointer to a “Timer type” object which defines the timer type and the time delay range.
- A check box to disable the timer.
- An graphical control which allows to define the timer time delay.

The block can be disabled using the “Out of service” check box. The time delay can be set using the “Time Setting” control (“Tdelay” parameter). The “Time Setting” control is a combo box if a range of discrete values has been defined in the “Timer Type” dialogue or otherwise an edit box.

2.1.2 Description

The *Description* tab page can be used to insert some information to identify the Timer protective element (both with a generic string and with an unique textual string similar to the *Foreign Key* approach used in the relational databases) and to identify the source of the data used to create it.

2.2 Timer Type(TypTimer)

The *Timer* block main characteristics must be configured in the “Timer Type” dialogue (*TypTimer* class). The dialogue consists of an unique page.

The block can be configured as a 3phase or a single phase timer using the “Phases” combo box (“nphase” parameter). The underlying types are:

- CalTimer (3 phase timer logic)
- CalTimer1p (a single phase timer logic)

The time delay range and unit can be set using the “Time Setting Range” (“rTdelay” parameter) and the unit combo box (“iunit” parameter).
The timer logic can set using the “Type” combo box (“iresetdel” parameter) as:

- *Set delay*
- *Output Hold Time*
- *Reset delay*

When the *Set delay* logic has been selected, the block creates a delay between the input setting time and the output signal setting time.

The typical behaviour of *Timer* block set as *Set Delay* is showed in Figure 2.1.

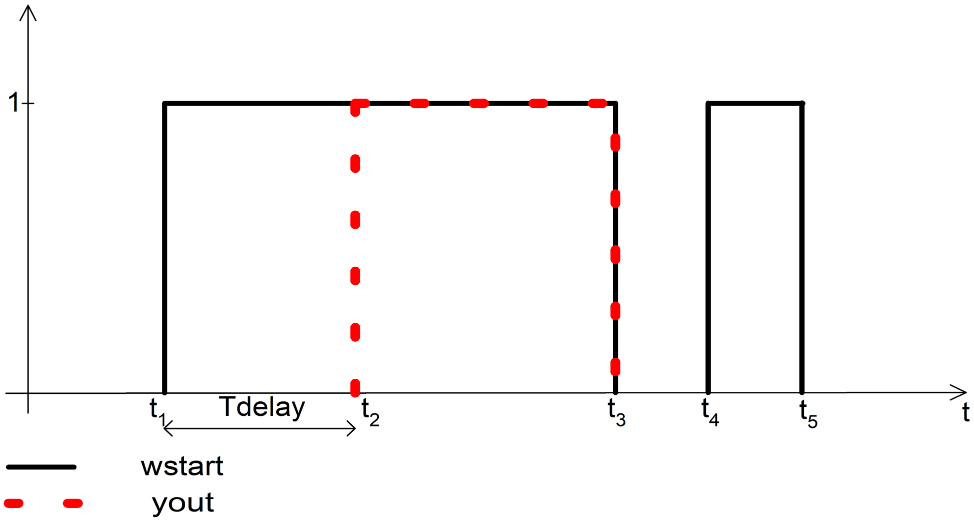

Figure 2.1: Behaviour of a *Timer* (“RelTimer” class) set as *Set Delay*

In the example the input starting signal is set at t_1; the block output signal is set at $t_2 = t_1 + tdelay$ and reset at t_3, without any delay when the input starting signal goes to zero. The $t_5 - t_4$ time difference is smaller than $tdelay$ and the block output signal status doesn’t have the time to be set.

The *Min Holding time* logic creates a delay between the input setting time and the output signal resetting time. No delay is created between the input setting time and the output signal setting time.

The typical behaviour of *Timer* block set as *Min Holding time* is showed in Figure 2.2.

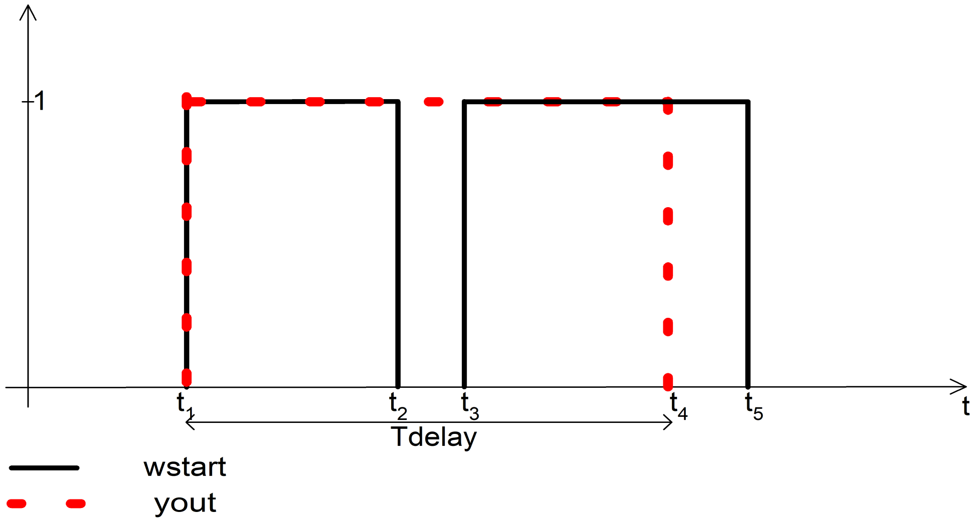

Figure 2.2: Behaviour of a *Timer* (“RelTimer” class) set as *Min Holding time*

In the example the input starting signal is set at t_1; the block output signal is also set at t_1, without any delay with the input starting signal, and is reset at $t_4 = t_1 + tdelay$. The input starting signal resets between t_2 and t_3 but it doesn’t affect the delay applied to the output signal reset. The block output signal reset even if the input starting signal is on.

The *Reset delay* logic creates a delay between the input resetting time and the output signal resetting time.
The typical behaviour of *Timer*“RelTimer ” block set as *Reset Delay* is showed in Figure 2.3.

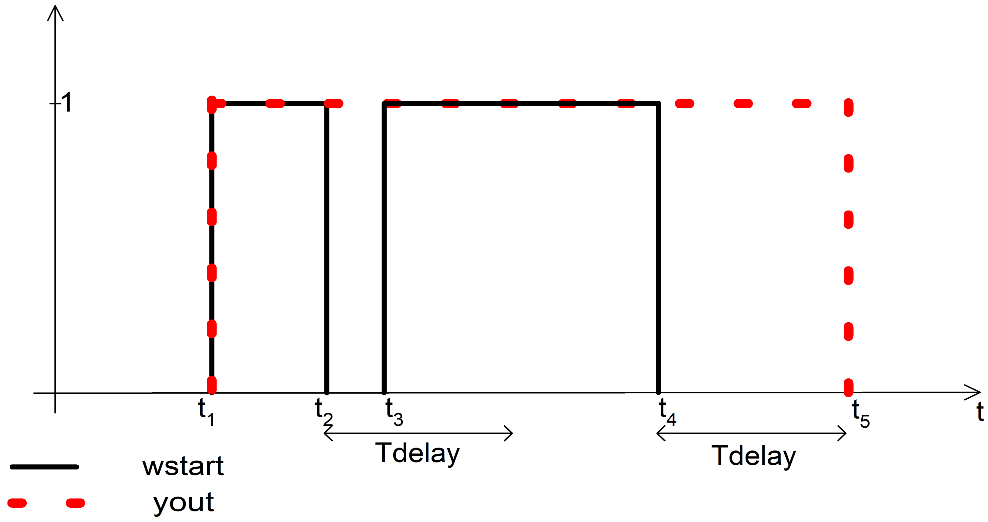

Figure 2.3: Behaviour of a *Timer* (“RelTimer” class) set as *Reset Delay*

In the example the input starting signal is set at t_1, is reset at t_2, is set at t_3 and is reset at t_4; the block output signal is also set at t_1, without any delay with the input starting signal, and is reset with a $Tdelay$ time after the last reset at $t_5 = t_4 + Tdelay$. The $t_3 - t_2$ time difference is smaller than $Tdelay$ and the block output signal doesn’t have the time to be reset.

3 Integration in the relay scheme

The *Timer*“RelTimer” type class name is *TypTimer*. The *Timer* dialogue class name is *RelTimer* . As already shown, there are two main versions of the block: a single phase and a three phase version. The number and the name of the input signals depends only upon which of these versions is used. The typical connection of a *Timer* block is in a distance protection scheme: a timer is located between each distance trip zone and the output block. The typical connection of a single phase *Timer*“RelTimer ” block is showed in Figure 3.1.

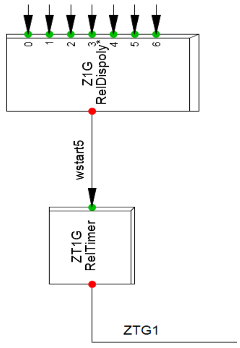

Figure 3.1: *DIgSILENT* Typical connection scheme of a single phase *Timer*“RelTimer” block.

If the relay model implements a single phase trip scheme a 3 phases timer block will be used. The connections associated with a three phase *Timer*“RelTimer” block are quite similar. The main difference is that an input signal for each phase is included.

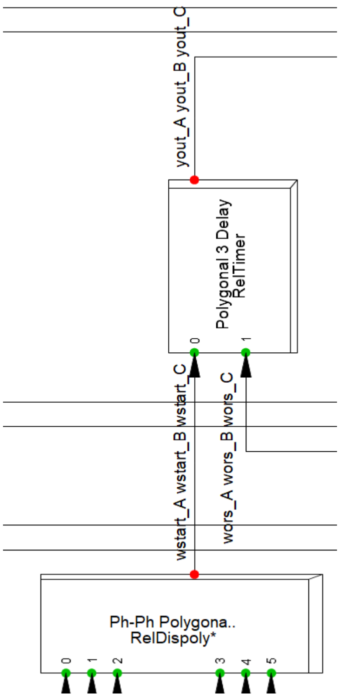

Figure 3.2: *DIgSILENT* Typical connection scheme of a three phase directional *Timer*“RelTimer” block with *OR* logic.

4 Logic

4.1 Simple timer

To implement a simple timer the block starting signal ("wstart") must be used as input signal. The block output "yout" is equal to input signal plus the timer block time delay ("Tdelay" variable). This logic can represented by the following simple relation: $yout = wstart + Tdelay$

4.1.1 Single phase

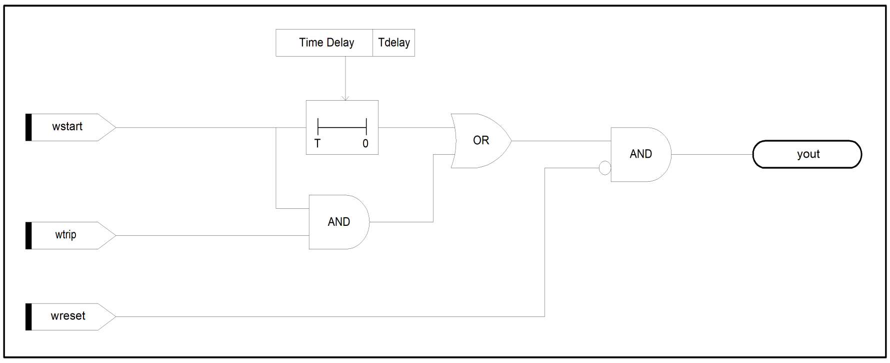

Figure 4.1: The *Single Phase Timer logic (CalTimer1p)*

4.1.2 Three phase

The three phase logic is identical to the single phase logic and is simply duplicated for each phase.

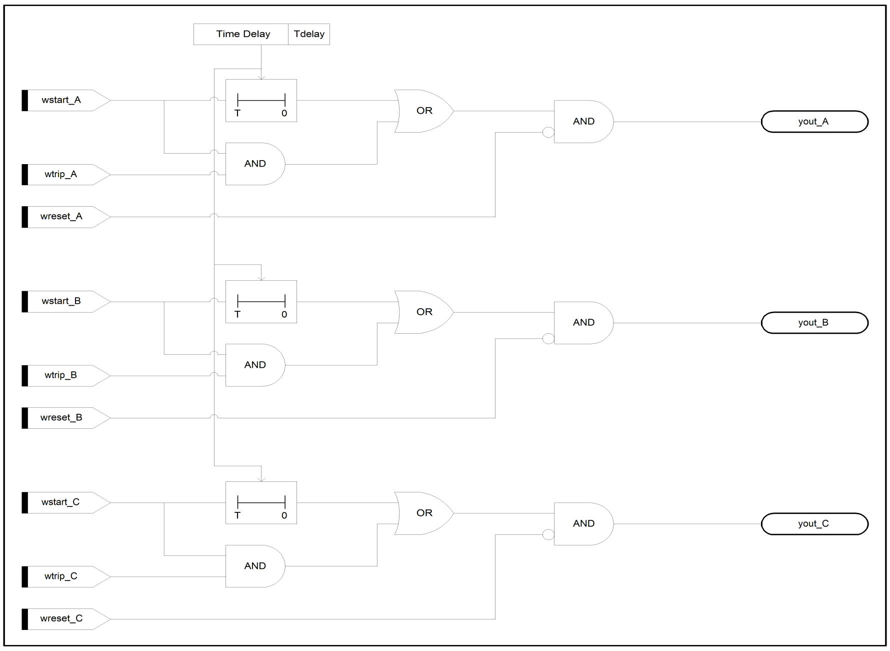

Figure 4.2: The *Three Phase Timer logic (CalTimer)*

4.2 Timer with OR Logic

In a timer with the OR Logic the output signal “yout” is equal to the smaller value between the *starting* signal (“wstart”) and the *OR starting* (“wors”) signal plus the timer block time delay (“Tdelay” variable). This logic can represented by the following function:
$yout = (wstart \quad OR \quad wors) + Tdelay$

4.2.1 Single phase

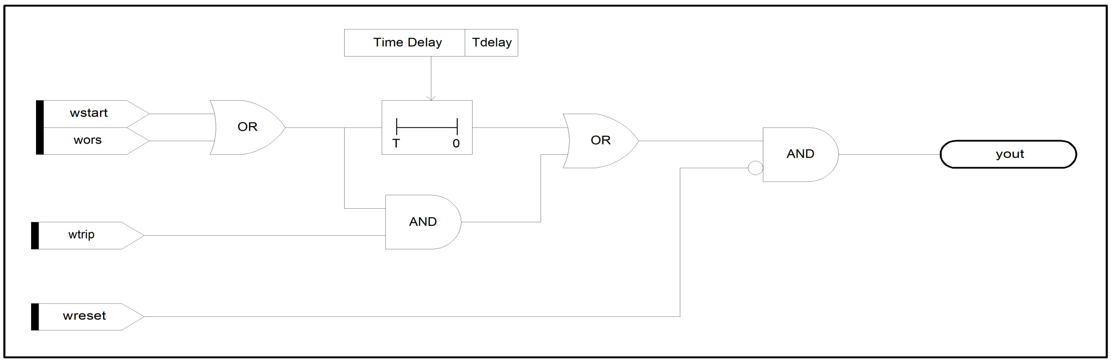

Figure 4.3: The *Single Phase Timer OR logic (CalTimer1p)*

4.2.2 Three phase

The three phase logic is identical to the single phase logic and is simply duplicated for each phase.

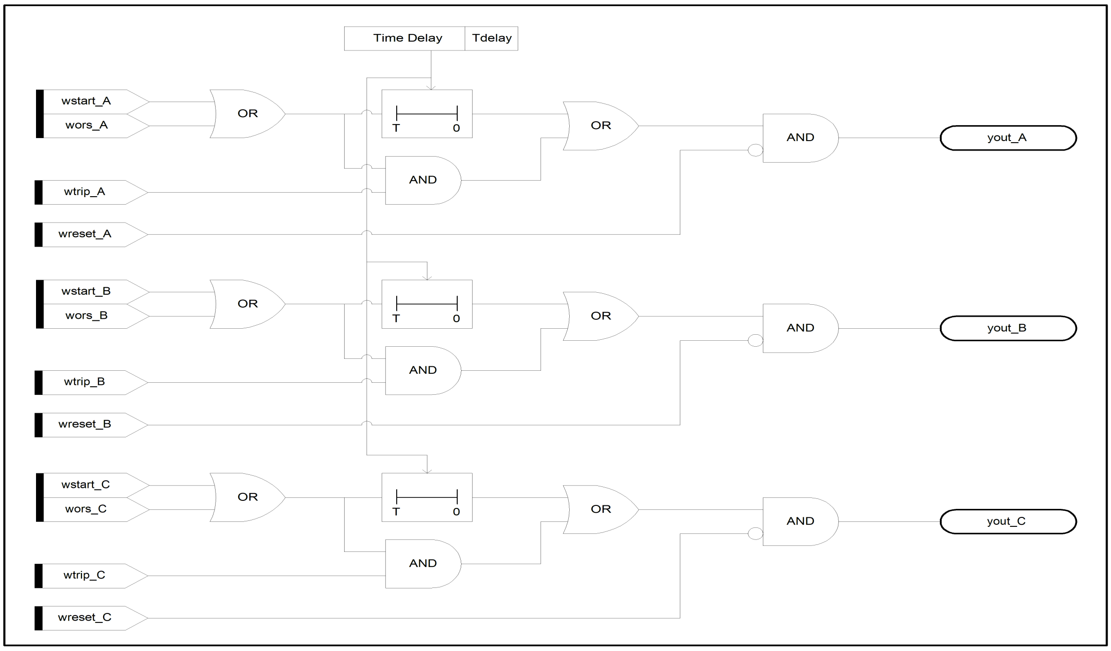

Figure 4.4: The *Three phase Timer OR logic (CalTimer)*

4.3 Timer with AND Logic

In a timer with the AND Logic the output signal “yout” is equal to the greater value between the *starting* signal (“wstart”) and the *AND starting* (“wands”) signal plus the timer block time delay (“Tdelay” variable). This logic can represented by the following function:
$yout = (wstart \quad AND \quad wands) + Tdelay$

4.3.1 Single phase

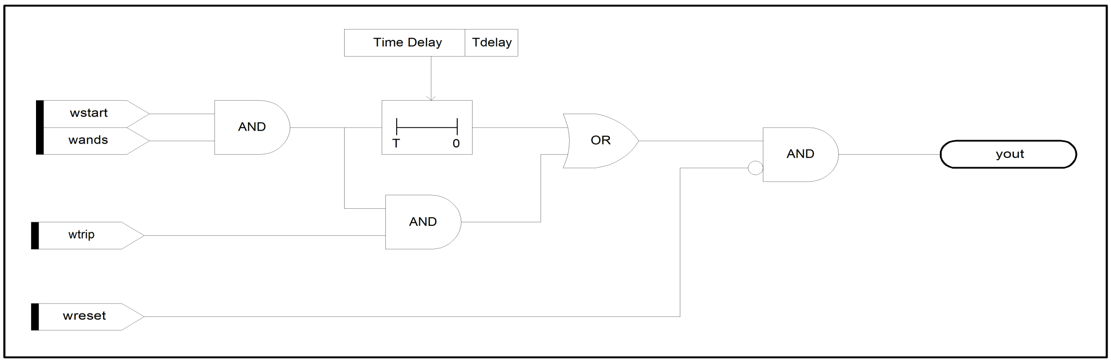

Figure 4.5: The *Single Phase Timer AND logic (CalTimer1p)*

4.3.2 Three phase

The three phase logic is identical to the single phase logic and is simply duplicated for each phase.

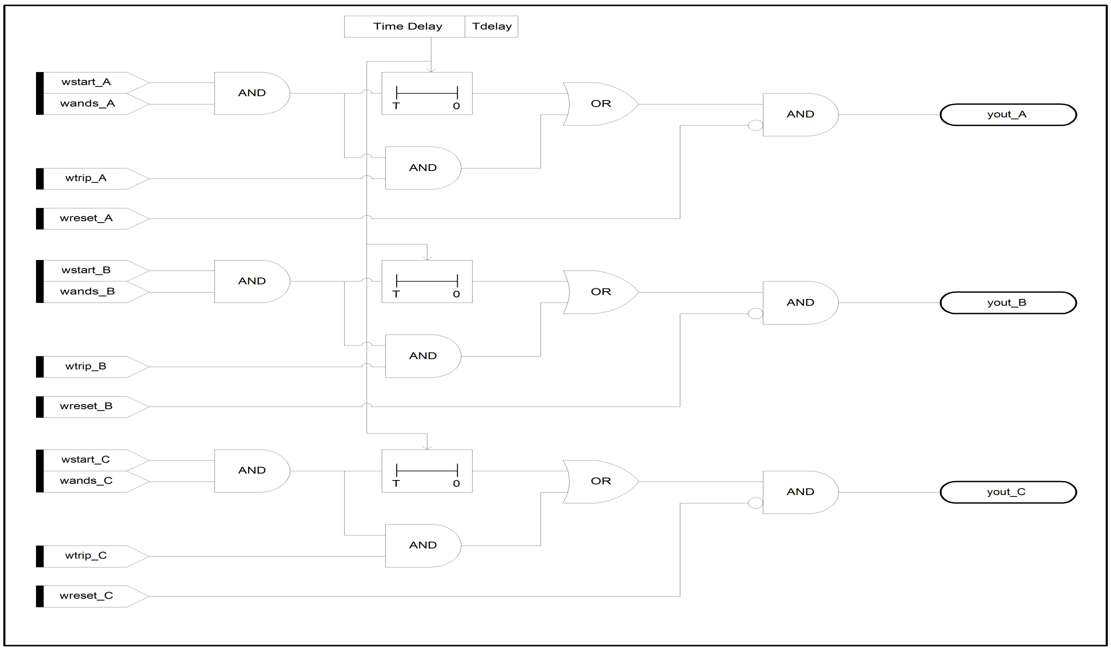

Figure 4.6: The *Three phase Timer AND logic (CalTimer)*

4.4 Timer with AND and OR logic

In a timer with both the AND and the OR Logic active, the output signal “yout” is equal to the timer block time delay (“Tdelay” variable) plus the greater value between the *AND starting* signal (“wands”) and the smaller value between the *Starting* signal (“wstart”) and the *OR Starting* signal (“wors”). This logic can represented by the following function:
$yout = ((wstart \quad OR \quad wors) \quad AND \quad wands) + Tdelay$

4.4.1 Single phase

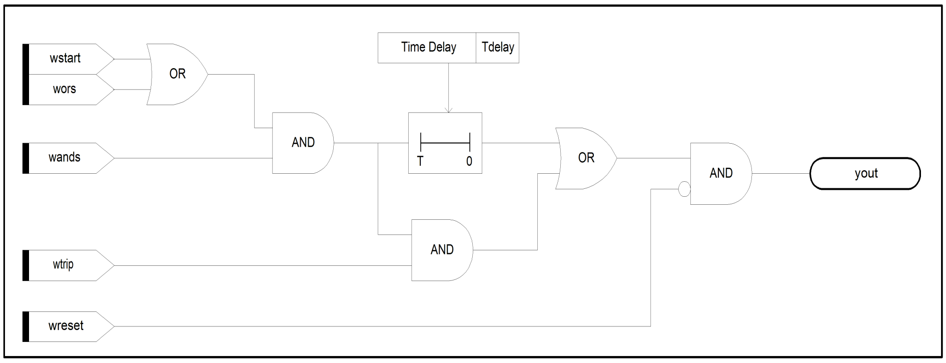

Figure 4.7: The *Single Phase Timer AND & OR logic (CalTimer1p)*

4.4.2 Three phase

The three phase logic is identical to the single phase logic and is simply duplicated for each phase.

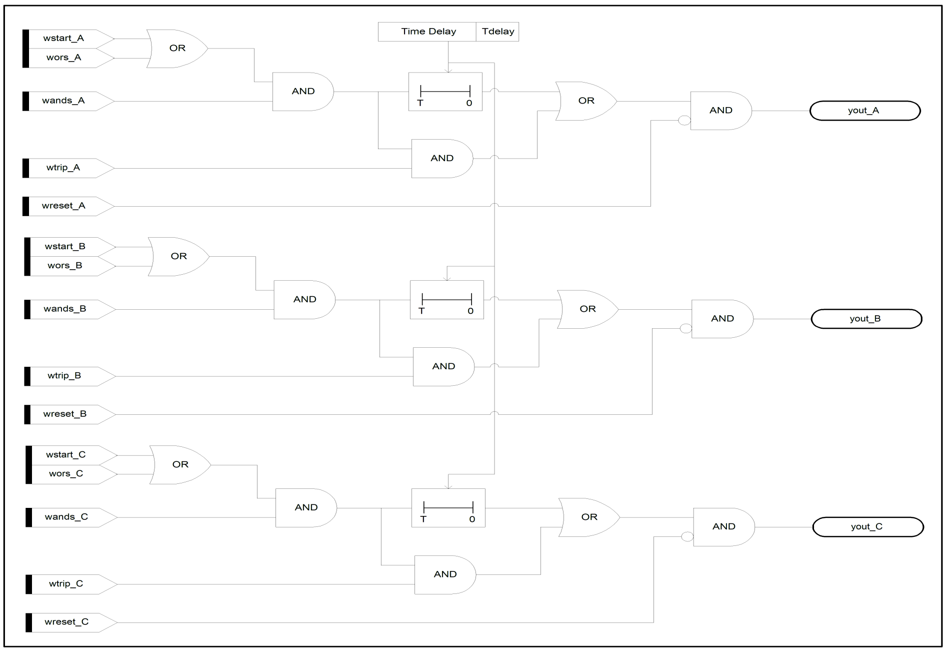

Figure 4.8: The *Three phase Timer AND & OR logic (CalTimer)*

4.5 Timer as a Flip-Flop

To implement a *flip-flop* the “set” input signal must be used. The “yout” output signal is set equal to the “set” input signal after that the *timer* block time delay (“Tdelay” variable) expires; during the simulation the block holds the value until a “wreset” *reset* signal is sent. The “yout” *output* signal is set equal to the “set” input signal without the *timer* block time delay when the “wtrip” *trip* signal is connected.

4.5.1 Single phase

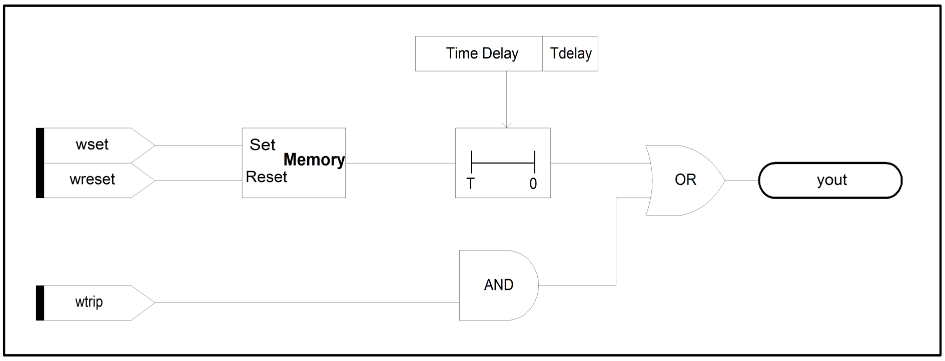

Figure 4.9: The *Single Phase Timer Flip-Flop logic (CalTimer1p)*

4.5.2 Three phase

The three phase logic is identical to the single phase logic and is simply duplicated for each phase.

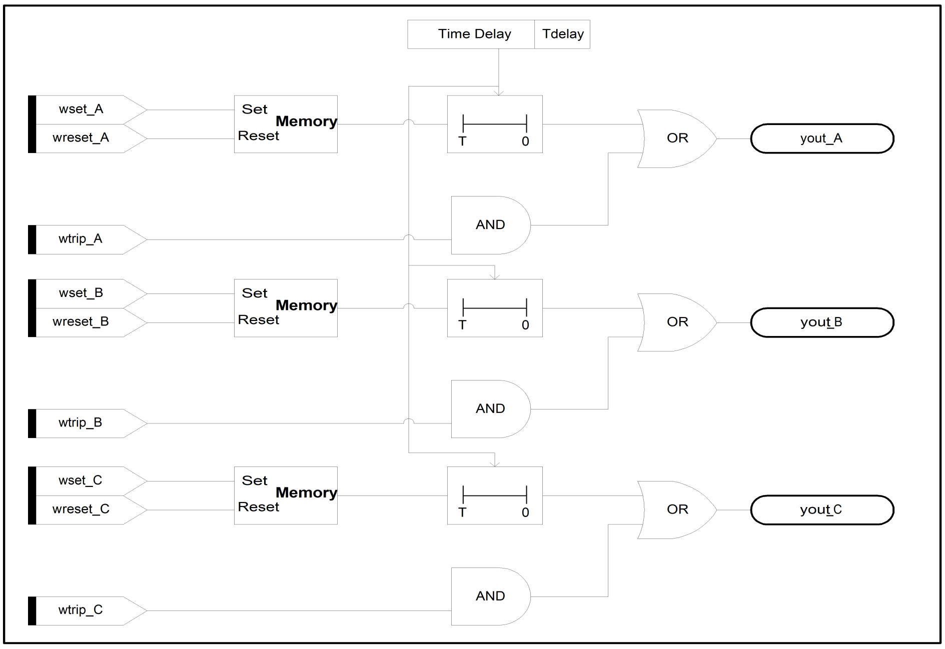

Figure 4.10: The *Three phase Flip Flop (CalTimer)*

A Parameter Definitions

A.1 Timer Type (TypTimer)

Table A.1: Input parameters of the Timer type (*TypTimer*)

Parameter	Description	Unit
loc_name	Name assigned by the user to the block type	Text
nphase	The number of timer (1 or 3)	Integer
rTdelay	Range of the time delay	Text
iunit	Unit of the time delay (Seconds or cycles)	Integer
iresetdel	Setting to configure the timer type. ("Set delay" or "Minimum holding time" or "Reset delay")	Integer

A.2 Timer Element (RelTimer)

Table A.2: Input parameters of the Timer element (*RelTimer*))

Parameter	Description	Unit
loc_name	Name assigned by the user to the block element	Text
typ_id	Pointer to the relevant TypTimer object	Pointer
outserv	Flag to put out of service the block	Y/N
Tdelay	Timer time delay in seconds	Real number
Tcdelay	Timer time delay in cycles	Real number

B Signal Definitions

B.1 Single phase

Table B.1: Input/output signals of the single phase Timer element (*CalTimer1p*)

Name	Description	Unit	Type	Model
wstart	Start signal	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wtrip	Trip input signal	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wset	Flip-flop mode set signal	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wors	2nd start signal used by the *OR mode*	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wands	2nd start signal used by the *AND mode*	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wreset	Resetting signal (used by any operation mode)	Sec(or 1/0 RMS/EMT simulation)	IN	Any
yout	Trip signal	Sec(or 1/0 RMS/EMT simulation)	OUT	Any

B.2 Three phase

Table B.2: Input/output signals of 3 phase Timer element (*CalTimer*)

Name	Description	Unit	Type	Model
wstart_A	Phase A start signal	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wstart_B	Phase B start signal	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wstart_C	Phase C start signal	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wtrip_A	Phase A trip input signal	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wtrip_B	Phase B trip input signal	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wtrip_C	Phase C trip input signal	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wset_A	Phase A *Flip-flop* mode set signal	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wset_B	Phase B *Flip-flop* mode set signal	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wset_C	Phase C *Flip-flop* mode set signal	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wors_A	Phase A 2nd start signal used by the OR mode	Sec(or 1/0 RMS/EMT simulation)	IN	Any

Table B.2: Input/output signals of 3 phase Timer element (*CalTimer*)

Name	Description	Unit	Type	Model
wors_B	Phase B 2nd start signal used by the OR mode	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wors_C	Phase C 2nd start signal used by the OR mode	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wands_A	Phase A 2nd start signal used by the AND mode	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wands_B	Phase B 2nd start signal used by the AND mode	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wands_C	Phase C 2nd start signal used by the AND mode	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wreset_A	Phase A resetting signal (used by any operation mode)	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wreset_B	Phase B resetting signal (used by any operation mode)	Sec(or 1/0 RMS/EMT simulation)	IN	Any
wreset_C	Phase C resetting signal (used by any operation mode)	Sec(or 1/0 RMS/EMT simulation)	IN	Any
yout_A	Phase A trip signal Sec(or 1/0 RMS/EMT simulation)	Sec(or 1/0 RMS/EMT simulation	OUT	Any
yout_B	Phase B trip signal Sec(or 1/0 RMS/EMT simulation)	Sec(or 1/0 RMS/EMT simulation	OUT	Any
yout_C	Phase C trip signal Sec(or 1/0 RMS/EMT simulation)	Sec(or 1/0 RMS/EMT simulation	OUT	Any
youtall	All phases trip Sec(or 1/0 RMS/EMT simulation)	Sec(or 1/0 RMS/EMT simulation	OUT	Any
yout	At least one phase trip Sec(or 1/0 RMS/EMT simulation)	Sec(or 1/0 RMS/EMT simulation	OUT	Any

List of Figures

2.1 Behaviour of a *Timer* (“RelTimer” class) set as *Set Delay* 2

2.2 Behaviour of a *Timer* (“RelTimer” class) set as *Min Holding time* 3

2.3 Behaviour of a *Timer* (“RelTimer” class) set as *Reset Delay* 3

3.1 *DIgSILENT* Typical connection scheme of a single phase *Timer*“RelTimer” block. 4

3.2 *DIgSILENT* Typical connection scheme of a three phase directional *Timer*“RelTimer” block with *OR* logic. 4

4.1 The *Single Phase Timer logic (CalTimer1p)* 5

4.2 The *Three Phase Timer logic (CalTimer)* 5

4.3 The *Single Phase Timer OR logic (CalTimer1p)* 6

4.4 The *Three phase Timer OR logic (CalTimer)* 6

4.5 The *Single Phase Timer AND logic (CalTimer1p)* 7

4.6 The *Three phase Timer AND logic (CalTimer)* 7

4.7 The *Single Phase Timer AND & OR logic (CalTimer1p)* 8

4.8 The *Three phase Timer AND & OR logic (CalTimer)* 8

4.9 The *Single Phase Timer Flip-Flop logic (CalTimer1p)* 9

4.10 The *Three phase Flip Flop (CalTimer)* 9

List of Tables

A.1 Input parameters of the Timer type (*TypTimer*) 10

A.2 Input parameters of the Timer element (*RelTimer*)) 10

B.1 Input/output signals of the single phase Timer element (*CalTimer1p*) 10

B.2 Input/output signals of 3 phase Timer element (*CalTimer*) 10

B.2 Input/output signals of 3 phase Timer element (*CalTimer*) 11