ON THE EFFECT OF INNER CONTROL LOOPS OF GRID-FORMING CONVERTERS ON THE POWER QUALITY OF POWER SYSTEMS

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Abstract

Grid forming converter (GFC) controls can be designed with or without inner control loops. If inner control loops are used, they can be realised in various ways. The paper shows, investigates and explains the effect that such inner control loops can have on power quality aspects of power systems. The main focus is on voltage unbalances (negative sequence components) and low-order harmonics. The analysis is done in the time-domain by means of EMT simulations, and in the frequency domain via impedance characteristics. The results indicate that the design and the parametrisation of inner control loops define the beneficial effect that a GFC can have on the power quality of power systems. In this aspect, a virtual synchronous machine (VSM) implementation without inner control loops can achieve a behaviour similar to a real synchronous machine without additional effort, i.e. it can reduce existing voltage unbalance and low-order harmonics by a similar amount. As a conclusion, if inner control loops are used, they should be designed with care, and GFCs tested thoroughly with respect to the mentioned power quality aspects, in order to ensure a continuing high power quality in future power systems.

1 Introduction

The technical brochure "High Penetration of Power Electronic Interfaced Power Sources and the Potential Contribution of Grid Forming Converters" of the ENTSO-E Technical Group on High Penetration of Power Electronic Interfaced Power Sources [1] defines seven requirements to be fulfilled by Class 3 power park modules (Class 3 PPMs), which nowadays are usually referred to as PPMs with "grid-forming converters" (GFCs):

- Creating system voltage
- Contributing to fault level (within first cycle)
- Contributing to inertia
- Supporting system survival to allow effective operation of low frequency demand disconnection
- Preventing adverse control interactions
- Acting as sink to counter harmonics and inter-harmonics in system voltage
- Acting as sink to counter unbalance in system voltage

The first points of the list are usually in the focus when discussing GFCs, as they are evident for power system stability of power electronic dominated power systems. The last points are of importance to ensure a continuing high power quality in future power systems. Conventional synchronous generators (SGs) have the capability to absorb unbalances and low-order harmonics (including inter-harmonics) from system voltage. If SGs will potentially be replaced by GFCs in future power systems, GFCs should show similar or better performance in these power quality aspects. This will prevent deterioration of the power quality and avoid increasing stress on the remaining (conventional) devices that act as sinks to counter existing unbalances and harmonics (incl. inter-harmonics) in the system voltage.

Grid forming converter controls can be designed with or without inner control loops. If inner control loops are used, they can be realised in various ways. The paper investigates the effect that such inner control loops can have on the mentioned power quality aspects of power systems. Using EMT simulations (refer to Chapter 2 for details on the test system and test cases), it is analysed to which amount exemplary GFC implementations with or without inner control loops (refer to Chapter 3 for information on the implementations) reduce existing voltage unbalances and low-order harmonics (refer to Chapter 4 for results). Analysis of the negative sequence impedance and the frequency-dependent impedance characteristics of GFC units is done to explain and understand the results. Conclusions are drawn in Chapter 5.

2 Test System and Test Cases

This chapter describes the test system and test cases used for the investigation.

2.1 Test system

The tests are done using EMT simulation in PowerFactory. A simple power system representation is used, which is implemented according to the testing suggested by VDE FNN for continuously voltage-injecting HVDC systems and power

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plants connected via DC link (chapter 7 in [2]), see Fig. 1. The short-circuit ratio (SCR) at the point of connection (PoC) of each device under test (DUT) is approximately 4. The network is inductive with an R/X ration of 0.1. Any line/cable capacitances are neglected. Note, the focus of the paper is on the impact of GFC on unbalances and low-order harmonics existing in the grid voltage; it is not on any possible controller interaction or a potential risk of resonances of the inner-loop converter controls with the grid impedance.

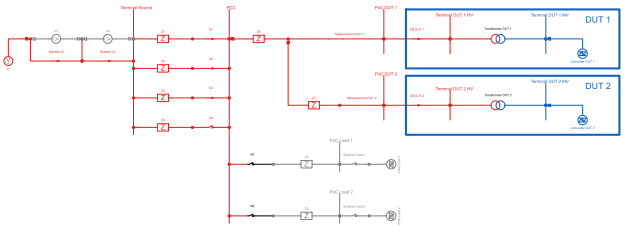

Fig. 1: Test network acc. to [2] implemented in PowerFactory

2.2 Test cases

Two test cases based on the tests defined in [2] are used. One device under test is connected to the test system. The basic power output is 50% of the nominal active power of the DUT, the reactive power at the PoC is controlled to zero by the DUT (both quantities in fundamental frequency, positive sequence).

2.2.1 Test case for voltage unbalances: The test is performed according to Section 7.2.4 of [2]. A negative sequence voltage of 2% is added to the grid voltage, by switching an according negative sequence voltage source into the network (voltage source "u2" in Fig. 1).

2.2.2 Test case for harmonic distortion: The test is inspired by Section 7.2.5 of [2]. Harmonic voltage of 2% in the 5th and 7th harmonic order (250 Hz and 350 Hz in the 50-Hz-system) are added to the ideal fundamental frequency grid voltage (50 Hz nominal frequency) at the same time.

2.3 Test system to determine the frequency-dependent impedances

To determine the frequency-dependent impedance characteristics of the generating units with different GFC implementations or with SG, EMT simulations with the same models in PowerFactory are used. The DUT, which includes the GFC or SG and the unit transformer, is connected to a controllable voltage source, which sequentially injects small harmonic voltage perturbations. The resulting harmonic currents at the DUT's terminal are measured to calculate the frequency-dependent impedance characteristic of the DUT. The impedance characteristics are determined in the frequency range from 1 Hz through 650 Hz (13th harmonic order).

3 Model implementations

The DUTs contain GFCs with different implementations, or an SG for comparison, and the unit transformer. Table 1 lists the investigated DUT implementations.

The unit transformer has a short-circuit voltage (impedance) of 10% (based on a slightly higher power rating of the transformer compared to the power rating of the GFC or SG, factor of 1.07).

3.1 Synchronous generator model for comparison

For comparison a typical synchronous generator (SG) is used. The SG has the same rated power and nominal power factor as the GFC. The acceleration time constant T_a is 10 s (inertia constant H = 5 s, rated to nominal active power of the SG). The PowerFactory standard model with default impedance settings is used (round rotor, $x_d = x_q = 200\%$, $x'_d = x'_q = 30\%$, $x''_d = x''_q = 20\%$, which are default steady-state, transient and subtransient time constants). Simple models of AVR and governor from the DIgSILENT Library are used with their default parameter settings.

3.2 Description of the GFC model

A typical implementation of a Virtual Synchronous Machine (VSM, see Fig. 2) with an acceleration time constant T_a of 10 s (H = 5 s) is used as GFC model. The VSM implementation is documented in [3]. The GFC uses a series reactance of 10% (input parameter of the static generator model in PowerFactory). Voltage and current measurements for the GFC control system are located at the bus between the converter's series reactance (which is included in the static generator model) and the unit transformer.

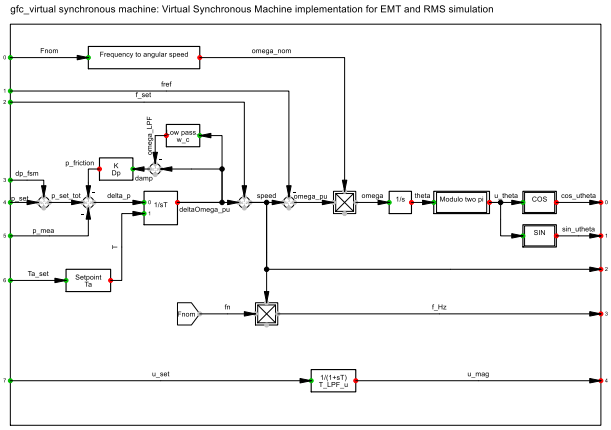

Fig. 2: Block diagram of the virtual synchronous machine implementation

The GFC model is further equipped with proportional AC voltage control, a model of the DC link, DC voltage control, a simple power source model and a frequency sensitive mode (FSM) controller (including LFSM-O/U), see Fig. 3.

The virtual impedance (VI, indicated in Fig. 3) is deactivated for the investigation, to prevent and exclude any possible overlay in the responses from inner control loops and virtual impedance, which may impact the results of the analysis.

The slot "Output voltage calc. / inner ctrl. loops" (see Fig. 3) is the link between the VSM controller, the VI (if used) and the converter. It holds the output voltage reference calculation for the converter w/o inner control loops. Only in case of a GFC implementation without inner control loops, this slot

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holds a model which calculates the output voltage reference signals directly based on the VSM output (adding the VI signals if used), including a voltage-drop limitation to avoid/limit over-currents (output current limitation) [3], which can be referred to as an output saturation and which is only used without subsequent inner control loops. The implementations of inner control loops are described in the following sections.

The output signals of the voltage calculation block or the inner control loops respectively are the reference for the pulse width modulation (PWM). The switching of the converter valves (IGBTs) is neglected, i.e. an average value model of the converter is used (controlled Thévenin equivalent in EMT simulation). This decision is by intention, as the focus of the investigation is not the harmonic emission of the GFC, but the impact on unbalances and harmonics, which are existing in the grid voltage.

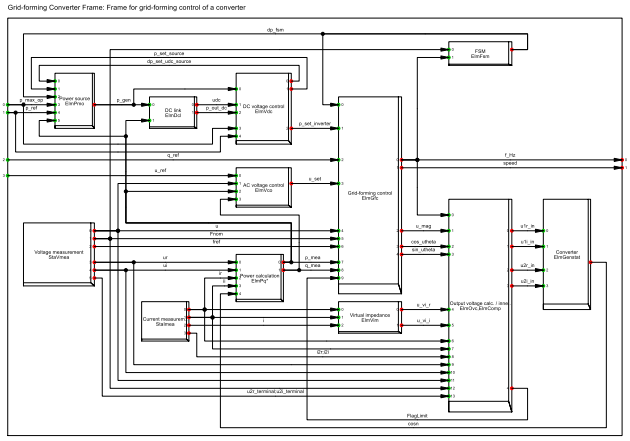

Fig. 3: Overview of the control structure of the GFC model (Composite Model Frame in PowerFactory)

3.3 Implemented inner control loops

Inner control loops are implemented as PI controllers in the rotating dq references frame (see Sections 3.3.1 - 3.3.3) and PR controllers in the stationary alpha-beta frame (see Section 3.3.4).

3.3.1 Inner voltage and current control in rotating dq reference frame: This implementation is hereafter referred to as "VSM PI ctrl. dq". The voltage reference signals from the VSM (and VI if active) and the measured voltages and currents are transformed into the rotating dq reference frame by simple Park transformation. The voltage angle output of the VSM is used as reference angle for the Park transformation. The transformed signals are then used by Proportional-Integral (PI) controllers to control the voltage and current (Fig. 4). This type of control structure is often found as a possible implementation in publications dealing with GFCs (for example in [4, 5, 6]). It shows a similarity in the inner control loop to conventional grid-following converter control. Actually, the PLL of a grid-following converter control is replaced by the synchronisation of the VSM (which also applies inertia), the reactive current control in the outer loop is replaced by voltage control in the outer loop (AC voltage controller as AVR of the VSM).

The voltage controller in the inner loop is implemented using a PI controller in the d-axis and another PI controller in the q-axis. Possible feed-forward terms are deactivated for the presented investigation.

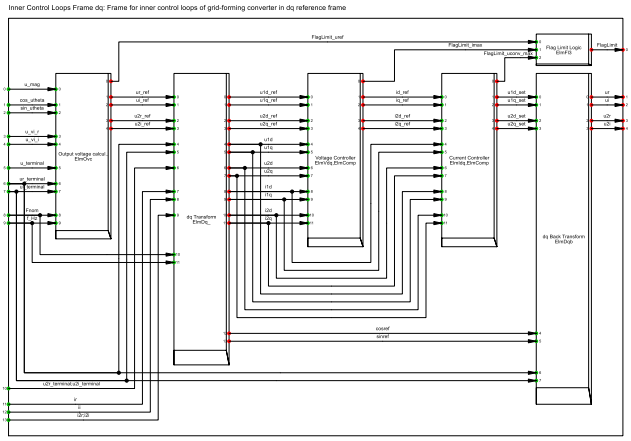

Fig. 4: Overview of the inner PI control loop structure implementation in the dq reference frame (Composite Model Frame in PowerFactory)

The current controller in the inner loop is implemented using a PI controller in the d-axis and another PI controller in the q-axis. Cross-coupling compensation between the d- and q-axis based on measured currents is used.

The PI controller implementations include current and voltage output limiters. The output of the current controller is transformed back from the dq reference to the alpha-beta reference. These signals are the converter voltage references.

Table 1: Overview of implemented models

Model short name	Description
No DUT	No device under test connected (open circuit test)
SG	Synchronous generator
VSM without inner ctrl. loops	Virtual synchronous machine implementation without inner control loops
VSM PI ctrl. dq	VSM implementation with inner PI control loops in rotating dq reference frame
VSM PI ctrl. dq NF	VSM implementation with inner PI control loops and notch filters for measured voltage and currents in rotating dq reference frame
VSM PI ctrl. dq NF i2=0	VSM implementation with inner PI control loops for positive and negative sequence in rotating dq reference frame, notch filters to extract positive and negative sequence voltages and currents, negative sequence current controller to control negative sequence current to zero
VSM PI ctrl. dq NF i2 u2	VSM implementation with inner PI control loops for positive and negative sequence in rotating dq reference frame, notch filters to extract positive and negative sequence voltages and currents, negative sequence voltage controller to emulate negative sequence impedance
VSM PR ctrl. alpha-beta	VSM implementation with inner PR control loops in stationary alpha-beta reference frame

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3.3.2 dq transformation with notch filters: As an extension of the control described in Section 3.3.1, the Park transformation which transforms the measured voltages and currents from alpha-beta to dq reference frame is further equipped with notch filters (NF). The notch filters are tuned at 2 times the fundamental frequency in order to filter out noise from unbalances, which appear as negative sequence components in the fundamental frequency of the natural three-phase system. The negative sequence fundamental frequency components transfer as ripple with doubled frequency into the signals in d- and q-axis. This ripple is filtered by the notch filter. In the voltage signals, sub-sequent first order low pass filters are used to further smooth the signals in d- and q-axis. Such additional low-pass filtering is not applied to the current signals, as experience has shown that this would make the dynamic response in the currents too slow. This extension is hereafter referred to as "VSM PI ctrl. dq NF".

3.3.3 Negative sequence current control: In addition to the extension described in Section 3.3.2, negative sequence signals are extracted from the measured voltage and current by means of an inverted Park transformation (double synchronous reference frame) with sub-sequent notch filters. Again, in the negative sequent voltage signals, additional sub-sequent first order low pass filters are used to further smooth the signals in d- and q- axis.

An additional PI current controller is used in the negative sequence to control the negative sequence current.

In the first variation of this implementation, the setpoint for the negative sequence current is put to zero. Consequently, the controller will force the negative sequence current to zero. This implementation is referred to as "VSM PI ctrl. dq NF i2=0" in the following.

In the second variation of this implementation, the setpoint for the negative sequence current is generated by a negative sequence voltage controller which emulates a negative sequence admittance. It is actually a cross-coupled proportional controller in the dq reference frame with additional low pass filters. In the test cases it is used to control $g_2 = 0$ p.u. (negative sequence conductance) and $b_2 = 4$ p.u. or $b_2 = 2$ p.u. respectively (negative sequence susceptance). This corresponds to a continuous dynamic voltage support in negative sequence with a gain $K_2 = 4$ or $K_2 = 2$. At the same time, it corresponds to a controlled negative sequence reactance of $x_2 = 25\%$ or $x_2 = 50\%$. This implementation is referred to as "VSM PI ctrl. dq NF i2 u2" in the following.

The output signals from the negative sequence current controller are back-transformed to the stationary alpha-beta frame and added to the back-transformed output signals from the positive sequence current controller. This gives the total voltage reference signals for the converter.

3.3.4 Inner voltage and current control in stationary alpha-beta reference frame: Instead of transforming the voltages and currents into a rotating dq reference frame, the signals in stationary alpha-beta reference frame are directly used for the inner control loops.

Proportional Resonant (PR) controllers are used in this implementation for inner loop voltage and current control. A documentation is found in [7]. Besides the actual PR controllers, it uses 100% feed-forward of measured currents or voltages respectively. The PR controller implementation is based on [8]. Output current and voltage limitation is realised at the output of the PR controllers. This implementation is referred to as "VSM PR ctrl. alpha-beta" in the following.

Utilising three single-phase PR controllers in the abc reference frame (i.e. in the phases) for inner loop voltage control and current control respectively is another possible implementation which shows promising behaviour, especially in the case of unbalanced network faults [7]. To compute the quadrature signals in each phase for the single-phase PR controllers in the abc reference frame, a second order generalized integrator [9] is employed, which serves as the input to the PR controllers [7]. This specific implementation is not included in the results presented in this paper.

4 Discussion of Results

This chapter presents and discusses the simulation results.

4.1 Voltage Unbalance

4.1.1 Result with initial parameter sets of the models: The simulation results of the voltage unbalance test case are depicted in Fig. 5 – Fig. 7 for a first run of simulations with the initial parameter set of the models. Fig. 5 shows the remaining negative sequence voltages, when the different models are connected to the test network. The "No DUT" case shows the 2% negative sequence applied to the grid voltage, which are visible at the PoC, when no generating unit is connected.

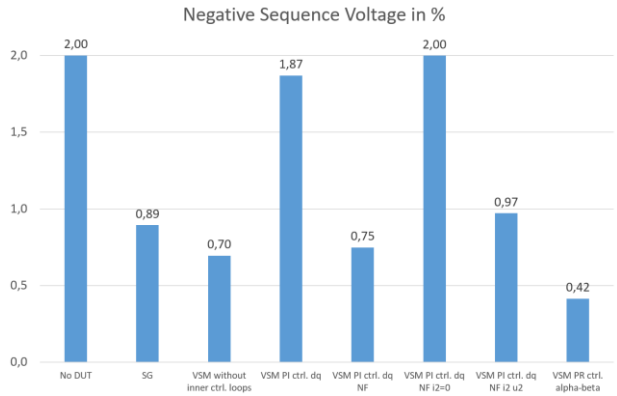

Fig. 5: Negative sequence voltages in %, higher gain of PI controllers in dq reference frame

As a reference, a synchronous generator is connected. The negative sequence voltage u_2 reduces from 2% to 0.89%. Together with the (mainly reactive) negative sequence current i_2, this makes a negative sequence impedance z_2, which is approx. 29%. This matches the expectation, as the negative sequence reactance x_2 of an SG is estimated as 20% following eq. (1). Together with 10% impedance of the transformer (on a slightly different base value) this makes approx. 30%.

$$x_2 = (x_d'' + x_q'')/2 \qquad (1)$$

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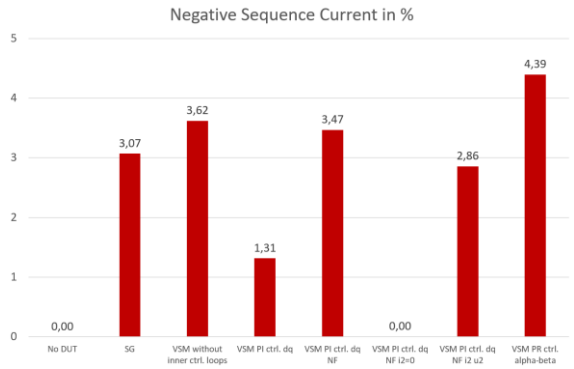

Fig. 6: Negative sequence currents in %, higher gain of PI controllers in dq reference frame

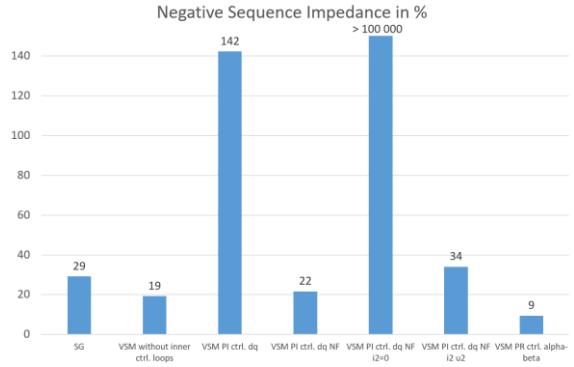

Fig. 7: Negative sequence impedances in %, higher gain of PI controllers in dq reference frame

The resulting u_2 in case of the VSM without inner control loops is even smaller (0.7%, Fig. 5). This is because of the series reactance of the converter, which is parameterised at 10%. Together with the 10% transformer impedance, this makes ca. 20%. The result is the simulation shows an impedance of 19% (Fig. 7) with a mainly reactive i_2 = 3.62% (Fig. 6).

Introducing inner PI control loops in dq references frame (VSM PI ctrl. dq) causes a significant increase in impedance z_2 (Fig. 7). The resulting u_2 is 1.87% (Fig. 5), i_2 is mainly resistive. The PI controllers with their given gains are fast enough to counter-act on the ripple in the signals in the d- and q axis. As a consequence, they suppress the negative sequence current, which means that the VSM with this implementation and parametrisation has minimal impact on voltage unbalance damping.

By adding notch filters, which reduce the ripple in the signals, the control becomes low-ohmic again (z_2 = 22%, Fig. 7, VSM PI ctrl. dq NF). i_2 is mainly reactive. It should be noted however, that the settling time is quite long (several seconds).

Controlling the negative sequence current to zero causes an (almost) open circuit behaviour in the negative sequence. The effective z_2 is higher than 100 000%, u_2 at the PoC remains at 2%, as expected (Fig. 5 – 7, VSM PI ctrl. dq NF i2=0).

Controlling the negative sequence voltage (VSM PI ctrl. dq NF i2 u2) gives freedom in defining easily the response in the negative sequence. With controller gain b_2 = 4 p.u., the expected reactance of $x2$ = 1/4 = 25% is achieved. Together with 10% transformer impedance, this makes an impedance of 35% (Fig. 7). The current i_2 is almost a pure reactive current. u_2 reduces to 0.97% (Fig. 5).

The PR controller implementation in the alpha-beta frame (VSM PR ctrl. alpha-beta) corresponds almost to a short-circuit in the negative sequence. The remaining impedance z_2 is approximately equivalent to the transformer impedance (9%, Fig. 7).

4.1.2 Result with reduced gains of inner PI controllers: As another variation, the gains of the inner PI controllers are reduced by a factor of 2. Results are illustrated in Fig. 8 - 10.

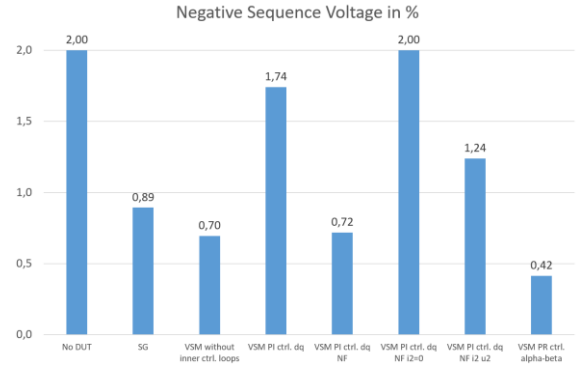

Fig. 8: Negative sequence voltages in %, reduced gain of PI controllers in dq reference frame

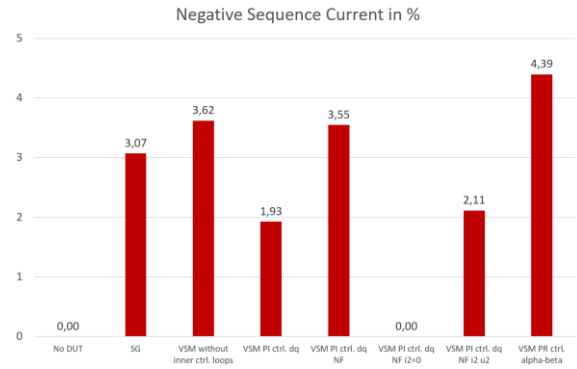

Fig. 9: Negative sequence currents in %, reduced gain of PI controllers in dq reference frame

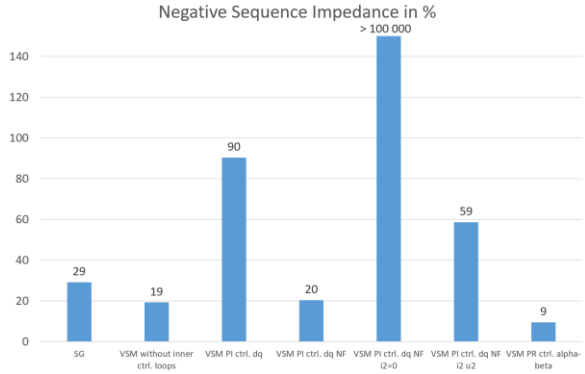

Fig. 10: Negative sequence impedances in %, reduced gain of PI controllers in dq reference frame

The reduced gains cause a smaller effective negative sequence impedance (compare Fig. 10 with Fig. 7). As a consequence, the existing negative sequence voltage at the PoC reduces to

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lower values (compare Fig. 8 with Fig. 5). In case of voltage control in the negative sequence (VSM PI ctrl. dq NF i2 u2) the susceptance gain g_2 is also reduced to $g_2 = 2$. Consequently, the resulting effective impedance is ca. 60% (x_2 = 1/2 = 50%, plus 10% transformer impedance; compare Fig. 10). u_2 reduces to 1.24%.

4.2 Low-order Harmonics

Fig. 11 – 13 show the results of the harmonic voltages, currents and impedances for the 5th and 7th harmonic order. In cases of inner PI control loops the results with *higher* gains are presented in these figures.

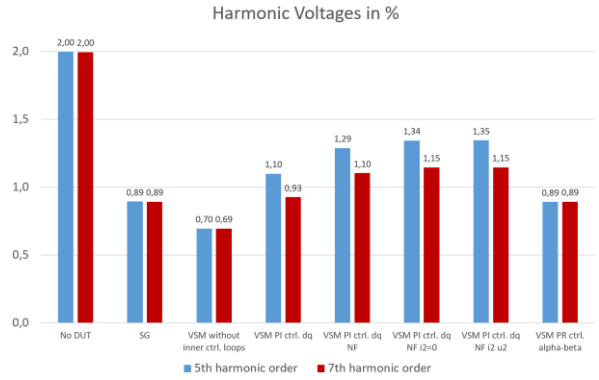

Fig. 11: Harmonic voltages in %, higher gain of PI controllers in dq reference frame

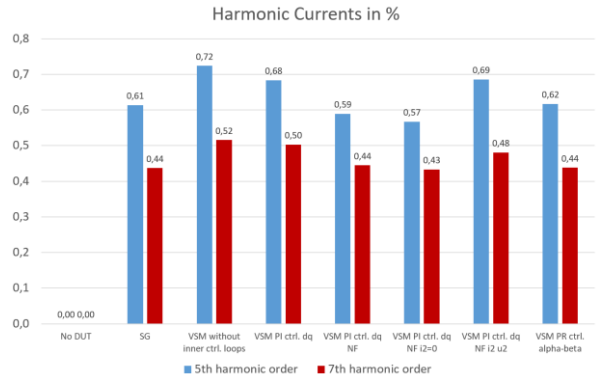

Fig. 12: Harmonic currents in %, higher gain of PI controllers in dq reference frame

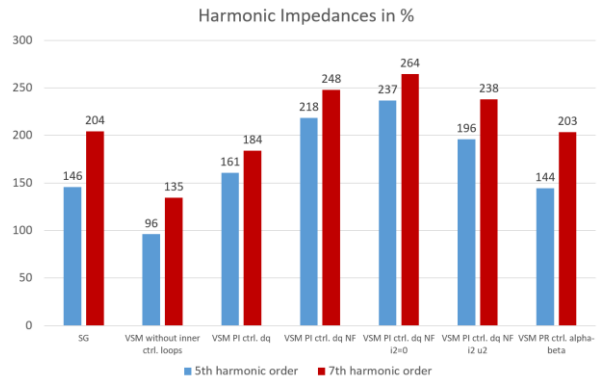

Fig. 13: Harmonic impedances in %, higher gain of PI controllers in dq reference frame

The existing harmonic voltages are reduced by all investigated GFC implementations. The reduction caused by the implementations with inner PI controllers parametrised with higher gains is not as substantial as that of the SG (Fig. 11). In contrast, the VSM without inner control loops lower the harmonic voltages even more (Fig. 11). The implementation with PR controllers causes a similar reduction compared to the SG (Fig. 11, VSM PR ctrl. alpha-beta).

The results for inner PI controllers with *smaller* gains are presented in Fig. 14 – 16. Again, the gains are reduced by a factor of 2, compared to the results shown in Fig. 11 – 13.

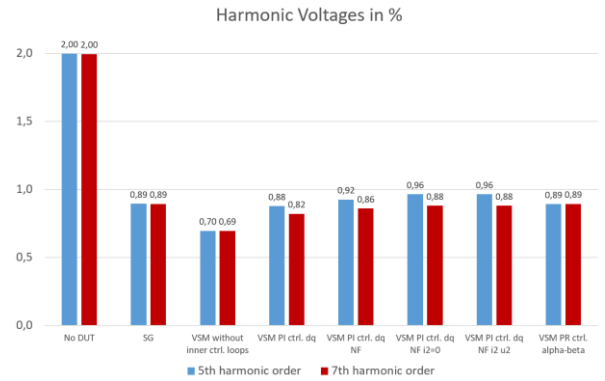

Fig. 14: Harmonic voltages in %, reduced gain of PI controllers in dq reference frame

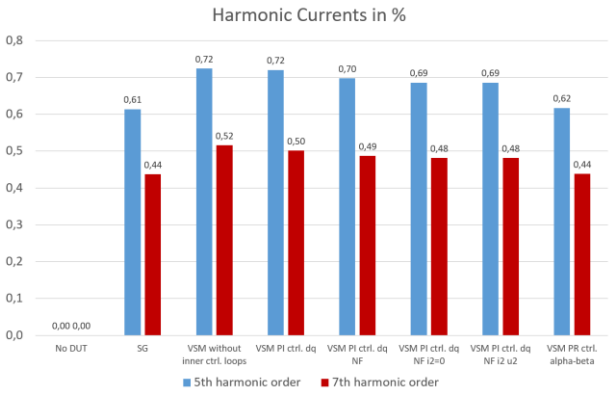

Fig. 15: Harmonic currents in %, reduced gain of PI controllers in dq reference frame

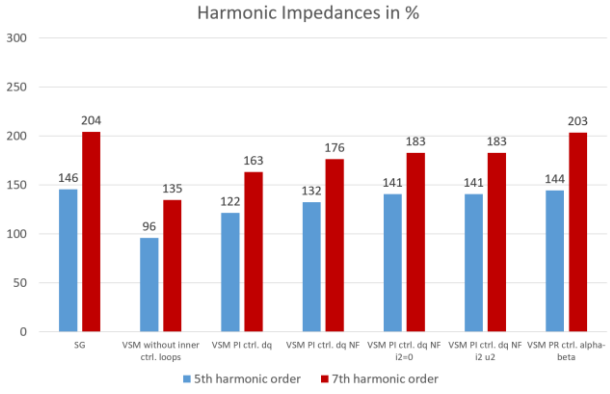

Fig. 16: Harmonic impedances in %, reduced gain of PI controllers in dq reference frame

With the smaller setting of the gains, a reduction of the harmonic voltages is achieved which is similar to the reduction

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caused by the SG (Fig. 14). With smaller gains, the resulting impedances in the 5th and 7th harmonic order are actually even slightly smaller than the impedance of the SG (Fig. 16).

4.3 Frequency-dependent Impedances

To better understand the results obtained by the simulations and presented in Sections 4.1 and 4.2, the frequency dependent impedances of the SG and the GFC with the different implementations are determined as explained in Section 2.3. Results for the impedance magnitude and angle in the positive and negative sequence are shown

- in Fig. 17 for the SG,
- in Fig. 18 for the VSM without inner control loops,
- in Fig. 19 for the VSM with inner PI control loops in dq reference frame without further filtering (VSM PI ctrl. dq),
- in Fig. 20 for the VSM with inner PI control loops in dq reference frame with NF (VSM PI ctrl. dq NF),
- in Fig. 21 for the VSM with inner PI control loops in dq reference frame with NF and voltage and current control in the negative sequence (VSM PI ctrl. dq NF i2 u2).

Fig. 17 indicates that the impedance of the SG is mainly a reactance that increases with the frequency or the harmonic order *h* respectively. The impedance of an SG can be estimated by eq. (2). The impedance of the unit transformer comes on top and is included in the determined impedance curves.

$$z_{SG} \approx h \cdot x''_d \qquad (2)$$

The impedance characteristics in the positive and negative sequence are identical above 75 Hz. Just around the nominal frequency, the positive sequence impedance of the SG is higher than the one in the negative sequence, because the positive sequence impedance increases to the transient impedance around fundamental frequency, and turns into the steady-state impedance at fundamental frequency. The positive sequence impedance at fundamental frequency is defined by the operating point (which is ca. 50% power in this case). An effect of the machine controllers is only visible around the nominal frequency.

The result indicates, that an SG can have a contribution to act as a sink only for *low-order* harmonics.

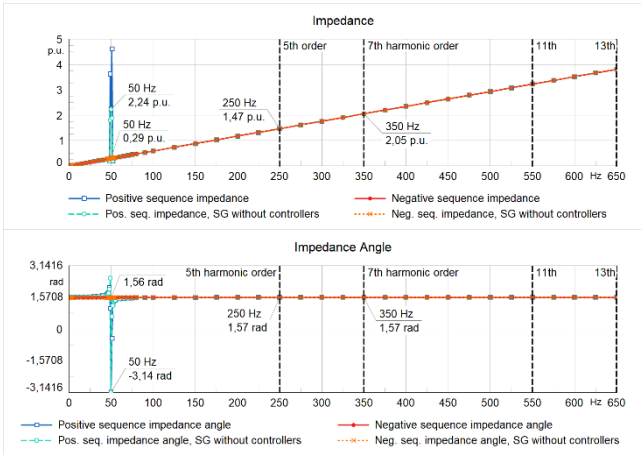

Fig. 17: Impedance of synchronous generator

The impedance of the VSM without inner control loops (Fig. 18) shows a similar frequency characteristic as the SG in the presented frequency range (compare Fig. 17). In the example, the curves of the VSM start at a smaller value and have a smaller slope, because of the smaller given value for the converter's series reactor. An effect of the VSM controllers is only visible in the positive sequence around and at the fundamental frequency.

It should be noted that the impedance of the VSM will look different at higher frequencies, because of the LCL-filter which is typically used to filter the switching frequency of the PWM, measurement input filters and control time delays in the digital controllers and due to the PWM.

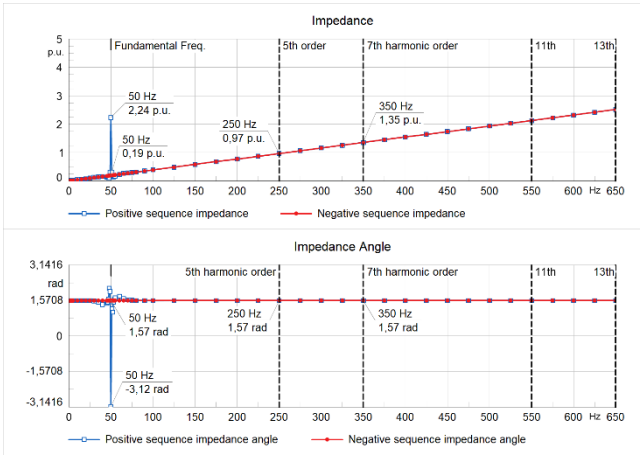

Fig. 18: Impedance of VSM without inner control loops

The inner PI controllers have a remarkable impact on the impedance (Fig. 19) in the frequency range of low-order harmonics. The impedance is shifted to a higher value, which depends on the gains. Higher gains cause a higher impedance. The impedance angle is rather resistive than reactive. The higher the gains, the more resistive is the impedance. At higher frequencies, the magnitude of the impedance comes closer to that of the VSM without inner control loops (compare the impedance at 650 Hz in Fig. 19 with Fig. 18).

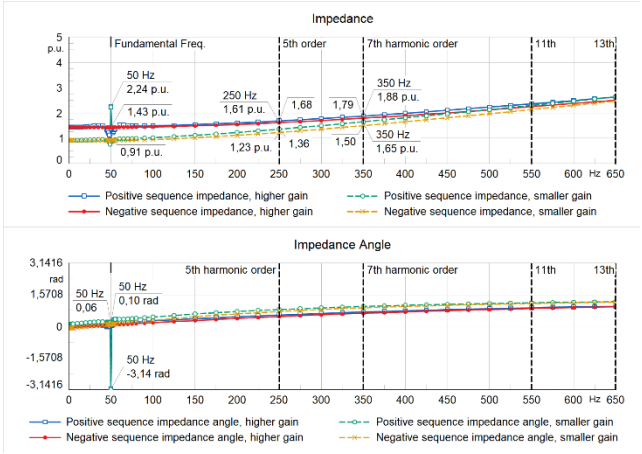

Fig. 19: Impedance of VSM with inner PI control loops in dq reference frame without further filtering (VSM PI ctrl. dq)

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The effect of the notch filters is particularly noticeable in the negative sequence at fundamental frequency and for positive sequence impedance in the 3rd harmonic order (Fig. 20, VSM PI ctrl. dq NF). The dq transformation shifts these perturbations to the second harmonic order in the dq reference frame, at which the notch filters are active and eliminate the ripple. As a result, the negative sequence impedance at the fundamental frequency and the positive sequence impedance at the 3rd order reduce to values similar to the values of the VSM without inner control loops (compare Fig. 20 to Fig. 18).

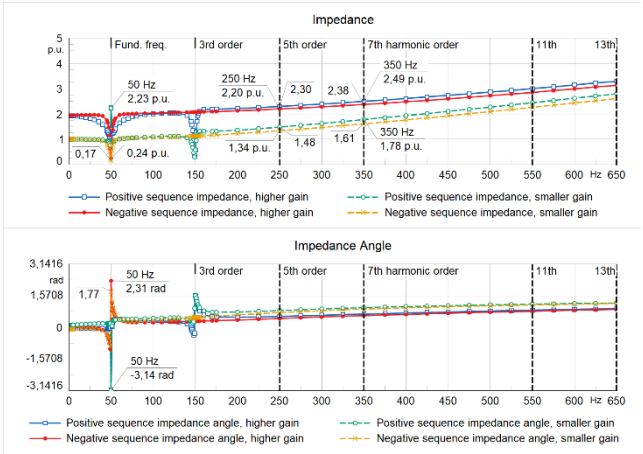

Fig. 20: Impedance of VSM with inner PI control loops in dq reference frame with NF (VSM PI ctrl. dq NF)

Above fundamental frequency, the impact of the controller gains on the effective harmonic impedance in case of the implementation with NF is higher than without NF (compare Fig. 20 to Fig. 19).

With controllers in the negative sequence (VSM PI ctrl. dq NF i2 u2) both the positive sequence as well as the negative sequence impedance characteristics similarly increase above and decrease below the nominal frequency (Fig. 21).

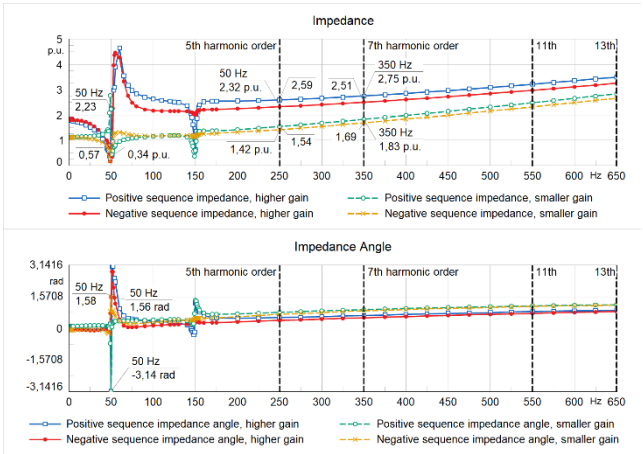

Fig. 21: Impedance of VSM with inner PI control loops in dq reference frame with NF and negative sequence voltage and current control (VSM PI ctrl. dq NF i2 u2)

5 Conclusions

The results indicate that, with respect to acting as a sink for existing unbalances and low-order harmonics in system voltage, a VSM implementation without inner control loops can achieve a behaviour similar to a real synchronous machine without additional effort. If inner control loops are used, their design and the selected parameter values define the amount of a beneficial effect that the GFC can have on the power quality of power systems.

As a conclusion, inner control loops should be designed with care, and GFCs tested thoroughly with respect to the mentioned power quality aspects, in order to ensure a continuing high power quality in future power systems, and to avoid increasing stress on remaining (conventional) devices acting as sinks to counter unbalances and low-order harmonics (incl. inter-harmonics) in the system voltage. Related requirements for maximum admissible impedances or frequency-dependent impedance envelope curves might be defined in grid codes.

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