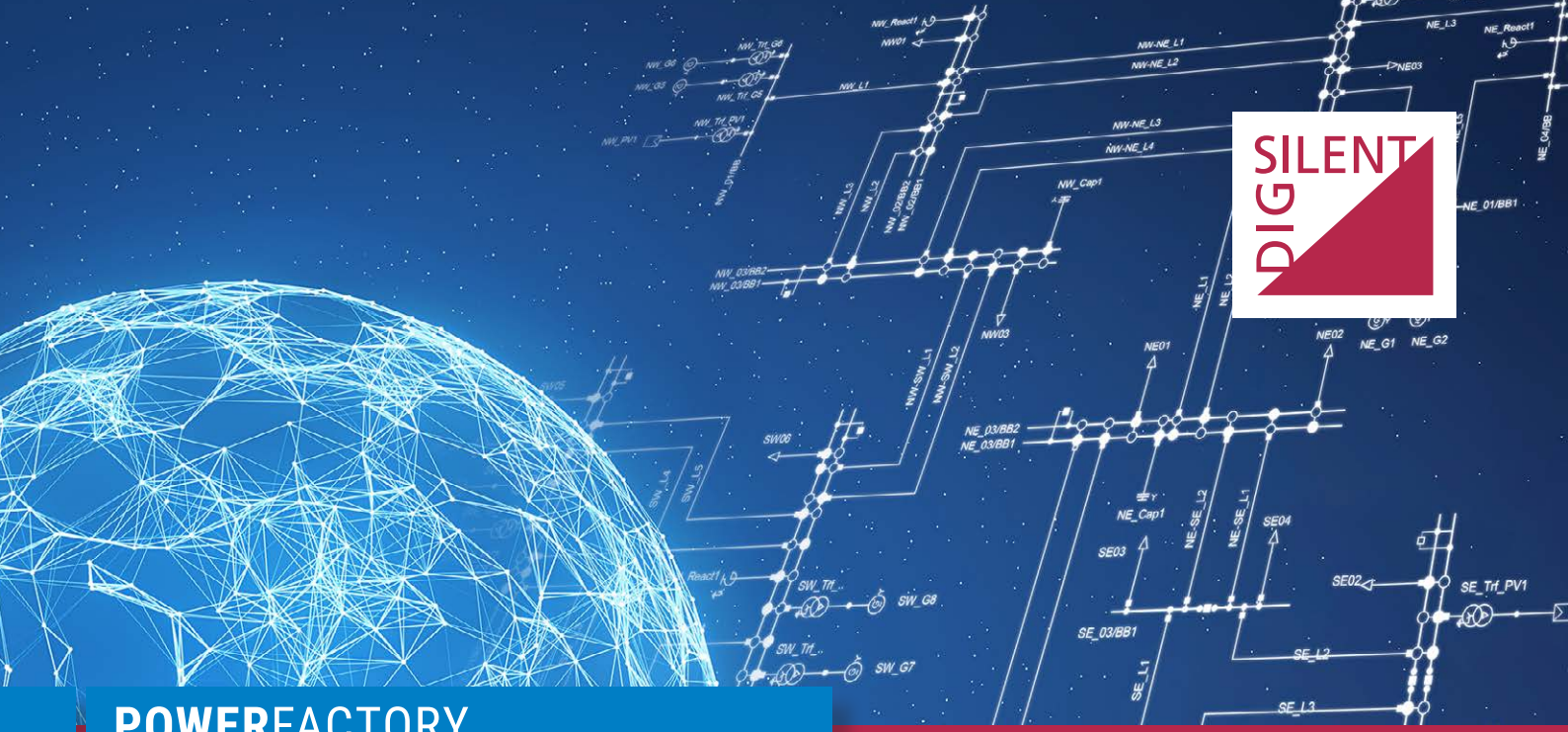

POWERFACTORY

PowerFactory 2021

Technical Reference

MMC Valve

ElmMmcvalve

PF2021

POWER SYSTEM SOLUTIONS

MADE IN GERMANY

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Revision 1

Contents

1 General Description

The *MMC Valve* element in *PowerFactory* is used for modelling modular multilevel converter sub-modules and it contains two pre-configured configurations. The MMC valve is a purely EMT model.

The available half-bridge and full-bridge configurations are presented in Figure 1.1 where IGBT devices together with anti-parallel diodes are shown. The representation is valid not only for IGBT devices, but also for other transistor devices with on/off capability. The element can be connected to DC terminals only.

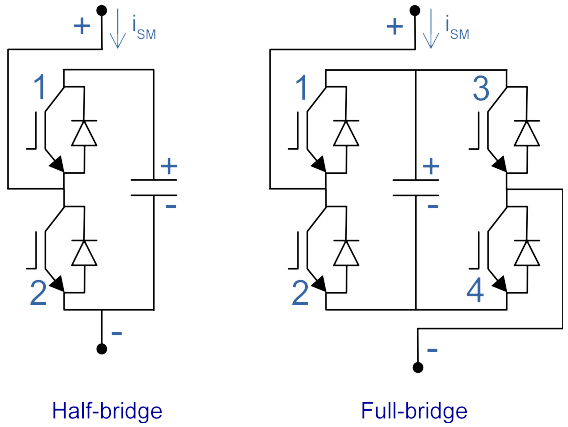

Figure 1.1: Equivalent diagram for the half-bridge and full-bridge configurations

Three different models are available:

- *Detailed* model,
- *Detailed equivalent circuit* model, and
- *Aggregate arm* model.

The *Detailed* model implements the configurations shown in 1.1 where only one submodule is modelled. The *Detailed equivalent circuit* and *Aggregate arm* models can be used to model multiple submodules in series by using the parameter $Nsubmod$. These models are used to represent the submodules of an arm of an MMC. The arm reactor is not included in the model and must be modelled externally. A detailed description of these models is given in section 2.

2 EMT simulation

In this section, the available models together with the available input and output signals are presented.

2.1 *EMT* models description

2.1.1 *Detailed* model

A transistor is modelled with a resistance Rton if the state of the transistor is On, and with a conductance if the state is Off. The same is valid for the anti-parallel diode. The equivalent circuit diagram is shown in Figure 2.1.

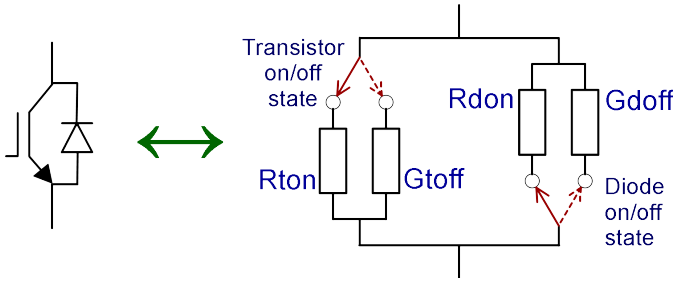

Figure 2.1: Equivalent circuit diagram of a IGBT with an anti-parallel diode

The capacitance of the MMC valve has an additional conductance modelled in parallel as shown in Figure 2.2.

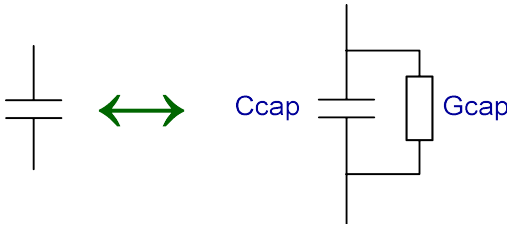

Figure 2.2: Equivalent circuit diagram of the capacitor

The state change logic differs for the diode (not controllable device) and the transistor (fully controllable device for example a GTO, IGBT or IGCT). The state of the diode is always Off if the current is negative and is On if the voltage difference of the diode is higher then 0. The switching to on and off state of the fully controllable devices depends also on the $gate$ input signal as shown in Figure 2.3.

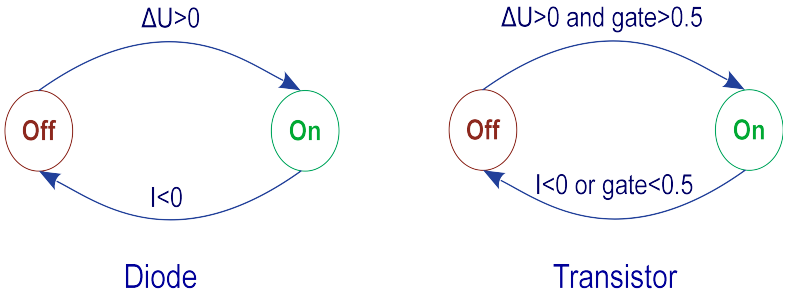

Figure 2.3: State diagram of a diode and a transistor

2.1.2 *Detailed equivalent circuit* model

The *Detailed equivalent circuit* (type 4) model is based on the theory exposed in [1]. Using this model in *PowerFactory* is practically equivalent to using $Nsubmod$ number of detailed models where the electrical nodes between the submodules have been reduced.

Each submodule is represented explicitly with its capacitor voltage dynamics and its valves. Each valve is represented as a two valued resistance, one for the on-state and one for the off-state.

A Thevenin equivalent circuit is derived for each submodule. For the j^{th} half-bridge submodule, the Thevenin resistance and voltage are given by

$$R_{submod,j} = \frac{R1 \cdot R2}{R1 + R2} \tag{1}$$

$$u_{submod,j} = \frac{R2}{R1 + R2} \cdot u_{cap,j} \tag{2}$$

where $u_{cap,j}$ is the j^{th} submodule capacitor voltage, $R1$ is the equivalent resistance of the upper transistor in parallel with the upper diode and $R2$ is the equivalent resistance of the lower transistor in parallel with the lower diode.

In order to reduce the internal number of nodes, a Thevenin equivalent is derived by summing up the contribution for all $Nsubmod$ submodules:

$$R_{Thev} = \sum_{j=1}^{Nsubmod} R_{submod,j} \tag{3}$$

$$u_{Thev} = \sum_{j=1}^{Nsubmod} u_{submod,j} \tag{4}$$

The total voltage output from all the submodules is then given as:

$$u_{submod} = u_{Thev} + R_{Thev} \cdot i \tag{5}$$

The submodule capacitor dynamics is given by:

$$C \cdot \frac{du_{cap,j}}{dt} = i_{cap,j} \tag{6}$$

where for a half-bridge submodule $i_{cap,j}$ is calculated as:

$$i_{cap,j} = \frac{R2}{R1+R2} \cdot i - G_{cap} \cdot u_{cap,j} - \frac{u_{cap,j}}{R1+R2} \tag{7}$$

G_{cap} represents the no-load losses for the capacitor.

The voltage equation for the element is:

$$u_1 - u_2 = u_{submod} \tag{8}$$

with $u_1 - u_2$ being the voltage difference across the MMC valve element.

2.1.3 *Aggregate arm* model

The *Aggregate arm* model is based on the theory exposed in [2]. The valves are not represented explicitly, but are instead represented by one equivalent capacitor and a voltage source.

The contribution from all valves is averaged using the switching function s_n defined as:

$$s_n = \frac{1}{Nsubmod} \cdot \sum S_i \tag{9}$$

where $Nsubmod$ is the number of submodules. $S_i = 0$ if the i_{th} submodule is turned off, $S_i = 1$ if the i_{th} submodule is inserted with positive polarity and $S_i = -1$ if the i_{th} submodule is inserted with negative polarity (only for the full-bridge model).

Assuming all submodule capacitors to be charged at the same voltage, the total voltage output from all the submodules will depend on their switching status and it is given by:

$$u_{submod} = s_n \cdot u_{capsum} + R_{on} \cdot i \tag{10}$$

where u_{capsum} is the sum of all capacitor voltages, i is the terminal current, R_{on} is the resulting on-state resistance of all switches. R_{on} depends on $Rton$, $Rdon$, the type of submodule (half- or full-bridge) and the state (on or off) of each submodule. Note that the off-conductances of the switches are not considered in this model.

The submodules capacitances are represented through an equivalent capacitor whose capacitance C_{eq} is calculated as:

$$C_{eq} = \frac{Ccap}{Nsubmod} \tag{11}$$

where $Ccap$ is the capacitance of a single submodule and $Nsubmod$ is the number of submodules.

The current flowing in the equivalent capacitor is zero if all submodules are bypassed while it is equal to the terminal current if all submodules are inserted. The equivalent capacitor current is calculated as:

$$i_{cap} = s_n \cdot i \tag{12}$$

The equivalent capacitor dynamics is according to the following equations:

$$C_{eq} \cdot \frac{du_{capsum}}{dt} = i_{cap} \tag{13}$$

The switching function is calculated based on the *gate* input and current direction. The voltage equation for the element is:

$$u_1 - u_2 = u_{submod} \tag{14}$$

with $u_1 - u_2$ being the voltage difference across the MMC valve element.

2.2 Control

The models can be controlled using the *gate* input signal, which is an array of signals for the state of each single valve. The *gate* input signal must be connected to the output of a pulse generator *ElmPulsegen*.

A half-bridge configuration requires an array signal of size $2 \cdot Nsubmod$ and a full-bridge configuration requires an array signal of size $4 \cdot Nsubmod$ (the *Detailed* model has $Nsubmod = 1$).

Normally, the *Detailed equivalent circuit* and *Aggregate arm* models can be used to represent one arm of a MMC and one pulse generator can be used to generate the signals required per arm. Therefore, these models can be connected directly in the control. In the case of the *Detailed* model, since the submodules are modelled separately, it is practical to use a *Vector of Objects* element ($IntVecobj$). The *Vector of Objects* element can be used to distribute the signals from the pulse generator to the individual submodules. For example, a pulse generator gate array output signal with size 200, can feed 50 full-bridge submodules by connecting the vector of objects to the pulse generator and inserting the submodules in the vector.

If the sorting option of the pulse generator is enabled, the submodule capacitor voltages of the MMC valve element must be provided as input to the pulse generator. This is possible only for the *Detailed* and *Detailed equivalent circuit* model.

2.3 Blocking mode

To block a submodule represented by a *Detailed* model, either a block signal needs to be provided and activated or all the gates should be set to inactive. To block a submodule represented by a *Detailed equivalent circuit* or *Aggregate arm* model, a block signal needs to be provided and activated.

During blocking of the *Detailed* model, the equivalent circuit of a submodule is presented in Figure 2.4 and in Figure 2.5. Modelling of the *Detailed equivalent circuit* model during blocking mode, is based on the same representation.

Modelling of the *Aggregate arm* model during blocking mode, is based on the circuit presented in Figure 2.6.

It is noted that for the full-bridge MMC in blocking state, a DC fault causes the blocked submodule capacitors to charge and block the short-circuit current.

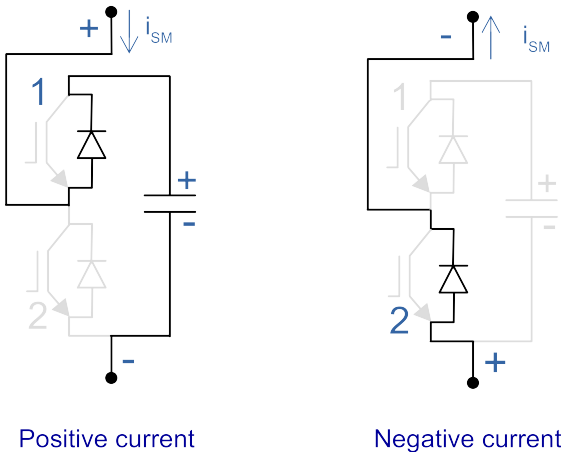

Figure 2.4: *Detailed* model equivalent diagram during blocking for the half-bridge configuration

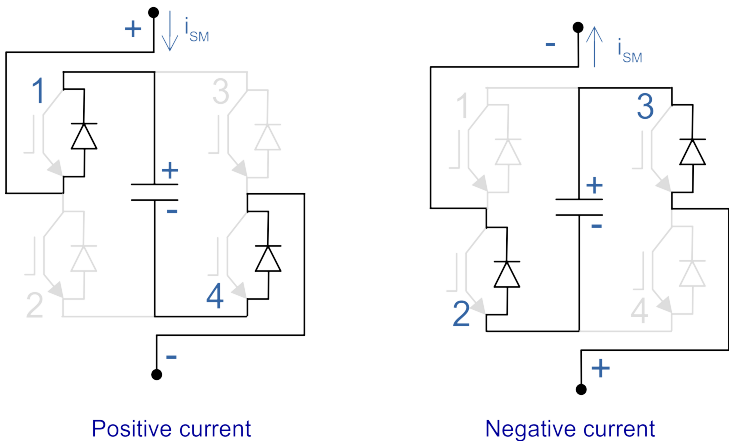

Figure 2.5: *Detailed* model equivalent diagram during blocking for the full-bridge configuration

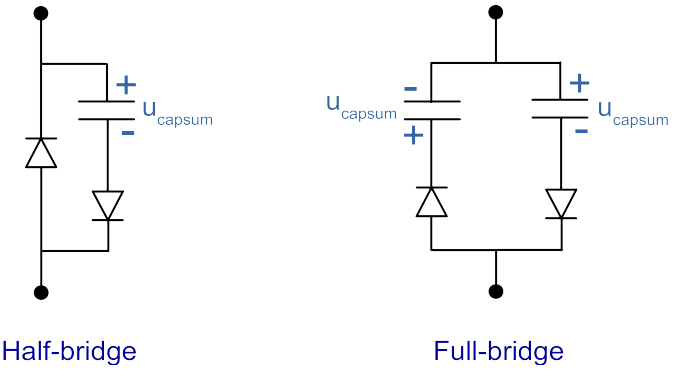

Figure 2.6: *Aggregate arm* model equivalent diagram during blocking

2.4 Inputs/Outputs of the EMT model

Table 2.1: Input definition of the dynamic models

Input Signal	Symbol	Description	Unit
gate		Array of gate signals for controlling each transistor	
block		Block signal for the transistors	

Table 2.2: Output variables definition of the *Detailed* model

Parameter	Symbol	Description	Unit
Ucap		Capacitor voltage	kV

Table 2.3: Output variables definition of the *Detailed equivalent circuit* model

Parameter	Symbol	Description	Unit
Ucap		Array of capacitor voltages	kV
Ucapsum		Sum of capacitor voltages	kV
Ummc		MMC output voltage (voltage difference between the connected terminals)	kV

Table 2.4: Output variables definition of the *Aggregate arm* model

Parameter	Symbol	Description	Unit
Ucapsum		Sum of capacitor voltages	kV
Ummc		MMC output voltage (voltage difference between the connected terminals)	kV

Note: If required, the gate signals can be viewed by entering 's:gate:x' in the $Variable\ Selection$ editor of ElmMmcvalve (Define Results for Simulation RMS/EMT...), where x is the transistor number (zero based). For a full-bridge configuration:

- 's:gate:0' is the gating signal for the first transistor;
- 's:gate:1' is the gating signal for the second transistor;
- 's:gate:2' is the gating signal for the third transistor;
- 's:gate:3' is the gating signal for the fourth transistor;

The same can be done with the submodule capacitor voltages for the *Detailed equivalent circuit* model: 's:Ucap:x' gives the capacitor voltage of submodule x.

3 References

[1] “Guide for the development of Models for HVDC Converters in a HVDC grid,” tech. rep., Cigre Working Group B4.57, December 2014.

[2] H. A. Saad, *MODÉLISATION ET SIMULATION D’UNE LIAISON HVDC DE TYPE VSC-MMC*. PhD thesis, ÉCOLE POLYTECHNIQUE DE MONTRÉAL, March 2015.

List of Figures

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