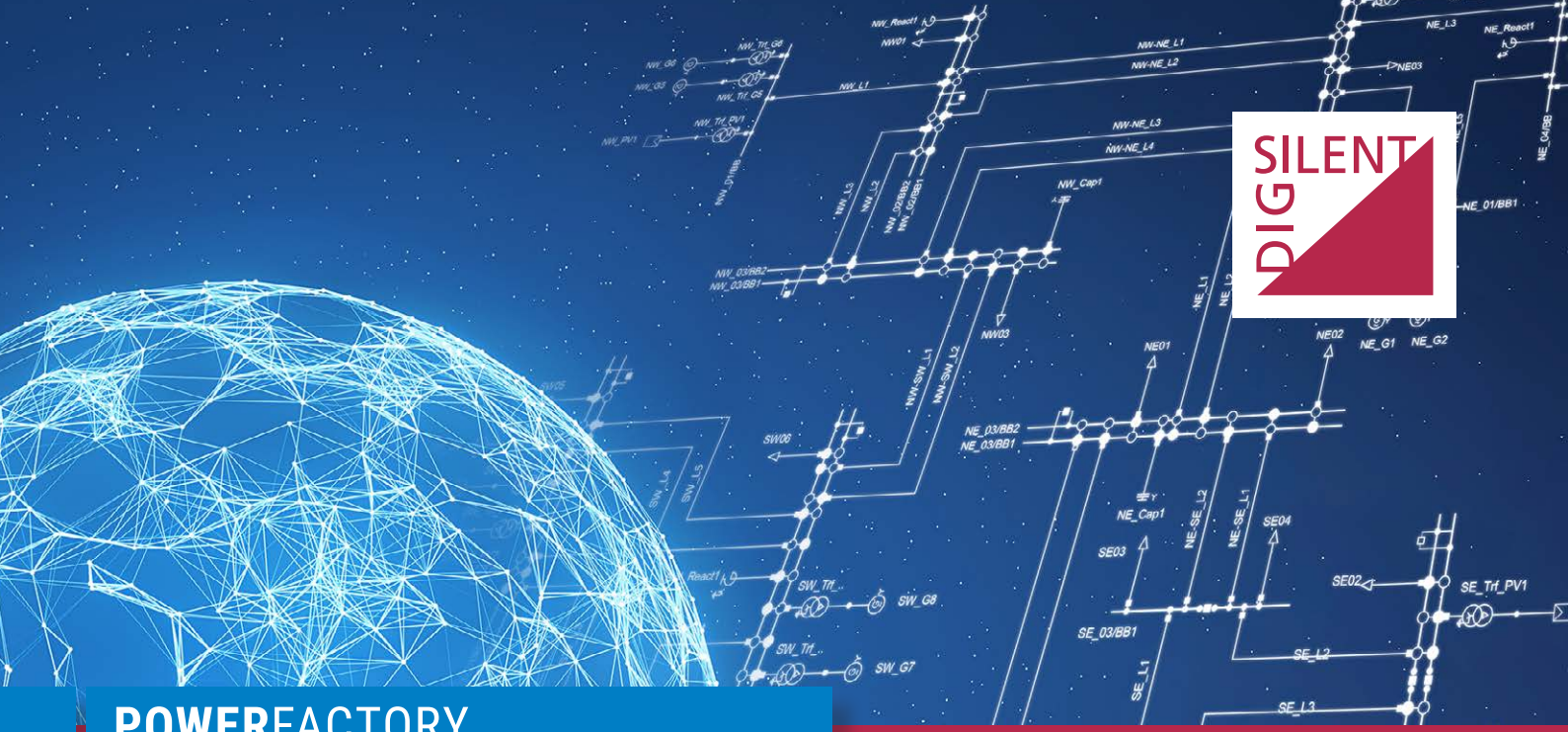

POWERFACTORY

PowerFactory 2021

Technical Reference

Clock

ElmClock

PF2021

POWER SYSTEM SOLUTIONS

MADE IN GERMANY

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Revision 1

Contents

1 General Description

The digital models need a clock input to trigger their calculations. The clock is a pulse generator which provides this signal. The clock model creates a signal with a clock pulse of a given duration and ratio Ton/Tp. Output signals are clock pulse and clock duration. The output for a clock signal with Ton/Tp=0.5 looks like:

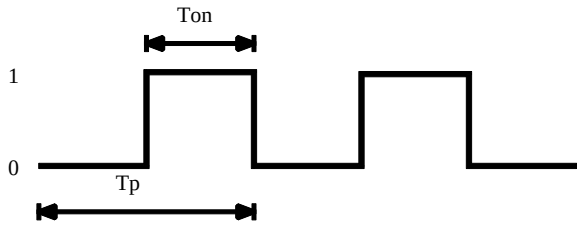

Figure 1.1: Clock Output

2 Dynamic Simulation

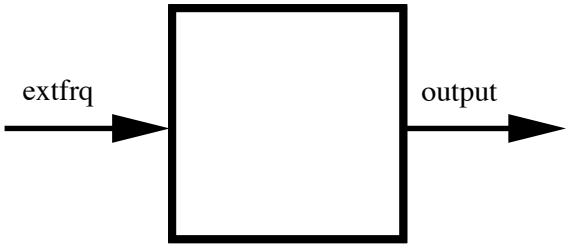

Figure 2.1: Clock Signals

Used Clock Frequency The *extfrq* signal input can be used to set the clock frequency. This is useful if the clock frequency is to be changed during simulation. If a signal is connected to *extfrq* the clock frequency is set to *extfrq*, regardless of the frequency or period set in the dialog box. If *Use measurement Frequency* is enabled the clock frequency is set by the *Start Measurement* command which is used only for the input of measured signals with a data acquisition board.

In most configurations *Use measurement Frequency* is disabled, therefore the clock period (*Tp*) is required. Both, clock period or clock frequency can be entered, the corresponding quantity is calculated automatically.

Table 2.1: Frequency Source

Signal connected to extfrq	extfrq not connected	
	Use measurement Frequency disabled	Use measurement Frequency enabled
clock frequency is extfrq	clock frequency is set to the parameter clock frequency (cFreq) of the element	clock frequency is software frequency of the Start Measurement command

Note: For proper functionality of the clock it is required that the simulation step size is smaller than the clock period.

3 Example Configuration

The examples show two small configurations where the *Fast Fourier Transformation* model is used to perform a FFT analysis on a signal.The analyzed signal is created with the *Fourier Source* model. The clock signal for the FFT is generated by the digital clock.

In the example block diagram on the right the clock frequency is set by an external block.

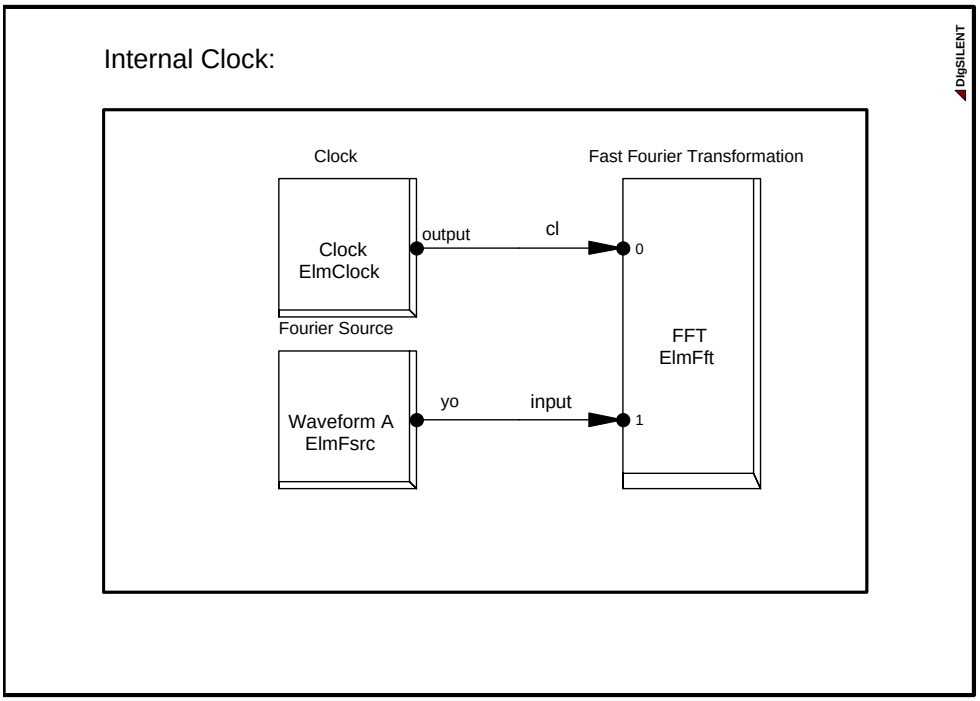

Figure 3.1: Block Diagram with internal clock

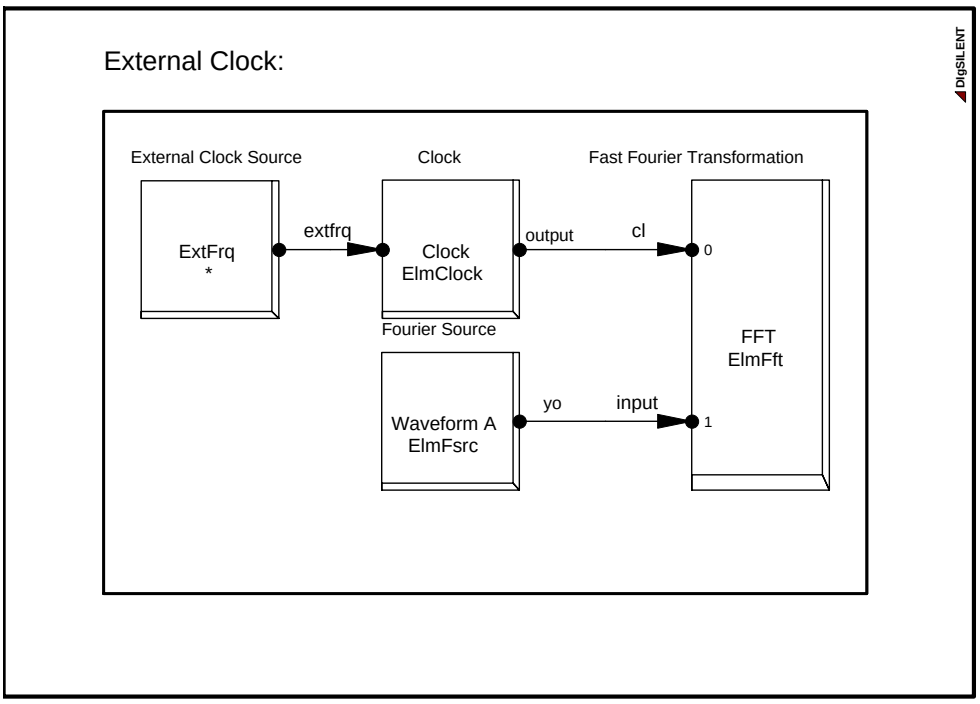

Figure 3.2: Block Diagramscwith external clock

Table 3.1: Example settings

	Object	Variable	Value
Simulation	*ComInc*	*dtemt* *dout_emt*	5.06e-6 s 5.06e-6 s
Clock	*ElmClock*	*cFreq* *tonTp*	12.8 kHz 0.5

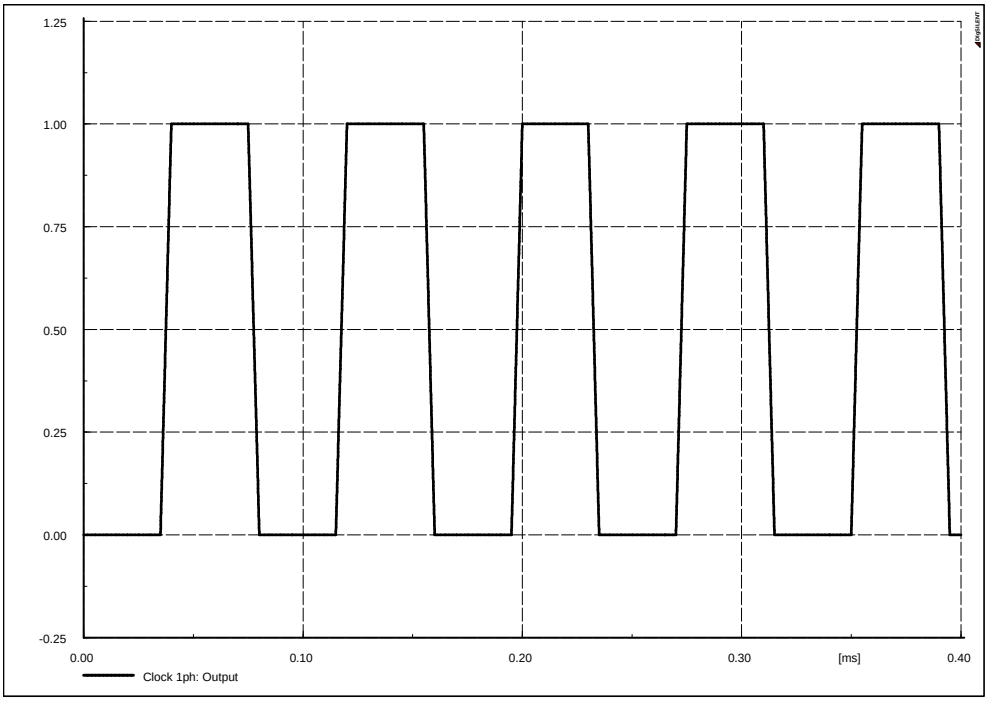

Figure 3.3: Plot clock output signal

A Parameter Definitions

Table A.1: Clock Parameters

Parameter	Description	Unit
loc_name	Name	
outserv	Out of service	
ctrlsim	Control simulation step size	
iopt_meas	Use measurement frequency	
cFreq	Clock frequency	kHz
Tp	Period	ms
tonTp	Ratio Ton/Tp	

B Signal Definitions

Table B.1: Input/Output signals

Name	Description	Unit	Type	Model
extfrq	External clock frequency	Hz	IN	RMS, EMT
output	Clock Signal		OUT	RMS, EMT

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