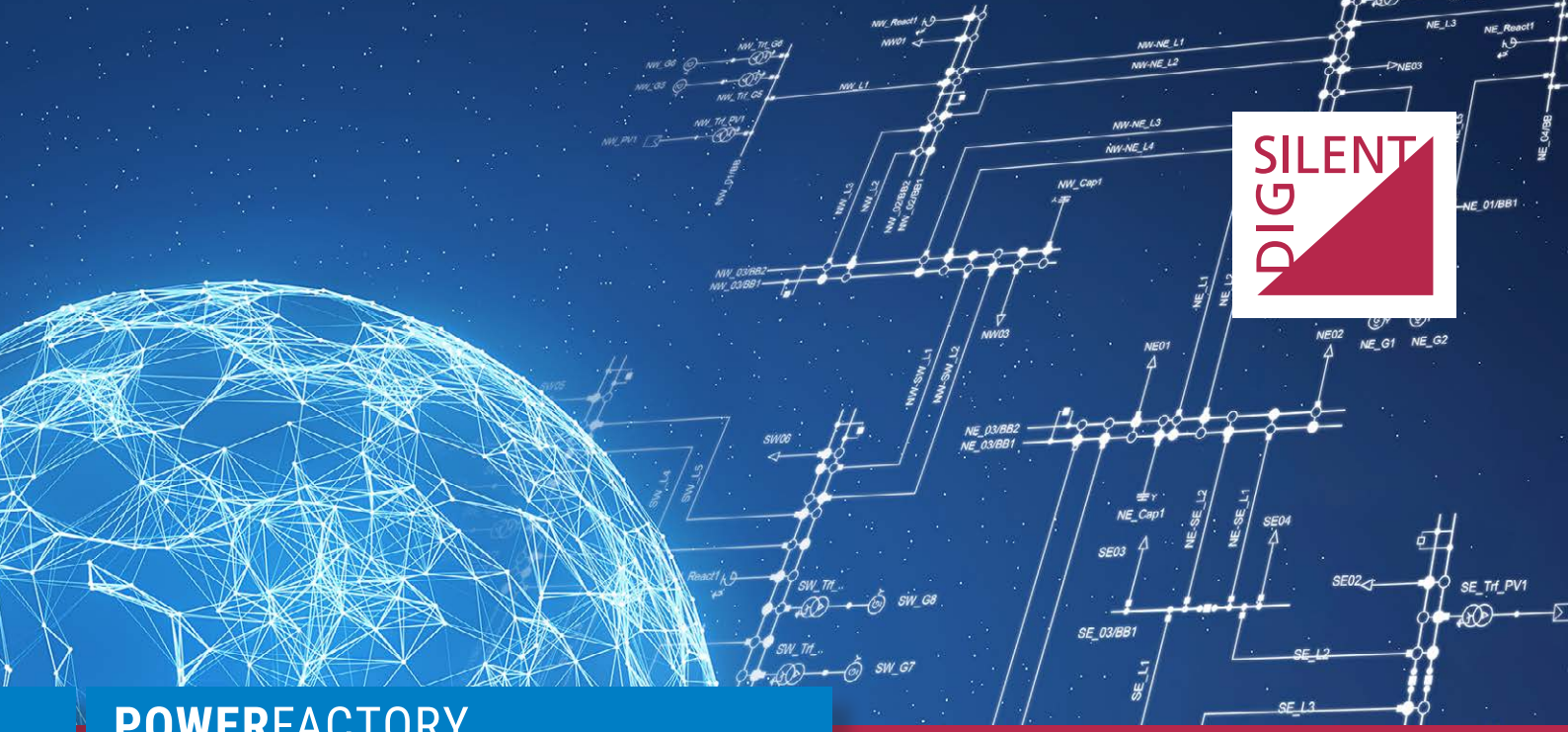

PowerFactory 2021

Technical Reference

DIgSILENT F59D Positive sequence overvoltage Gene

PF2021

POWER SYSTEM SOLUTIONS

MADE IN GERMANY

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1 F59D Positive sequence overvoltage

1.1 Intent

To simulate a set of positive sequence over voltage protective element.

1.2 Functionality

The *F59D Positive sequence overvoltage* generic relay model simulates a set of positive sequence over voltage elements. One inverse/definite time and 3 definite time elements are available.

1.3 Inputs

- One 3 phase VT (”Phase Vt” block, *StaVt* class).

1.4 Available Units

Measurement

- One 3phase sequence measurement element (”Measurement seq” block, *RMS Calculation* enabled, *Filter* disabled [RelMeasure class]).

Protective elements

- One inverse/definite time positive sequence overvoltage element (”U1>” block, *RelChar* class).
- Three definite time positive sequence overvoltage elements (”U1>>”, ”U1>>>” and ”U1>>>>” block, *RelUlim* class).

Output logic

- One relay trip element (”Output logic” block, *RelLogdip* class).

1.5 Outputs

- *yout* associated by default to any protective element trip.
- *inv_trip* associated by default to the inverse/definite time positive sequence overvoltage element trip (”U1>” block).
- *def_trip* associated by default to the definite time positive sequence overvoltage element trip(”U1>>”, ”U1>>>” and ”U1>>>>” block).

The output logic can be configured in the ”Logic” tab page of the ”Output Logic” block.