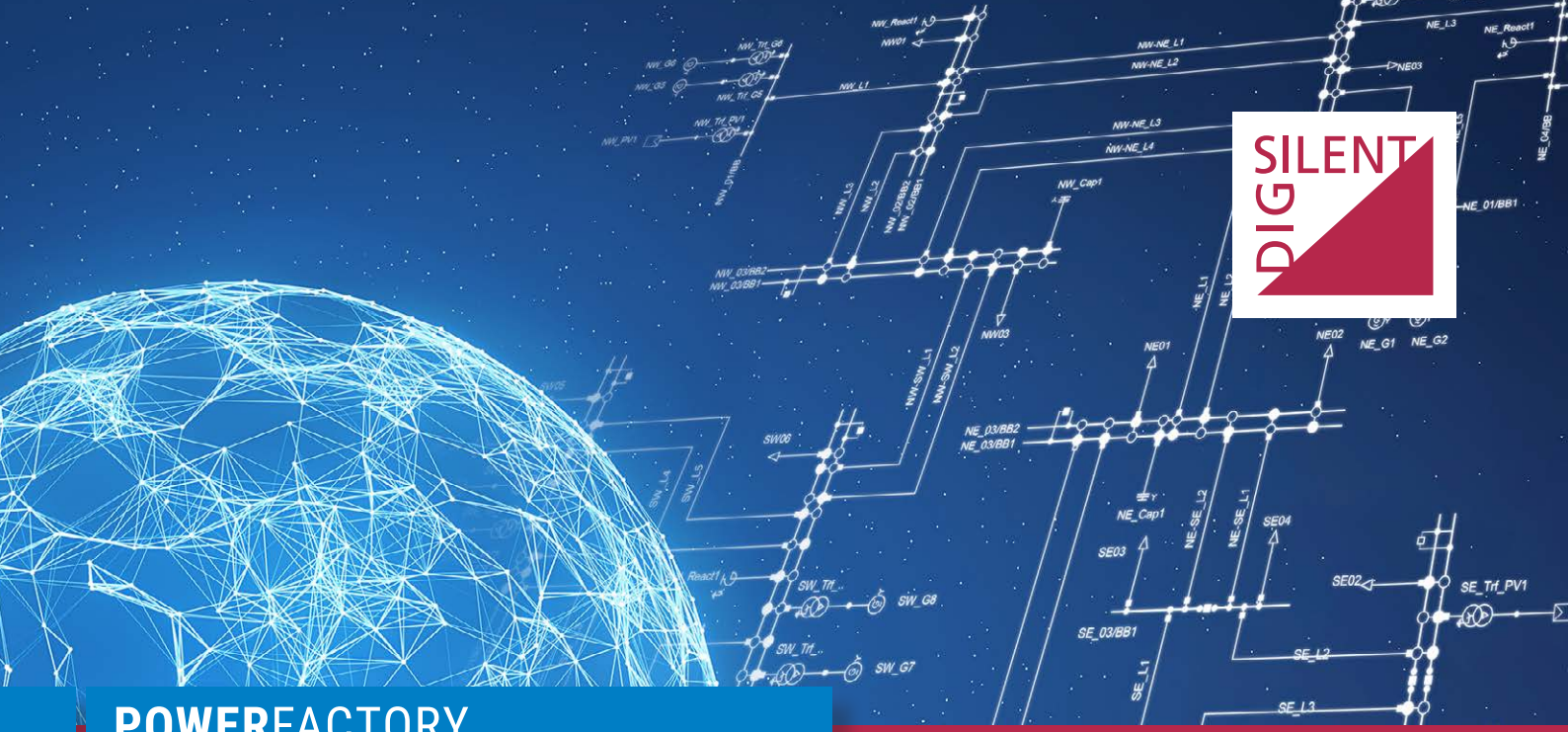

PowerFactory 2021

Technical Reference

DIgSILENT F67_F50_F51 Phase directional overcurren

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POWER SYSTEM SOLUTIONS

MADE IN GERMANY

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Contents

1 F67_F50_F51 Phase directional overcurrent

1.1 Intent

To simulate a simple set of inverse/definite time 3 phase directional overcurrent elements.

1.2 Functionality

The *F67_F50_F51 Phase Directional overcurrent* relay model simulates two directional phase inverse time and two directional phase definite time overcurrent elements.

The following inverse time trip and reset characteristics can be used in the two phase inverse time elements:

Trip characteristic	Reset characteristic
IEC Class A (Standard Inverse)	IEC Class A(Standard Inverse) reset
IEC Class B (Very Inverse)	IEC Class B(Very Inverse)reset
IEC Class C (Extremely Inverse)	IEC Class C(Extremely Inverse)reset
IEC Long Time Inverse	IEC Long Time Inverse reset
IEC Short Time Inverse	IEC Short Time Inverse reset
IEEE Moderately Inverse	IEEE Moderately Inverse reset
IEEE Inverse	IEEE Inverse reset
IEEE Very Inverse	IEEE Very Inverse reset
IEEE Extremely Inverse	IEEE Extremely Inverse reset
IEEE Short Time Inverse	IEEE Short Time Inverse reset
RD (Logarithmic) inverse	
RI inverse	
I2t	I2t reset
IAC Extremely Inverse	
IAC Inverse	
IAC Short Inverse	
IAC Very Inverse	
CO2 Short time inverse	
CO8 Long time inverse	

The reset characteristic can be enable or disabled by the user. The reset time delay can be set with a separated relay model parameter.
Each characteristic can be set with an user configurable minimum and a maximum trip time.

The directional logic is based on the angle comparison between the phase current vectors and the phase voltage vectors and on the active power or the reactive power evaluation. Each logic can be disabled by the user, if not present in the modeled relay, disabling the relevant relay model block. Please refer to the ”TechRef_directional.pdf” technical reference for more details about the directional logics.

Four relay input signals can be used to block the protective elements. Each protective element can be set to ignore the blocking input or to ignore the blocking input after that a user’s definable

time has expired after the element trip (”Blocking” tab page).

The output logic can be customized in the relay output logic block. Four relay input signals can be used to block the protective elements.

1.3 Inputs

- One 3 phase CT (”Phase Ct” block, *StaCt* class).
- Four blocking signals (*iblock_1* blocking the ”I>” element, *iblock_2* blocking the ”I>>” element, *iblock_3* blocking the ”I>>>” element, and *block_4* blocking the ”I>>>>” element).
- Six directional signals (*fwd_A*,*fwd_B*,*fwd_C*,*rev_A*,*rev_B*,*rev_C*).

1.4 Available Units

Measurement

- One 3phase measurement element (”Measurement” block, *RMS Calculation* enabled, *Filter* disabled [RelMeasure class]).

Protective elements

- Two inverse/definite time 3 phase overcurrent elements (”I>”, and ”I>>” block, [*RelToc* class]).
- Two definite time 3 phase overcurrent elements (”I>>>” and ”I>>>>” block [*RelIoc* class]).
- Two 3 phase overcurrent directional elements (”VI Angle dir” and ”Pcosphi, Qsinphi” block, [*RelDir* class]).

Output logic

- One relay trip element (”Output logic” block, *RelLogdip* class).

1.5 Outputs

- *yout* associated by default to any protective element trip.
- *y_s* associated by default to any protective element start.
- *toc_start* associate to an inverse time phase element start signal.
- *ioc_start* associate to a definite time phase element start signal.

The output logic can be configured in the ”Logic” tab page of the ”Output Logic” block.