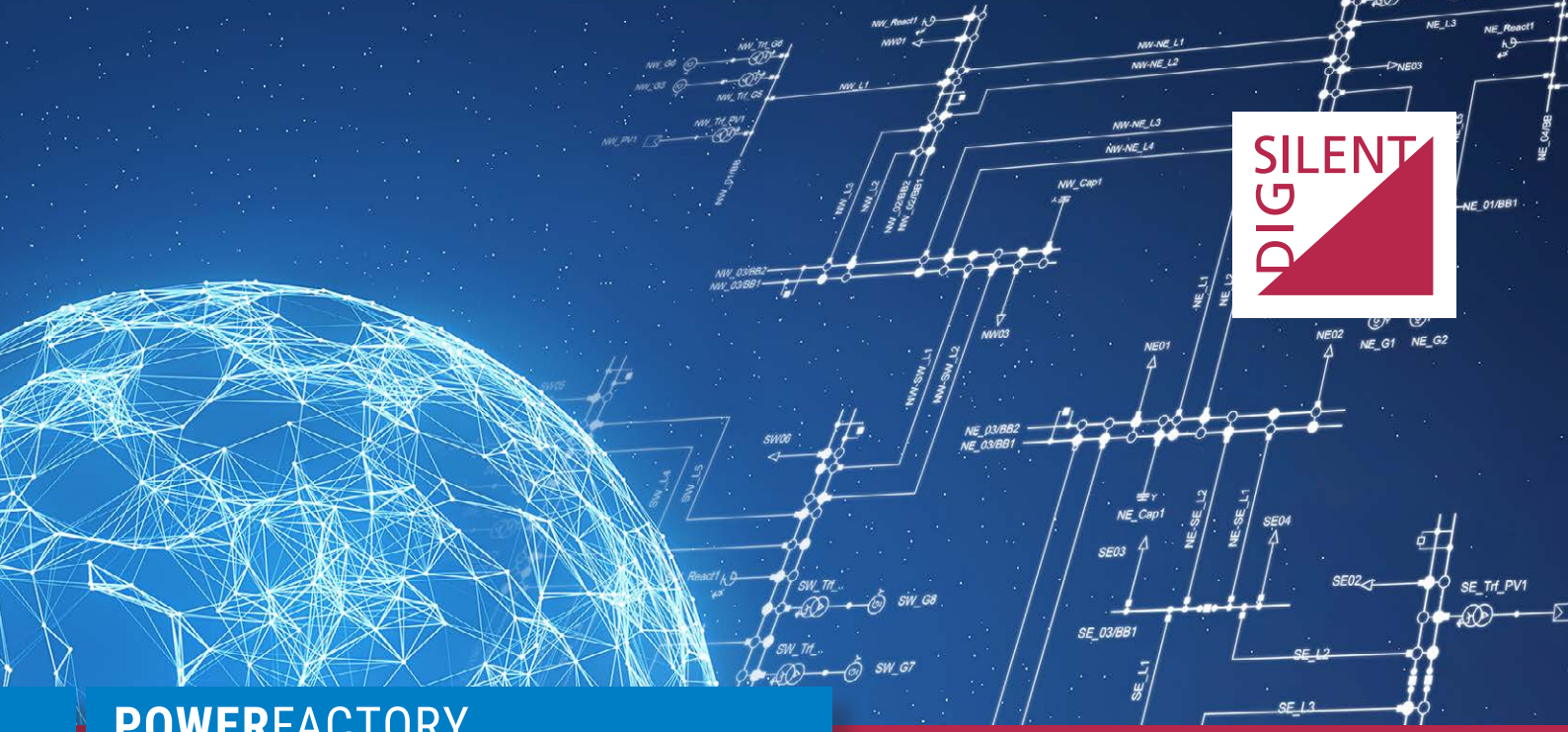

POWERFACTORY

PowerFactory 2021

Technical Reference

Pulse Generator

ElmPulsegen

PF2021

POWER SYSTEM SOLUTIONS

MADE IN GERMANY

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1 General Description

The *Pulse Generator* element in *PowerFactory* generates pulses for controlled modular multi-level converters.

The *Pulse Generator* is a purely EMT model and is described in chapter 2.

2 EMT simulation

As an input, a sinusoidal reference signal is required which is used for generating the output pulses. For PWM modulation and when the option *Precise crossing time* is selected, a natural sampling method is used when generating the pulses.

The *ElmPulsegen* element in *PowerFactory* can be configured to run as a sampled system, updating the gate output signals once in every defined sampling period. For typical MMC applications this option reduces the required simulation time and is recommended to be used when a higher number of *ElmMmcvalve* elements are controlled by it.

The blocking of the MMC is implemented in the MMC valve element (*ElmMmcvalve*). The usage of the blocking signal in the pulse generator is not obligatory. If used, the simulation performance during blocking is increased due to the fact that no switching events are executed in this case. The same block signal needs to be connected to the *ElmMmcvalve* and *ElmPulsegen*.

The size of the output signals array depends on the selected number of valves (submodules) and the valve type selected. For each half-bridge valve there are two signals and for each full-bridge valve there are four signals.

2.1 PS PWM

For the phase-shifting PWM one carrier signal is internally generated per sub-module. For a half-bridge configuration, the carriers are phase-shifted by an angle of $360°/nvalves$. For a full-bridge converter, carriers are phase-shifted by an angle of $180°/nvalves$.

2.1.1 Half-bridge configuration

In Figure 2.1 the carriers are shown for a system of four half-bridge submodules with a frequency of $150Hz$, with values from -1 to 1 with starting value of -1 in descending order. In Figure 2.2 the carriers are shown for a system of four half-bridge submodules with a frequency of $150Hz$, with values from 0 to 1 with starting value of 0 in ascending order.

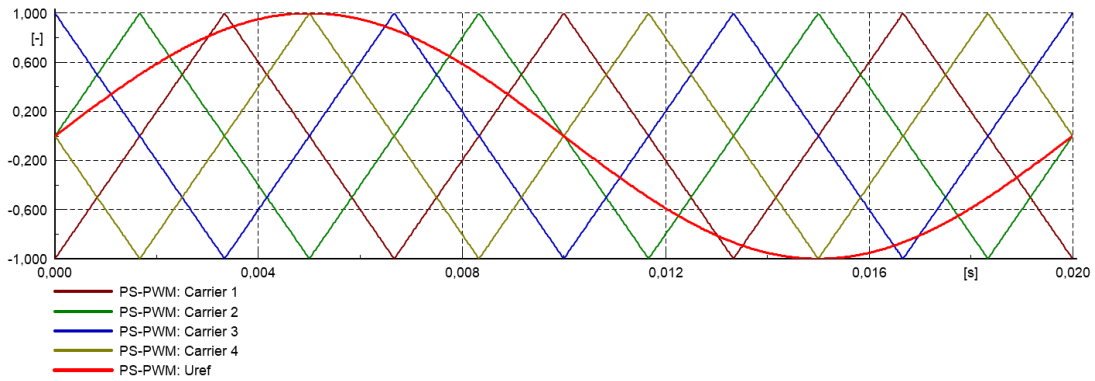

Figure 2.1: Phase-shifting carriers for a half-bridge system in descending order

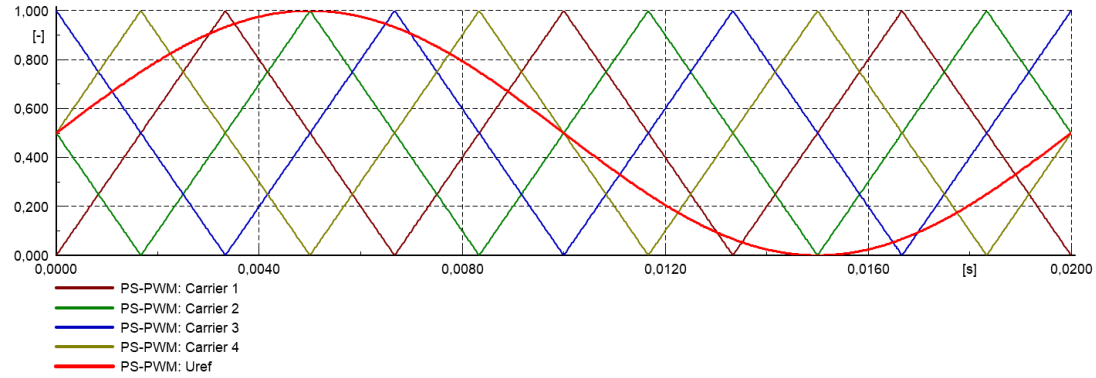

Figure 2.2: Phase-shifting carriers for a half-bridge system in ascending order

2.1.2 Full-bridge configuration

For the full-bridge configuration a unipolar switching can be used where the second reference voltage is automagically created by mirroring the $Uref$ input signal.

In Figure 2.3 the carriers are shown for a system of four full-bridge submodules with a frequency of $150Hz$, with values from -1 to 1 with starting value of -1 in descending order.

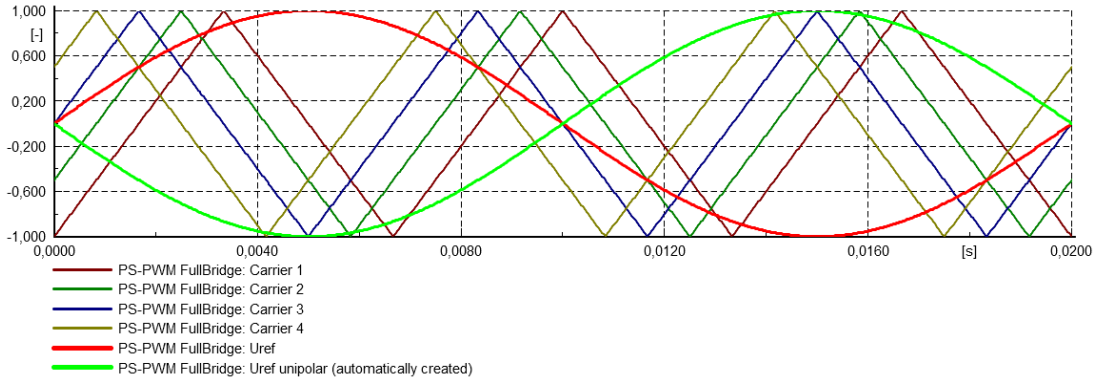

Figure 2.3: Phase-shifting carriers for a full-bridge system and unipolar switching

Another option is to base the switching on two input signals $Uref$ and $Urefadd$. An example of such a system is shown in Figure 2.4.

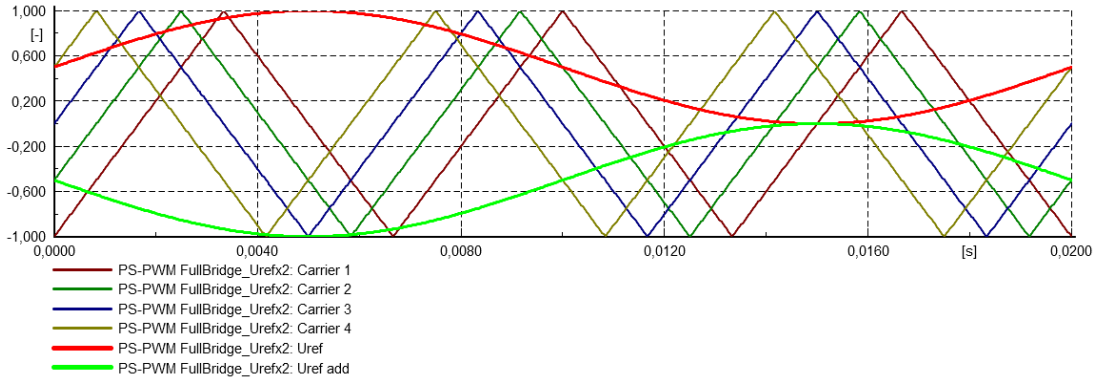

Figure 2.4: Phase-shifting carriers for a full-bridge system and unipolar switching

2.2 PD PWM

For the phase-disposition PWM one carrier signal is internally generated per sub-module.

2.2.1 Half-bridge configuration

In Figure 2.5 the carriers are shown for a system of four half-bridge submodules with a frequency of $150Hz$, with values from 0 to 1.

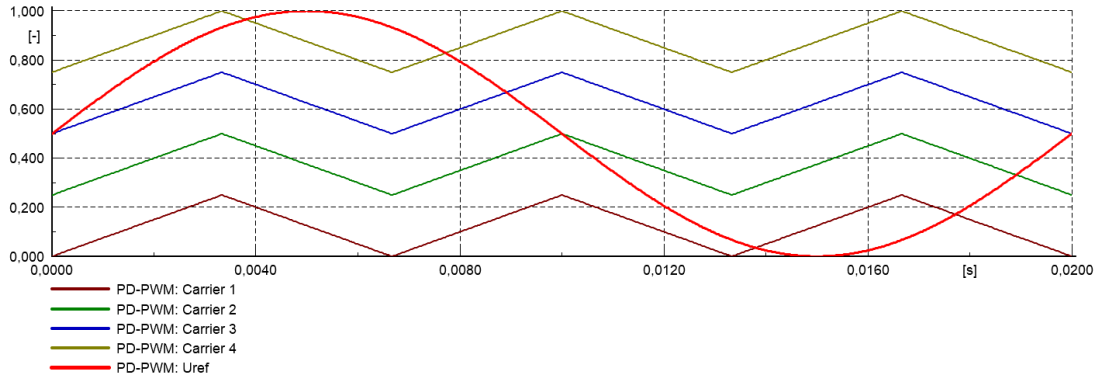

Figure 2.5: Phase disposition carriers for a half-bridge system

2.2.2 Full-bridge configuration

For the full-bridge configuration a unipolar switching can be used where the second reference voltage is automagically created by mirroring the $Uref$ input signal. In Figure 2.6 the carriers are shown for a system of four full-bridge submodules with a frequency of $150Hz$, with values from 0 to 1.

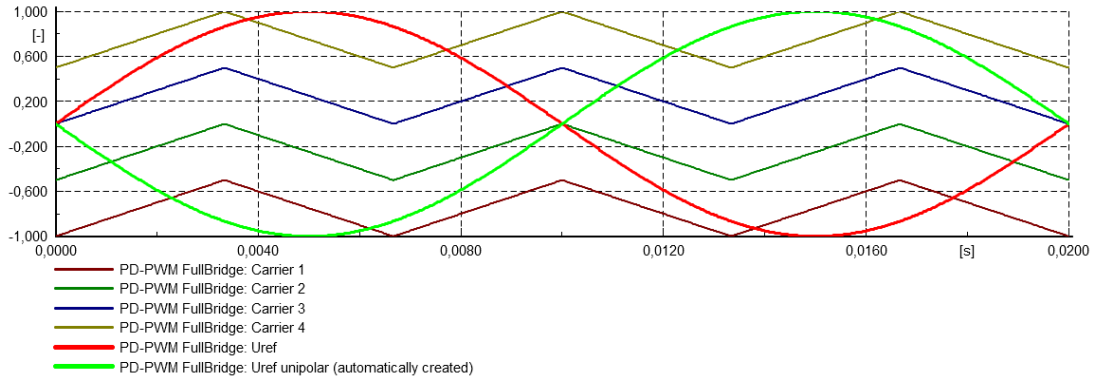

Figure 2.6: Phase disposition carriers for a full-bridge system

2.3 NLC

For the nearest level control, the input signal $Uref$ is shifted and stretched so that when it is rounded to integer values, it directly represents the number of submodules on at any given time.

The sorting option requires the input of an array signal $Ucap$ consisting of the capacitor voltages values. The transistors are sorted depending on the values of $Ucap$. The input signal $Iarm$ is also required for the sorting algorithm. If the value of the arm current $Iarm$ is positive, the transistors are sorted in ascending order. Else, if the value is negative, the transistors are sorted in descending order.

2.3.1 Half-bridge configuration

In Figure 2.7 the number of the submodules with ON state for a system of four submodules is shown together with the modified input signal from which the ON-states are determined.

The input signal $Uref$ is shifted and stretched so that the lower limit is 0 and the upper limit corresponds to the number of submodules. The internal signal $Urefmodified$ is then rounded to integer values and it directly represents the number of submodules on at any given time.

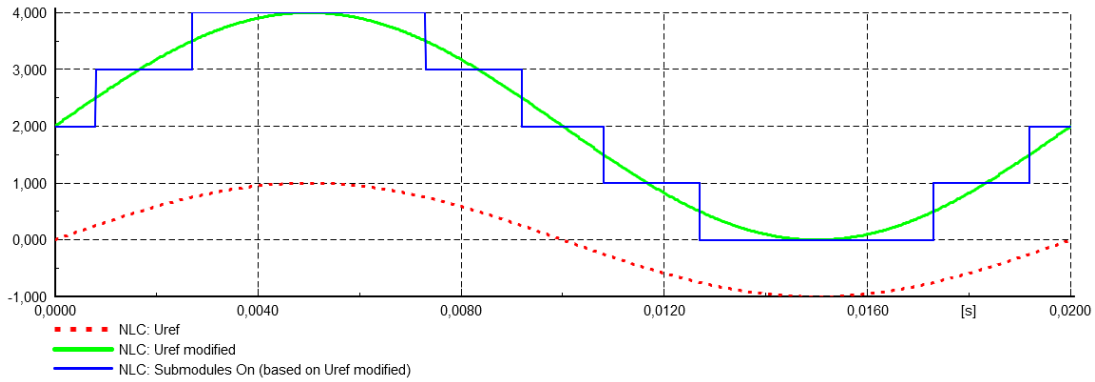

Figure 2.7: NLC: Number of turned on submodules

2.3.2 Full-bridge configuration

For the full-bridge configuration, positive $Uref$ input signal turns the submodules on with positive voltage polarity and negative $Uref$ input signal turns the submodules on with negative voltage polarity.

The input signal $Uref$ is shifted and stretched so that the lower limit corresponds to the negative number of the submodules and the upper limit corresponds to the number of submodules. The internal signal $Urefmodified$ is then rounded to integer values.

In Figure 2.8 the number of the submodules with ON state for a system of five submodules is shown together with the modified input signal from which the ON-states are determined.

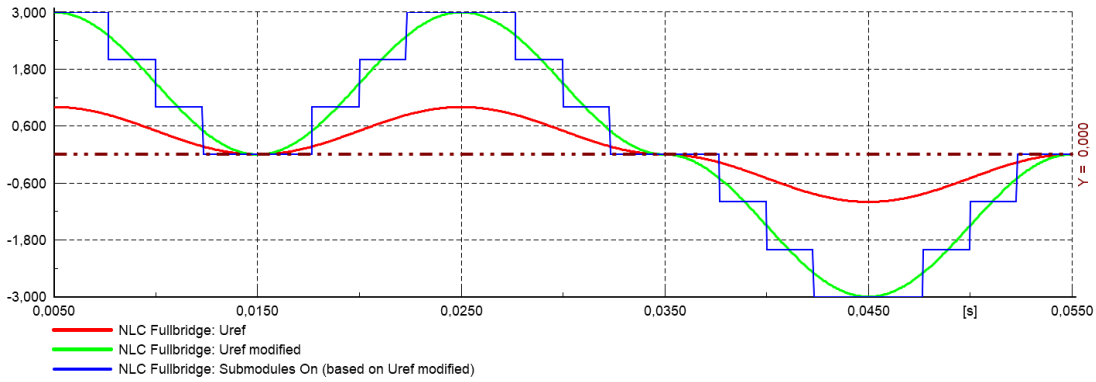

Figure 2.8: NLC: Number of turned on submodules for full-bridge configuration

2.4 Input and output signals

Table 2.1: Input definition

Input Signal	Symbol	Description	Unit
Uref		Sinusoidal reference signal	
Urefadd		Additional reference signal (only for PS-PWM Full-bridge with enabled option 'Use additional reference signal')	
Ucap		Array of capacitor voltages (only for NLC with sorting)	
Iarm		Arm current (only for NLC with sorting)	
block		Blocking signal (optional for performance improvement)	

Table 2.2: Output definition

Output Signal	Symbol	Description	Unit
gate		Array of gate signals	

Note: If required, the gate signals can be viewed by entering 's:gate:x' in the $Variable\ Selection$ editor of ElmPulsegen (Define Results for Simulation RMS/EMT...), where x is the gate number (zero based). For a half-bridge configuration:

- 's:gate:0' is the gating signal for the first transistor of the first submodule;
- 's:gate:1' is the gating signal for the second transistor of the first submodule;

- 's:gate:2' is the gating signal for the first transistor of the second submodule;
- 's:gate:3' is the gating signal for the second transistor of the second submodule;

Note: If required, the carrier signals can be viewed by entering 's:__SIG:x' in the $Variable\ Selection$ editor of ElmPulsegen (Define Results for Simulation RMS/EMT...), where x is the carrier number (zero based). For an ElmPulsegen with four submodels:

- 's:__SIG:0' is the first carrier signal;
- 's:__SIG:1' is the second carrier signal;
- 's:__SIG:2' is the third carrier signal;
- 's:__SIG:3' is the fourth carrier signal.

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