



POWERFACTORY

PowerFactory 2021

Technical Reference

DigSILENT F87L Line Differential (angular 1 phase) Ge

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POWER SYSTEM SOLUTIONS
MADE IN GERMANY

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1 F87L Line Differential (angular 1 phase)

1.1 Intent

To simulate the single phase current angle comparison differential feature for line protection.

1.2 Functionality

The *F87L Line differential (angular 1 phase)* generic relay model simulates a single current angle comparison differential element with differential restraint region angle and radius. An unrestrained differential threshold is also available. The differential trip can be set with a configurable time delay.

The phase current vectors are summed together to obtain an equivalent vector which is used, together with the signal received from the remote CT, by the differential element.

1.3 Inputs

- Two 3 phase CTs ("Phase Ct", and "Phase Remote Ct" block, *StaCt* class).

1.4 Available Units

Measurement

- Two 3phase measurement elements ("Measurement", and "Remote Measurement" block, *RMS Calculation* enabled, *Filter* disabled [*RelMeasure* class]).
- One single phase measurement element ("Differential RMS Meas" block, *RMS Calculation* enabled, *Filter* disabled [*RelMeasure* class]).

The remote line end measurement data are provided by the "Phase Remote Ct" slot which contains the reference to a CT located at the other side of the line.

Protective elements

- Two vector summation elements ("Phase current summation", and "Phase remote current summation" block, [*RelLogdip* class]).
- A differential element with *Type* equal to *1ph Phase comparison* ("Differential" block, [*RelBiasidiff* class]).

Output logic

- One relay trip element ("Output logic" block, *RelLogdip* class).

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1.5 Outputs

- *yout* associated by default to the differential element trip (any phase).
- *y_s* associated by default to the differential element trip (any phase). Its behavior is identical to the *yout* signal and has been added to guarantee compatibility with the *F79 (reclosing)* generic relay.

The output logic can be configured in the "Logic" tab page of the "Output Logic" block.