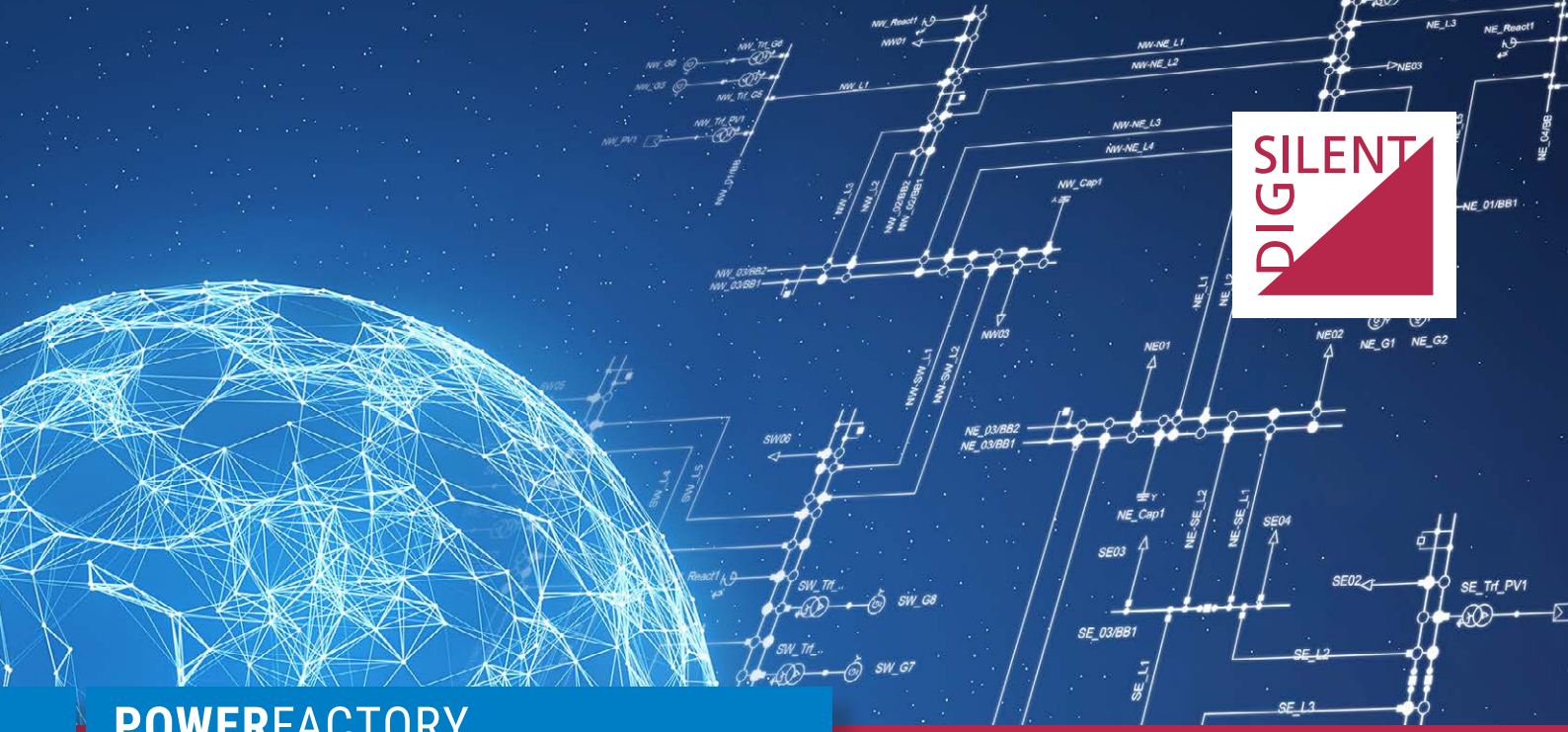

POWERFACTORY

PowerFactory 2021

Technical Reference

DIgSILENT F67N_F50N_F51N Neutral directional overc

PF2021

POWER SYSTEM SOLUTIONS

MADE IN GERMANY

Publisher:
DIgSILENT GmbH
Heinrich-Hertz-Straße 9
72810 Gomaringen / Germany
Tel.: +49 (0) 7072-9168-0
Fax: +49 (0) 7072-9168-88
info@digsilent.de

Please visit our homepage at:
https://www.digsilent.de

November 15, 2019
PowerFactory 2021
Revision 924

Contents

1 F67N_F50N_F51N Neutral directional overcurrent 1

1.1 Intent 1

1.2 Functionality 1

1.3 Inputs 2

1.4 Available Units 2

1.5 Outputs 2

1 F67N_F50N_F51N Neutral directional overcurrent

1.1 Intent

To simulate a set of inverse/definite time neutral/ground directional overcurrent elements.

1.2 Functionality

The *F67N_F50N_F51N Neutral directional overcurrent* relay model simulates one neutral/ground directional inverse time and two neutral/ground directional definite time overcurrent elements.

The following inverse time trip and reset characteristics can be used in the ground directional inverse time element:

Trip characteristic	Reset characteristic
IEC Class A (Standard Inverse)	IEC Class A(Standard Inverse) reset
IEC Class B (Very Inverse)	IEC Class B(Very Inverse)reset
IEC Class C (Extremely Inverse)	IEC Class C(Extremely Inverse)reset
IEC Long Time Inverse	IEC Long Time Inverse reset
IEC Short Time Inverse	IEC Short Time Inverse reset
IEEE Moderately Inverse	IEEE Moderately Inverse reset
IEEE Inverse	IEEE Inverse reset
IEEE Very Inverse	IEEE Very Inverse reset
IEEE Extremely Inverse	IEEE Extremely Inverse reset
IEEE Short Time Inverse	IEEE Short Time Inverse reset
RD (Logarithmic) inverse	
RI inverse	
I2t	I2t reset
IAC Extremely Inverse	
IAC Inverse	
IAC Short Inverse	
IAC Very Inverse	
CO2 Short time inverse	
CO8 Long time inverse	

The reset characteristic can be enable or disabled by the user. The reset time delay can be set with a separated relay model parameter.
Each characteristic can be set with an user configurable minimum and a maximum trip time.

The directional logic is base on the angle comparison between the zero sequence current vector and the zero sequence voltage vector or on the active or reactive power evaluation. Each logic can be disabled by the user, if not present in the modeled relay, disabling the relevant relay model block. Please refer to the ”TechRef_directional.pdf” technical reference for more details about the directional logics.

Three relay input signals can be used to block the protective elements. Each protective element can be set to ignore the blocking input or to ignore the blocking input after that a user’s definable

time has expired after the element trip (”Blocking” tab page).

The output logic can be customized in the relay output logic block. Three relay input signals can be used to block the protective elements.

1.3 Inputs

- One 3 phase/single phase CT (”Ct” block, *StaCt* class).
- Three blocking signals (*iblock_1* blocking the ”Ig>” element, *iblock_2* blocking the ”Ig>>” element, and *iblock_3* blocking the ”Ig>>>” element).
- Two directional signals (*fwd*,*rev*).

1.4 Available Units

Measurement

- One single phase measurement element (”Measurement” block, *RMS Calculation* enabled, *Filter* disabled [RelMeasure class]).

Protective elements

- One inverse/definite time directional ground overcurrent element (”Ig>” block, [*RelToc* class]).
- Two definite time directional ground overcurrent elements (”Ig>>” and ”Ig>>>” block [*RelIoc* class]).
- Two single phase overcurrent directional elements (”V0I0 Angle dir” and ”Pcosphi, Qsinphi” [*RelDir* class]).

Output logic

- One relay trip element (”Output logic” block, *RelLogdip* class).

1.5 Outputs

- *yout* associated by default to any protective element trip.
- *y_s* associated by default to any protective element start.
- *toc_start* associate to the inverse time ground element start signal.
- *ioc_start* associate to a definite time ground element start signal.

The output logic can be configured in the ”Logic” tab page of the ”Output Logic” block.