

# PowerFactory 2021

**Technical Reference** 

Schneider SEPAM x4x

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## 1 Model information

Manufacturer Schneider

Model SEPAM x4x

**Variants** The Schneider SEPAM x4x PowerFactory relay models simulate the protective features present in the Schneider SEPAM 40 relay family.

# 2 General description

The Sepam series 40 family of protection and metering units is designed for the operation of machines and electrical distribution networks of industrial installations and utility substations for all levels of voltage. The Sepam series 40 family consists of the following simple, high-performing solutions, suited to demanding applications that call for current and voltage metering:

- S40 (substation protection, I and U measurement).
- T40 (transformer protection, I and U measurement).
- G40 (generator protection, I and U measurement).
- S41 (substation protection, I and U measurement, Directional earth fault)
- M41 (motor protection, Directional earth fault).
- S42 (substation protection, I and U measurement, Directional earth fault and phase overcurrent).
- T42 (transformer protection, I and U measurement, Directional earth fault and phase overcurrent).

The PowerFactory Schneider SEPAM x4x relay models are monolithic models and simulate most of the protective features available in the relays.

The following model versions are available:

- SEPAM G40
- SEPAM M41
- SEPAM S40
- SEPAM S4x
- SEPAM T4x
- SEPAM x4x

Please notice that the x4x PowerFactory relay model represents a generic model supporting all the SEPAM G40, M41, S40, S41, S42, T40, and T42 relay main features. The features which are not available in the specific SEPAM relay model the user is going to simulate must be manually disabled.

The S4x PowerFactory relay model represents a generic model which simulate the S41 and S42 relay main features.

The model implementations have been based on the information available in the relay technical brochure and manual [1].

#### 3 Supported features

## 3.1 Measurement and acquisition

It represents the interface between the power system and the relay protective elements.

The phase currents flowing in the power system are converted by a block which simulates a 3 phase CT, by a block which simulates a 3 phase Vt, and by a block which models a single phase CT detecting the earth current; the secondary currents are then measured in the relay model by six measurement elements which simulate the digital sampling of the relay.

#### 3.1.1 Available elements and input signals

The *Measurement and acquisition* feature consists of the following elements:

- One 3 phase current transformer ("Ct-3P" block).
- One neutral current transformer ("Core CT" block).
- One 3 phase voltage transformer ("Vt" block).
- One 3 phase measurement element ("Measure Ph" block).
- One 3 phase sequence components measurement element ("Measure Seq" block).
- One 3 phase measurement element calculating the phase-phase voltages ("Measure Delta V" block).
- One single phase neutral current measurement element ("Meas. Earth" block).
- One 3phase 2<sup>nd</sup> harmonic measurement element ("Measure 2nd harmonic" block).
- One frequency measurement element ("Meas Freq" block).

The following relay input signals are available in the G40, M41, S40, S4x, T4x, and x4x relay model to block the protective elements:

- Block 5051 1A controlling the "50/51 1A DT" "I> DT" "50/51 1A def reset" "50/51 1A idmt reset" "50/51 1B DT" "I> DT" "50/51 1B def reset" "50/51 1B idmt reset" block.
- Block 5051 2A controlling "50/51 2A DT" "I> DT" "50/51 2A def reset" "50/51 2A idmt reset" "50/51 2B DT" "I> DT" "50/51 2B def reset" "50/51 2B idmt reset" block.

- Block 50N51N 1A controlling "50N/51N 1A def reset" "50N/51N 1A idmt reset" "50N/51N 1B idmt reset"
- Block 50N51N 2A controlling "50N/51N 2A def reset" "50N/51N 2A idmt reset" "50N/51N 2B def reset" "50N/51N 2B idmt reset"

#### 3.1.2 Functionality

The "Ct-3P" and the "Core Ct" block represent ideal CTs. Using the CT default configuration the current at the primary side are converted to the secondary side using the CT ratio. The CT saturation and/or its magnetizing characteristic are not considered. Please set the "Detailed Model" check box in the "Detailed Data" tab page of the CT dialog and insert the data regarding the CT burden, the CT secondary resistance and the CT excitation parameter if more accurate simulation results are required.

The input current and voltage values are sampled by the measurement block at 36 samples/cycle. The values are processed by a DFT filter, operating over a cycle, which then calculates the voltage and current RMS values used by the protective elements.

#### 3.1.3 Data input

The CT secondary rated current (1 or 5 A) value and the VT rated voltage value must be set in every measurement blocks.

If no core CT is available please select the 3 phases CT also in the "Core Ct" slot: the earth current will be calculated assuming that an Holmgreen's connection of the phases is used.

## 3.2 Protective elements

A set of inverse time and definite time overcurrent elements, voltage and frequency elements is modeling the relay protective functions. All the inverse characteristics available in the relay are available in the inverse time overcurrent model blocks.

#### 3.2.1 Available Units

#### **SEPAM G40**

- Four inverse time phase overcurrent elements with a definite time reset characteristic ("50/51 1A def reset", "50/51 1B def reset", "50/51 2A def reset", and "50/51 2B def reset" block).
- Four inverse time phase overcurrent elements with an inverse time reset characteristic ("50/51 1A idmt reset", "50/51 1B idmt reset", "50/51 2A idmt reset", and "50/51 2B idmt reset" block).
- Four definite time phase overcurrent elements with a definite time reset characteristic ("50/51 1A DT", "50/51 1B DT", "50/51 2A DT", and "50/51 2B DT" block).
- One voltage restrained inverse time phase overcurrent element with a definite time reset characteristic ("50V/51V def reset" block).

- One voltage restrained inverse time phase overcurrent element with an inverse time reset characteristic ("50V/51V idmt reset" block).
- One voltage restrained definite time phase overcurrent element with a definite time reset characteristic ("50V/51V DT" block).
- Four inverse time neutral overcurrent elements with a definite time reset characteristic ("50N/51N 1A def reset", "50N/51N 1B def reset", "50N/51N 2A def reset", and "50N/51N 2B def reset" block).
- Four inverse time neutral overcurrent elements with an inverse time reset characteristic ("50N/51N 1A idmt reset", "50N/51N 1B idmt reset", "50N/51N 2A idmt reset", and "50N/51N 2B idmt reset" block).
- Two negative sequence inverse time elementS ("46 1" and "46 2" block).
- Two thermal overload elements ("Thermal K", "49 A" and "49 B" block). The "Thermal K" block allows setting the percentage of I2 used in the thermal image calculation.
- One forward direction active overpower with definite time trip characteristic element ("P Fwd" block).
- One reverse direction active overpower with definite time trip characteristic element ("P Rev" block).
- One forward direction reactive overpower with definite time trip characteristic element ("Q Fwd" block).
- One reverse direction reactive overpower with definite time trip characteristic element ("Q Rev" block).
- Two phase-phase undervoltage elements ("27 1", "27 2" block).
- Two phase-phase overvoltage elements ("59 1" and "59 2" block).
- One phase-neutral undervoltage element ("27S" block).
- Two zero sequence overvoltage elements ("59N 1" and "59N 2" block).
- One negative sequence overvoltage element ("47" block).
- Four under frequency elements ("81L 1", "81L 2", "81L 3", and "81L 4" block).
- Two over frequency elements ("81H 1" and "81H 2" block).

#### **SEPAM M41**

- Four inverse time phase overcurrent elements with a definite time reset characteristic ("50/51 1A def reset", "50/51 1B def reset", "50/51 2A def reset", and "50/51 2B def reset" block).
- Four inverse time phase overcurrent elements with an inverse time reset characteristic ("50/51 1A idmt reset", "50/51 1B idmt reset", "50/51 2A idmt reset", and "50/51 2B idmt reset" block).
- Four definite time phase overcurrent elements with a definite time reset characteristic ("50/51 1A DT", "50/51 1B DT", "50/51 2A DT", and "50/51 2B DT" block).
- Four inverse time neutral overcurrent elements with a definite time reset characteristic ("50N/51N 1A def reset", "50N/51N 1B def reset", "50N/51N 2A def reset", and "50N/51N 2B def reset" block).

- Four inverse time neutral overcurrent elements with an inverse time reset characteristic ("50N/51N 1A idmt reset", "50N/51N 1B idmt reset", "50N/51N 2A idmt reset", and "50N/51N 2B idmt reset" block).
- Two directional inverse time neutral overcurrent elements with a definite time reset characteristic ("67N 1 def reset", and "67N 2 def reset" block).
- Two directional inverse time neutral overcurrent elements with an inverse time reset characteristic ("67N 1 idmt reset", and "67N 2 idmt reset" block).
- One phase undercurrent element ("37" block).
- One forward direction active overpower with definite time trip characteristic element ("P Fwd" block).
- One reverse direction active overpower with definite time trip characteristic element ("P Rev" block).
- One forward direction reactive overpower with definite time trip characteristic element ("Q Fwd" block).
- One reverse direction reactive overpower with definite time trip characteristic element ("Q Rev" block).
- Two negative sequence inverse time elementS ("46 1" and "46 2" block).
- Two thermal overload elements ("Thermal K", "49 A" and "49 B" block). The "Thermal K" block allows setting the percentage of I2 used in the thermal image calculation.
- Two phase-phase undervoltage elements ("27 1", "27 2" block).
- Two phase-phase overvoltage elements ("59 1" and "59 2" block).
- One phase-neutral undervoltage element ("27S" block).
- One "remanent" voltage overvoltage element monitoring the phase A-phase B voltage ("27R" block).
- Two zero sequence overvoltage elements ("59N 1" and "59N 2" block).
- One negative sequence overvoltage element ("47" block).
- Two positive sequence undervoltage elements ("27D/47 1" and "27D/47 2" block).
- Four under frequency elements ("81L 1", "81L 2", "81L 3", and "81L 4" block).
- Two over frequency elements ("81H 1" and "81H 2" block).

#### SEPAM S40

- Four inverse time phase overcurrent elements with a definite time reset characteristic ("50/51 1A def reset", "50/51 1B def reset", "50/51 2A def reset", and "50/51 2B def reset" block).
- Four inverse time phase overcurrent elements with an inverse time reset characteristic ("50/51 1A idmt reset", "50/51 1B idmt reset", "50/51 2A idmt reset", and "50/51 2B idmt reset" block).
- Four definite time phase overcurrent elements with a definite time reset characteristic ("50/51 1A DT", "50/51 1B DT", "50/51 2A DT", and "50/51 2B DT" block).

- Four inverse time neutral overcurrent elements with a definite time reset characteristic ("50N/51N 1A def reset", "50N/51N 1B def reset", "50N/51N 2A def reset", and "50N/51N 2B def reset" block).
- Four inverse time neutral overcurrent elements with an inverse time reset characteristic ("50N/51N 1A idmt reset", "50N/51N 1B idmt reset", "50N/51N 2A idmt reset", and "50N/51N 2B idmt reset" block).
- Two negative sequence inverse time elementS ("46 1" and "46 2" block).
- Two phase-phase undervoltage elements ("27 1", "27 2" block).
- Two phase-phase overvoltage elements ("59 1" and "59 2" block).
- One phase-neutral undervoltage element ("27S" block).
- Two zero sequence overvoltage elements ("59N 1" and "59N 2" block).
- One negative sequence overvoltage element ("47" block).
- Four under frequency elements ("81L 1", "81L 2", "81L 3", and "81L 4" block).
- Two over frequency elements ("81H 1" and "81H 2" block).
- Auto reclosing feature ("Reclosing" block).

#### **SEPAM S4x**

- Four inverse time phase overcurrent elements with a definite time reset characteristic ("50/51 1A def reset", "50/51 1B def reset", "50/51 2A def reset", and "50/51 2B def reset" block).
- Four inverse time phase overcurrent elements with an inverse time reset characteristic ("50/51 1A idmt reset", "50/51 1B idmt reset", "50/51 2A idmt reset", and "50/51 2B idmt reset" block).
- Four definite time phase overcurrent elements with a definite time reset characteristic ("50/51 1A DT", "50/51 1B DT", "50/51 2A DT", and "50/51 2B DT" block).
- Two directional inverse time phase overcurrent elements with a definite time reset characteristic ("67 1 def reset", and "67 2 def reset" block).
- Two directional inverse time phase overcurrent elements with an inverse time reset characteristic ("67 1 idmt reset", and "67 2 idmt reset" block).
- Two directional definite time phase overcurrent elements with a definite time reset characteristic ("67 1 DT", and "67 2 DT" block).
- Four inverse time neutral overcurrent elements with a definite time reset characteristic ("50N/51N 1A def reset", "50N/51N 1B def reset", "50N/51N 2A def reset", and "50N/51N 2B def reset" block).
- Four inverse time neutral overcurrent elements with an inverse time reset characteristic ("50N/51N 1A idmt reset", "50N/51N 1B idmt reset", "50N/51N 2A idmt reset", and "50N/51N 2B idmt reset" block).
- Two directional inverse time neutral overcurrent elements with a definite time reset characteristic ("67N 1 def reset", and "67N 2 def reset" block).
- Two directional inverse time neutral overcurrent elements with an inverse time reset characteristic ("67N 1 idmt reset", and "67N 2 idmt reset" block).

- Two negative sequence inverse time elementS ("46 1" and "46 2" block).
- One forward direction active overpower with definite time trip characteristic element ("P Fwd" block).
- One reverse direction active overpower with definite time trip characteristic element ("P Rev" block).
- Two phase-phase undervoltage elements ("27 1", "27 2" block).
- Two phase-phase overvoltage elements ("59 1" and "59 2" block).
- One phase-neutral undervoltage element ("27S" block).
- Two zero sequence overvoltage elements ("59N 1" and "59N 2" block).
- One negative sequence overvoltage element ("47" block).
- Four under frequency elements ("81L 1", "81L 2", "81L 3", and "81L 4" block).
- Two over frequency elements ("81H 1" and "81H 2" block).
- Auto reclosing feature ("Reclosing" block).

#### **SEPAM T4x**

- Four inverse time phase overcurrent elements with a definite time reset characteristic ("50/51 1A def reset", "50/51 1B def reset", "50/51 2A def reset", and "50/51 2B def reset" block).
- Four inverse time phase overcurrent elements with an inverse time reset characteristic ("50/51 1A idmt reset", "50/51 1B idmt reset", "50/51 2A idmt reset", and "50/51 2B idmt reset" block).
- Four definite time phase overcurrent elements with a definite time reset characteristic ("50/51 1A DT", "50/51 1B DT", "50/51 2A DT", and "50/51 2B DT" block).
- Two directional inverse time phase overcurrent elements with a definite time reset characteristic ("67 1 def reset", and "67 2 def reset" block).
- Two directional inverse time phase overcurrent elements with an inverse time reset characteristic ("67 1 idmt reset", and "67 2 idmt reset" block).
- Two directional definite time phase overcurrent elements with a definite time reset characteristic ("67 1 DT", and "67 2 DT" block).
- Four inverse time neutral overcurrent elements with a definite time reset characteristic ("50N/51N 1A def reset", "50N/51N 1B def reset", "50N/51N 2A def reset", and "50N/51N 2B def reset" block).
- Four inverse time neutral overcurrent elements with an inverse time reset characteristic ("50N/51N 1A idmt reset", "50N/51N 1B idmt reset", "50N/51N 2A idmt reset", and "50N/51N 2B idmt reset" block).
- Two directional inverse time neutral overcurrent elements with a definite time reset characteristic ("67N 1 def reset", and "67N 2 def reset" block).
- Two directional inverse time neutral overcurrent elements with an inverse time reset characteristic ("67N 1 idmt reset", and "67N 2 idmt reset" block).
- Two negative sequence inverse time elementS ("46 1" and "46 2" block).

- Two thermal overload elements ("Thermal K", "49 A" and "49 B" block). The "Thermal K" block allows setting the percentage of I2 used in the thermal image calculation.
- Two phase-phase undervoltage elements ("27 1", "27 2" block).
- Two phase-phase overvoltage elements ("59 1" and "59 2" block).
- One phase-neutral undervoltage element ("27S" block).
- Two zero sequence overvoltage elements ("59N 1" and "59N 2" block).
- One negative sequence overvoltage element ("47" block).
- Four under frequency elements ("81L 1", "81L 2", "81L 3", and "81L 4" block).
- Two over frequency elements ("81H 1" and "81H 2" block).

#### SEPAM x4x

- · Four inverse time phase overcurrent elements with a definite time reset characteristic ("50/51 1A def reset", "50/51 1B def reset", "50/51 2A def reset", and "50/51 2B def reset" block).
- Four inverse time phase overcurrent elements with an inverse time reset characteristic ("50/51 1A idmt reset", "50/51 1B idmt reset", "50/51 2A idmt reset", and "50/51 2B idmt reset" block).
- · Four definite time phase overcurrent elements with a definite time reset characteristic ("50/51 1A DT", "50/51 1B DT", "50/51 2A DT", and "50/51 2B DT" block).
- One voltage restrained inverse time phase overcurrent element with a definite time reset characteristic ("50V/51V def reset" block).
- · One voltage restrained inverse time phase overcurrent element with an inverse time reset characteristic ("50V/51V idmt reset" block).
- One voltage restrained definite time phase overcurrent element with a definite time reset characteristic ("50V/51V DT" block).
- Two directional inverse time phase overcurrent elements with a definite time reset characteristic ("67 1 def reset", and "67 2 def reset" block).
- · Two directional inverse time phase overcurrent elements with an inverse time reset characteristic ("67 1 idmt reset", and "67 2 idmt reset" block).
- · Two directional definite time phase overcurrent elements with a definite time reset characteristic ("67 1 DT", and "67 2 DT" block).
- Four inverse time neutral overcurrent elements with a definite time reset characteristic ("50N/51N 1A def reset", "50N/51N 1B def reset", "50N/51N 2A def reset", and "50N/51N 2B def reset" block).
- · Four inverse time neutral overcurrent elements with an inverse time reset characteristic ("50N/51N 1A idmt reset", "50N/51N 1B idmt reset", "50N/51N 2A idmt reset", and "50N/51N 2B idmt reset" block).
- Two directional inverse time neutral overcurrent elements with a definite time reset characteristic ("67N 1 def reset", and "67N 2 def reset" block).
- · Two directional inverse time neutral overcurrent elements with an inverse time reset characteristic ("67N 1 idmt reset", and "67N 2 idmt reset" block).

- One phase undercurrent element ("37" block).
- One forward direction active overpower with definite time trip characteristic element ("P Fwd" block).
- One reverse direction active overpower with definite time trip characteristic element ("P Rev" block).
- One forward direction reactive overpower with definite time trip characteristic element ("Q Fwd" block).
- One reverse direction reactive overpower with definite time trip characteristic element ("Q Rev" block).
- Two negative sequence inverse time elementS ("46 1" and "46 2" block).
- Two thermal overload elements ("Thermal K", "49 A" and "49 B" block). The "Thermal K" block allows setting the percentage of I2 used in the thermal image calculation.
- Two phase-phase undervoltage elements ("27 1", "27 2" block).
- Two phase-phase overvoltage elements ("59 1" and "59 2" block).
- One phase-neutral undervoltage element ("27S" block).
- One "remanent" voltage overvoltage element monitoring the phase A-phase B voltage ("27R" block).
- Two zero sequence overvoltage elements ("59N 1" and "59N 2" block).
- One negative sequence overvoltage element ("47" block).
- Two positive sequence undervoltage elements ("27D/47 1" and "27D/47 2" block).
- Four under frequency elements ("81L 1", "81L 2", "81L 3", and "81L 4" block).
- Two over frequency elements ("81H 1" and "81H 2" block).

#### 3.2.2 Functionality

Each phase inverse time overcurrent element is represented in the model by three blocks: Indeed each inverse time overcurrent element can be set in the relay to use:

- · one of the available inverse time trip characteristics with a definite time reset characteristic.
- one of the available inverse time trip characteristics with an inverse time reset characteristic.
- a definite time trip characteristic (with an extended trip threshold) and a definite time reset characteristic.

The block whom name is ended by the "(Def reset)" string represent the element when a definite time reset characteristic is set. The block whom name is ended by the "(Idmt reset)" string represent the element when a inverse time reset characteristic is set. The block whom name is ended by the "(DT)" string represent the element when a definite time trip characteristic is set. The protective element in the relay is unique therefore only one between these three blocks can be enabled at the same time.

Each block is hosting a double set of tripping characteristics: in this way the time delay can be entered as a T sec value (using the characteristics whom name is ended by the "(T)" string) or

as "TMS" value (using the characteristics whom name is ended by the "(TMS)" string). ("50/51 1A def reset", "50/51 1A idmt reset", "50/51 2A def reset", "50/51 2A idmt reset", "50/51 1B def reset", "50/51 1B idmt reset", "50/51 2B def reset", "50/51 2B idmt reset" block).

Each neutral inverse time overcurrent element is represented in the model by two blocks: Indeed each inverse time overcurrent element can be set in the relay to use:

- one of the available inverse time trip characteristics with a definite time reset characteristic.
- one of the available inverse time trip characteristics with an inverse time reset characteristic.

The block whom name is ended by the "(Def reset)" string represent the element when a definite time reset characteristic is set. The block whom name is ended by the "(Idmt reset)" string represent the element when a inverse time reset characteristic is set. The protective element in the relay is unique therefore only one between these two blocks can be enabled at the same time.

Each block is hosting a double set of tripping characteristics: in this way the time delay can be entered as a T sec value (using the characteristics whom name is ended by the "(T)" string) or as "TMS" value (using the characteristics whom name is ended by the "(TMS)" string). ("50N/51N 1A def reset", "50N/51N 1A idmt reset", "50N/51N 2A def reset", "50N/51N 2A idmt reset", "50N/51N 1B def reset", "50N/51N 1B idmt reset", "50N/51N 2B def reset", "50N/51N 2B idmt reset" block).

The inverse time overcurrent elements support the following trip characteristics:

- EI/F IEEE extremely inverse (T)
- EI/F IEEE extremely inverse (TMS)
- EIT/C IEC extremely inverse (T)
- EIT/C IEC extremely inverse (TMS)
- IAC Extremely Inverse (T)
- IAC Extremely Inverse (TMS)
- IAC Inverse (T)
- IAC Inverse (TMS)
- IAC Very Inverse (T)
- IAC Very Inverse (TMS)
- IEC ultra inverse (T)
- IEC ultra inverse (TMS)
- LTI/B IEC long-time inverse (T)
- LTI/B IEC long-time inverse (TMS)
- MI/D IEEE moderately inverse (T)
- MI/D IEEE moderately inverse (TMS)
- RI-Type inverse (T)
- RI-Type inverse (TMS)

- SIT/A IEC standard inverse (T)
- SIT/A IEC standard inverse (TMS)
- VI/E IEEE very inverse (T)
- VI/E IEEE very inverse (TMS)
- VIT/B IEC very inverse (T)
- VIT/B IEC very inverse (TMS)
- EIT/C extremely inverse (T)
- EIT/C extremely inverse (TMS)
- LTI/B long-time inverse (T)
- LTI/B long-time inverse (TMS)
- SIT/A standard inverse (T)
- SIT/A standard inverse (TMS)
- VIT/B very inverse (T)
- VIT/B very inverse (TMS)
- ultra inverse (T)
- ultra inverse (TMS)

The relationship between current and time values for the trip characteristics whom name contains the "IEC" string complies with the IEC 60255-3 standards. When the characteristic name contains the "IEEE" string the relationship between current and time values complies with the ANSIIEEE C37.112 standards.

A delayed reset characteristic is available for every IEEE or IEC tripping characteristic and can be enabled or disabled by the user.

The "RI" and the "IAC" characteristic are special characteristics which are used mainly in combination with existing mechanical relays.

 $2^{nd}$  harmonic blocking The phase and the ground overcurrent elements can be blocked when the current  $2^{nd}$  harmonic content is greater than a given (17% fixed) threshold.

### 3.2.3 Data input

The relationships between the relay settings and the model parameters can be found in the following tables (the relay model parameter names are listed between brackets):

## SEPAM G40 :

Address	Relay Setting	Model block	Model setting	Note
	Phase-to-phase undervoltage 27 1 Us set point	27 1	Pickup Voltage (Uset)	
	Phase-to-phase undervoltage 27 1 Time delay T	27 1	Time Delay (Tdel)	
	Phase-to-phase undervoltage 27 2 Us set point	27 2	Pickup Voltage (Uset)	
	Phase-to-phase undervoltage 27 2 Time delay T	27 2	Time Delay (Tdel)	
	Phase-to-neutral undervoltage 27S Us set point	27S	Pickup Voltage (Uset)	
	Phase-to-neutral undervoltage 27S Time delay T	27S	Time Delay (Tdel)	
	Directional active overpower 32P Tripping direction	P Fwd	Tripping direction (idir)	Enable the block, no parameter must be set; the "P Fwd" block is monitoring only the forward direction active power
	Directional active overpower 32P Ps set point	P Fwd	Input Setting (Ipset)	
	Directional active overpower 32P Time delay T	P Fwd	Time Dial (Tpset)	
	Directional active overpower 32P Tripping direction	P Rev	Tripping direction (idir)	Enable the block, no parameter must be set; the "P Rev" block is monitoring only the reverse direction active power
	Directional active overpower 32P Ps set point	P Rev	Input Setting (Ipset)	
	Directional active overpower 32P Time delay T	P Rev	Time Dial (Tpset)	
	Directional active overpower 32Q Tripping direction	Q Fwd	Tripping direction (idir)	Enable the block, no parameter must be set; the "Q Fwd" block is monitoring only the forward direction reactive power
	Directional active overpower 32Q Ps set point	Q Fwd	Input Setting (Ipset)	
	Directional active overpower 32Q Time delay T	Q Fwd	Time Dial (Tpset)	
	Directional reactive over- power 32Q Tripping direction	Q Rev	Tripping direction (idir)	Enable the block, no parameter must be set; the "Q Rev" block is monitoring only the reverse direction reactive power
	Directional reactive over- power 32Q Ps set point	Q Rev	Input Setting (Ipset)	
	Directional reactive over- power 32Q Time delay T	Q Rev	Time Dial (Tpset)	
	Negative sequence / unbalance 46 1 Curve	46 1	Characteristic (pcharac)	
	Negative sequence / unbalance 46 1 Is set point	46 1	Current Setting (Ipset)	
	Negative sequence / unbalance 46 1 Time delay T	46 1	Time Dial (Tpset)	
	Negative sequence / unbalance 46 2 Curve	46 2	Characteristic (pcharac)	

Address	Relay Setting	Model block	Model setting	Note
	Phase overcurrent 50/51 2 Is	50/51 1B DT	Current Setting (Ipset)	
	set point	50/51 1B def	Current Setting (Ipset)	
		50/51 1B idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50/51 2 Time delay T	50/51 1B DT	Time Dial (Tpset)	
		50/51 1B def reset	Time Dial (Tpset)	
		50/51 1B idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50/51 2 Timer hold delay T1	50/51 1B DT	Reset Delay (ResetT)	
		50/51 1B def reset 50/51 1B	Reset Delay (ResetT)  Reset Delay (ResetT)	
		idmt reset	neset Delay (nesett)	
	Phase overcurrent 50/51 3 Tripping curve	50/51 2A DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50/51 2A def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50/51 2A idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50/51 3 Is set point	50/51 2A DT	Current Setting (Ipset)	
		50/51 2A def reset	Current Setting (Ipset)	
	DI . 50/51 0	50/51 2A idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50/51 3 Time delay T	50/51 2A DT	Time Dial (Tpset)	
		50/51 2A def reset 50/51 2A	Time Dial (Tpset) Time Dial (Tpset)	
		idmt reset		
	Phase overcurrent 50/51 3 Timer hold delay T1	50/51 2A DT	Reset Delay (ResetT)	
		50/51 2A def reset	Reset Delay (ResetT)	
		50/51 2A idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50/51 4 Tripping curve	50/51 2B DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50/51 2B def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50/51 2B idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50/51 4 Is set point	50/51 2B DT	Current Setting (Ipset)	
		50/51 2B def reset	Current Setting (Ipset)	

Address	Relay Setting	Model block	Model setting	Note
		50/51 2B idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50/51 4 Time delay T	50/51 2B DT	Time Dial (Tpset)	
		50/51 2B def reset	Time Dial (Tpset)	
		50/51 2B idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50/51 4 Timer hold delay T1	50/51 2B DT	Reset Delay (ResetT)	
		50/51 2B def reset	Reset Delay (ResetT)	
		50/51 2B idmt reset	Reset Delay (ResetT)	
	Voltage-restrained phase overcurrent 50V/51V Tripping curve	50V/51V DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50V/51V def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50V/51V idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Voltage-restrained phase overcurrent 50V/51V Is set point	50V/51V DT	Current Setting (Ipset)	
		50V/51V def reset	Current Setting (Ipset)	
		50V/51V idmt reset	Current Setting (Ipset)	
	Voltage-restrained phase overcurrent 50V/51V Time delay T	50V/51V DT	Time Dial (Tpset)	
		50V/51V def reset	Time Dial (Tpset)	
		50V/51V idmt reset	Time Dial (Tpset)	
	Voltage-restrained phase overcurrent 50V/51V Timer hold delay T1	50V/51V DT	Reset Delay (ResetT)	
		50V/5V1 def reset	Reset Delay (ResetT)	
		50V/51V idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 1 Tripping curve	50N/51N 1A DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50N/51N 1A def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 1A idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 1 Is0 set point	50N/51N 1A DT	Current Setting (Ipset)	
		50N/51N 1A def reset	Current Setting (Ipset)	
		50N/51N 1A idmt reset	Current Setting (Ipset)	

Address	Relay Setting	Model block	Model setting	Note
	Phase overcurrent 50N/51N 1 Time delay T	50N/51N 1A DT	Time Dial (Tpset)	
	-	50N/51N 1A def reset	Time Dial (Tpset)	
		50N/51N 1A idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 1 Timer hold delay T1	50N/51N 1A DT	Reset Delay (ResetT)	
	,	50N/51N 1A def reset	Reset Delay (ResetT)	
		50N/51N 1A idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 2 Tripping curve	50N/51N 1B DT	Characteristic (pcharac)	Enable the block when the"Definite time" Tripping curve is active
		50N/51N 1B def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 1B idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 2 Is0 set point	50N/51N 1B DT	Current Setting (Ipset)	
		50N/51N 1B def reset	Current Setting (Ipset)	
		50N/51N 1B idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 2 Time delay T	50N/51N 1B DT	Time Dial (Tpset)	
		50N/51N 1B def reset	Time Dial (Tpset)	
		50N/51N 1B idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 2 Timer hold delay T1	50N/51N 1B DT	Reset Delay (ResetT)	
		50N/51N 1B def reset	Reset Delay (ResetT)	
		50N/51N 1B idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 3 Tripping curve	50N/51N 2A DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50N/51N 2A def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 2A idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 3 Is0 set point	50N/51N 2A DT	Current Setting (Ipset)	
		50N/51N 2A def reset	Current Setting (Ipset)	
		50N/51N 2A idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 3 Time delay T	50N/51N 2A DT	Time Dial (Tpset)	
		50N/51N 2A def reset	Time Dial (Tpset)	

Address	Relay Setting	Model block	Model setting	Note
		50N/51N 2A idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 3 Timer hold delay T1	50N/51N 2A DT	Reset Delay (ResetT)	
		50N/51N 2A def reset	Reset Delay (ResetT)	
		50N/51N 2A idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 4 Tripping curve	50N/51N 2B DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50N/51N 2B def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 2B idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 4 Is0 set point	50N/51N 2B DT	Current Setting (Ipset)	
		50N/51N 2B def reset	Current Setting (Ipset)	
		50N/51N 2B idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 4 Time delay T	50N/51N 2B DT	Time Dial (Tpset)	
		50N/51N 2B def reset	Time Dial (Tpset)	
		50N/51N 2B idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 4 Timer hold delay T1	50N/51N 2B DT	Reset Delay (ResetT)	
		50N/51N 2B def reset	Reset Delay (ResetT)	
		50N/51N 2B idmt reset	Reset Delay (ResetT)	
	Phase-to-phase overvoltage 59 1 Us set point	59 1	Pickup Voltage (Uset)	
	Phase-to-phase overvoltage 59 1 Time delay T	59 1	Time Delay (Tdel)	
	Phase-to-phase overvoltage 59 2 Us set point	59 2	Pickup Voltage (Uset)	
	Phase-to-phase overvoltage 59 2 Time delay T	59 2	Time Delay (Tdel)	
	Neutral voltage displacement 59N 1 Vs0 set point	59N 1	Pickup Voltage (Uset)	
	Neutral voltage displacement 59N 1 Time delay T	59N 1	Time Delay (Tdel)	
	Neutral voltage displacement 59N 2 Vs0 set point	59N 2	Pickup Voltage (Uset)	
	Neutral voltage displacement 59N 2 Time delay T	59N 2	Time Delay (Tdel)	
	Underfrequency 81L 1 Fs set points	81L1	Frequency (Fset)	
	Underfrequency 81L 1 Time delay T	81L1	Time Delay (Tdel)	
	Underfrequency 81L 2 Fs set points	81L2	Frequency (Fset)	
	Underfrequency 81L 2 Time delay T	81L2	Time Delay (Tdel)	

Address	Relay Setting	Model block	Model setting	Note
	Underfrequency 81L 3 Fs set points	81L3	Frequency (Fset)	
	Underfrequency 81L 3 Time delay T	81L3	Time Delay (Tdel)	
	Underfrequency 81L 4 Fs set points	81L4	Frequency (Fset)	
	Underfrequency 81L 4 Time delay T	81L4	Time Delay (Tdel)	
	Overfrequency 81H 1 Fs set points	81H 1	Frequency (Fset)	
	Overfrequency 81H 1 Time delay T	81H 1	Time Delay (Tdel)	
	Overfrequency 81H 2 Fs set points	81H 2	Frequency (Fset)	
	Overfrequency 81H 2 Time delay T	81H 2	Time Delay (Tdel)	

## SEPAM M41 :

Address	Relay Setting	Model block	Model setting	Note
	Positive sequence undervolt- age and phase rotation direc- tion check 27D/47 1 Vsd set point	27D/47 1	Pickup Voltage (Uset)	
	Positive sequence undervolt- age and phase rotation direc- tion check 27D/47 1 Time de- lay	27D/47 1	Time Delay (Tdel)	
	Positive sequence undervolt- age and phase rotation direc- tion check 27D/47 2 Vsd set point	27D/47 2	Pickup Voltage (Uset)	
	Positive sequence undervolt- age and phase rotation direc- tion check 27D/47 2 Time de- lay	27D/47 2	Time Delay (Tdel)	
	Phase-to-phase undervoltage 27 1 Us set point	27 1	Pickup Voltage (Uset)	
	Phase-to-phase undervoltage 27 1 Time delay T	27 1	Time Delay (Tdel)	
	Phase-to-phase undervoltage 27 2 Us set point	27 2	Pickup Voltage (Uset)	
	Phase-to-phase undervoltage 27 2 Time delay T	27 2	Time Delay (Tdel)	
	Phase-to-neutral undervoltage 27S Us set point	27S	Pickup Voltage (Uset)	
	Phase-to-neutral undervoltage 27S Time delay T	27S	Time Delay (Tdel)	
	Directional active overpower 32P Tripping direction	P Fwd	Tripping direction (idir)	Enable the block, no parameter must be set; the "P Fwd" block is monitoring only the forward direction active power
	Directional active overpower 32P Ps set point	P Fwd	Input Setting (Ipset)	
	Directional active overpower 32P Time delay T	P Fwd	Time Dial (Tpset)	
	Directional active overpower 32P Tripping direction	P Rev	Tripping direction (idir)	Enable the block, no parameter must be set; the "P Rev" block is monitoring only the reverse direction active power
	Directional active overpower 32P Ps set point	P Rev	Input Setting (Ipset)	

Address	Relay Setting	Model block	Model setting	Note
	Directional active overpower 32P Time delay T	P Rev	Time Dial (Tpset)	
	Directional active overpower 32Q Tripping direction	Q Fwd	Tripping direction (idir)	Enable the block, no parameter must be set; the "Q Fwd" block is monitoring only the forward direction reactive power
	Directional active overpower 32Q Ps set point	Q Fwd	Input Setting (Ipset)	
	Directional active overpower 32Q Time delay T	Q Fwd	Time Dial (Tpset)	
	Directional reactive over- power 32Q Tripping direction	Q Rev	Tripping direction (idir)	Enable the block, no parameter must be set; the "Q Rev" block is monitoring only the reverse direction reactive power
	Directional reactive over- power 32Q Ps set point	Q Rev	Input Setting (Ipset)	
	Directional reactive over- power 32Q Time delay T	Q Rev	Time Dial (Tpset)	
	Phase-to-neutral undervoltage 27S Us set point	27S	Pickup Voltage (Uset)	
	Phase-to-neutral undervoltage 27S Time delay T	27\$	Time Delay (Tdel)	
	Phase undercurrent 37 Is set point	37	Pickup Current (Ipset)	
	Phase undercurrent 37 Time delay T	37	Time Setting (Tset)	
	Negative sequence / unbalance 46 1 Curve	46 1	Characteristic (pcharac)	
	Negative sequence / unbalance 46 1 Is set point	46 1	Current Setting (Ipset)	
	Negative sequence / unbalance 46 1 Time delay T	46 1	Time Dial (Tpset)	
	Negative sequence / unbalance 46 2 Curve	46 2	Characteristic (pcharac)	
	Negative sequence / unbalance 46 2 Is set point	46 2	Current Setting (Ipset)	
	Negative sequence / unbalance 46 2 Time delay T	46 2	Time Dial (Tpset)	
	Negative sequence overvoltage 47 Vsi set point	47	Pickup Voltage (Uset)	
	Negative sequence overvoltage 47 Time delay T	47	Time Delay (Tdel)	
	Thermal Overload 49RMS 1 Set points	49A	Current Setting (Ipset)	
	Thermal Overload 49RMS 1 Time constant T1	49A	Time Dial (Tpset)	
	Thermal Overload 49RMS 1 Accounting for negative sequence component	Thermal K	K (K)	In the "Logic" tab page
	Thermal Overload 49RMS 2 Set points	49B	Current Setting (Ipset)	
	Thermal Overload 49RMS 2 Time constant T1	49B	Time Dial (Tpset)	
	Thermal Overload 49RMS 2 Accounting for negative sequence component	Thermal K	K (K)	In the "Logic" tab page
	Phase overcurrent 50/51 1 Tripping curve	50/51 1A DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active

Address	Relay Setting	Model block	Model setting	Note
		50/51 1A def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50/51 1A idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50/51 1 Is set point	50/51 1A DT	Current Setting (Ipset)	
		50/51 1A def reset	Current Setting (Ipset)	
		50/51 1A idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50/51 1 Time delay T	50/51 1A DT	Time Dial (Tpset)	
		50/51 1A def reset 50/51 1A	Time Dial (Tpset) Time Dial (Tpset)	
		idmt reset	Time Diai (Tpset)	
	Phase overcurrent 50/51 1 Timer hold delay T1	50/51 1A DT	Reset Delay (ResetT)	
		50/51 1A def reset	Reset Delay (ResetT)	
	_	50/51 1A idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50/51 2 Tripping curve	50/51 1B DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50/51 1B def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50/51 1B idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50/51 2 Is set point	50/51 1B DT	Current Setting (Ipset)	
		50/51 1B def reset	Current Setting (Ipset)	
		50/51 1B idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50/51 2 Time delay T	50/51 1B DT	Time Dial (Tpset)	
		50/51 1B def reset	Time Dial (Tpset)	
		50/51 1B idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50/51 2 Timer hold delay T1	50/51 1B DT	Reset Delay (ResetT)	
		50/51 1B def reset	Reset Delay (ResetT)	
		50/51 1B idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50/51 3 Tripping curve	50/51 2A DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50/51 2A def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active

Address	Relay Setting	Model block	Model setting	Note
	Phase overcurrent 50N/51N 1 Is0 set point	50N/51N 1A DT	Current Setting (Ipset)	
	·	50N/51N 1A def reset	Current Setting (Ipset)	
		50N/51N 1A idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 1 Time delay T	50N/51N 1A DT	Time Dial (Tpset)	
	,	50N/51N 1A def reset	Time Dial (Tpset)	
		50N/51N 1A idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 1 Timer hold delay T1	50N/51N 1A DT	Reset Delay (ResetT)	
	·	50N/51N 1A def reset	Reset Delay (ResetT)	
		50N/51N 1A idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 2 Tripping curve	50N/51N 1B DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50N/51N 1B def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 1B idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 2 Is0 set point	50N/51N 1B DT	Current Setting (Ipset)	
		50N/51N 1B def reset	Current Setting (Ipset)	
		50N/51N 1B idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 2 Time delay T	50N/51N 1B DT	Time Dial (Tpset)	
		50N/51N 1B def reset	Time Dial (Tpset)	
		50N/51N 1B idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 2 Timer hold delay T1	50N/51N 1B DT	Reset Delay (ResetT)	
		50N/51N 1B def reset	Reset Delay (ResetT)	
		50N/51N 1B idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 3 Tripping curve	50N/51N 2A DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50N/51N 2A def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 2A idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 3 Is0 set point	50N/51N 2A DT	Current Setting (Ipset)	
		50N/51N 2A def reset	Current Setting (Ipset)	

Address	Relay Setting	Model block	Model setting	Note
		50N/51N 2A idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 3 Time delay T	50N/51N 2A DT	Time Dial (Tpset)	
	·	50N/51N 2A def reset	Time Dial (Tpset)	
		50N/51N 2A idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 3 Timer hold delay T1	50N/51N 2A DT	Reset Delay (ResetT)	
		50N/51N 2A def reset	Reset Delay (ResetT)	
		50N/51N 2A idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 4 Tripping curve	50N/51N 2B DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50N/51N 2B def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 2B idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 4 Is0 set point	50N/51N 2B DT	Current Setting (Ipset)	
		50N/51N 2B def reset	Current Setting (Ipset)	
		50N/51N 2B idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 4 Time delay T	50N/51N 2B DT	Time Dial (Tpset)	
		50N/51N 2B def reset	Time Dial (Tpset)	
		50N/51N 2B idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 4 Timer hold delay T1	50N/51N 2B DT	Reset Delay (ResetT)	
		50N/51N 2B def reset	Reset Delay (ResetT)	
		50N/51N 2B idmt reset	Reset Delay (ResetT)	
	Phase-to-phase overvoltage 59 1 Us set point	59 1	Pickup Voltage (Uset)	
	Phase-to-phase overvoltage 59 1 Time delay T	59 1	Time Delay (Tdel)	
	Phase-to-phase overvoltage 59 2 Us set point	59 2	Pickup Voltage (Uset)	
	Phase-to-phase overvoltage 59 2 Time delay T	59 2	Time Delay (Tdel)	
	Neutral voltage displacement 59N 1 Vs0 set point	59N 1	Pickup Voltage (Uset)	
	Neutral voltage displacement 59N 1 Time delay T	59N 1	Time Delay (Tdel)	
	Neutral voltage displacement 59N 2 Vs0 set point	59N 2	Pickup Voltage (Uset)	
	Neutral voltage displacement 59N 2 Time delay T	59N 2	Time Delay (Tdel)	
	Directional earth fault 67N 1 Characteristic angle $\theta$ 0	Dir Ground	Max. Torque Angle (mtau)	In the "Voltage Polarizing " tab page.

Address	Relay Setting	Model block	Model setting	Note
	Underfrequency 81L 4 Time delay T	81L4	Time Delay (Tdel)	
	Overfrequency 81H 1 Fs set points	81H 1	Frequency (Fset)	
	Overfrequency 81H 1 Time delay T	81H 1	Time Delay (Tdel)	
	Overfrequency 81H 2 Fs set points	81H 2	Frequency (Fset)	
	Overfrequency 81H 2 Time delay T	81H 2	Time Delay (Tdel)	

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Address	Relay Setting	Model block	Model setting	Note
	Phase-to-phase undervoltage 27 1 Us set point	27 1	Pickup Voltage (Uset)	
	Phase-to-phase undervoltage 27 1 Time delay T	27 1	Time Delay (Tdel)	
	Phase-to-phase undervoltage 27 2 Us set point	27 2	Pickup Voltage (Uset)	
	Phase-to-phase undervoltage 27 2 Time delay T	27 2	Time Delay (Tdel)	
	Phase-to-neutral undervoltage 27S Us set point	27S	Pickup Voltage (Uset)	
	Phase-to-neutral undervoltage 27S Time delay T	27S	Time Delay (Tdel)	
	Negative sequence / unbalance 46 1 Curve	46 1	Characteristic (pcharac)	
	Negative sequence / unbalance 46 1 Is set point	46 1	Current Setting (Ipset)	
	Negative sequence / unbalance 46 1 Time delay T	46 1	Time Dial (Tpset)	
	Negative sequence / unbalance 46 2 Curve	46 2	Characteristic (pcharac)	
	Negative sequence / unbalance 46 2 Is set point	46 2	Current Setting (Ipset)	
	Negative sequence / unbalance 46 2 Time delay T	46 2	Time Dial (Tpset)	
	Negative sequence overvoltage 47 Vsi set point	47	Pickup Voltage (Uset)	
	Negative sequence overvoltage 47 Time delay T	47	Time Delay (Tdel)	
	Phase overcurrent 50/51 1 Tripping curve	50/51 1A DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50/51 1A def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50/51 1A idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50/51 1 Is set point	50/51 1A DT	Current Setting (Ipset)	
	•	50/51 1A def reset	Current Setting (Ipset)	
		50/51 1A idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50/51 1 Time delay T	50/51 1A DT	Time Dial (Tpset)	

Address	Relay Setting	Model block	Model setting	Note
		50N/51N 1A idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 2 Tripping curve	50N/51N 1B DT	Characteristic (pcharac)	Enable the block when the"Definite time" Tripping curve is active
		50N/51N 1B def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 1B idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 2 Is0 set point	50N/51N 1B DT	Current Setting (Ipset)	
		50N/51N 1B def reset	Current Setting (Ipset)	
		50N/51N 1B idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 2 Time delay T	50N/51N 1B DT	Time Dial (Tpset)	
		50N/51N 1B def reset	Time Dial (Tpset)	
		50N/51N 1B idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 2 Timer hold delay T1	50N/51N 1B DT	Reset Delay (ResetT)	
		50N/51N 1B def reset	Reset Delay (ResetT)	
		50N/51N 1B idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 3 Tripping curve	50N/51N 2A DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50N/51N 2A def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 2A idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 3 Is0 set point	50N/51N 2A DT	Current Setting (Ipset)	
		50N/51N 2A def reset	Current Setting (Ipset)	
		50N/51N 2A idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 3 Time delay T	50N/51N 2A DT	Time Dial (Tpset)	
		50N/51N 2A def reset	Time Dial (Tpset)	
		50N/51N 2A idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 3 Timer hold delay T1	50N/51N 2A DT	Reset Delay (ResetT)	
		50N/51N 2A def reset	Reset Delay (ResetT)	
		50N/51N 2A idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 4 Tripping curve	50N/51N 2B DT	Characteristic (pcharac)	Enable the block when the"Definite time" Tripping curve is active

Address	Relay Setting	Model block	Model setting	Note
		50N/51N 2B def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 2B idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 4 Is0 set point	50N/51N 2B DT	Current Setting (Ipset)	
		50N/51N 2B def reset	Current Setting (Ipset)	
		50N/51N 2B idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 4 Time delay T	50N/51N 2B DT	Time Dial (Tpset)	
		50N/51N 2B def reset	Time Dial (Tpset)	
		50N/51N 2B idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 4 Timer hold delay T1	50N/51N 2B DT	Reset Delay (ResetT)	
	•	50N/51N 2B def reset	Reset Delay (ResetT)	
		50N/51N 2B idmt reset	Reset Delay (ResetT)	
	Phase-to-phase overvoltage 59 1 Us set point	59 1	Pickup Voltage (Uset)	
	Phase-to-phase overvoltage 59 1 Time delay T	59 1	Time Delay (Tdel)	
	Phase-to-phase overvoltage 59 2 Us set point	59 2	Pickup Voltage (Uset)	
	Phase-to-phase overvoltage 59 2 Time delay T	59 2	Time Delay (Tdel)	
	Neutral voltage displacement 59N 1 Vs0 set point	59N 1	Pickup Voltage (Uset)	
	Neutral voltage displacement 59N 1 Time delay T	59N 1	Time Delay (Tdel)	
	Neutral voltage displacement 59N 2 Vs0 set point	59N 2	Pickup Voltage (Uset)	
	Neutral voltage displacement 59N 2 Time delay T	59N 2	Time Delay (Tdel)	
	Recloser 79 Number of cycles	Reclosing	Operations to lockout (oplockout)	
	Recloser 79 Activation of cycle 1	Reclosing	Logic (Trip1 column)	in the "Logic" tab page
	Recloser 79 Activation of cycles 2, 3 and 4	Reclosing	Logic (Trip2, Trip3, Trip4 column)	in the "Logic" tab page
	Recloser 79 Memory time de- lay	Reclosing	Reset Time (resettime)	
	Recloser 79 Isolation time delay cycle 1	Reclosing	Reclosing interval 1 (re- cltime1)	
	Recloser 79 Isolation time delay cycle 2	Reclosing	Reclosing interval 2 (recltime2)	
	Recloser 79 Isolation time delay cycle 3	Reclosing	Reclosing interval 3 (recltime3)	
	Recloser 79 Isolation time delay cycle 4	Reclosing	Reclosing interval 4 (recltime4)	
	Underfrequency 81L 1 Fs set points	81L1	Frequency (Fset)	
	Underfrequency 81L 1 Time delay T	81L1	Time Delay (Tdel)	

Address	Relay Setting	Model block	Model setting	Note
	Underfrequency 81L 2 Fs set points	81L2	Frequency (Fset)	
	Underfrequency 81L 2 Time delay T	81L2	Time Delay (Tdel)	
	Underfrequency 81L 3 Fs set points	81L3	Frequency (Fset)	
	Underfrequency 81L 3 Time delay T	81L3	Time Delay (Tdel)	
	Underfrequency 81L 4 Fs set points	81L4	Frequency (Fset)	
	Underfrequency 81L 4 Time delay T	81L4	Time Delay (Tdel)	
	Overfrequency 81H 1 Fs set points	81H 1	Frequency (Fset)	
	Overfrequency 81H 1 Time delay T	81H 1	Time Delay (Tdel)	
	Overfrequency 81H 2 Fs set points	81H 2	Frequency (Fset)	
	Overfrequency 81H 2 Time delay T	81H 2	Time Delay (Tdel)	

## SEPAM S4x :

Address	Relay Setting	Model block	Model setting	Note
	Phase-to-phase undervoltage 27 1 Us set point	27 1	Pickup Voltage (Uset)	
	Phase-to-phase undervoltage 27 1 Time delay T	27 1	Time Delay (Tdel)	
	Phase-to-phase undervoltage 27 2 Us set point	27 2	Pickup Voltage (Uset)	
	Phase-to-phase undervoltage 27 2 Time delay T	27 2	Time Delay (Tdel)	
	Phase-to-neutral undervoltage 27S Us set point	27S	Pickup Voltage (Uset)	
	Phase-to-neutral undervoltage 27S Time delay T	27S	Time Delay (Tdel)	
	Directional active overpower 32P Tripping direction	P Fwd	Tripping direction (idir)	Enable the block, no parameter must be set; the "P Fwd" block is monitoring only the forward direction active power
	Directional active overpower 32P Ps set point	P Fwd	Input Setting (Ipset)	
	Directional active overpower 32P Time delay T	P Fwd	Time Dial (Tpset)	
	Directional active overpower 32P Tripping direction	P Rev	Tripping direction (idir)	Enable the block, no parameter must be set; the "P Rev" block is monitoring only the reverse direction active power
	Directional active overpower 32P Ps set point	P Rev	Input Setting (Ipset)	
	Directional active overpower 32P Time delay T	P Rev	Time Dial (Tpset)	
	Negative sequence / unbalance 46 1 Curve	46 1	Characteristic (pcharac)	
	Negative sequence / unbalance 46 1 Is set point	46 1	Current Setting (Ipset)	
	Negative sequence / unbalance 46 1 Time delay T	46 1	Time Dial (Tpset)	
	Negative sequence / unbalance 46 2 Curve	46 2	Characteristic (pcharac)	

Address	Relay Setting	Model block	Model setting	Note
	Negative sequence / unbalance 46 2 Is set point	46 2	Current Setting (Ipset)	
	Negative sequence / unbalance 46 2 Time delay T	46 2	Time Dial (Tpset)	
	Negative sequence overvoltage 47 Vsi set point	47	Pickup Voltage (Uset)	
	Negative sequence overvoltage 47 Time delay T	47	Time Delay (Tdel)	
	Phase overcurrent 50/51 1 Tripping curve	50/51 1A DT	Characteristic (pcharac)	Enable the block when the"Definite time" Tripping curve is active
		50/51 1A def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50/51 1A idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50/51 1 Is set point	50/51 1A DT	Current Setting (Ipset)	
		50/51 1A def reset	Current Setting (Ipset)	
		50/51 1A idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50/51 1 Time delay T	50/51 1A DT	Time Dial (Tpset)	
		50/51 1A def reset	Time Dial (Tpset)	
		50/51 1A idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50/51 1 Timer hold delay T1	50/51 1A DT	Reset Delay (ResetT)	
		50/51 1A def reset	Reset Delay (ResetT)	
		50/51 1A idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50/51 2 Tripping curve	50/51 1B DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50/51 1B def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50/51 1B idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50/51 2 Is set point	50/51 1B DT	Current Setting (Ipset)	
		50/51 1B def reset	Current Setting (Ipset)	
		50/51 1B idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50/51 2 Time delay T	50/51 1B DT	Time Dial (Tpset)	
		50/51 1B def reset	Time Dial (Tpset)	
		50/51 1B idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50/51 2 Timer hold delay T1	50/51 1B DT	Reset Delay (ResetT)	

Phase overcurrent 50N/51N

3 Tripping curve

50N/51N 2A

Characteristic (pcharac)

Tripping

Enable the block

the"Definite time" curve is active

Address	Relay Setting	Model block	Model setting	Note
		50N/51N 2A def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 2A idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 3 Is0 set point	50N/51N 2A DT	Current Setting (Ipset)	
		50N/51N 2A def reset	Current Setting (Ipset)	
		50N/51N 2A idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 3 Time delay T	50N/51N 2A DT	Time Dial (Tpset)	
		50N/51N 2A def reset	Time Dial (Tpset)	
		50N/51N 2A idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 3 Timer hold delay T1	50N/51N 2A DT	Reset Delay (ResetT)	
		50N/51N 2A def reset	Reset Delay (ResetT)	
		50N/51N 2A idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 4 Tripping curve	50N/51N 2B DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50N/51N 2B def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 2B idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 4 Is0 set point	50N/51N 2B DT	Current Setting (Ipset)	
		50N/51N 2B def reset	Current Setting (Ipset)	
		50N/51N 2B idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 4 Time delay T	50N/51N 2B DT	Time Dial (Tpset)	
		50N/51N 2B def reset	Time Dial (Tpset)	
		50N/51N 2B idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 4 Timer hold delay T1	50N/51N 2B DT	Reset Delay (ResetT)	
		50N/51N 2B def reset	Reset Delay (ResetT)	
		50N/51N 2B idmt reset	Reset Delay (ResetT)	
	Phase-to-phase overvoltage 59 1 Us set point	59 1	Pickup Voltage (Uset)	
	Phase-to-phase overvoltage 59 1 Time delay T	59 1	Time Delay (Tdel)	
	Phase-to-phase overvoltage 59 2 Us set point	59 2	Pickup Voltage (Uset)	
	Phase-to-phase overvoltage 59 2 Time delay T	59 2	Time Delay (Tdel)	

Address	Relay Setting	Model block	Model setting	Note
		67 2 idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Directional phase overcur- rent 67 2 Is set point	67 2 DT	Current Setting (Ipset)	
		67 2 def re- set	Current Setting (Ipset)	
		67 2 idmt re- set	Current Setting (Ipset)	
	Directional phase overcur- rent 67 2 Time delay T	67 2 DT	Time Dial (Tpset)	
		67 2 def reset	Time Dial (Tpset)	
		67 2 idmt re- set	Time Dial (Tpset)	
	Directional phase overcur- rent 67 2 Timer hold delay T1	67 2 DT	Reset Delay (ResetT)	
		67 2 def re- set	Reset Delay (ResetT)	
		67 2 idmt re- set	Reset Delay (ResetT)	
	Directional earth fault 67N 1 Characteristic angle $\theta$ 0	Dir Ground	Max. Torque Angle (mtau)	In the "Voltage Polarizing" tab page.
	Directional earth fault 67N 1 Tripping direction	67N 1 def re- set	Tripping Direction (idir)	
		67N 1 idmt reset	Tripping Direction (idir)	
	Directional earth fault 67N 1 Tripping curve	67N 1 def re- set	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		67N 1 idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
	Directional earth fault 67N 1 Is0 set point	67N 1 def re- set	Current Setting (Ipset)	
		67N 1 idmt reset	Current Setting (Ipset)	
	Directional earth fault 67N 1 Time delay T	67N 1 def re- set	Time Dial (Tpset)	
		67N 1 idmt reset	Time Dial (Tpset)	
	Directional earth fault 67N 1 Timer hold delay T1	67N 1 def re- set	Reset Delay (ResetT)	
		67N 1 idmt reset	Reset Delay (ResetT)	
	Directional earth fault 67N 2 Characteristic angle $\theta$ 0	Dir Ground	Max. Torque Angle (mtau)	In the "Voltage Polarizing" tab page.
	Directional earth fault 67N 2 Tripping direction	67N 2 def re- set	Tripping Direction (idir)	
		67N 2 idmt reset	Tripping Direction (idir)	
	Directional earth fault 67N 2 Tripping curve	67N 2 def reset	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		67N 2 idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
	Directional earth fault 67N 2 Is0 set point	67N 2 def re- set	Current Setting (Ipset)	

Address	Relay Setting	Model block	Model setting	Note
		67N 2 idmt	Current Setting (Ipset)	
	Directional earth fault 67N 2 Time delay T	reset 67N 2 def re- set	Time Dial (Tpset)	
	Time delay 1	67N 2 idmt reset	Time Dial (Tpset)	
	Directional earth fault 67N 2 Timer hold delay T1	67N 2 def reset	Reset Delay (ResetT)	
		67N 2 idmt reset	Reset Delay (ResetT)	
	Recloser 79 Number of cycles	Reclosing	Operations to lockout (oplockout)	
	Recloser 79 Activation of cycle 1	Reclosing	Logic (Trip1 column)	in the "Logic" tab page
	Recloser 79 Activation of cycles 2, 3 and 4	Reclosing	Logic (Trip2, Trip3, Trip4 column)	in the "Logic" tab page
	Recloser 79 Memory time de- lay	Reclosing	Reset Time (resettime)	
	Recloser 79 Isolation time delay cycle 1	Reclosing	Reclosing interval 1 (re- cltime1)	
	Recloser 79 Isolation time delay cycle 2	Reclosing	Reclosing interval 2 (recltime2)	
	Recloser 79 Isolation time delay cycle 3	Reclosing	Reclosing interval 3 (recltime3)	
	Recloser 79 Isolation time delay cycle 4	Reclosing	Reclosing interval 4 (recltime4)	
	Underfrequency 81L 1 Fs set points	81L1	Frequency (Fset)	
	Underfrequency 81L 1 Time delay T	81L1	Time Delay (Tdel)	
	Underfrequency 81L 2 Fs set points	81L2	Frequency (Fset)	
	Underfrequency 81L 2 Time delay T	81L2	Time Delay (Tdel)	
	Underfrequency 81L 3 Fs set points	81L3	Frequency (Fset)	
	Underfrequency 81L 3 Time delay T	81L3	Time Delay (Tdel)	
	Underfrequency 81L 4 Fs set points	81L4	Frequency (Fset)	
	Underfrequency 81L 4 Time delay T	81L4	Time Delay (Tdel)	
	Overfrequency 81H 1 Fs set points	81H 1	Frequency (Fset)	
	Overfrequency 81H 1 Time delay T	81H 1	Time Delay (Tdel)	
	Overfrequency 81H 2 Fs set points	81H 2	Frequency (Fset)	
	Overfrequency 81H 2 Time delay T	81H 2	Time Delay (Tdel)	

## SEPAM T4x :

Address	Relay Setting	Model block	Model setting	Note
	Phase-to-phase undervoltage 27 1 Us set point	27 1	Pickup Voltage (Uset)	
	Phase-to-phase undervoltage 27 1 Time delay T	27 1	Time Delay (Tdel)	
	Phase-to-phase undervoltage 27 2 Us set point	27 2	Pickup Voltage (Uset)	

definite time Reset curve is ac-

Address	Relay Setting	Model block	Model setting	Note
	Phase overcurrent 50N/51N 4 Is0 set point	50N/51N 2B DT	Current Setting (Ipset)	
		50N/51N 2B def reset	Current Setting (Ipset)	
		50N/51N 2B idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 4 Time delay T	50N/51N 2B DT	Time Dial (Tpset)	
	•	50N/51N 2B def reset	Time Dial (Tpset)	
		50N/51N 2B idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 4 Timer hold delay T1	50N/51N 2B DT	Reset Delay (ResetT)	
		50N/51N 2B def reset	Reset Delay (ResetT)	
		50N/51N 2B idmt reset	Reset Delay (ResetT)	
	Phase-to-phase overvoltage 59 1 Us set point	59 1	Pickup Voltage (Uset)	
	Phase-to-phase overvoltage 59 1 Time delay T	59 1	Time Delay (Tdel)	
	Phase-to-phase overvoltage 59 2 Us set point	59 2	Pickup Voltage (Uset)	
	Phase-to-phase overvoltage 59 2 Time delay T	59 2	Time Delay (Tdel)	
	Neutral voltage displacement 59N 1 Vs0 set point	59N 1	Pickup Voltage (Uset)	
	Neutral voltage displacement 59N 1 Time delay T	59N 1	Time Delay (Tdel)	
	Neutral voltage displacement 59N 2 Vs0 set point	59N 2	Pickup Voltage (Uset)	
	Neutral voltage displacement 59N 2 Time delay T	59N 2	Time Delay (Tdel)	
	Directional phase overcurrent 67 1 Characteristic angle $\theta$	Dir Phase	Max. Torque Angle (mtau)	In the "Voltage Polarizing" tab page.
	Directional phase overcur- rent 67 1 Tripping direction	67 1 DT	Tripping Direction (idir)	
		67 1 def re- set	Tripping Direction (idir)	
		67 1 idmt re- set	Tripping Direction (idir)	
	Directional phase overcur- rent 67 1 Tripping curve	67 1 DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		67 1 def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		67 1 idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Directional phase overcur- rent 67 1 Is set point	67 1 DT	Current Setting (Ipset)	
		67 1 def reset	Current Setting (Ipset)	
		67 1 idmt re- set	Current Setting (Ipset)	
	Directional phase overcur- rent 67 1 Time delay T	67 1 DT	Time Dial (Tpset)	

### SEPAM x4x :

Address	Relay Setting	Model block	Model setting	Note
	Phase-to-phase undervoltage 27 1 Us set point	27 1	Pickup Voltage (Uset)	
	Phase-to-phase undervoltage 27 1 Time delay T	27 1	Time Delay (Tdel)	
	Phase-to-phase undervoltage 27 2 Us set point	27 2	Pickup Voltage (Uset)	
	Phase-to-phase undervoltage 27 2 Time delay T	27 2	Time Delay (Tdel)	
	Positive sequence undervolt- age and phase rotation direc- tion check 27D/47 1 Vsd set point	27D/47 1	Pickup Voltage (Uset)	
	Positive sequence undervolt- age and phase rotation direc- tion check 27D/47 1 Time de- lay	27D/47 1	Time Delay (Tdel)	
	Positive sequence undervoltage and phase rotation direction check 27D/47 2 Vsd set point	27D/47 2	Pickup Voltage (Uset)	
	Positive sequence undervolt- age and phase rotation direc- tion check 27D/47 2 Time de- lay	27D/47 2	Time Delay (Tdel)	
	Remanent undervoltage 27R Us set point	27R	Pickup Voltage (Uset)	
	Remanent undervoltage 27R Time delay T	27R	Time Delay (Tdel)	
	Phase-to-neutral undervoltage 27S Us set point	27\$	Pickup Voltage (Uset)	
	Phase-to-neutral undervoltage 27S Time delay T	27\$	Time Delay (Tdel)	
	Phase undercurrent 37 Is set point	37	Pickup Current (Ipset)	
	Phase undercurrent 37 Time delay T	37	Time Setting (Tset)	
	Negative sequence / unbalance 46 Curve	46	Characteristic (pcharac)	
	Negative sequence / unbalance 46 ls set point	46	Current Setting (Ipset)	
	Negative sequence / unbalance 46 Time delay T	46	Time Dial (Tpset)	
	Thermal Overload 49RMS 1 Set points	49A	Current Setting (Ipset)	
	Thermal Overload 49RMS 1 Time constant T1	49A	Time Dial (Tpset)	
	Thermal Overload 49RMS 1 Accounting for negative sequence component	Thermal K	K (K)	In the "Logic" tab page
	Thermal Overload 49RMS 2 Set points	49B	Current Setting (Ipset)	
	Thermal Overload 49RMS 2 Time constant T1	49B	Time Dial (Tpset)	
	Thermal Overload 49RMS 2 Accounting for negative sequence component	Thermal K	K (K)	In the "Logic" tab page
	Phase overcurrent 50/51 1 Tripping curve	50/51 1A DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active

Address	Relay Setting	Model block	Model setting	Note
	Voltage-restrained phase overcurrent 50V/51V Is set point	50V/51V DT	Current Setting (Ipset)	
		50V/51V def reset	Current Setting (Ipset)	
		50V/51V idmt reset	Current Setting (Ipset)	
	Voltage-restrained phase overcurrent 50V/51V Time delay T	50V/51V DT	Time Dial (Tpset)	
		50V/51V def reset	Time Dial (Tpset)	
		50V/51V idmt reset	Time Dial (Tpset)	
	Voltage-restrained phase overcurrent 50V/51V Timer hold delay T1	50V/51V DT	Reset Delay (ResetT)	
		50V/5V1 def reset	Reset Delay (ResetT)	
		50V/51V idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 1 Tripping curve	50N/51N 1A DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50N/51N 1A def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 1A idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 1 Is0 set point	50N/51N 1A DT	Current Setting (Ipset)	
	·	50N/51N 1A def reset	Current Setting (Ipset)	
		50N/51N 1A idmt reset	Current Setting (Ipset)	
	Phase overcurrent 50N/51N 1 Time delay T	50N/51N 1A DT	Time Dial (Tpset)	
		50N/51N 1A def reset	Time Dial (Tpset)	
		50N/51N 1A idmt reset	Time Dial (Tpset)	
	Phase overcurrent 50N/51N 1 Timer hold delay T1	50N/51N 1A DT	Reset Delay (ResetT)	
		50N/51N 1A def reset	Reset Delay (ResetT)	
		50N/51N 1A idmt reset	Reset Delay (ResetT)	
	Phase overcurrent 50N/51N 2 Tripping curve	50N/51N 1B DT	Characteristic (pcharac)	Enable the block when the "Definite time" Tripping curve is active
		50N/51N 1B def reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a definite time Reset curve is active
		50N/51N 1B idmt reset	Characteristic (pcharac)	Enable the block when an IDMT Tripping curve with a inverse time Reset curve is active
	Phase overcurrent 50N/51N 2 Is0 set point	50N/51N 1B DT	Current Setting (Ipset)	

 $2^{nd}$  harmonic blocking The  $2^{nd}$  harmonic blocking can be disabled putting out of service the "2nd harm limit" block.

## 3.3 Output logic

It represents the output stage of the relay; it's the interface between the relay and the power breaker.

#### 3.3.1 Available elements and relay output signals

The trip logic is implemented by the "Logic" block.

The relay trip output signal is "yout".

#### 3.3.2 Functionality

The "Logic" block collects the trip signals coming from the protective elements and, when any protective element trips, operates the power breaker and the "yout" relay output contact.

#### 3.3.3 Data input

To disable the relay model ability to open the power circuit breaker simply disable the "Logic" block.

# 4 Features not supported

The following features are not supported:

## M41

- Excessive starting time/locked rotor.
- · Starts per hour.

## 5 References

[1] Schneider Electric Industries SAS, 89, boulevard Franklin Roosevelt F - 92500 Rueil-Malmaison (France). *Electrical network protection Sepam series 40 User's manual 2004 PCRED301006EN/3 10-2004*, 2004.