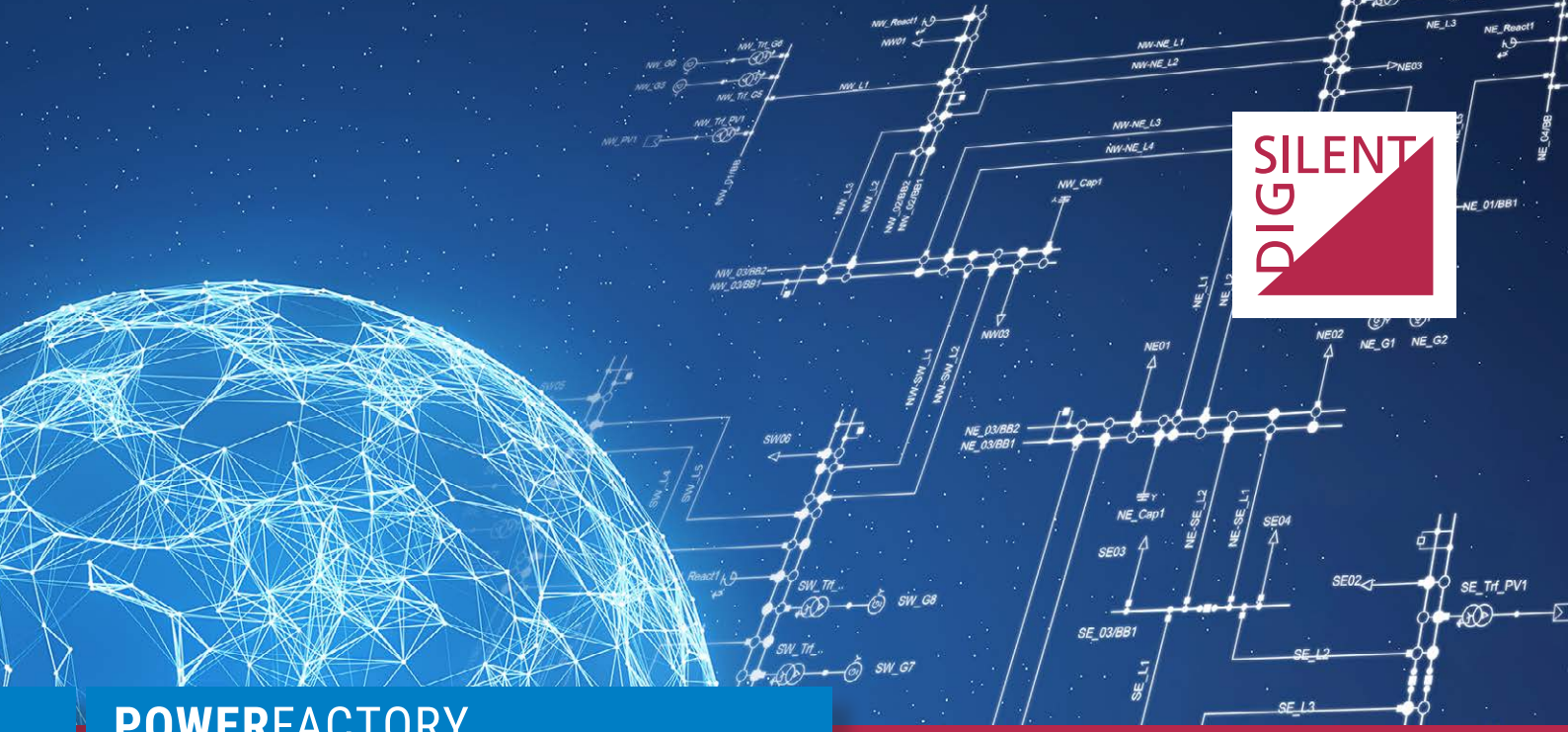

POWERFACTORY

PowerFactory 2021

Technical Reference

PWM Converter

ElmVsc, ElmVscmono

PF2021

POWER SYSTEM SOLUTIONS

MADE IN GERMANY

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January 28, 2021
PowerFactory 2021
Revision 2

Contents

1 General Description

The PWM converter model can be configured to represent both a self-commutated, voltage source AC/DC two-level converter and a modular multilevel converter. The selection between two-level or modular multilevel converter is performed through the *Converter Type* drop-down list in the Basic Data page.

PowerFactory offers two different PWM converter models, one with two DC-connections (*ElmVsc*), shown in Figure 1.1, and one with one DC-connection (*ElmVscmono*), shown in Figure 1.2. This Technical Reference is valid for both. The internal model used in both cases is the same, the only difference is that in the case of *ElmVscmono* the negative DC-pole is directly earthed as shown in Figure 1.2 and manual connection cannot be done.

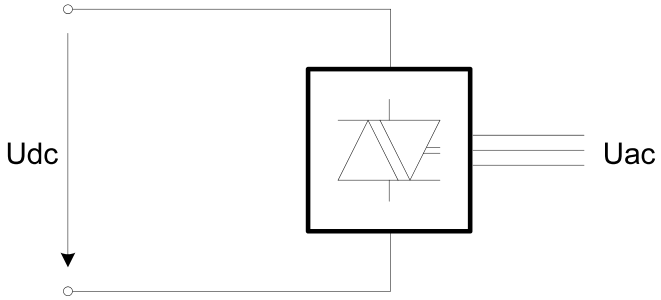


Figure 1.1: PWM-converter with two DC-connection (*ElmVsc*)

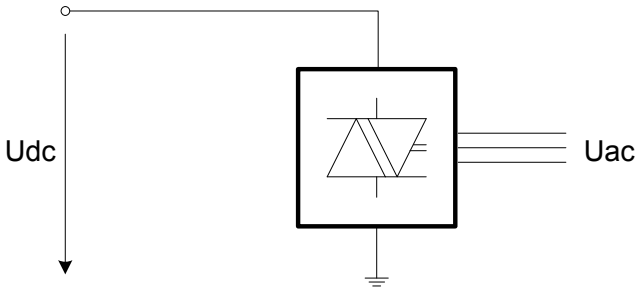


Figure 1.2: PWM-converter with one DC-connection (*ElmVscmono*)

1.1 Two-level Converter

The model equations for the two-level converter are derived from the circuit according to Figure 1.3. The circuit is composed of valves with turn-off capability (two dashes), which are usually realized by IGBTs. However, fundamental frequency models for Load Flow, Stability etc. are valid for other circuit designs as well, e.g. three level designs. Only the detailed PWM-converter model for EMT-simulations is restricted to the topology according to Figure 1.3.

The two-level converter supports sinusoidal and rectangular modulation. The definition of the K_0-factor depends on the selected modulation, see section 1.3.5.

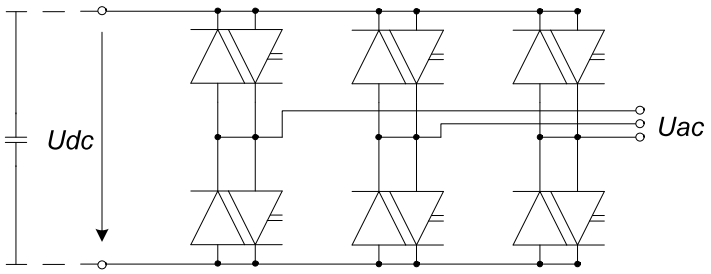
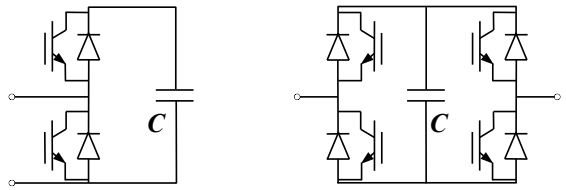


Figure 1.3: Equivalent circuit, with DC-capacitance (optionally included in the model only for RMS-simulations)

1.2 Modular Multilevel Converter (MMC)



Half-bridge Submodule Full-bridge Submodule

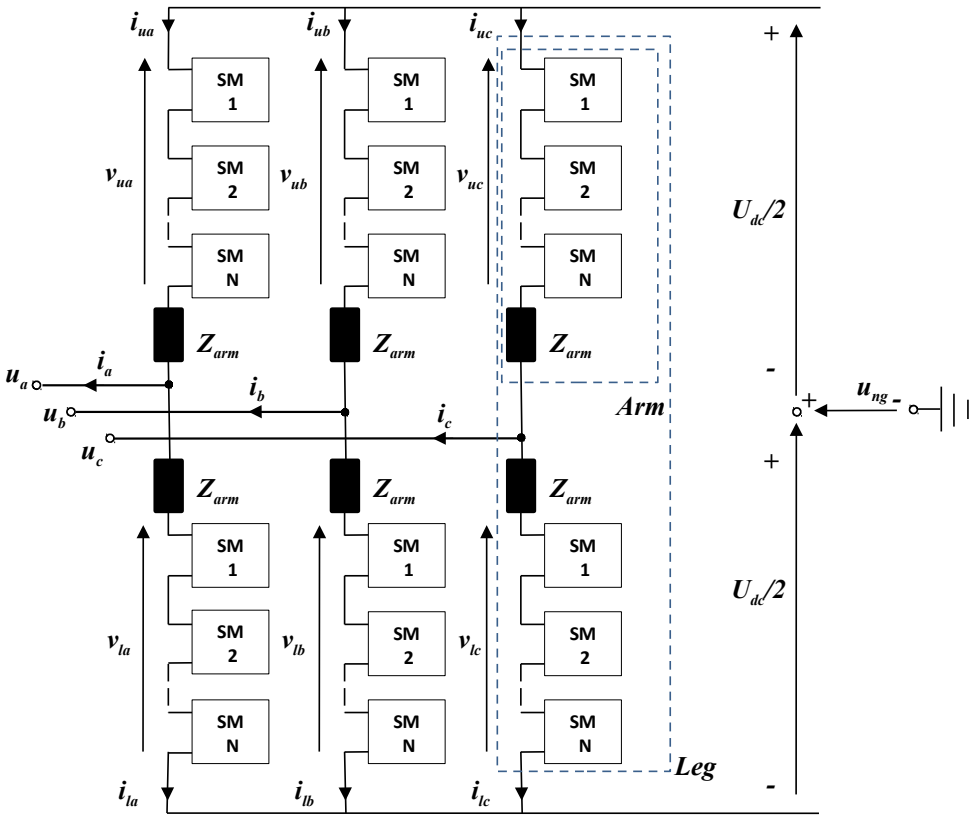


Figure 1.4: Modular multilevel converter topology

The MMC model is based on the topology shown in Figure 1.4. Both submodules with half-bridge and full-bridge configuration are supported.

Four MMC models are supported for EMT simulations: *Controlled voltage source*, *Average value*, *Aggregate arm* and *Detailed equivalent circuit*. All models are described in section 6.

When the MMC is blocked, for example due to a DC fault, the submodules are bypassed and the MMC behaves as a six-pulse diode rectifier.

The pulse generation can be performed internally or externally (in a DSL model). For the *Detailed equivalent circuit* the gate state of each valve can be controlled externally.

When the pulse generation is performed internally, the EMT half-bridge MMC model supports three modulation methods: Phase-Shift PWM, Phase-Disposition PWM and Nearest Level Control. The full-bridge model supports only Nearest Level Control. Nearest Level Control technique is more efficient as the number of levels of the MMC increases [1]. Additionally a *continuous* modulation method is also available, except for the *Detailed equivalent circuit*. When this method is selected, the MMC is switched in a continuous way as if it had an infinite number of submodules. Simulations using *continuous* modulation method is much faster than when using other modulation methods, but results are reasonable only if the number of submodules is sufficiently high. *Continuous* modulation can be useful for preliminary studies, needed for ex. to tune controller parameters.

1.3 Fundamental Frequency Model

The converter models for load flow calculation, RMS-simulation and the *Controlled voltage source* model for EMT-simulations are based on a fundamental frequency approach, both for two-level converter and MMC.

1.3.1 Losses

The most important type of losses are no-load losses resulting from periodically recharging the transistor capacitances (switching losses). These losses are basically V^2-losses and can approximately be modelled by an equivalent resistance between the DC-terminals.

The representation of station and line losses of an HVDC transmission system for load-flow calculations is shown in Figure 1.5.

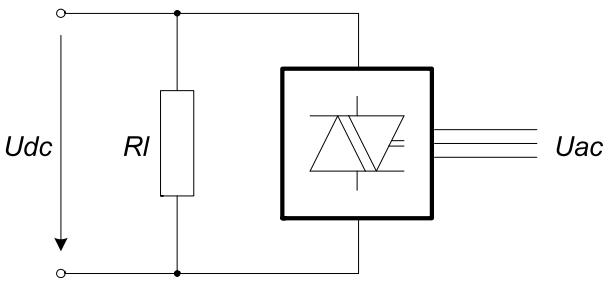


Figure 1.5: PWM-converter with equivalent resistance representing switching losses

Grid-connected PWM-converters are connected to the AC-system through a reactance. For simplifying the modelling of converter and reactance, an AC-reactance is included in the built-in

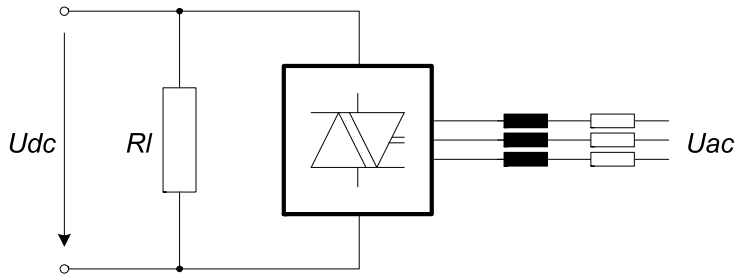


Figure 1.6: PWM-converter with no-load losses, series reactance and load-losses

model. Load losses can be modelled by specifying the series resistance.

The complete fundamental frequency model, including no-load losses, the grid-side reactance and load-losses is shown in Figure 1.6. For modelling the reactance externally, using *PowerFactory*'s series inductance model, the value of the built-in reactance can simply be set equal to zero.

The PWM converter losses are specified in the fundamental frequency models as the sum of:

- No-load losses: specified with the parameter $Pnold$ in [kW].
- Switching losses: specified with the parameter $swtLossFactor$ in [kW/A].
- Resistive losses: specified with the parameter $resLossFactor$ in [Ohm].

The PWM converter losses in MW are calculated depending on the DC side representation (the calculation of the different type of losses is given in the subchapters 1.3.2,1.3.3 and 1.3.4.). The load losses associated with the resistive part of the grid-side reactance are excluded.

The total losses for the element in MW and Mvar are obtained as:

$$\begin{aligned} Ploss &= P_{busac} + P_{busdc} \\ Qloss &= 0 \end{aligned} \tag{1}$$

where P_{busac} and P_{busdc} are calculation parameters available for the element.

The load losses are calculated as the difference between the total losses and the no-load losses:

$$\begin{aligned} Plossld &= Ploss - Plossnld \\ Qlossld &= 0 \end{aligned} \tag{2}$$

where the no-load losses $Plossnld$ are calculated depending on the DC side representation (subchapters 1.3.2,1.3.3 and 1.3.4).

1.3.2 DC Side Representation of Two-level PWM Converter

In fundamental frequency models, the two-level PWM converter is modelled on the DC side according to the equivalent circuit shown in Figure 1.7.

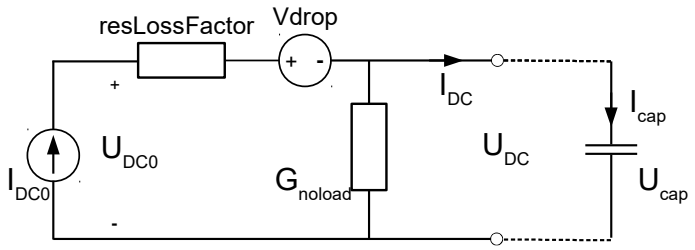


Figure 1.7: Equivalent circuit for the DC side of the two-level PWM converter. The capacitor is modelled externally

The capacitor is modelled externally and the voltage at the converter DC terminals is equal to the capacitor voltage:

$$U_{cap} = U_{DC} \tag{3}$$

Active power conservation between AC- and DC-side is assumed, leading to:

$$P_{AC} = \Re(\underline{U}_{AC} \cdot \underline{I}^*_{AC}) = U_{DC} \cdot I_{DC} + DCPoleLosses = P_{DC} + DCPoleLosses \tag{4}$$

where:

- U_{DC}: DC-voltage
- P_{AC}: AC-active power
- $\underline{U}_{AC}$: AC-voltage phasor (RMS-value)
- $\underline{I}^*_{AC}$: Conjugate complex value of AC-current phasor (RMS-value)
- I_{DC}: DC-current
- P_{DC}: DC-power

The DCPoleLosses are calculated as:

$$\begin{aligned} DCPoleLosses &= Plossnld + resLossFactor \cdot I^2_{DC} + V_{drop} \cdot I_{DC} \\ Plossnld &= G_{noload} \cdot U^2_{DC} \end{aligned} \tag{5}$$

where:

- $G_{noload} = \dfrac{Pnold}{1000 \cdot U^2_{DC,nom}}$ where $U_{DC,nom}$ is expressed in kV
- $V_{drop} = sign(I_{DC}) \cdot swtLossFactor \cdot (1 - exp^{-200 \cdot |I_{DC}|})$

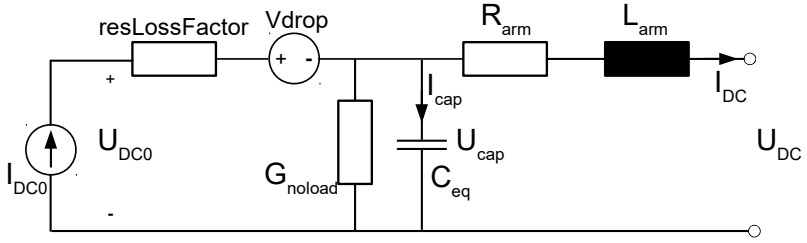


Figure 1.8: Equivalent circuit for the DC side of the half-bridge MMC

1.3.3 DC Side Representation of Half-Bridge MMC

The DC representation of the MMC for fundamental frequency models is a simplified one and does not allow to reproduce phenomena related to energy balancing and circulating currents. The half-bridge MMC is modelled on the DC side according to the equivalent circuit shown in Figure 1.8.

The equivalent arm capacitor is modelled internally. The equivalent arm capacitor voltage is related to the converter DC terminal voltage by the following equation:

$$U_{cap} = U_{DC} + U_{Zarm} \tag{6}$$

where:

$$U_{Zarm} = iZarmDCside \cdot \left(\frac{2}{3} \cdot R_{arm} \cdot I_{DC} + \frac{2}{3} \cdot L_{arm} \cdot \frac{dI_{DC}}{dt} \right) \tag{7}$$

and

- R_{arm}: Arm reactor resistance
- L_{arm}: Arm reactor inductance
- $iZarmDCside$ is either 0 or 1

$iZarmDCside$ is a parameter that can be defined on the *Advanced* tab of the *Basic Data* page, by selecting the flag “Consider arm reactor on DC side”. If the flag is not checked the arm reactor is not considered on the DC side (as in *PowerFactory* 2017 version) and $iZarmDCside = 0$. When the flag is checked, $iZarmDCside = 1$. The factor 2/3 is due to the fact that, as seen from the DC side, each arm has an impedance equal to $2 \cdot Z_{arm}$ and 3 of them are in parallel.

Active power conservation between AC- and DC-side is assumed, leading to:

$$P_{AC} = U_{DC} \cdot I_{DC} + U_{Zarm} \cdot I_{DC} + U_{cap} \cdot I_{cap} + DCPoleLosses \tag{8}$$

where the DCPoleLosses are calculated as:

$$DCPoleLosses = Plossnld + resLossFactor \cdot (I_{DC} + I_{cap})^2 + V_{drop} \cdot (I_{DC} + I_{cap})$$

Notice that V_{drop} is calculated as in section 1.3.2 but using $I_{DC} + I_{cap}$ instead of only I_{DC}. The small current flowing into G_{noload} is neglected.

1.3.4 DC Side Representation of Full-Bridge MMC

For the full-bridge MMC the DC terminal voltage is coupled to the equivalent arm capacitor voltage through the DC bias of the insertion index [4], which can be varied from -1 to 1 (for a half-bridge MMC the insertion index DC bias is always assumed equal to 1). The full-bridge MMC is able to continue operation on the AC side even with zero voltage at DC terminals, assuming that the equivalent arm capacitor voltage is kept around its nominal value.

In fundamental frequency models, the full-bridge MMC is modelled on the DC side according to the equivalent circuit shown in Figure 1.9.

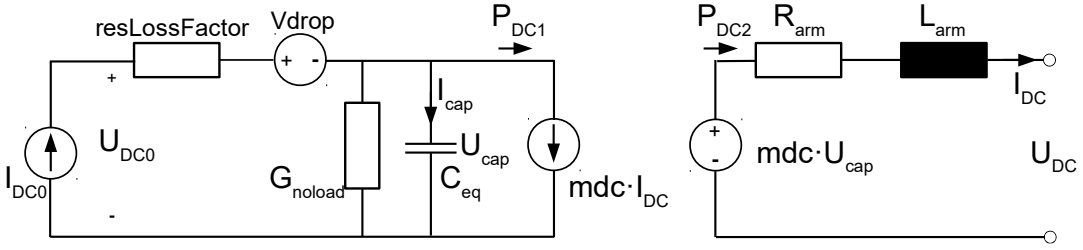


Figure 1.9: Equivalent circuit for the DC side of the full-bridge MMC

The equivalent arm capacitor is modelled internally. Assuming that the insertion index DC bias mdc is the same for the arms in the three phases, the equivalent arm capacitor voltage is related to the converter DC terminal voltage by the following equation:

$$mdc \cdot U_{cap} = U_{DC} + U_{Zarm} \tag{9}$$

where U_{Zarm} is defined in equation 7 and mdc is an input for the fundamental frequency RMS and EMT models. For the *Aggregate arm* and *Detailed equivalent circuit* models an insertion index DC bias per phase can be input to the model, which normally can contain also higher order (for. ex. second) harmonic components.

With reference to the equivalent circuit in Figure 1.9, the power on the capacitor side P_{DC1} is equal to the power on the terminals side P_{DC2}:

$$P_{DC1} = U_{cap} \cdot (mdc \cdot I_{DC}) = (mdc \cdot U_{cap}) \cdot I_{DC} = P_{DC2} \tag{10}$$

Active power conservation between AC- and DC-side is assumed, leading to:

$$P_{AC} = U_{DC} \cdot I_{DC} + U_{Zarm} \cdot I_{DC} + U_{cap} \cdot I_{cap} + DCPoleLosses \tag{11}$$

where the DC losses are calculated as:

$$DCPoleLosses = Plossnld + resLossFactor \cdot (mdc \cdot I_{DC} + I_{cap})^2 + V_{drop} \cdot (mdc \cdot I_{DC} + I_{cap})$$
$$Plossnld = G_{noload} \cdot U_{cap}^2 \quad (12)$$

Notice that V_{drop} is calculated as in section 1.3.2 but using $mdc \cdot I_{DC} + I_{cap}$ instead of only I_{DC}. The small current flowing into G_{noload} is neglected.

For a full-bridge MMC the equivalent arm capacitor voltage is related to the DC terminal voltage through the insertion index DC bias. The capacitor voltage and the insertion index DC bias are initialized in load flow based on the following criteria:

- $|U_{DC} + U_{Zarm}| \leq U_{DC,nom} ==> \begin{cases} U_{cap} = U_{DC,nom} \\ -1 < mdc = \frac{U_{DC}+U_{Zarm}}{U_{cap}} < 1 \end{cases}$
- $|U_{DC} + U_{Zarm}| > U_{DC,nom} ==> \begin{cases} U_{cap} = |U_{DC} + U_{Zarm}| \\ |mdc| = 1 \end{cases}$

1.3.5 AC Side Representation

At fundamental frequency, the converter is modelled by a DC-voltage controlled AC-voltage source conserving active power balance between AC- and DC-side. For values of $|Pm| < 1$ (where $|Pm|$ is the modulation index magnitude), the following equations can be applied:

$$U_{ACr} = K_0 \cdot Pmr \cdot U_{DC0}$$
$$U_{ACi} = K_0 \cdot Pmi \cdot U_{DC0} \quad (13)$$

The variables in equations (13) and (4) are defined as follows:

- U_{ACr}: Real part of AC-voltage (RMS-value)
- U_{ACi}: Imaginary part of AC-voltage (RMS-value)
- K_0: Constant depending on the modulation method
- Pmr: Real part of modulation index
- Pmi: Imaginary part of modulation index
- U_{DC0}: DC-voltage including voltage drop due to losses

U_{DC0} is shown in Figure 1.7 for the two-level converter, in Figure 1.8 for the half-bridge MMC and in Figure 1.9 for the full-bridge MMC.

The pulse width modulation index, which can be defined by magnitude and phase, by real- and imaginary part or by d- and q- axis components is the (complex) control variable of the PWM-converter.

The VSC two-level converter supports sinusoidal and rectangular modulation. The definition of the different modulation-modes is illustrated in Figure 1.10, Figure 1.11 and Figure 1.12. [1] The fundamental frequency MMC model supports only sinusoidal modulation.

- If no modulation is applied, the modulation indices are equal to one and the converter cannot be controlled (see Figure 1.10). The K_0 factor is in this case:

$$K_0 = \frac{\sqrt{2} \cdot \sqrt{3}}{\pi} \tag{14}$$

- Rectangular modulation means that there is a fixed on-off ratio of the pulse stream (see Figure 1.11). The K_0 factor is again defined according to (14).
- In case of sinusoidal modulation, the average of every on-off pulse corresponds to the sinusoidal reference signal (see Figure 1.12). The amount of harmonics is here considerably lower compared to the case of rectangular modulation. This is the standard modulation method in power applications. The K_0 factor is here:

$$K_0 = \frac{\sqrt{3}}{2 \cdot \sqrt{2}} \tag{15}$$

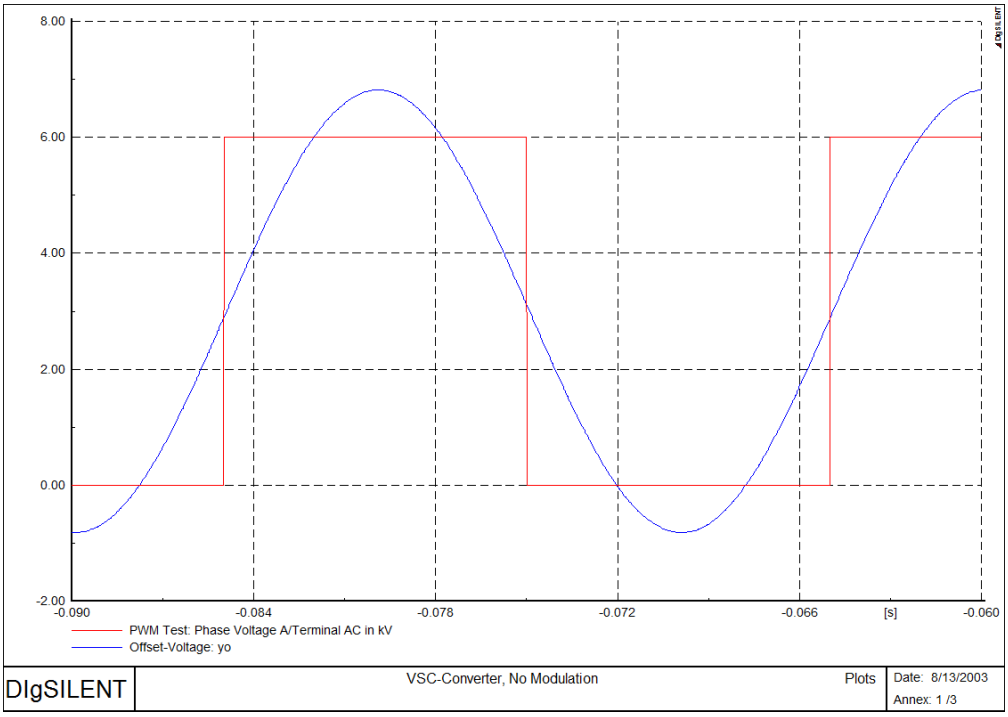


Figure 1.10: Actual voltage and fundamental frequency component in case of no modulation

In all steady-state functions and RMS-simulation, real and imaginary parts of the AC-voltage correspond to the positive sequence component. In EMT-simulations, they correspond to the space-phasor.

[1] The DC-offset is not considered by the fundamental frequency model

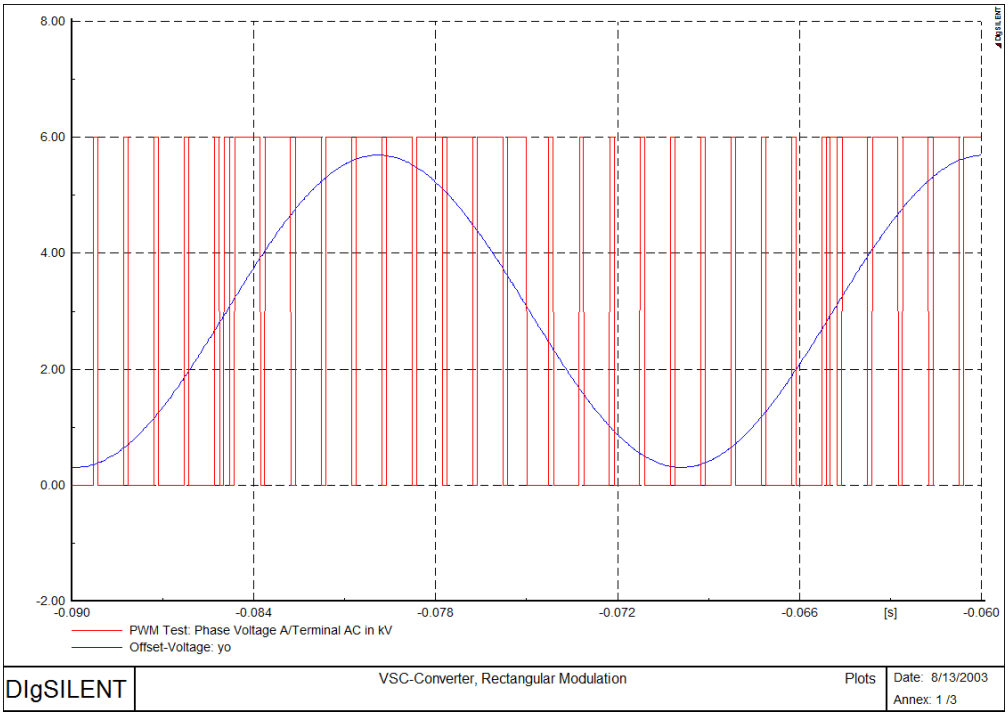


Figure 1.11: Actual voltage and fundamental frequency component for rectangular modulation

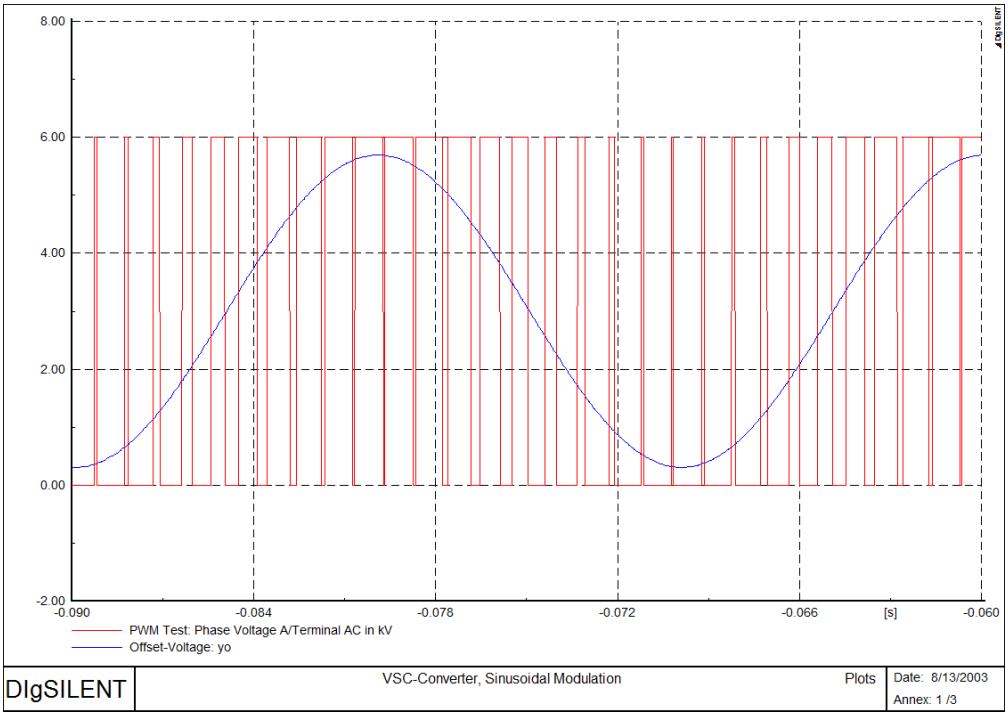


Figure 1.12: Actual voltage and fundamental frequency component for sinusoidal modulation

1.3.6 Saturation

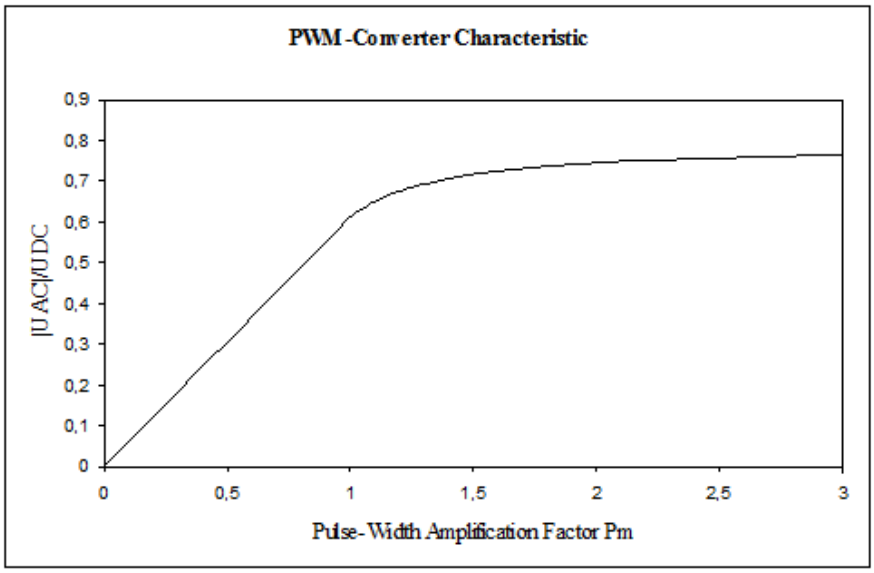


Figure 1.13: PWM-converter saturation

In case of $|Pm| > 1$ and with sinusoidal PWM modulation, the converter starts saturating resulting in the fundamental frequency relationship between the AC-RMS-value and the DC-voltage according to Figure 1.13. As an additional result of converter saturation, low order harmonics start to increase and thus only low levels of saturation are usually allowed.

To extend the linear range of operation of the converter and for a better utilization of the DC-link voltage, the sinusoidal modulation technique can be modified by the injection of a third harmonic in the modulating signals. The third harmonic will not be present in the grid line-line voltages. Four options are available for the third harmonic injection:

- None.
- Sinusoidal, 1/6 amplitude.
- Sinusoidal, 1/4 amplitude.
- Equivalent to SVPWM.

Choosing "None", sinusoidal modulation will be implemented. Sinusoidal modulation with third harmonic injection of type "Sinusoidal, 1/6 Amplitude" is often referred in the literature as THIPWM. The fourth option results in a modulation equivalent to the space vector modulation technique.

The original sinusoidal modulating signal are given as:

$$m_{a,sin} = A \cdot cos(\omega \cdot t)$$
$$m_{b,sin} = A \cdot cos(\omega \cdot t - 2/3\pi)$$
$$m_{c,sin} = A \cdot cos(\omega \cdot t + 2/3\pi)$$

The resulting modulating signals with third harmonic injection are given as:

$$m_a = m_{a,sin} + v_0$$
$$m_b = m_{b,sin} + v_0$$
$$m_c = m_{c,sin} + v_0$$

where v_0 depends on the selected third harmonic injection method.

For ”Sinusoidal, 1/6 Amplitude”:

$$v_0 = A/6 \cdot cos(3 \cdot \omega \cdot t)$$

For ”Sinusoidal, 1/4 Amplitude”:

$$v_0 = A/4 \cdot cos(3 \cdot \omega \cdot t)$$

For ”Equivalent to SVPWM”:

$$v_0 = \frac{max(m_{a,sin},m_{b,sin},m_{c,sin}) + min(m_{a,sin},m_{b,sin},m_{c,sin})}{2}$$

A modulating signal with different types of third harmonic injection is shown in figure 1.14.

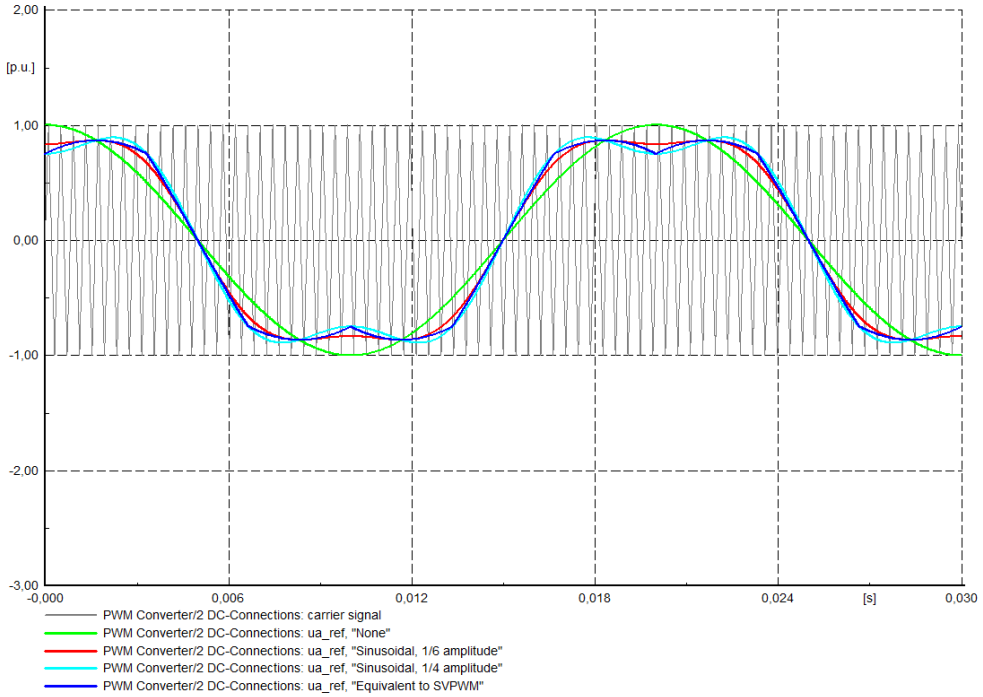


Figure 1.14: PWM Converter reference signal. Pulse width modulation index is equal to 1

The fundamental frequency relationship between the AC-RMS-value and the DC-voltage according to Figure 1.13 is no longer valid if third harmonic injection is used. Depending on the type of third harmonic injection selected, in the overmodulation region the fundamental frequency relationship between AC-RMS-value and the DC-voltage is modified according to figure 1.15.

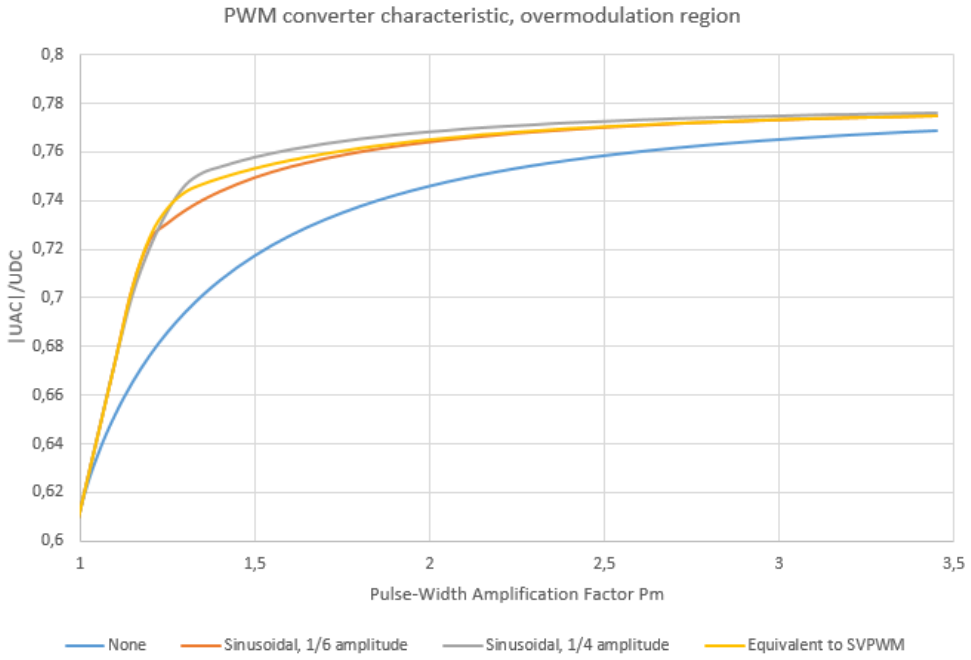


Figure 1.15: PWM-converter saturation with third harmonic injection

2 Load Flow Analysis

In load flow analysis it is common practice not to specify control-variables directly but to define the controlled variables instead. The control-variable (modulation index) is then resulting from the Load Flow calculation.

For load-flow analysis several common control conditions are supported by the PWM-converter model. The meaning and the typical application of each control mode are described below:

- Vac-phi: Specifies magnitude and phase of the AC-terminal. Typical control mode for motor-side converters in variable speed drive applications.
- Vdc-phi: Specifies the DC-voltage and the AC-voltage phase. No typical application.
- PWM-phi: Load-flow setup without control. The pulse-width modulation factor is directly set in magnitude and phase.
- Vdc-Q: Specifies DC-voltage and reactive power output/flow. Typical applications: STATCOM, shunt-converter of UPFC, grid-side converter of doubly-fed induction machines, VSC-HVDC applications.
- P-Vac: Specifies AC-voltage magnitude and active power. This is equivalent to a “PV” characteristic of conventional synchronous machines. Typical applications: Grid-Side converter of converter driven synchronous machines, VSC-HVDC.
- P-Q: Specifies P and Q at the AC-side. This control mode is equivalent to a “PQ”-characteristic of synchronous machines. Typical applications: Same as “P-Vac”.
- Vdc-Vac: Specifies DC- and AC-voltage. Typical applications similar to the control mode “Vdc-Q”: STATCOM, grid-side converter of doubly-fed induction machines, VSC-HVDC applications.
- P-cos(phi): Specifies P and cos(phi) at the AC-side. This control mode can be typically apply on grid-side converter of renewables with PWM converters.
- Vdc-cos(phi): Specifies DC-voltage and cos(phi). Some typical applications: VSC-HVDC implementations and renewables.

For remotely controlled power flow quantities (P, Q), the controlled cubicle can be selected and the orientation of the flow needs to be specified. In case of voltage control, there is the possibility to control a remote bus-bar or terminal.

2.1 Positive Sequence

In load flow studies, the two-level and the modular multilevel converter are represented at the positive sequence as:

$$\underline{U}_{AC1} = \underline{U}_{bus1} + \underline{Z}_{sr} \cdot \underline{I}_{AC1} \tag{18a}$$

$$\underline{U}_{AC1} = \underline{U}_{bus1} + (\underline{Z}_{sr} + \frac{\underline{Z}_{arm}}{2}) \cdot \underline{I}_{AC1} \tag{18b}$$

where $\underline{Z}_{sr}$ is the impedance of the series reactor, $\underline{Z}_{arm}$ is the impedance of the arm reactor, $\underline{U}_{AC1}$ is the internal converter positive sequence voltage phasor, $\underline{I}_{AC1}$ is the converter positive

sequence current phasor and $\underline{U}_{bus1}$ is the bus positive sequence voltage phasor. The first equation is valid for a two-level converter, the second equation holds for a MMC. The impedance $\underline{Z}_{arm}$ is considered exclusively for an MMC.

2.2 Negative Sequence

In unbalanced load flow studies, the two-level and the modular multilevel converter can be represented at the negative sequence as a constant impedance or as a current source model.

2.2.1 Constant impedance model

The equations describing the negative sequence behaviour of the converter are:

$$\underline{U}_{bus2} + (\underline{Z}_{sr} + \underline{Z}_2) \cdot \underline{I}_{AC2} = 0 \tag{19a}$$

$$\underline{U}_{bus2} + (\underline{Z}_{sr} + \underline{Z}_2 + \frac{\underline{Z}_{arm}}{2}) \cdot \underline{I}_{AC2} = 0 \tag{19b}$$

where $\underline{Z}_2$ is the additional negative sequence impedance which can be specified (in p.u.) in the *Advanced* tab of the *Load Flow* page, $\underline{I}_{AC2}$ is the converter negative sequence current phasor and $\underline{U}_{bus2}$ is the bus negative sequence voltage phasor. The first equation is valid for a two-level converter, the second equation holds for an MMC. The negative sequence impedance $\underline{Z}_2$ can be used for example to emulate the action of a controller which blocks the flow of negative sequence current.

2.2.2 Current source model

In load flow it is possible to control the injected negative sequence current through the input $i2r\_set$ and $i2i\_set$, using a Quasi-Dynamic Simulation Model (ElmQdsl).

If these input are not connected, a constant impedance model is considered.

2.3 Zero Sequence

In unbalanced load flow studies, the two-level and the modular multilevel converter are represented at the zero sequence as an impedance. The equations describing the zero sequence behaviour of the converter are:

$$\underline{U}_{bus0} + (\underline{Z}_{sr0} + \underline{Z}_0) \cdot \underline{I}_{AC0} = 0 \tag{20a}$$

$$\underline{U}_{bus0} + (\underline{Z}_{sr0} + \underline{Z}_0 + \frac{\underline{Z}_{arm}}{2}) \cdot \underline{I}_{AC0} = 0 \tag{20b}$$

where $\underline{Z}_{sr0}$ is the zero-sequence impedance of the series reactor. $\underline{Z}_0$ is the additional zero sequence impedance which can be specified in the *Advanced* tab of the *Basic Data* page, $\underline{I}_{AC0}$ is the converter zero sequence current phasor and $\underline{U}_{bus0}$ is the bus zero sequence voltage

phasor. The first equation is valid for a two-level converter, the second equation holds for a MMC.

The zero-sequence impedance $\underline{Z}_{sr0}$ of the series reactor is defined as:

$$\underline{Z}_{sr0} = \Re(\underline{Z}_{sr}) \cdot R0toR1 + j \cdot \Im(\underline{Z}_{sr}) \cdot X0toX1 \tag{21}$$

where $R0toR1$ and $X0toX1$ can be defined in the Basic data page.

This modelling approach is also valid in unbalanced RMS studies and in EMT studies when the *Controlled voltage source* model is selected, if input signals for controlling the zero sequence are not provided. The additional zero sequence impedance $\underline{Z}_0$ is not considered for the detailed EMT model and for the controlled voltage source model when the input *Pm0* is connected.

2.4 Consider Modulation Index Limit

For a given control mode, the solution of the Load Flow calculation will satisfy the control objective for the PWM converter, disregarding the physical limits due to the actual DC voltage. To account for these limits, the flag *Consider modulation index limit* should be checked and a maximum PWM factor should be specified. In this case, the load flow solution will limit the pulse modulation index to the specified value and the control objective might not be achieved. A warning message is printed in the output window.

2.5 P-setpoint Adaption

For control modes *P-Vac*, *P-Q*, or *P-cos(phi)*, the active power setpoint can be modified by the following controllers, if selected:

- DC-voltage dependent P-droop
- Angle-difference dependent P-droop
- Active power participation

When the ***DC-voltage dependent P-droop*** option is selected, the active power setpoint is modified according to:

$$P = P_{set} + \frac{1}{K} \cdot (Vdc - Vdc_{set}) \cdot signPQorient$$

When the ***Angle-difference dependent P-droop*** option is selected, the active power setpoint is modified. If the option *Consider active power setpoint* is selected, the new active power setpoint is given according to:

$$P = P_{set} - Kpphi \cdot (phiu_{local} - phiu_{remote}) \cdot signPQorient$$

If the option *Consider active power setpoint* is not selected, the new active power setpoint is given according to:

$$P = -Kpphi \cdot (phiu_{local} - phiu_{remote}) \cdot signPQorient$$

When the ***Active power participation*** option is selected, the active power setpoint is modified. If the option *Consider active power setpoint* is selected, the new active power setpoint is given according to:

$$P = P_{set} - P_{meas} \cdot K_{part} \cdot signPQorient$$

If the option *Consider active power setpoint* is not selected, the new active power setpoint is given according to:

$$P = -P_{meas} \cdot K_{part} \cdot signPQorient$$

where:

- P_{set} is the active power setpoint.
- Vdc_{set} is the DC voltage setpoint.
- P is the modified active power setpoint.
- K is the specified factor for *DC-voltage dependent P-droop*.
- $Kpphi$ is the specified factor for *Angle-difference dependent P-droop*.
- K_{part} is the specified factor for *Active power participation*.
- $phiu_{remote}$ is the positive-sequence voltage angle of the remote busbar.
- $phiu_{local}$ is the positive-sequence voltage angle of the local busbar.
- P_{meas} is the active power measured (assumed positive with load orientation) at a specified cubicle/boundary.
- $signPQorient$ specifies the sign of the active and reactive power flow at the controlled remote cubicle, if selected.

For control modes *Vdc-phi*, *Vdc-Q*, *Vdc-Vac*, or *Vdc-cos(phi)*, when the ***DC-voltage dependent P-droop*** option is selected, an additional equation is considered:

$$Vdc = K \cdot (P - P_{set}) + Vdc_{set}$$

When controlling the power flow at a remote cubicle, the user must specify the *Orientation* of the active and reactive power flow at the controlled remote cubicle, through the parameter *iQorient* in the load flow page.

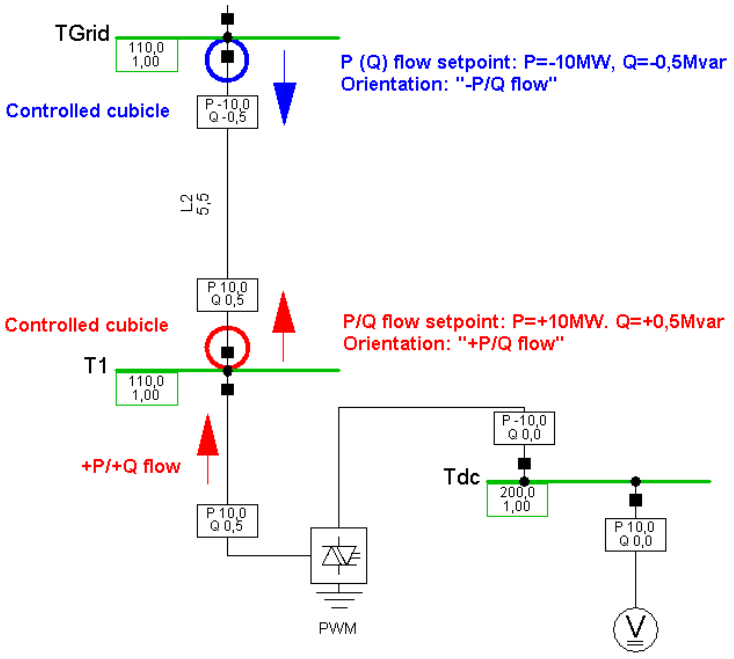


Figure 2.1: Power flow orientation example.

This parameter determines the sign of $signPQorient$ in the above equations. The parameter must be selected as *+P/Q Flow* if the power flow at the controlled point is in the same direction as the power flow at the PWM converter terminals. If the power flow at the controlled point is in opposite direction, the parameter must be selected as *-P/Q Flow*. The power flow for the PWM converter is defined according to generator convention, with positive power flow when exiting the terminals. Figure 2.1 shows the correct way to select the orientation of the power flow and the sign of the power setpoint.

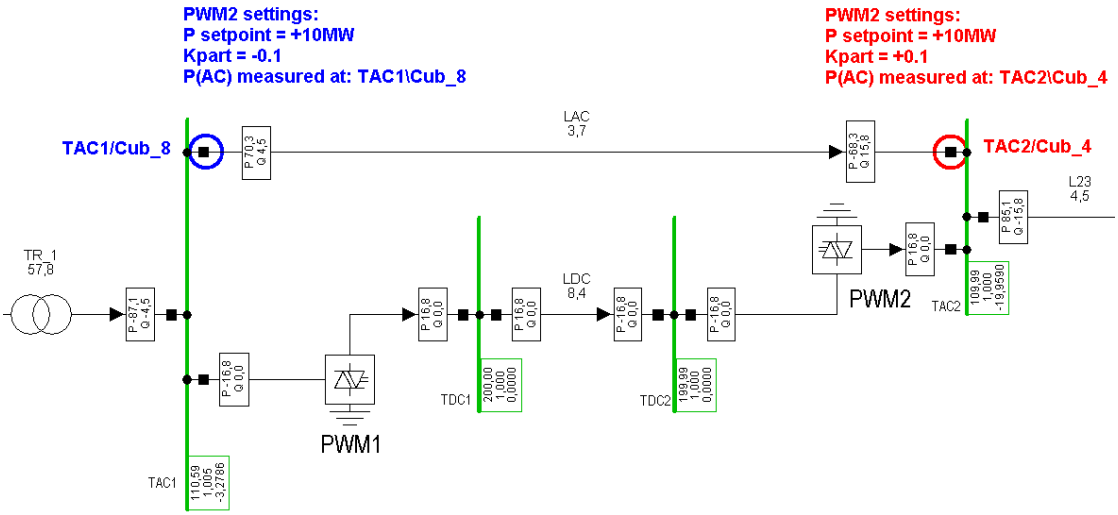


Figure 2.2: *Active power participation* example for PWM2. Active power setpoint is P=10MW.

The *Angle-difference dependent P-droop* and the *Active power participation* options can be used to adapt the active power of the converter depending on the active power flow on a parallel AC line. When the *Active power participation* option is selected, the sign of the parameter *Kpart* depends on the orientation of the power flow at the point where the parameter *Pmeas*

is measured. Figure 2.2 shows how to correctly define the sign of *Kpart*. In the example, the converter PWM2 is performing the active power control and has the *Active power participation* option selected.

2.6 Frequency Control

The possibility for the PWM converter to participate to primary and secondary frequency control is available only for the control modes *P-Vac*, *P-Q*, or *P-cos(phi)*. Participation of the PWM to secondary frequency control is available if a Power-Frequency controller is defined and selected for the PWM through *Ext. secondary controller* in the load flow page. The modified active power P is calculated as:

$$P = P_{set} + (Kp \cdot dpsco - Kpf \cdot dFin) \cdot signPQorient$$

where

- P_{set} is the active power setpoint.
- Kpf is the primary frequency bias.
- $dFin = F - Fnom$ is the frequency deviation.
- Kp is the PWM converter participation factor for secondary frequency control, as defined in the Power-Frequency controller.
- $dpsco$ is the power unbalance, as calculated by the Power-Frequency controller
- $signPQorient$ specifies the sign of the active and reactive power flow at the controlled remote cubicle.

The corresponding calculation quantities (signal) for the frequency deviation can be found in the variable selection dialogue ($s : dFin$ in Hz).

2.7 Operational Limits

Active and reactive power limits can be entered in the Operational Limits tab of the load flow page. These limits are considered in load flow analysis only if the options *Consider Active Power Limits* or *Consider Reactive Power Limits* are selected in the Load Flow calculation dialogue.

Since the capability of a PWM-converter to help the stability of the system is limited, it is common to describe this capability using a P-Q diagram. *PowerFactory* allows defining the Capability Curve, which can be manually entered. The P-Q characteristic is defined using either p.u. values or MW/Mvar values. *PowerFactory* allows defining the Capability Curve considering voltage dependent limits.

The minimum and maximum active power operational limits can be entered in MW.

3 Short-Circuit Calculation

3.1 VDE/IEC Short-Circuit

PWM-converters can be considered as one of the following in any VDE/IEC short-circuit calculation:

- No short-circuit contribution
- Static converter-fed drive
- Equivalent synchronous machine

An additional configuration as *Full size converter* is available for the short-circuit calculation according to IEC60909-2016.

The common equivalent circuit is shown in Figure 3.1.

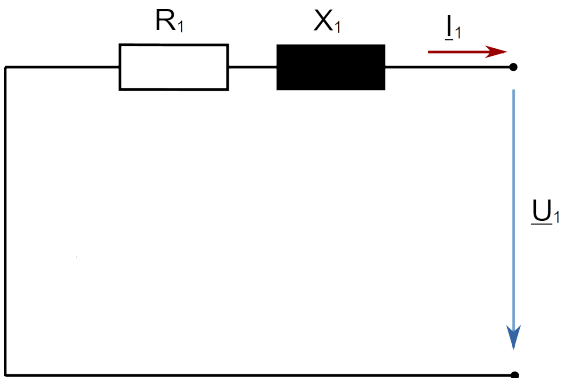


Figure 3.1: Equivalent positive sequence circuit for use in the VDE/IEC short-circuit calculation

The impedance $\underline{Z}_1 = R_1 + j \cdot X_1$ is calculated as follows:

$$X_1 = \frac{|Z_1|}{\sqrt{1 + (R/X)^2}} \tag{22}$$

$$R_1 = R/X \cdot X_1 \tag{23}$$

where:

- $|Z_1|$ is the magnitude of the impedance in [Ω]
- R/X is the R/X ratio

Details of the different configurations and the calculation of the impedance are given in the sections below. PWM-converters are only considered for the calculation of maximum short-circuit currents in the VDE/IEC short-circuit calculation and are always neglected when calculating minimum short-circuit currents.

Note: Short-circuit calculations according to VDE/IEC focus on AC networks, hence the DC side of the PWM-converter will be neglected.

3.1.1 No Short-Circuit Contribution

In this configuration, the PWM-converter will not contribute to VDE/IEC short-circuit calculations.

3.1.2 Static Converter-Fed Drive

PWM-converters configured as a *Static Converter-Fed Drive* will only contribute to the subtransient and peak short-circuit currents.

The impedance $\underline{Z}_1 = R_1 + j \cdot X_1$, as shown in Figure 3.1, is calculated as follows:

$$|Z_1| = \frac{1}{3} \cdot \frac{U_{r,AC}^2}{S_r} \tag{24}$$

$$R/X = 0.1 \tag{25}$$

where:

- $U_{r,AC}$ is the rated AC voltage in [kV] (*e:Unom*)
- S_r is the rated apparent power in [MVA] (*e:Snom*)

Steady-State and Breaking Current As per IEC60909, static converter-fed drives do not contribute to breaking or steady-state currents.

Unbalanced Faults As per IEC60909, static converter-fed drives are always neglected for unbalanced faults.

3.1.3 Equivalent Synchronous Machine

PWM-converters configured using the option *Equivalent Synchronous Machine* allow input of an individual contribution per converter.

Note: This model is not explicitly included in VDE/IEC standards and should be utilised at the user's discretion.

The impedance $\underline{Z}_1 = R_1 + j \cdot X_1$, as shown in Figure 3.1, is calculated as follows:

$$|Z_1| = c \cdot \frac{U_{r,AC}}{\sqrt{3} \cdot I_k''} \tag{26}$$

$$R/X = R/X'' \tag{27}$$

where:

- c is the VDE/IEC voltage factor

- $U_{r,AC}$ is the rated AC voltage in [kV] (*e:Unom*)
- $I_k^{''}$ is the subtransient short-circuit current in [kA] (*e:Ikss*)
- $R/X^{''}$ is the subtransient R/X ratio (*e:rtox*)

The voltage factor, c, is used in the calculation of $|Z_1|$ to ensure that the PWM-converter will not contribute more than the specified subtransient short-circuit contribution, even with a fault at the terminals. This models the power electronic nature of the converter.

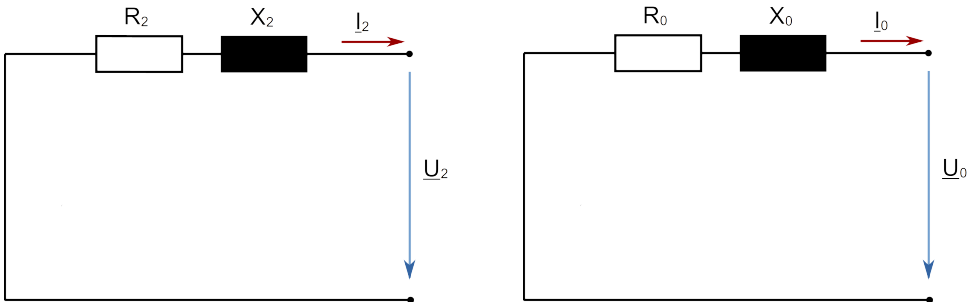
Alternative Input Modes The subtransient short-circuit level can be entered as $S_k^{''}$ or $I_k^{''}$, where $S_k^{''} = \sqrt{3} \cdot U_{r,AC} \cdot I_k^{''}$

The subtransient R/X ratio can be entered as $R/X^{''}$ or $X^{''}/R$, where $R/X^{''} = \left(X^{''}/R\right)^{-1}$

Breaking and Steady-State Current For breaking and steady-state current calculations, the *Equivalent Synchronous Machine* is treated like an external grid, i.e.:

$$I_k = I_b = I_k^{''} \tag{28}$$

Unbalanced Faults The equivalent circuits for the negative and zero sequence are shown in Figure 3.2.



(a) Negative sequence (b) Zero sequence

Figure 3.2: Equivalent negative and zero sequence circuits for use in the VDE/IEC short-circuit calculation

The impedances $\underline{Z}_2 = R_2 + j \cdot X_2$ and $\underline{Z}_0 = R_0 + j \cdot X_0$ are calculated as follows:

$$\underline{Z}_2 = (r_{2,shc} + j \cdot x_{2,shc}) \cdot \frac{U_{r,AC}^2}{S_r} \tag{29}$$

$$\underline{Z}_0 = (r_0 + j \cdot x_0) \cdot \frac{U_{r,AC}^2}{S_r} \tag{30}$$

where:

- $U_{r,AC}$ is the rated AC voltage in [kV] (*e:Unom*)
- S_r is the rated apparent power in [MVA] (*e:Snom*)

- $r_{2,shc}$ is the negative sequence short-circuit resistance in [p.u.] (*e:r2shc*)
- $x_{2,shc}$ is the negative sequence short-circuit reactance in [p.u.] (*e:x2shc*)
- r_0 is the additional zero sequence resistance in [p.u.] (*e:r0*)
- x_0 is the additional zero sequence reactance in [p.u.] (*e:x0*)

3.1.4 Full Size Converter

PWM-converters configured using the option *Full Size Converter* model a type of wind or photovoltaic generation which is connected to the network via power electronics. This model is only available for the short-circuit calculation according to IEC60909-2016.

Due to the unique characteristics of power electronics, *Full Size Converters* are treated as ideal current sources and do not use the equivalent impedance shown in Figure 3.1; i.e. $|Z1| = \infty$. Instead, they inject the specified currents based on the fault type:

- $I''_{k3,PF}$ for 3-phase faults; in [kA] (*e:Ikss3PF*)
- $I''_{k2,PF}$ for 2-phase or 2-phase-to-ground faults; in [kA] (*e:Ikss2PF*)
- $I''_{k1,PF}$ for 1-phase-to-ground faults; in [kA] (*e:Ikss1PF*)

If the *Externally Modelled Unit Transformer* option is used, $I''_{k3,PF}$, $I''_{k2,PF}$ and $I''_{k1,PF}$ are referred to the HV side of the transformer.

Breaking and Steady-State Current For breaking and steady-state calculations, the *Full Size Converter* uses the input value for the maximum steady-state contribution *e:ikPFmax* in [kA].

If the *Externally Modelled Unit Transformer* option is used, $I_{k,PF}$ is referred to the HV side of the transformer.

$$I_k = I_b = I_{k,PF} \tag{31}$$

Note: PWM-converters will always be neglected for the calculation of minimum short-circuit currents, hence the input value for the minimum steady-state contribution will not be used.

Unbalanced Faults For unbalanced faults, the negative and zero sequence models shown in Figure 3.2 are used. However, dedicated sets of parameters for the negative sequence impedance (*e:r2iec* and *e:x2iec*) and zero sequence (*e:r0iec* and *e:x0iec*) are used.

If the *Externally Modelled Unit Transformer* option is used, $\underline{Z}_2$ is referred to the HV side of the transformer and distributed as described in Section 3.1.5. The zero sequence is not distributed.

Note: Even with the *Externally Modelled Unit Transformer* option enabled, the per-unit system used for the negative sequence impedance remains that of the PWM-converter.

3.1.5 Externally Modelled Unit Transformer

Input values obtained from manufacturers for *Full Size Converters* are typically referred to the HV side of the converter unit transformer. In most cases, the PWM-converter is assumed to model the whole unit; i.e. the nominal voltage of the model is equal to the HV side of the unit transformer. However, if the network model requires the unit transformer to be modelled separately, this option can be used to facilitate this approach.

The following conditions must be met for a transformer to be considered a unit transformer:

- there must be exactly one transformer connected to the PWM-converter;
- it must be a 2-winding transformer (*ElmTr2*);
- it must be a 3-phase transformer; and
- it must be explicitly marked as a unit transformer (*iblock* on the Short-Circuit VDE/IEC page)

With this option enabled and a unit transformer present, relevant equations are referred to the HV side of the transformer and assumed to be in the following form:

$$\underline{Z} = \underline{Z}_T + \left(\frac{U_{r,HV}}{U_{r,LV}}\right)^2 \cdot \underline{Z}_{PWM} \tag{32}$$

where:

- $\underline{Z}$ is the impedance of the whole unit seen from the HV side of the unit transformer in [Ω]
- $\underline{Z}_T$ is the impedance of the unit transformer referred to the HV side in [Ω]
- $U_{r,HV}$ is the rated voltage on the HV side of the unit transformer in [kV] (*t:utrn_h*)
- $U_{r,LV}$ is the rated voltage on the LV side of the unit transformer in [kV] (*t:utrn_l*)
- $\underline{Z}_{PWM}$ is impedance of the PWM-converter in [Ω]

Note: The impedance correction factor kT for unit transformers of *Full Size Converters* is ignored, i.e. $kT = 1.0$

.

3.2 Complete Short-Circuit

PWM-converters can be configured as one of the following in the complete short-circuit calculation:

- Equivalent synchronous machine
- Dynamic voltage support
- Constant Voltage
- Constant Current
- Full size converter

The common equivalent circuit is shown in Figure 3.3.

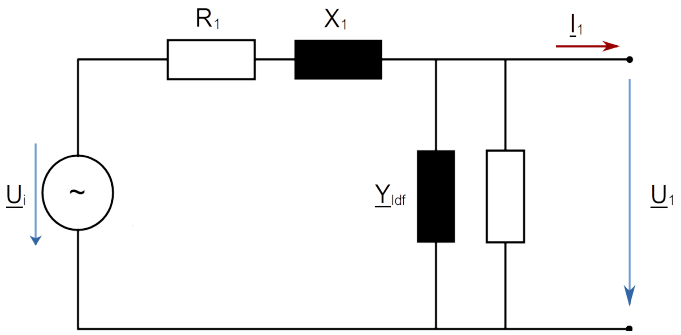


Figure 3.3: Equivalent positive sequence circuit for use in the complete short-circuit calculation

The impedance $\underline{Z}_1 = R_1 + j \cdot X_1$ is calculated as follows:

$$X_1 = \frac{|Z_1|}{\sqrt{1 + (R/X)^2}} \tag{33}$$

$$R_1 = R/X \cdot X_1 \tag{34}$$

where:

- $|Z_1|$ is the magnitude of the impedance in [Ω]
- R/X is the R/X ratio

The load flow admittance $\underline{Y}_{ldf} = G_{ldf} + j \cdot B_{ldf}$ and the internal voltage $\underline{U}_i$ depend on the initialisation of the complete short-circuit.

- With load flow initialisation:

$$\underline{Y}_{ldf} = \frac{\underline{I}_{1,ldf}}{\underline{U}_{1,ldf}} \tag{35}$$

$$\underline{U}_i = \underline{U}_{1,ldf} \tag{36}$$

- Without load flow initialisation:

$$\underline{Y}_{ldf} = 0 \tag{37}$$

$$\underline{U}_i = c \cdot \frac{U_{r,AC}}{\sqrt{3}} \tag{38}$$

where:

- $\underline{U}_{1,ldf}$ is the positive sequence pre-fault voltage in [kV]
- $\underline{I}_{1,ldf}$ is the positive sequence pre-fault current in [kA]
- c is the pre-fault voltage factor (Short-Circuit command input)
- $U_{r,AC}$ is the rated AC voltage in [kV] (*e:Unom*)

Note: Complete short-circuit calculations focus on AC networks, hence the DC side of the PWM-converter will be neglected.

3.2.1 Equivalent Synchronous Machine

PWM-converters configured using the option *Equivalent Synchronous Machine* allow input of an individual subtransient and transient contribution per converter. Both contributions are considered as rotating contributions.

Subtransient Contribution The impedance $\underline{Z}_1 = R_1 + j \cdot X_1$, as shown in Figure 3.3, is calculated as follows:

$$c = \frac{\sqrt{3} \cdot |\underline{U}_i|}{U_{r,AC}} \tag{39}$$

$$|Z_1| = c \cdot \frac{U_{r,AC}}{\sqrt{3} \cdot I_k''} \tag{40}$$

$$R/X = R/X'' \tag{41}$$

where:

- $U_{r,AC}$ is the rated AC voltage in [kV] (*e:Unom*)
- I_k'' is the subtransient short-circuit current in [kA] (*e:Ikss*)
- R/X'' is the subtransient R/X ratio (*e:rtox*)

The voltage factor, c, is used in the calculation of $|Z_1|$ to ensure that the PWM-converter will not contribute more than the specified subtransient short-circuit contribution, even with a fault at the terminals. This models the power electronic nature of the converter.

Transient Contribution The impedance $\underline{Z}_1 = R_1 + j \cdot X_1$, as shown in Figure 3.3, is calculated as follows (depending on whether a subtransient contribution has been specified):

- With $I_k^{''} > 0$

$$c = \frac{\sqrt{3} \cdot |\underline{U}_i|}{U_{r,AC}} \tag{42}$$

$$|Z_k^{''}| = c \cdot \frac{U_{r,AC}}{\sqrt{3} \cdot I_k^{''}} \tag{43}$$

$$|Z_k^{'}| = c \cdot \frac{U_{r,AC}}{\sqrt{3} \cdot I_k^{'}} \tag{44}$$

$$R_1 = R/X^{''} \cdot \frac{|Z_k^{''}|}{\sqrt{1 + (R/X^{''})^2}} \tag{45}$$

$$X_1 = \sqrt{\left|Z_k^{'}\right|^2 - {R_1}^2} \tag{46}$$

- With $I_k^{''} = 0$

$$c = \frac{\sqrt{3} \cdot |\underline{U}_i|}{U_{r,AC}} \tag{47}$$

$$|Z_1| = c \cdot \frac{U_{r,AC}}{\sqrt{3} \cdot I_k^{'}} \tag{48}$$

$$R/X = R/X^{''} \tag{49}$$

where:

- $U_{r,AC}$ is the rated AC voltage in [kV] (*e:Unom*)
- $I_k^{''}$ is the subtransient short-circuit current in [kA] (*e:Ikss*)
- $I_k^{'}$ is the transient short-circuit current in [kA] (*e:Iks*)
- $R/X^{''}$ is the subtransient R/X ratio (*e:rtox*)

The voltage factor, c, is used in the calculation of $|Z_1|$ to ensure that the PWM-converter will not contribute more than the specified transient short-circuit contribution, even with a fault at the terminals. This models the power electronic nature of the converter.

The additional dependence on the subtransient short-circuit contribution is used to keep the resistive part of the impedance constant, so that the change in short-circuit contribution is modelled as a time-dependent reactance.

Alternative Input Modes The subtransient and transient short-circuit levels can be entered as $S_k^{''}$ and $S_k^{'}$ or $I_k^{''}$ and $I_k^{'}$, where $S_k^{''} = \sqrt{3} \cdot U_{r,AC} \cdot I_k^{''}$ and $S_k^{'} = \sqrt{3} \cdot U_{r,AC} \cdot I_k^{'}$

The subtransient R/X ratio can be entered as $R/X^{''}$ or $X^{''}/R$, where $R/X^{''} = \left(X^{''}/R\right)^{-1}$

Unbalanced Faults For unbalanced faults, the negative and zero sequence models shown in Figure 3.2 are used.

3.2.2 Dynamic Voltage Support

PWM-converters configured using the option *Dynamic Voltage Support* are similar to an *Equivalent Synchronous Machine*, but the transient contribution is modelled as a constant current injection. The subtransient contribution is considered as a rotating contribution.

Note: This model is deprecated and will be removed in future versions.

Subtransient Contribution The impedance $\underline{Z}_1 = R_1 + j \cdot X_1$, as shown in Figure 3.3, is calculated as follows:

$$c = \frac{\sqrt{3} \cdot |\underline{U}_i|}{U_{r,AC}} \tag{50}$$

$$|Z_1| = c \cdot \frac{U_{r,AC}}{\sqrt{3} \cdot I_k^{''}} \tag{51}$$

$$R/X = R/X^{''} \tag{52}$$

where:

- $U_{r,AC}$ is the rated AC voltage in [kV] (*e:Unom*)
- $I_k^{''}$ is the subtransient short-circuit current in [kA] (*e:Ikss*)
- $R/X^{''}$ is the subtransient R/X ratio (*e:rtox*)

The voltage factor, c, is used in the calculation of $|Z_1|$ to ensure that the PWM-converter will not contribute more than the specified subtransient short-circuit contribution, even with a fault at the terminals. This models the power electronic nature of the converter.

Transient Contribution The transient contribution is modelled as a constant current injection, i.e. $|Z_1| = \infty$. For more information, see Section 3.2.6.

Alternative Input Modes The subtransient and transient short-circuit levels can be entered as $S_k^{''}$ and $S_k^{'}$, or $I_k^{''}$ and $I_k^{'}$, where $S_k^{''} = \sqrt{3} \cdot U_{r,AC} \cdot I_k^{''}$ and $S_k^{'} = \sqrt{3} \cdot U_{r,AC} \cdot I_k^{'}$

The subtransient R/X ratio can be entered as $R/X^{''}$ or $X^{''}/R$, where $R/X^{''} = \left(X^{''}/R\right)^{-1}$

Unbalanced Faults For unbalanced faults, the negative and zero sequence models shown in Figure 3.2 are used.

3.2.3 Constant Voltage

PWM-converters configured using the option *Const V.* aim to maintain the pre-fault voltage during short-circuit conditions. Both subtransient and transient contributions are considered as rotating contributions.

Subtransient and Transient Contribution The impedance $\underline{Z}_1 = R_1 + j \cdot X_1$, as shown in Figure 3.3, is calculated as follows:

$$|Z_1| = \frac{u_k}{100} \cdot \frac{U_{r,AC}^2}{S_r} \tag{53}$$

$$R_1 = \frac{P_{CU}}{1000 * S_r} \cdot \frac{U_{r,AC}^2}{S_r} \tag{54}$$

$$X_1 = \sqrt{|Z_1|^2 - {R_1}^2} \tag{55}$$

where:

- u_k is the magnitude of the short-circuit impedance in [%] (*e:uk*)
- $U_{r,AC}$ is the rated AC voltage in [kV] (*e:Unom*)
- S_r is the rated apparent power in [MVA] (*e:Snom*)
- P_{CU} are the copper losses in [kW] (*e:Pcu*)

For *Half-bridge type MMC* or *Full-bridge type MMC* PWM-converters, the additional impedance of the arms is considered as follows:

$$\underline{Z}_1 = \underline{Z}_1 + \frac{R_{arm} + j \cdot \omega \cdot L_{arm} \cdot 0.001}{2} \tag{56}$$

where:

- R_{arm} is the arm resistance in [Ω] (*e:Rarm*)
- L_{arm} is the arm inductance in [mH] (*e:Larm*)
- ω is the angular frequency in [rad/s], with $\omega = 2 \cdot \pi \cdot f_N$
- f_N is the nominal frequency in [Hz]

The load flow admittance is always neglected; i.e. $\underline{Y}_{ldf} = 0$.

Unbalanced Faults For unbalanced faults, the negative and zero sequence models are identical to the positive sequence model shown in Figure 3.3, but use $\underline{U}_{2,ldf}$ and $\underline{U}_{0,ldf}$, respectively, for the inner voltage $\underline{U}_i$. If the complete short-circuit is initialised without a load flow, it follows that $\underline{U}_{2,ldf} = 0$ and $\underline{U}_{0,ldf} = 0$.

3.2.4 Constant Current

PWM-converters configured using the option *Const I.* aim to maintain the pre-fault current during short-circuit conditions. Both, subtransient and transient, contributions are considered as rotating contributions.

Note: While similar in name, the *Const I.* configuration is fundamentally different from the *Constant Current Injection* described in Section 3.2.6 in terms of behaviour during short-circuit conditions and should not be confused with the latter.

Subtransient and Transient Contribution Due to the nature of this configuration, it does not use the equivalent circuit shown in Figure 3.3, but instead evaluates the following equation:

$$\underline{I}_1 - \underline{I}_{1,ldf} = 0 \tag{57}$$

where:

- $\underline{I}_1$ is the positive sequence short-circuit current in [kA]
- $\underline{I}_{1,ldf}$ is the positive sequence pre-fault current in [kA]

Unbalanced Faults For unbalanced faults, the following additional equations are evaluated:

$$\underline{I}_2 - \underline{I}_{2,ldf} = 0 \tag{58}$$
$$\underline{I}_0 - \underline{I}_{0,ldf} = 0 \tag{59}$$

where:

- $\underline{I}_2$ is the negative sequence short-circuit current in [kA]
- $\underline{I}_{2,ldf}$ is the negative sequence pre-fault current in [kA]
- $\underline{I}_0$ is the zero sequence short-circuit current in [kA]
- $\underline{I}_{0,ldf}$ is the zero sequence pre-fault current in [kA]

3.2.5 Full Size Converter

PWM-converters configured using the option *Full Size Converter* represent generation which is connected to the network via power electronics. This type is typically found in wind power or photovoltaic plants. Both contributions, subtransient and transient, are modelled as constant current injections.

Subtransient Contribution The transient contribution is modelled as a constant current injection; i.e. $|Z_1| = \infty$. For more information, see Section 3.2.6.

Transient Contribution The transient contribution is modelled as a constant current injection; i.e. $|Z_1| = \infty$. For more information, see Section 3.2.6.

Unbalanced Faults For unbalanced faults, the negative and zero sequence models shown in Figure 3.2 are used. However, dedicated sets of parameters for the negative sequence impedance (*e:r2iec* and *e:x2iec*) and zero sequence (*e:r0iec* and *e:x0iec*) are used.

If the *Externally Modelled Unit Transformer* option is used, $\underline{Z}_2$ is referred to the HV side of the transformer and distributed as described in Section 3.1.5. The zero sequence is not distributed.

Note: Even with the *Externally Modelled Unit Transformer* option enabled, the per-unit system used for the negative sequence impedance remains that of the PWM-converter.

3.2.6 Constant Current Injection

Constant current injections inject a fixed positive sequence current at their terminals. The magnitude of the injected current depends on the voltage dip after the short-circuit calculation has been performed with only rotating machines participating. The angle of the injected current is chosen so that the additional voltage at the fault location, caused by the current injection, is in phase with the pre-fault voltage.

The magnitude of the injected current is calculated as follows:

$$\begin{aligned} I_{max} &= i_{max} \cdot I_r \\ \Delta u_1 &= \frac{|\underline{U}_{1,ldf}| - |\underline{U}_{1,rot}|}{U_{r,AC}} \\ |I_1| &= \begin{cases} K \cdot \Delta u_1 \cdot I_{max} & \text{if } K \cdot \Delta u_1 < 1 \\ I_{max} & \text{if } K \cdot \Delta u_1 \geq 1 \end{cases} \end{aligned} \tag{60}$$

where:

- i_{max} is the maximum current injection in [p.u.] (*e:imax*)
- I_r is the nominal current in [kA] ($I_r = S_r/(\sqrt{3} \cdot U_{r,AC})$)
- S_r is the rated apparent power in [MVA] (*e:Snom*)
- $U_{r,AC}$ is the rated AC voltage in [kV] (*e:Unom*)
- $\underline{U}_{1,ldf}$ is the positive sequence pre-fault voltage in [kV]
- $\underline{U}_{1,rot}$ is the positive sequence post-fault voltage from rotating machines in [kV]
- K is a scaling factor (*e:K*)

Note: The voltages are always measured at the converter terminal, including when the *Externally Modelled Unit Transformer* option is enabled.

Current Iteration The magnitude of the injected current depends on the voltage dip from rotating machines. In most cases, the injected current will cause an increase in the terminal voltage. Hence, there will be a discrepancy between the final voltage at the terminal and the voltage used to calculate the injection. The *Current Iteration* option in the Short-Circuit command attempts to rectify this issue by re-calculating the voltage dip with the additional voltage caused by the converter injection. This is an iterative process, as the voltage increase at the terminal is also influenced by network topology and other injections.

The iterative process only adapts the magnitude of the injected current $|I_1|$, not the phase angle.

3.3 ANSI Short-Circuit

PWM-converters can be configured as one of the following in the ANSI short-circuit calculation:

- No short-circuit contribution
- Equivalent synchronous machine

The common equivalent circuit is shown in Figure 3.4.

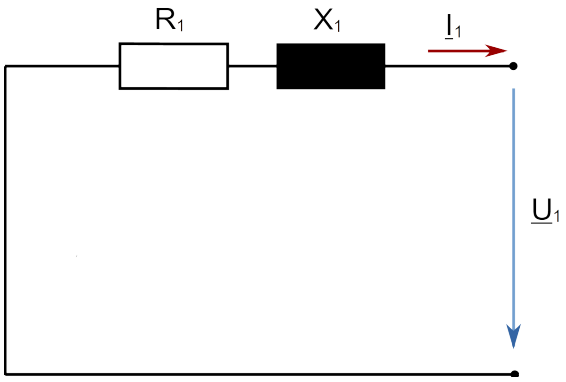


Figure 3.4: Equivalent positive sequence circuit for use in the ANSI short-circuit calculation

The impedance $\underline{Z}_1 = R_1 + j \cdot X_1$ is calculated as follows:

$$X_1 = \frac{|Z_1|}{\sqrt{1 + (R/X)^2}} \tag{61}$$

$$R_1 = R/X \cdot X_1 \tag{62}$$

where:

- $|Z_1|$ is the magnitude of the impedance in [Ω]
- R/X is the R/X ratio

Details of the different configurations and the calculation of the impedance are given in the sections below.

Note: ANSI short-circuit calculations focus on AC networks, hence the DC side of the PWM-converter will be neglected.

3.3.1 No Short-Circuit Contribution

In this configuration, the PWM-converter will not contribute to ANSI short-circuit calculations.

3.3.2 Equivalent Synchronous Machine

PWM-converters not configured using the option *No Short-Circuit Contribution* allow input of an individual contribution per converter.

The impedance $\underline{Z}_1 = R_1 + j \cdot X_1$ is calculated as follows:

$$|Z_1| = u_{prefault} \cdot \frac{U_{r,AC}}{\sqrt{3} \cdot I_k^{''}} \tag{63}$$

$$R/X = R/X^{''} \tag{64}$$

where:

- $u_{prefault}$ is the pre-fault voltage factor (Short-Circuit command input)
- $U_{r,AC}$ is the rated AC voltage in [kV] (*e:Unom*)
- $I_k^{''}$ is the subtransient short-circuit current in [kA] (*e:Ikss*)
- $R/X^{''}$ is the subtransient R/X ratio (*e:rtox*)

The voltage factor, $u_{prefault}$, is used in the calculation of $|Z_1|$ to ensure that the PWM-converter will not contribute more than the specified short-circuit level, even with a fault at the terminals. This models the power electronic nature of the converter.

Momentary Current Contribution For the calculation of momentary currents, the model is considered as described above.

Interrupting Current Contribution For the calculation of interrupting currents, the model is considered as described above and always considered as a “remote contribution”.

30-Cycle Current Contribution For the calculation of 30-cycle currents, the model is neglected.

Unbalanced Faults For unbalanced faults, the negative and zero sequence models shown in Figure 3.2 are used.

3.4 IEC 61363

PWM-converters are not considered in the IEC61363 short-circuit calculation.

4 Harmonics

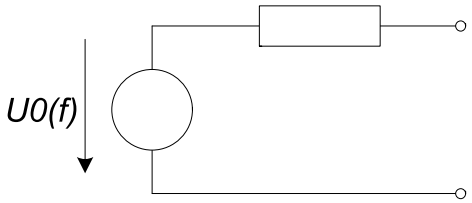


Figure 4.1: Harmonic voltage source

A voltage source converter defines the voltage waveform at the bus-bar to which it is connected (see Figure 1.10, Figure 1.11 and Figure 1.12), therefore the most accurate harmonic model is a harmonic voltage source behind an impedance, as shown in Figure 4.1. The impedance in Figure 4.1 represents the series-reactor that is either modelled externally or internally to the PWM-converter model. The impedance of the internal series-reactor is considered in the equations of the harmonic voltage source model. In case of an MMC, half the value of the arm reactor (see eq. 91) is also considered in series with the series-reactor.

The harmonic voltage can be defined by selecting a *harmonic injection* on the Harmonics-page of the PWM-converter model and setting the model to *const. V*, as shown in Figure 4.2.

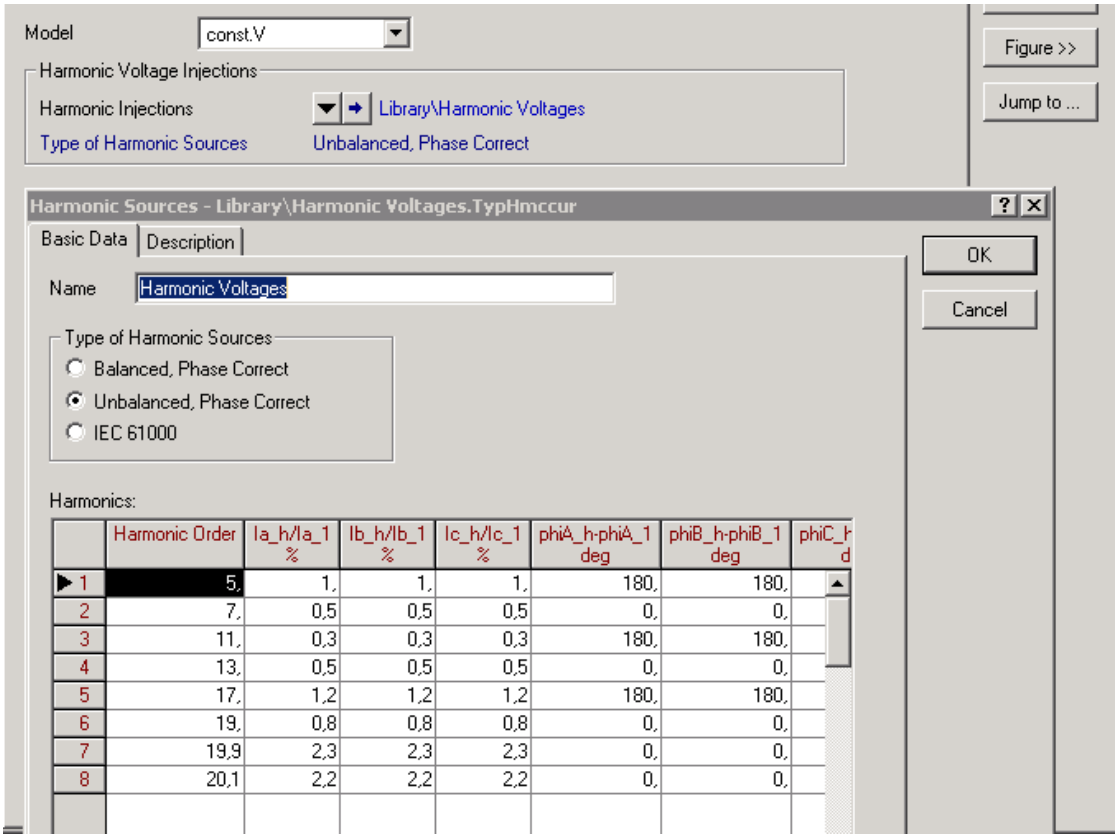


Figure 4.2: Harmonic voltage definition

To represent the converter in a more realistic way, a harmonic current type can be defined and the amplitude and angle of the harmonic currents can be defined as shown in Figure 4.2. Here

you can choose between a balanced and unbalanced representation. Notice that, even if a harmonic current type is used here, what is actually defined is the amplitude and angle for the harmonic voltages at the specified frequencies, relative to the positive sequence voltage from load flow. At the moment, it is not possible to define a harmonic voltage type for the PWM converter.

Especially inter-harmonics resulting from the modulations are typical for PWM converters. Figure 4.2 shows how to define these harmonics. The angle of the harmonic-spectrum-table is defined with reference to the fundamental frequency component of each phase assuming that a fundamental frequency component of zero degrees corresponds to a cosine-shape.

In many applications, harmonic injections are given as harmonic current injections at the converter's output. When setting the parameter model to *const. I* the PWM converter is modelled as a harmonic current source in parallel with an admittance. The harmonics tab allows to specify or select the harmonic sources object. The spectrum of harmonic infeeds may be entered according to one of two options: balanced or unbalanced. Also, the harmonic current can refer to either the Fundamental Current or to the Rated Current.

When modelled as an harmonic current source, the parallel admittance is determined by entering in the Harmonics page the values for positive, negative and zero sequence resistance and reactance. Positive sequence values (*r1hmc* and *x1hmc*) are used for harmonic frequencies of order 4, 7, 10, etc. Negative sequence values (*r2hmc* and *x2hmc*) are used for harmonic frequencies of order 2, 5, 8, etc. Zero sequence values (*r0hmc* and *x0hmc*) are used for harmonic frequencies of order 3, 6, 9, etc.

Note that these values of resistances and reactances (*r1hmc*, *x1hmc*, *r2hmc*, *x2hmc*, *r0hmc* and *x0hmc*) are used only when harmonic current source representation is selected. Instead, the voltage source model uses only the impedance of the series-reactor (i.e. for positive, negative and zero sequence).

It is possible to specify a frequency dependence for the sequence resistance and reactance, according to a polynomial characteristic. If no frequency dependence is specified, the resistance value is considered constant with respect to frequency, while the value of the reactance is considered proportional to frequency (i.e. the value of the inductance is considered constant with respect to frequency).

5 RMS-Simulation

For RMS-Simulation, the model is equivalent to the fundamental frequency model described in section 1.3. Sequence modelling of the PWM converter in RMS-simulations is done as described in sections 2.1, 2.2 and 2.3. A DC capacitance can be included internally in the two-level converter model during RMS-simulations.

Alternatively, the PWM can be represented as independent current/voltage sources on the AC and DC side. To use this model, the user has to select the *Independent AC and DC voltage/current source model* flag on the RMS or EMT data page. The model described in section 5.7 can be useful when the user wants to interface its own element and control model to the rest of the grid, without the need of creating a variation where the PWM would be replaced by voltage/current sources.

The control mode defined on the load flow page is available through the parameter *i_acdc*, which can be defined as output from the PWM slot in a frame and hence used in the DSL control if needed.

5.1 PWM Converter Control

Control is performed similarly for the two-level and the modular multilevel converters. The pulse width modulation index (magnitude and phase) can be defined in different ways, depending on the application:

- Pmr, Pmi: Real and imaginary part of the pulse width modulation index. Reference system is here the global reference-frame, which is usually defined by a reference-machine, external network or voltage source (or even a PWM-converter), therefore this set of inputs must always be used in combination with phase measurement devices (e.g. PLL) and reference-frame transformations.
- Pmd, Pmq, cosref, sinref: This set of input variables is convenient in grid-connected applications. It allows specifying a pulse-width modulation index-vector, with reference to a reference-system that is defined by cosref and sinref. A very common application is to measure the voltage angle using a PLL and to connect the output of a dq-current controller to Pmd and Pmq. The output of the PLL must be connected to cosref, sinref. This set of input variables avoids the explicit definition of reference-frame transformations.
- id_ref, iq_ref, cosref, sinref: as input variables reference values for the d- and q-axis currents can be used, when an internal current controller is defined on the RMS-simulation page (see also Figure 5.1). Similar to the previous set of input variables, the currents are defined with reference to a reference-system that is defined by cosref and sinref. Also here the explicit definition of transformation from local to global reference-frame is not needed.
- Pm_in, dphiu: Magnitude and phase of the pulse-width modulation index. This representation is fully equivalent to Pmr and Pmi (dphiu is expressed with reference to the global reference-frame).
- Pm_in, f0 (F0Hz): Pm_in defines the magnitude of the pulse-width modulation index. The frequency f0 allows varying the frequency of the output voltage. This is especially useful in variable speed-drive applications, in which a PWM-converter is used for driving an induction machine. The variable F0Hz can be used alternatively to f0 and defines the frequency in Hz (f0 is in p.u.).

The line-line RMS value of the PWM positive sequence internal voltage is calculated as:

$$\underline{U}_{AC1} = K_0 \cdot Pm \cdot U_{DC0} \cdot (cosphi + j \cdot sinphi) \tag{65}$$

The voltage U_{DC0} is determined, given the DC-link voltage U_{DC} and the converter losses, from the following equations:

$$\begin{aligned} I_{DC} &= I_{dp} + I_{cap} \\ V_{drop} &= sign(I_{DC}) \cdot swtLossFactor \cdot (1 - exp^{-200 \cdot |I_{DC}|}) \\ U_{DC0} &= U_{DC} + V_{drop} + resLossFactor \cdot I_{DC} \end{aligned} \tag{66}$$

where

- I_{cap} is the current flowing into the internally modelled DC-link capacitor, if any (or the equivalent DC-link capacitor for the MMC).
- I_{dp} is the current out of the positive DC-terminal.

For the definition of the voltage U_{DC0} for the MMC, refer to Figures 1.8 and 1.9.

Depending on the selected control inputs, Pm, $cosphi$ and $sinphi$ are calculated as described below (the angle $phiu$ is defined at the end of this section):

- Control inputs Pm_in, $f0$ ($F0Hz$) or Pm_in, $dphiu$ are used:

$$\begin{aligned} Pm &= Pm\_in \\ phiu1 &= phiu + dphiu \\ cosphi &= cos(phiu1) \\ sinphi &= sin(phiu1) \end{aligned}$$

- Control inputs Pmr, Pmi are used:

$$\begin{aligned} Pm &= \sqrt{Pmr^2 + Pmi^2} \\ cosphi &= Pmr/Pm \\ sinphi &= Pmi/Pm \end{aligned}$$

- Control inputs Pmd, Pmq are used:

$$\begin{aligned} Pm &= \sqrt{Pmd^2 + Pmq^2} \\ cosphi &= (Pmd \cdot cosu - Pmq \cdot sinu)/Pm \\ sinphi &= (Pmd \cdot sinu + Pmq \cdot cosu)/Pm \end{aligned}$$

- Control inputs id_ref, iq_ref are used:

$$\begin{aligned} Pm &= \sqrt{Pmd_{ctrl}^2 + Pmq_{ctrl}^2} \\ cosphi &= (Pmd_{ctrl} \cdot cosu - Pmq_{ctrl} \cdot sinu)/Pm \\ sinphi &= (Pmd_{ctrl} \cdot sinu + Pmq_{ctrl} \cdot cosu)/Pm \end{aligned}$$

Pmd_{ctrl} and Pmq_{ctrl} are calculated with a PI controller, according to Figure 5.1. The value of $cosu$ and $sinu$, which define the transformation between global- and dq-reference frames, depends on whether the input $cosref$ and $sinref$ are connected or not. When they are connected:

$$cosu = cosref$$
$$sinu = sinref$$

When they are not connected, the dq-transformation is defined by default with reference to the terminal voltage $\underline{U}_{bus1}$:

$$cosu = \Re(\underline{U}_{bus1})/|\underline{U}_{bus1}|$$
$$sinu = \Im(\underline{U}_{bus1})/|\underline{U}_{bus1}|$$

The angle $phiu$ is calculated depending whether $f0$, $F0Hz$ or none of them are connected:

- Input $f0$ is used:

$$\frac{d(phiu)}{dt} = 2 \cdot \pi \cdot Fnom \cdot (f0 - f_{ref})$$

- Input $F0Hz$ is used:

$$\frac{d(phiu)}{dt} = 2 \cdot \pi \cdot F0Hz - 2 \cdot \pi \cdot Fnom \cdot f_{ref}$$

- Input $f0$ and $F0Hz$ are not used (or no reference machine is defined in the system):

$$\frac{d(phiu)}{dt} = 0$$

where f_{ref} is the p.u. frequency of the reference machine in the system.

In addition, for RMS-simulations of the two-level converter the cell capacitor *Cdc* can be modelled internally and its value can be entered in the RMS dialogue. Note that for EMT-simulations of the two-level converter, the cell capacitor cannot be defined internally in the model.

5.2 Control of MMC

In RMS simulations, the half-bridge MMC is controlled in the same way as in section 5.1.

The full-bridge MMC is also controlled in the same way but it has one additional input, the insertion index DC bias mdc, which relates the equivalent arm capacitor voltage to the DC terminal voltage, see equation 6 and Figure 1.9. The insertion index DC bias must be adapted by the controller for example in case of operation with low DC voltage while continuing normal operation on the AC side. The equivalent arm capacitor voltage is also available as an output ($yUcell$) for control purposes.

5.3 Negative Sequence

In unbalanced RMS simulations, the PWM converter can be represented at the negative sequence as a constant impedance, a current source or a voltage source model.

5.3.1 Constant Impedance Model

The PWM converter is modelled at the negative sequence as an impedance, as described in section 2.2, when the available input to control the negative sequence current and voltage are not connected.

5.3.2 Current Source Model

It is available only if the built-in current controller is not used. The negative sequence current references have to be supplied through the input *i2d_ref* and *i2q_ref*. The following equations describe the behaviour of the negative sequence current source:

$$i2d\_ref = i2r \cdot cosu + i2i \cdot sinu \tag{67}$$

$$i2q\_ref = i2r \cdot sinu - i2i \cdot cosu \tag{68}$$

where $i2r$ and $i2i$ are the real and imaginary part of the negative sequence grid current in p.u. of the nominal converter current, $cosu$ and $sinu$ are defined as in section 5.1.

5.3.3 Voltage Source Model

It is available only if the built-in current controller is not used. The negative sequence voltage references have to be supplied through the input *u2r_in* and *u2i_in*. The following equations are used:

$$(u2r\_in + j \cdot u2i\_in) \cdot U_{nom} = \underline{U}_{bus2} + \underline{Z}_{sr} \cdot \underline{I}_{AC2} \tag{69}$$

$$(u2r\_in + j \cdot u2i\_in) \cdot U_{nom} = \underline{U}_{bus2} + (\underline{Z}_{sr} + \frac{\underline{Z}_{arm}}{2}) \cdot \underline{I}_{AC2} \tag{70}$$

where $\underline{Z}_{sr}$ is the series reactor impedance, $\underline{I}_{AC2}$ is the converter negative sequence current phasor, U_{nom} is the PWM nominal voltage defined in the Basic Data page and $\underline{U}_{bus2}$ is the bus negative sequence voltage phasor. The first equation is valid for a two-level converter, the second equation holds for an MMC. Note: in *PowerFactory* 2018, the negative sequence voltage input were based on the AC bus nominal voltage, $U_{bus,nom}$.

5.4 Zero Sequence

In unbalanced RMS simulations, the PWM converter can be represented at the zero sequence as a constant impedance or a voltage source model.

5.4.1 Constant Impedance Model

The PWM converter is modelled at zero sequence as an impedance, as described in section 2.3.

5.4.2 Voltage Source Model

The zero sequence voltage references have to be supplied through the input *u0r_in* and *u0i_in*. The following equations are used:

$$(u0r\_in + j \cdot u0i\_in) \cdot U_{nom} = \underline{U}_{bus0} + \underline{Z}_{sr0} \cdot \underline{I}_{AC0} \quad (71)$$

$$(u0r\_in + j \cdot u0i\_in) \cdot U_{nom} = \underline{U}_{bus0} + (\underline{Z}_{sr0} + \frac{\underline{Z}_{arm}}{2}) \cdot \underline{I}_{AC0} \quad (72)$$

where $\underline{Z}_{sr0}$ is the zero sequence series reactor impedance defined in section 2.3, $\underline{I}_{AC0}$ is the converter zero sequence current phasor, U_{nom} is the PWM nominal voltage defined in the Basic Data page and $\underline{U}_{bus0}$ is the bus zero sequence voltage phasor. The first equation is valid for a two-level converter, the second equation holds for an MMC.

5.5 Built-in Current Controller

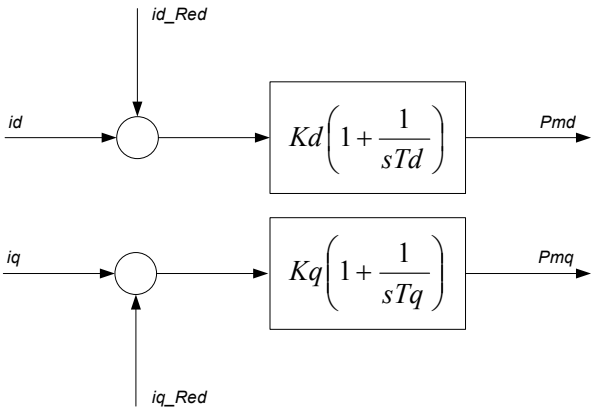


Figure 5.1: Block-diagram of the built-in current controller

In many applications, a dq-current controller is building the fastest stage of a PWM-converter-controller. Enabling the flag *Use Integrated Current Controller* enables the built-in controller according to Figure 5.1.

The input currents to the controller are the converter's AC-currents expressed in a reference frame that is defined by the input signals *cosref*, *sinref*. The output signals *Pmd* and *Pmq* are defined in the same reference frame and transformed back to a global reference frame using the same reference angle.

The current-references *id_ref* and *iq_ref* are available as additional input signals to the PWM-converter model.

If the integration time constants parameters of the built-in current controller are set to zero (Td=0s, Tq=0s), the controller is disabled and the converter output currents *id* and *iq* are set equal to the input variables *id_ref* and *iq_ref*. Hence the PWM converter is operating as a current source. Notice that if the input *id_ref* and *iq_ref* are used, but the *Use Integrated Current Controller* flag is not selected, the PWM is modelled as a controlled voltage source with *Pmr* and *Pmi* (or *Pmd* and *Pmq*) constant to their initial value.

5.6 Blocking Mode in RMS-simulations

For some applications it is desirable to consider the PWM converter as a non switched rectifier diode model. Using the input signal *block* the PWM model can be switched from a controlled IGBT mode to a non switched rectifier diode operating mode.

- Using parameter event (EvtParam):
  Name of Variable = *block*
- Connecting the *block* input signal
  block=1 ⇒ block (Diode Mode)
  block=0 ⇒ release blocking

5.6.1 Blocking Mode of Two-level Converter

In RMS simulations, the behaviour of the PWM converter during blocking mode is approximated in *PowerFactory* by using a two slope DC-current - DC-voltage characteristic, as shown in Figure 5.2. For low DC-currents, the operation mode is here referred to as “Regular Diode Mode”, while for high DC-currents the operation mode is here referred to as “High Current Diode Mode”. The condition for switching between the two modes is specified at the end of this section.

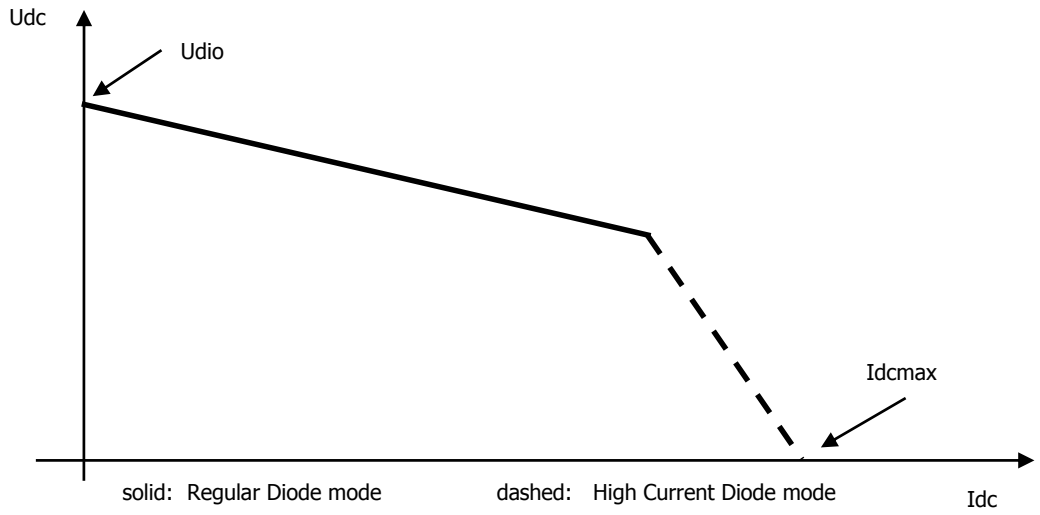


Figure 5.2: Blocking mode, two slope characteristic

When in “Regular diode mode”, the AC- and DC-side equivalent circuit diagrams of the converter are shown in Figure 5.3.

The commutation reactance (parameter *Xd*) can be defined in the RMS dialogue and it represents the total commutation reactance including the series reactor and the external transformer

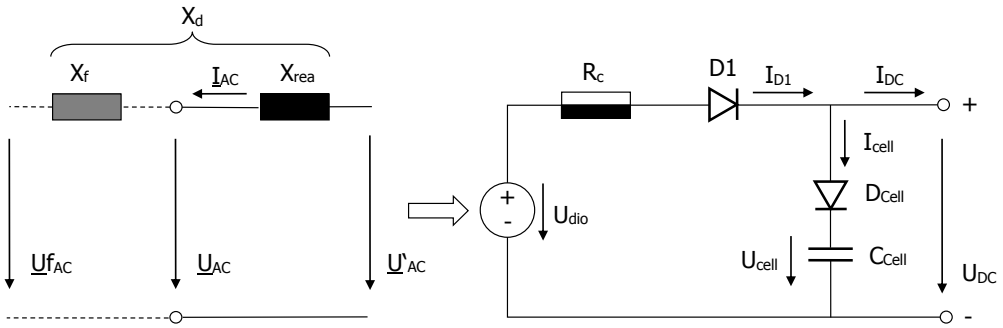


Figure 5.3: Equivalent circuit diagram (AC- and DC-side), regular diode mode

(for an MMC, the arm reactance must also be considered). *Xrea* is the reactance of the series reactor and is defined in the Basic data page through the parameters *uk* and *Pcu*. If the value defined by the user for the commutation reactance is lower than the reactance of the series reactor, this last value is used for the commutation reactance.

The equivalent commutating resistance is equal to:

$$R_c = \frac{3X_d}{\pi} \tag{73}$$

The commutation AC-voltage $\underline{U}f_{AC}$ is calculated as:

$$\underline{U}f_{AC} = \sqrt{3} \cdot (\underline{U}_{AC}/\sqrt{3} - j \cdot (X_d - X_{rea}) \cdot \underline{I}_{AC}) \tag{74}$$

The DC-voltage U_{di0} is calculated as follow:

$$U_{di0} = \frac{3\sqrt{2}}{\pi} \cdot |\underline{U}f_{AC}| \tag{75}$$

The DC-current is given by:

$$I_{D1} = \frac{U_{di0} - U_{DC}}{R_c} \tag{76}$$

In addition the following equations must be fulfilled:

$$U_{DC} \cdot I_{D1} = -P_{AC} \tag{77}$$

$$\sqrt{3} \cdot \underline{U}_{AC} \cdot \underline{I}^*_{AC} = P_{AC} + jQ_{AC} \tag{78}$$

The value of the reactive power Q_{AC} depends on the value of the overlap angle ol. Since for a diode rectifier the value of the ignition delay angle $\alpha = 0$, the cosinus of the overlap angle ($cos(ol)$) can be calculated as:

$$cos(ol) = cos(\alpha) - \frac{2 \cdot R_c \cdot I_{D1}}{U_{di0}} = 1 - \frac{2 \cdot R_c \cdot I_{D1}}{U_{di0}} \tag{79}$$

If $cos(ol) > 0.5$, corresponding to an overlap angle $ol < 60°$, the reactive power is calculated according to:

$$Q_{AC} = \sqrt{3} \cdot |\frac{4 \cdot k \cdot I_{D1} \cdot cos(\pi/6)}{\sqrt{(2)} \cdot \pi}| \cdot |\underline{U}f_{AC}| \cdot Q_{factor} \tag{80}$$

where

$$k = \frac{\sqrt{(cos(2 \cdot \alpha) - cos(2(\alpha + ol)))^2 + (2 \cdot ol + sin(2 \cdot \alpha) - sin(2(\alpha + ol)))^2}}{4(cos(\alpha) - cos(\alpha + ol))}$$

$$Q_{factor} = \frac{2 \cdot ol + sin(2 \cdot \alpha) - sin(2(\alpha + ol))}{4(cos(\alpha) - cos(\alpha + ol))}$$

When instead $cos(ol) < 0.5$, i.e. the overlap angle $ol > 60°$, the diode bridge is in an abnormal operating mode and the magnitude of the AC-current is calculated as:

$$|\underline{I}_{AC}| = I_{D1} \cdot Iac2Idc \tag{81}$$

where the factor *Iac2Idc* is calculated by using the equations of the “Regular Diode Mode”, an overlap angle of 60° ($cos(ol) = 0.5$) and assuming an AC-voltage of 1 p.u.

When in “High Current Diode Mode”, the equivalent circuit of the converter is shown in Figure 5.4.

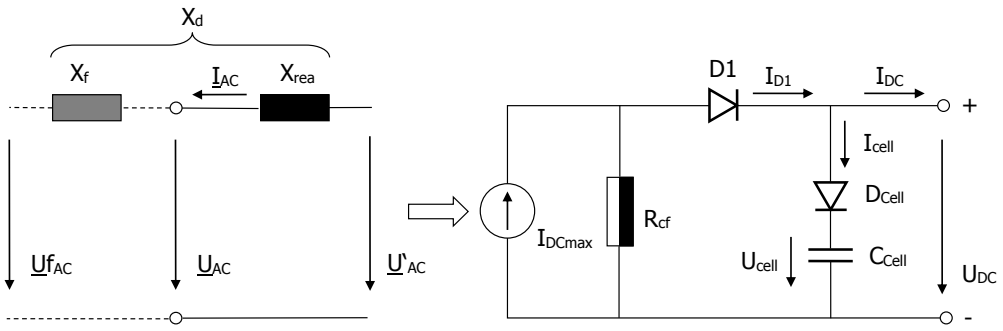


Figure 5.4: Equivalent circuit diagram (AC- and DC-side), high current diode mode

In this case, the equivalent commutating resistance is set equal to:

$$R_{cf} = 2 \cdot \sqrt{2} \cdot \frac{3}{\pi} \cdot X_d \tag{82}$$

The maximum DC-current is calculated as:

$$I_{DCmax} = \frac{\sqrt{2} \cdot |\underline{U}f_{AC}|}{\sqrt{3} \cdot X_d} \tag{83}$$

and the DC-current is thus given as:

$$I_{D1} = I_{DCmax} - \frac{U_{DC}}{R_{cf}} \tag{84}$$

The transition from “Regular Diode Mode” to “High Current Diode Mode” is done if the DC-current calculated assuming the regular diode mode according to Equation 76 is higher than the DC-current calculated for the high current diode mode according to Equation 84.

The diode “Dcell” in Figures 5.3 and 5.4 avoids the discharge of the cell capacitor during short-circuits on the DC-side. In cases where this function is not be implemented (tipically, applications with two-level converters), the DC-capacitor can be defined directly in the grid, externally to the PWM converter model.

5.6.2 Blocking Mode of MMC

During DC-faults causing high DC-currents, the submodules of the MMC with half-bridge configuration are blocked and sometimes shorted through a dedicated thyristor to avoid damaging the anti-parallel diodes. When all submodules are blocked, the half-bridge MMC can be represented by a six-pulse bridge diode rectifier as in the case of a two-level converter. Blocking of the half-bridge MMC during RMS simulations is implemented in a similar way as for the two-level converter, with the main difference that the equivalent DC-capacitor of the half-bridge MMC is disconnected, since all submodules are bypassed. The equations presented in section 5.6.1 are still valid, but the voltage U_{DC} should be replaced by $U_{DC} + U_{Zarm}$, with U_{Zarm} defined in equation 7.

The full-bridge MMC has the capability to block the DC current during DC-faults. This characteristic is due to the charging of the arm capacitors inserted in the circuit. This blocking characteristic is implemented in the RMS model of the full-bridge MMC by assuming that two arm capacitors (each charged at the voltage of the equivalent capacitor) are always inserted in the circuit during a DC fault. The equations presented in section 5.6.1 are still valid, but the voltage U_{DC} should be replaced by $U_{DC} + 2 \cdot U_{cap} + U_{Zarm}$, where U_{cap} is the equivalent arm capacitor voltage and U_{Zarm} is defined in equation 7.

If the value defined by the user for the commutation reactance is lower than the sum of the reactances of the series and arm reactors, this last value is used for the commutation reactance.

5.7 Independent AC and DC voltage/current source model

When the *Independent AC and DC voltage/current source model* flag on the RMS or EMT data page is selected, the PWM is represented by a simple model made up of a voltage or current source on the AC side and a voltage or current source on the DC side. The AC and DC sources are totally independent. The choice between voltage or current source is based on the input provided by the customer. This model assumes that the modelling of the converter element and

its control are performed externally. Thus, it allows interfacing custom models to the rest of the grid.

The following figures show how the voltage and current source are modelled and the corresponding input signals.

The impedance parameters can be defined on the RMS or EMT data page. Whenever dq-input are used the input signals *cosref* and *sinref* should also be provided, see section 5.1. The negative sequence current source model is equivalent to the one described in 5.3.2.

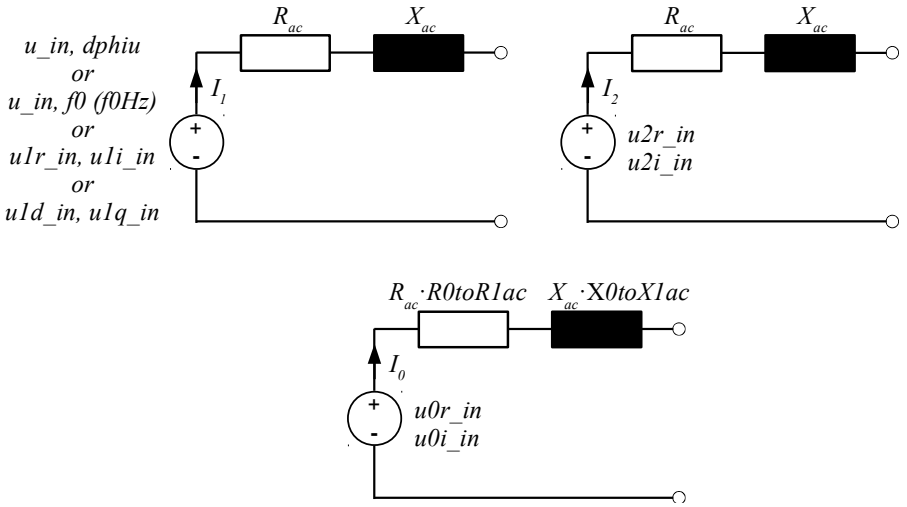


Figure 5.5: Positive, negative and zero sequence voltage source model (AC-side)

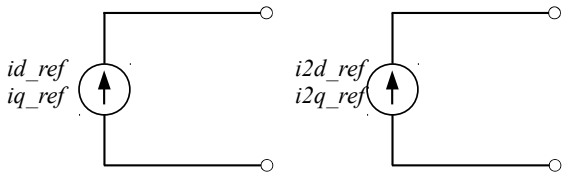


Figure 5.6: Positive and negative sequence current source model (AC-side)

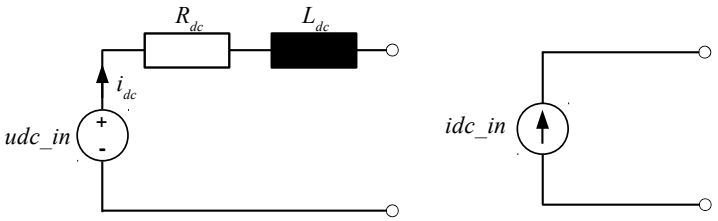


Figure 5.7: Voltage and current source model (DC-side)

6 EMT Simulation

For EMT-simulations of the **two-level converter**, there are two models available:

- *Controlled voltage source*: fundamental frequency model according to section 1.3, which is equivalent to the stability model according to section 5, including the built-in current controller.
- *Detailed model*: based on the circuit according to Figure 1.3. The valves are represented by switches having an on- and an off-resistance (Ron, Goff) and a snubber-circuit in parallel (see Figure 6.1).

Note that for EMT-simulations of the two-level converter, the cell capacitor cannot be defined internally in the model, but it must be defined explicitly as a separate element in the grid.

For EMT-simulations of the **MMC**, there are four models available:

- *Controlled voltage source*: as for the two-level converter.
- *Average value*: based on the circuit according to Figure 1.4. The valves are not represented explicitly. The AC-side is represented through controlled voltage sources including the harmonic content due to the switching according to the modulation method. The DC-side representation is based on power balance between AC-side, DC-side and converter losses, see Figures 1.8 and 1.9. An equivalent capacitor is used to model the total capacitance of the MMC, due to the submodule capacitors.
- *Aggregate arm*: based on the circuit according to Figure 1.4. The valves are not represented explicitly. Each arm of the MMC is averaged using a switching function and it is represented by one equivalent capacitor and a voltage source. Capacitor voltages of all submodules are assumed balanced. This model allows to conduct studies regarding circulating current and energy balancing phenomena.
- *Detailed equivalent circuit*: based on the circuit according to Figure 1.4. Each submodule is represented explicitly with its capacitor and valves. Each valve is represented by a two-value resistor, depending on the gate signal and on the arm current direction. The number of nodes within an arm is reduced in order to increase simulation speed. Each submodule is represented by a Thevenin equivalent and since all submodules in an arm are connected in series, a single Thevenin equivalent can be used to represent all submodules. A sorting algorithm is used in order to keep the capacitor voltages balanced among all submodules in an arm. This model is equivalent to a detailed representation of all valves, but runs much faster.

If the integration step size is too large, the two-level converter will automatically be set to *Control voltage source* model, since in this case it is not possible to accurately represent the switching. For the MMC *Average value* and *Aggregate arm* models, the modulation will be considered as “continuous” and a warning message is printed in the output window. Note that this check is not performed for the MMC *Detailed equivalent circuit* model.

In case of EMT-simulations of the *Detailed model* of the two-level converter and of the switched models of the MMC (when modulation is not “continuous”), it may be necessary to decrease the parameter *Resolution factor* to avoid incorrect switching events. The parameter *Resolution factor* can be found selecting the *Calculate Initial Conditions* (*ComInc*) command, under the *Solver Options - Advanced* tab.

Moreover, the *Independent AC and DC voltage/current source model* is available also for EMT simulations. The model has been introduced in section 6 and its input signals for EMT simulation are described in section 6.11.

As for RMS simulation, the control mode defined on the load flow page is available through the parameter *i_acdc*, which can be defined as output from the PWM slot in a frame and hence used in the DSL control if needed.

6.1 Detailed Model of Two-level Converter

The detailed model of the two-level converter is based on the circuit topology of Figure 1.3. The controlled valves are represented as switches with an on-resistance and an off-conductance with a snubber circuit in parallel, according to Figure 6.1. The anti-parallel diodes, which are not shown in Figure 6.1, are also represented as switches. The on-resistance and off-conductance (parameters *Ron* and *Goff*) are assumed equal for the controlled valves and the diodes.

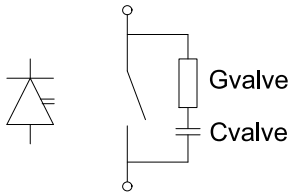


Figure 6.1: Valve represented as switch

For the detailed model and during EMT-simulations it is possible to get the capacitive voltage of the snubber circuit of the individual valve for each phase bridge using the following output signals:

- Upc_A: valve (thyristor) for phase A (AC) to ”+” DC path
- Upc_B: valve (thyristor) for phase B (AC) to ”+” DC path
- Upc_C: valve (thyristor) for phase C (AC) to ”+” DC path

- Umc_A: valve (thyristor) for phase A (AC) to ”-” DC path
- Umc_B: valve (thyristor) for phase B (AC) to ”-” DC path
- Umc_C: valve (thyristor) for phase C (AC) to ”-” DC path

In the current model, only two-level circuits can be simulated in detail. EMT-simulations with a detailed converter model are initialised from load-flow results. However, in general a flat initialisation of the detailed converter model from load-flow results is not possible, since the actual converter currents are not pure sinusoids.

6.1.1 Internal PWM triggering

The built-in trigger-circuit can be used to realize the PWM switching according to the selected modulation method using the specified modulation frequency:

- Sinusoidal modulation
- Rectangular modulation
- No modulation

When using the built-in trigger circuit, the same input signals as in the stability model can be used (including the built-in current-controller). For the detailed EMT model it is recommended to connect the signals *cosref*, *sinref* from an external PLL. In addition, only for the EMT detailed model, three input signals *urefA*, *urefB* and *urefC* defining the phase reference voltages are available for controlling the converter, with no need for the PLL input signals.

The built-in trigger circuit allows to represent the effects of dead-time in the converter valves, via a dedicated parameter *Tdeadtime* defined in the EMT dialogue page. The effects of dead-time modelling are mainly observed in the magnitude of the low-order harmonics of the output current.

6.1.2 External PWM triggering

The firing and blocking of the valves can be triggered from an external (DSL) model using one of the two following set of input signals:

- *u_a*, *u_b*, *u_c*
- *g1*, *g2*, *g3*, *g4*, *g5*, *g6*

The signals *u_a*, *u_b* and *u_c* control the output of a leg and not the state of each single controlled valve. They do not allow to introduce a dead-time between the turn-off and turn-on of the two controlled valves of the same leg. These signals define the on/off states of the three-phase legs of the converter according to the logic:

- A value higher than 0.5 indicates that the output is connected to the positive DC voltage.
- A value below 0.5 indicates that the output is connected to the negative DC voltage.

The signals *g1*, *g2*, *g3*, *g4*, *g5*, *g6* control the state of each individual controlled valve. Signals *g1*, *g4* refer to the upper and lower controlled valve in phase-a leg respectively; *g2*, *g5* refer to the upper and lower controlled valve in phase-b leg respectively; *g3*, *g6* refer to the upper and lower controlled valve in phase-c leg respectively. These signals allow non-standard PWM modulation techniques to be used. The signals define the on/off states of the controlled valve according to the logic:

- A value higher than 0.5 indicates that the valve is in the on-state.
- A value below 0.5 indicates that the valve is in the off-state.

6.2 MMC *Average value* model

The MMC *Average value* model (type 5) is based on the theory exposed in [1] and [2]. The valves are not represented explicitly and the AC side is represented through a controlled voltage source in each arm. The equations are derived with reference to Figure 1.4. The *Average value* model assumes that capacitor voltages of all submodules are equal, therefore no circulating currents flow between phase legs. The number of submodule capacitors inserted in each phase leg is always equal to the number of submodules per arm, N.

With reference to Figure 1.4, the following equations are valid for phase *a* of the modular multi-level converter:

$$u_a = -v_{ua} - R_{arm} \cdot i_{ua} - L_{arm} \cdot \frac{di_{ua}}{dt} + \frac{U_{DC}}{2} + u_{ng} \quad (85)$$

$$u_a = v_{la} + R_{arm} \cdot i_{la} + L_{arm} \cdot \frac{di_{la}}{dt} - \frac{U_{DC}}{2} + u_{ng} \quad (86)$$

$$i_a = i_{ua} - i_{la} \quad (87)$$

Assuming no circulating current flows in the converter arms, the upper and lower arm currents are:

$$i_{ua} = -i_{la} = \frac{i_a}{2} \quad (88)$$

Let

$$e_a = \frac{v_{la} - v_{ua}}{2} \quad (89)$$

Using the above equations, the relation between the terminal voltage, current and the converter voltages is expressed as:

$$e_a + u_{ng} = u_a + \frac{R_{arm}}{2} \cdot i_a + \frac{L_{arm}}{2} \cdot \frac{di_a}{dt} \quad (90)$$

Similar equations are valid for phase *b* and phase *c*. Transforming these equations into a static reference frame using alpha, beta and zero coordinates, the system is described by the uncoupled equations:

$$\underline{e}_{\alpha\beta} = \underline{u}_{\alpha\beta} + \frac{R_{arm}}{2} \cdot \underline{i}_{\alpha\beta} + \frac{L_{arm}}{2} \cdot \frac{d\underline{i}_{\alpha\beta}}{dt} \quad (91)$$

$$e_0 + u_{ng} = u_0 + \frac{R_{arm}}{2} \cdot i_0 + \frac{L_{arm}}{2} \cdot \frac{di_0}{dt} \quad (92)$$

If a series reactor is specified in the dialogue window (parameters uk and Pcu), its resistance and inductance are added in series with $R_{arm}/2$ and $L_{arm}/2$, respectively.

Reference signals for the controlled voltage sources in the lower arms of each phase (v_{la}, v_{lb} and v_{lc}) are generated internally given the input control signals. These reference signals are used to determine the number of inserted submodules in the lower arms, depending on the selected modulation technique. The number of inserted submodules in the upper arms are determined so to have always N submodule capacitors inserted in each leg. Reference [1] describes the three modulation techniques supported by the model.

The DC-side of the multilevel converter is modelled according to Figure 1.8 for a half-bridge MMC and according to Figure 1.9 for a full-bridge MMC, Power balance between AC-active power, DC-power and converter losses is assumed. All currents on the AC- and DC-side are

assumed positive when exiting the terminal. To account for the N submodule capacitors per arm, an equivalent capacitance C_{eq} is represented on the DC-side. This capacitance is calculated as [1]:

$$C_{eq} = \frac{6 \cdot C}{N} \tag{93}$$

where C is the capacitance of a single submodule and N is the number of submodules per arm.

The dynamics of the voltage on the DC-side during normal operation is determined as:

$$I_{cap} = C_{eq} \cdot \frac{dU_{cap}}{dt} \tag{94}$$

$$mdc \cdot U_{cap} = U_{DC} + U_{Zarm} \tag{95}$$

where U_{Zarm} is defined in equation 7 and $mdc = 1$ for a half-bridge MMC and $-1 < mdc < 1$ for a full-bridge MMC.

In the general case, a zero sequence AC-current may flow through the DC-side [2]. The positive DC-pole current I_{DCp} (assumed positive when exiting the terminal) is given as:

$$mdc \cdot I_{DCp} = -\frac{P_{losses} + P_{AC}}{U_{cap}} - I_{cap} - \frac{3 \cdot i_{AC0}}{2} \tag{96}$$

where $mdc = 1$ for a half-bridge MMC and $-1 < mdc < 1$ for a full-bridge MMC.

The relation between positive and negative DC-pole currents is given as:

$$I_{DCp} + I_{DCn} + 3 \cdot i_{AC0} = 0 \tag{97}$$

The instantaneous zero sequence current i_{AC0} in Equations 96 and 97 is considered only in EMT-simulations. Equation 96 assumes that i_{AC0} divides equally between positive and negative DC-poles.

6.3 MMC *Aggregate arm* model

The MMC *Aggregate arm* model is based on the theory exposed in [3]. The valves are not represented explicitly and each of the six arms is averaged using its switching function s_n defined as:

$$s_n = \frac{1}{N} \cdot \sum S_i \tag{98}$$

where N is the number of submodules per arm. $S_i = 0$ if the i_{th} submodule is turned off, $S_i = 1$ if the i_{th} submodule is inserted with positive polarity and $S_i = -1$ if the i_{th} submodule is inserted with negative polarity (only for the full-bridge model).

Assuming all submodule capacitors in one arm to be charged at the same voltage, the total voltage output from all the submodules will depend on their switching status and it is given by:

$$v_{SM} = s_n \cdot u_{cap} + k_N \cdot N \cdot R_{on} \cdot i_{arm} \tag{99}$$

where $k_N = 1$ for a half-bridge MMC and $k_N = 2$ for a full-bridge MMC and R_{on} is the on-state resistance of the switches.

The submodules capacitance in one arm is represented through an equivalent capacitor C_{eq}, calculated as:

$$C_{eq} = \frac{C}{N} \tag{100}$$

where C is the capacitance of a single submodule and N is the number of submodules per arm.

The current flowing in the equivalent capacitor per arm is zero if all submodules are bypassed while it is equal to the arm current if all submodules are inserted. The equivalent capacitor current is calculated as:

$$i_{cap} = s_n \cdot i_{arm} \tag{101}$$

Based on the above equations the equivalent circuit shown in Figure 6.2 can be used to represent the MMC. Each arm uses the above equations, with the corresponding switching function and arm quantities.

The voltage equations for the upper and lower arms are written for each phase ($k = a,b,c$) as:

$$u_{up,k} + R_{arm} \cdot i_{up,k} + L_{arm} \cdot \frac{di_{up,k}}{dt} + v_{SM,up,k} = \frac{U_{DC}}{2} + u_{ng} \tag{102}$$

$$u_{low,k} - R_{arm} \cdot i_{low,k} - L_{arm} \cdot \frac{di_{low,k}}{dt} - v_{SM,low,k} = -\frac{U_{DC}}{2} + u_{ng} \tag{103}$$

The current equations are:

$$i_k = i_{up,k} - i_{low,k} \tag{104}$$

$$I_{DCp} = \sum i_{up,k} \tag{105}$$

$$I_{DCp} + I_{DCn} + \sum i_k = 0 \tag{106}$$

The equivalent arm capacitor dynamics is according to the following equations:

$$C_{eq} \cdot \frac{du_{cap,up,k}}{dt} = i_{cap,up,k} \tag{107}$$

$$C_{eq} \cdot \frac{du_{cap,low,k}}{dt} = i_{cap,low,k} \tag{108}$$

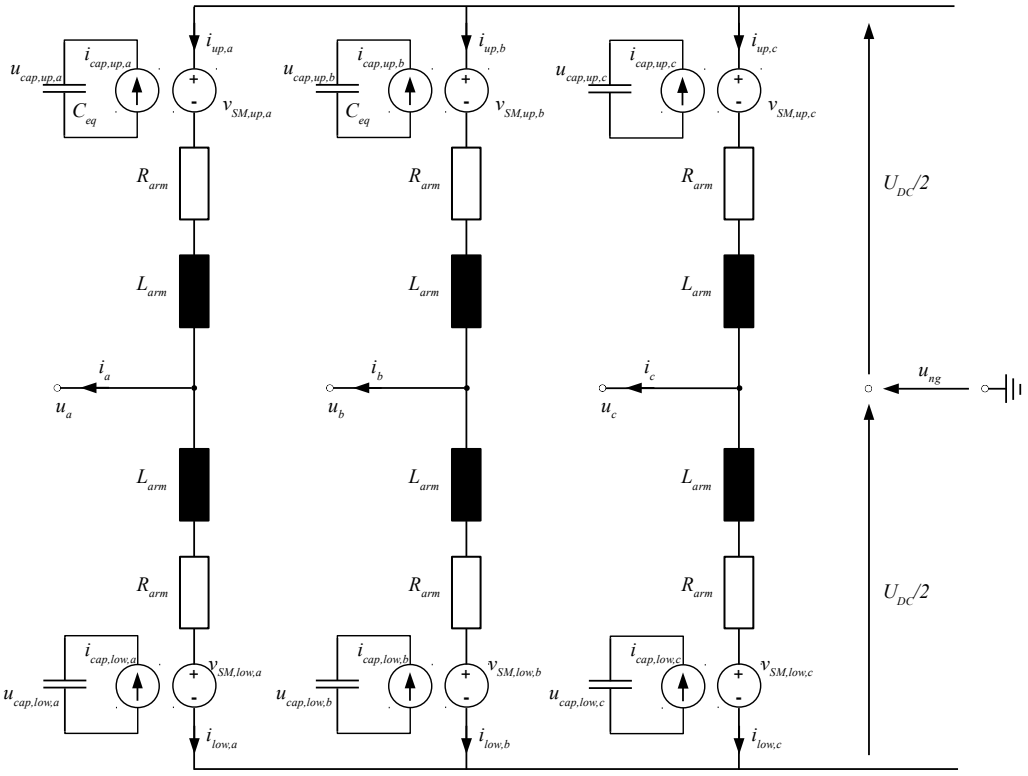


Figure 6.2: Equivalent circuit for the Aggregate arm model

In some applications a second harmonic filter can be used in each arm to reduced second harmonics in the circulating current [5]. The second harmonic filter is shown in the equivalent circuit in Figure 6.3. The filter is optional and can be selected for the *Aggregate arm* model on the *Advanced* tab of the *EMT* page, where the parameters *Lfilt* and *Cfilt* can be entered. The resistance of the filter, not shown in the figure, is calculated as $R_{filt} = L_{filt}/L_{arm} \cdot R_{arm}$. The following relations hold: $L_{arm1} + L_{filt} = L_{arm}$ and $R_{arm1} + R_{filt} = R_{arm}$.

When the filter is selected the above circuit equations are modified to account for the presence of the filter components.

The switching function is calculated per arm, given the control input and the selected modulation.

6.4 MMC *Detailed equivalent circuit* model

The MMC *Detailed equivalent circuit* model (type 4) is based on the theory exposed in [1]. Each submodule is represented explicitly with its capacitor voltage dynamics and its valves. Each valve is represented as a two valued resistance, one for the on-state and one for the off-state.

A Thevenin equivalent circuit is derived for each submodule. For a half-bridge submodule, the Thevenin resistance and voltage are given by

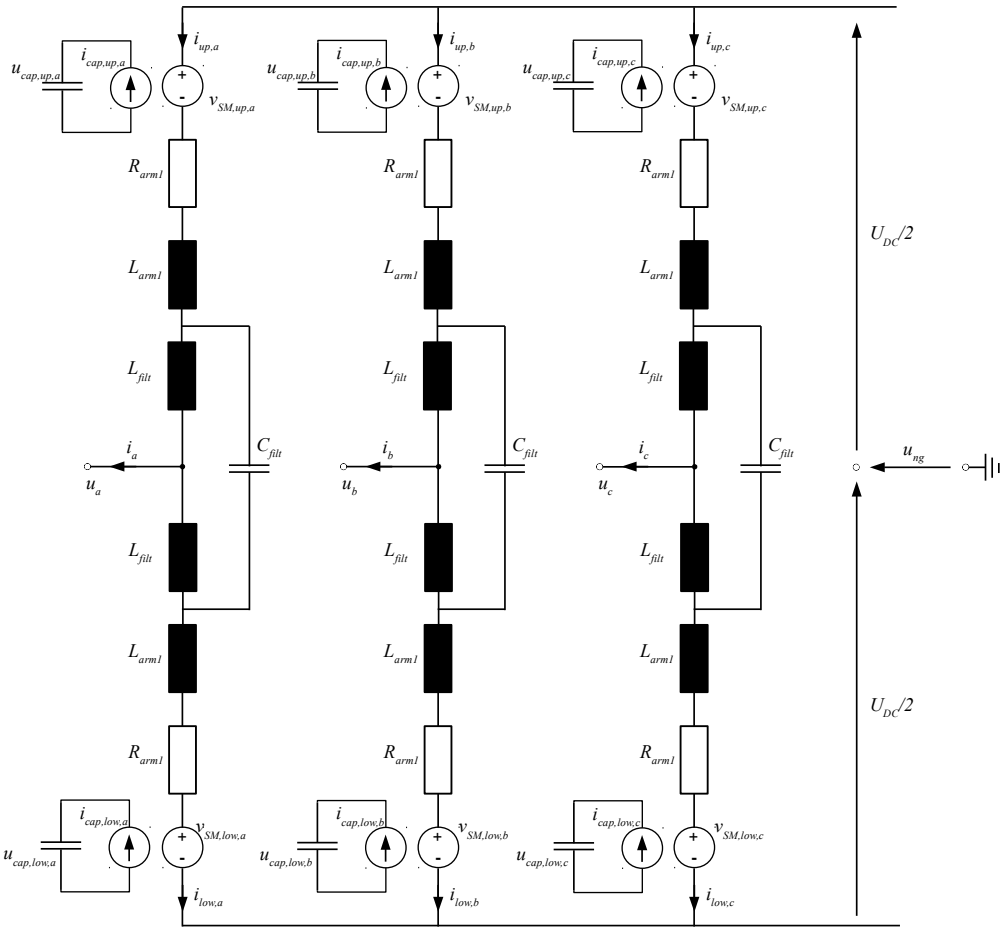


Figure 6.3: Equivalent circuit for the Aggregate arm model with 2nd harmonic filter

$$R_{submod} = \frac{R1 \cdot R2}{R1 + R2} \tag{109}$$

$$u_{submod} = \frac{R2}{R1 + R2} \cdot u_{cap} \tag{110}$$

where $R1$ ($R2$) is the resistance of the upper (lower) transistor in parallel with the upper (lower) diode.

In order to reduce the internal number of nodes, a Thevenin equivalent is derived for each arm by summing up the contribution for all submodules in that arm:

$$R_{Thev} = \sum_{j=1}^{N} R_{submod,j} \tag{111}$$

$$u_{Thev} = \sum_{j=1}^{N} u_{submod,j} \tag{112}$$

The total voltage output from all the submodules in an arm is given as:

$$v_{SM} = u_{Thev} + R_{Thev} \cdot i_{arm} \tag{113}$$

The voltage equations for the upper and lower arms are written for each phase ($k = a,b,c$) as:

$$u_{up,k} + R_{arm} \cdot i_{up,k} + L_{arm} \cdot \frac{di_{up,k}}{dt} + v_{SM,up,k} = \frac{U_{DC}}{2} + u_{ng} \tag{114}$$

$$u_{low,k} - R_{arm} \cdot i_{low,k} - L_{arm} \cdot \frac{di_{low,k}}{dt} - v_{SM,low,k} = -\frac{U_{DC}}{2} + u_{ng} \tag{115}$$

The current equations are:

$$i_k = i_{up,k} - i_{low,k} \tag{116}$$

$$I_{DCp} = \sum i_{up,k} \tag{117}$$

$$I_{DCp} + I_{DCn} + \sum i_k = 0 \tag{118}$$

The submodule capacitor dynamics is given by:

$$C \cdot \frac{du_{cap,j}}{dt} = i_{cap,j} \tag{119}$$

where for a half-bridge submodule $icap_j$ is calculated as:

$$i_{cap,j} = \frac{R2}{R1 + R2} \cdot i_{arm} - G_{cap} \cdot u_{cap,j} - \frac{u_{cap,j}}{R1 + R2} \tag{120}$$

G_{cap} represents the no-load losses for the capacitor.

The second harmonic filter is also available for the *Detailed equivalent circuit* model. Its modelling is the same as already described for the *Aggregate arm* model.

6.5 Control of *Controlled voltage source* model

The *Controlled voltage source* model in EMT-simulations is controlled in the same way as the RMS converter model, see section 5.1. The only difference is the definition of the angle $phiu$, which is now given as:

- Input $f0$ is used:

$$\frac{d(phiu)}{dt} = 2 \cdot \pi \cdot Fnom \cdot f0$$

- Input $F0Hz$ is used:

$$\frac{d(phiu)}{dt} = 2 \cdot \pi \cdot F0Hz$$

- Input $f0$ and $F0Hz$ are not used:

$$\frac{d(phiu)}{dt} = 2 \cdot \pi \cdot Fnom$$

The line-line RMS value of the converter internal voltage in the global stationary reference frame is:

$$\underline{u}_{\alpha\beta} = K_0 \cdot Pm \cdot U_{DC0} \cdot (cosphi + j \cdot sinphi) \quad (121)$$

For the MMC, K_0 is always calculated according to sinusoidal modulation. U_{DC0} is calculated according to Figures 1.8 and 1.9.

A zero sequence input, *Pm0*, for the pulse modulation index is also available. If *Pm0* is not connected, the PWM converter is represented at the zero sequence as described in 2.3. The additional zero sequence impedance $\underline{Z}_0$ is not considered for the controlled voltage source model when the input *Pm0* is connected. The controlled voltage source model is only valid for small *Pm0* values and the effect of *Pm0* on the saturation of the phase modulation indexes (Pma, Pmb, Pmc) is neglected. Whenever this effect cannot be neglected, simulation with the detailed model should be preferred.

6.6 Control of MMC *Average value* model

6.6.1 Control of half-bridge MMC *Average value* model

The half-bridge MMC *Average value* model can be controlled using the same control input as for the two-level converter. A zero sequence input, *Pm0*, for the pulse modulation index is

also available. In this case, the insertion indexes are generated internally and, depending on the selected modulation method, used for controlling the number of submodules (and thus the equivalent voltage sources) switched-on in the lower arms.

The insertion indexes for the lower arms can also be provided through input $nlow\_a$, $nlow\_b$, $nlow\_c$. The insertion index DC bias must be one for the half-bridge MMC *Average value* model.

Three modulation methods are available, *Phase-Shift PWM*, *Phase-Disposition PWM* and *Nearest Level Control*. Figures 6.4, 6.5 and 6.6 illustrate how the number of submodules switched-on in one arm is determined, according to the three different available modulation methods. In the considered example, the number of submodules per arm is $N = 4$. *Continuous modulation*, described in section 1.2, is also available.

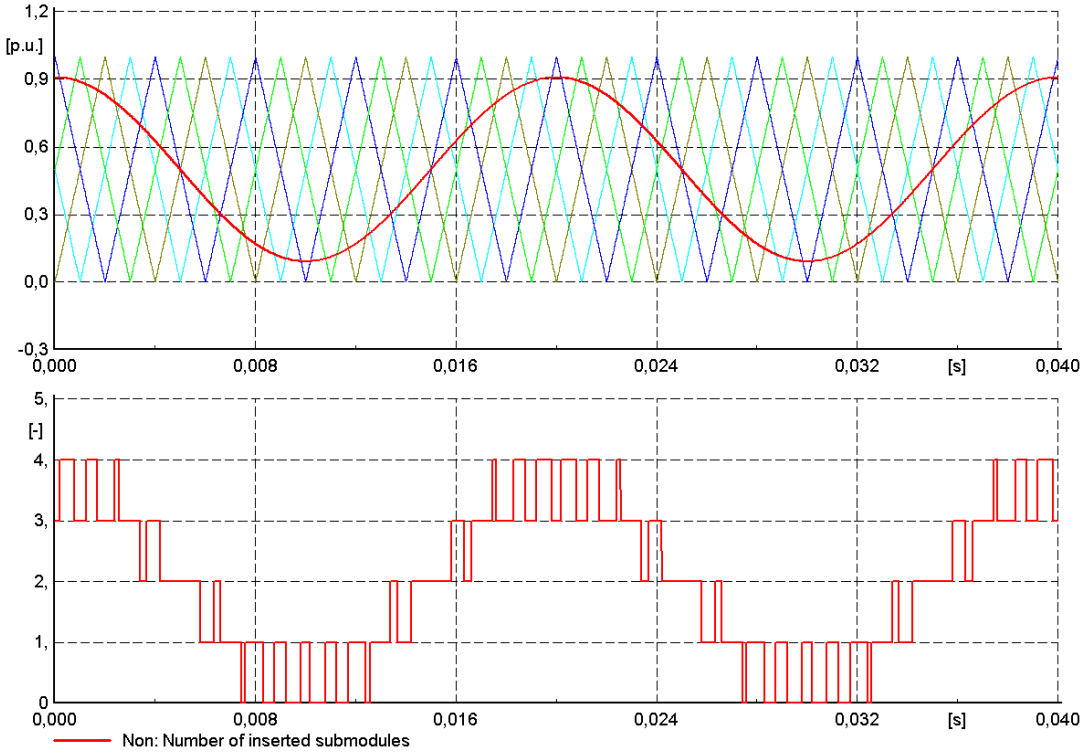


Figure 6.4: Number of lower arm submodules switched on according to Phase-Shift PWM

Alternatively, instead of using the available modulation methods the user can implement the modulation externally and directly control the number of switched-on submodules in the lower arms by providing the input signals N_{la}, N_{lb}, N_{lc}.

The number of inserted submodules in the upper arms are calculated so to always have N switched-on submodules per phase leg.

6.6.2 Control of full-bridge MMC *Average value* model

The full-bridge MMC *Average value* model can be controlled as explained in the previous section for the half-bridge MMC.

However, the insertion index DC bias for the full-bridge model can be varied, so that the equivalent arm capacitor voltage is decoupled from the DC terminal voltage, see Figure 1.9.

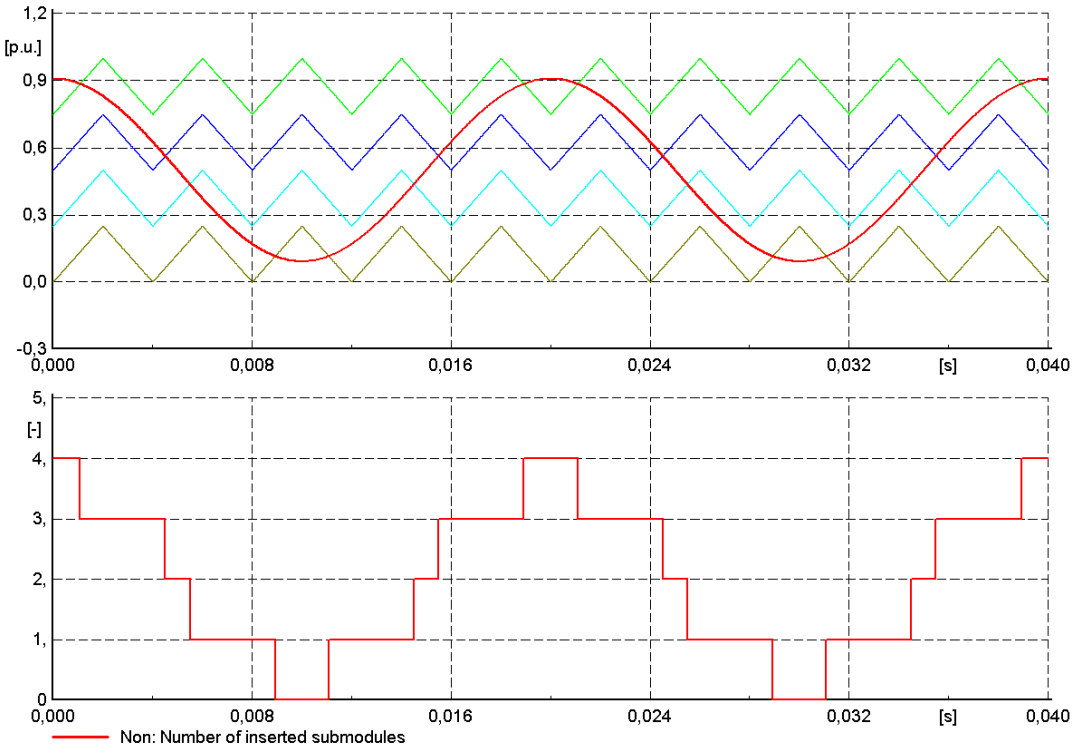


Figure 6.5: Number of lower arm submodules switched on according to Phase-Disposition PWM

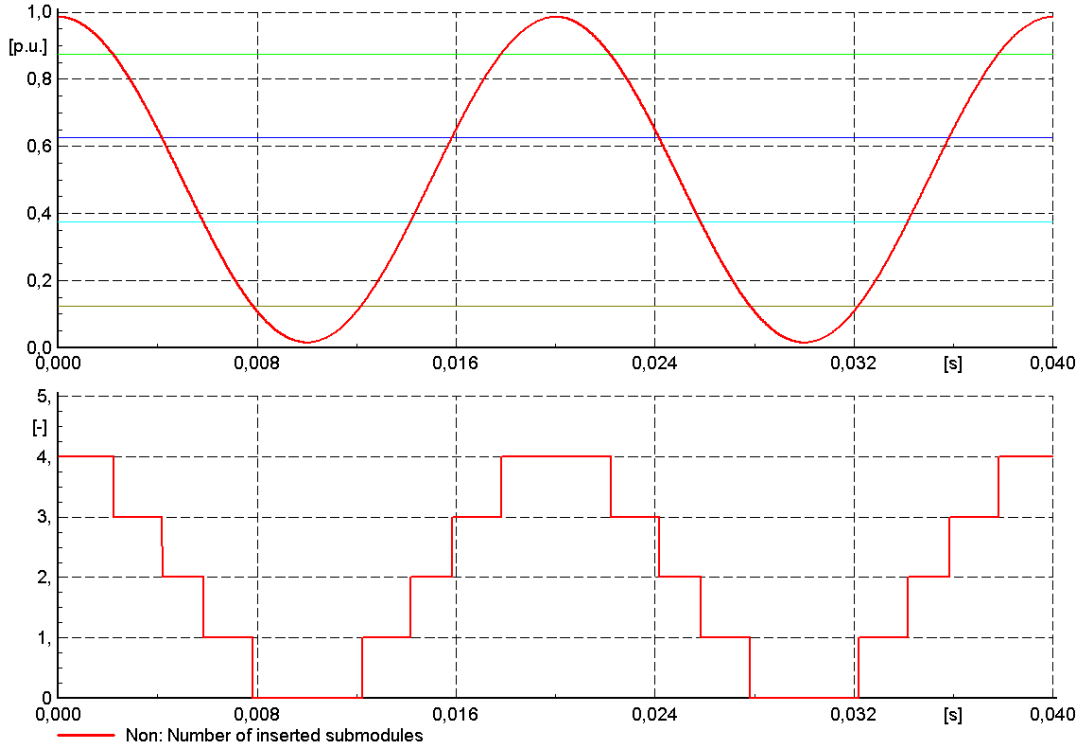


Figure 6.6: Number of lower arm submodules switched on according to Nearest Level Control

If the MMC is controlled through real and imaginary (or d- and q-axis) components of the pulse modulation factor in a similar way as for the two-level converter, the DC bias of the insertion index can be varied with the mdc input signal. In this case, the reference signals calculated internally and passed to the modulation module are:

$$ref_{low,a} = \frac{1}{2} \cdot (mdc + Pm0 + Pm \cdot cos(phiu)) \quad (122)$$

$$ref_{low,b} = \frac{1}{2} \cdot (mdc + Pm0 + Pm \cdot cos(phiu - 2/3 \cdot \pi)) \quad (123)$$

$$ref_{low,c} = \frac{1}{2} \cdot (mdc + Pm0 + Pm \cdot cos(phiu + 2/3 \cdot \pi)) \quad (124)$$

where Pm and $phiu$ are calculated as in section 6.5.

Alternatively, the input signals $nlow\_a$, $nlow\_b$, $nlow\_c$ or N_{la}, N_{lb}, N_{lc} can be used. The insertion index DC bias must still be provided for a full-bridge MMC. The DC bias can be varied between -1 and 1. For example, a negative N_{la} means that $|N_{la}|$ submodules are inserted with negative polarity in phase a lower arm.

For the full-bridge MMC *Average value* model the number of inserted submodules in the upper arm is calculated based on the assumption:

$$|N_{l,a}| + |N_{u,a}| = N \quad (125)$$

$$N_{l,a} + N_{u,a} = mdc \cdot N \quad (126)$$

6.7 Control of MMC *Aggregate arm* model

For the half-bridge and full-bridge MMC *Aggregate arm* model, the inserted number of submodules can be controlled independently for each of the six arms. Therefore, input signals for the upper arms are also available (nup_a, nup_b, nup_c or N_{ua}, N_{ub}, N_{uc}) along with the input signals for the lower arms described in section 6.6.

Alternatively, if the MMC is controlled through real and imaginary (or d- and q-axis) components of the pulse modulation factor in a similar way as for the two-level converter, the DC bias of the insertion index can be varied with the mdc_a, mdc_b, mdc_c input signals. This input signals may contain also fundamental frequency and second harmonic components, depending on the implemented control scheme for arm energy balancing or circulating current shaping. In this case, the reference signals calculated internally and passed to the modulation module are:

$$ref_{up,a} = \frac{1}{2} \cdot (mdc_a - Pm0 - Pm \cdot cos(phiu)) \quad (127)$$

$$ref_{up,b} = \frac{1}{2} \cdot (mdc_b - Pm0 - Pm \cdot cos(phiu - 2/3 \cdot \pi)) \quad (128)$$

$$ref_{up,c} = \frac{1}{2} \cdot (mdc_c - Pm0 - Pm \cdot cos(phiu + 2/3 \cdot \pi)) \quad (129)$$

$$ref_{low,a} = \frac{1}{2} \cdot (mdc_a + Pm0 + Pm \cdot cos(phiu)) \quad (130)$$

$$ref_{low,b} = \frac{1}{2} \cdot (mdc_b + Pm0 + Pm \cdot cos(phiu - 2/3 \cdot \pi)) \quad (131)$$

$$ref_{low,c} = \frac{1}{2} \cdot (mdc_c + Pm0 + Pm \cdot cos(phiu + 2/3 \cdot \pi)) \quad (132)$$

It is noted that for the half-bridge model, the mdc_a, mdc_b, mdc_c input signals (the same applies to the other input signals) might contain fundamental frequency and second harmonic components but reducing the DC component below 1 could result in loss of control of the current on the AC side. This is due to the fact that the half-bridge MMC cannot insert submodules with negative polarity and the generated AC voltage peak is reduced if the number of inserted submodules per arm is reduced.

6.8 Control of MMC *Detailed equivalent circuit*

For the half-bridge and full-bridge MMC *Detailed equivalent circuit* model, the inserted number of submodules can be controlled in exactly the same way as described for the *Aggregate arm* model. In case of Nearest Level Control or Phase-Disposition PWM, a sorting algorithm for the capacitor voltages is implemented internally in order to select which submodules are inserted. The sorting algorithm is applied whenever a switching action occurs. Sorting is performed based on the magnitude of all submodule capacitor voltages in an arm and on the arm current direction.

Alternatively, the half-bridge and full-bridge MMC *Detailed equivalent circuit* model can be controlled using the *gate* input signal, which is an array of signals for the state of each single valve. The MMC *gate* input signal must be connected through a vector of objects *IntVecobj* to the output of six (one per each arm) pulse generators *ElmPulsegen*. The ordering of the six pulse generators in the vector of objects must be the following: upper arm phase A, upper arm phase B, upper arm phase C, lower arm phase A, lower arm phase B and lower arm phase C. If the pulse generator is using *NLC* or *PD-PWM* modulation with sorting algorithm option selected, the submodule capacitor voltages of the MMC must be provided as input to the vector of objects. The submodule capacitor voltages are available as *Ucap* output signal from the PWM, with the same order for the arms as described above for the gates. The arm currents are also available as output from the PWM (for ex. *Iup_A*) and can be connected to the respective pulse generator. Summarizing, ia a control frame the vector of objects should have as output the signal *gate* connected to the MMC input signal *gate*. The vector of objects should have as input the signal *Ucap* connected to the output signal *Ucap* from the MMC. The MMC output arm current should be connected as input to the corresponding pulse generator *Iarm* input signal. Note that if in the pulse generators the sorting algorithm option is not selected, the *Ucap* and *Iarm* input signals to the pulse generator do not have to be connected.

For a large number of submodules, it is recommended to use the *Detailed equivalent circuit* along with six pulse generators, since the pulse generator offers the possibility to update the switch state of all valve with a fixed sampling time. This can result in faster simulations.

Please refer to the *ElmPulsegen* technical reference.

The submodule capacitor voltages are available as *Ucap* output signal. Each single submodule capacitor voltage is accessible for plotting. As an example, for an MMC with 10 submodules per arm in order to plot the capacitor voltage the following signals must be defined in the PWM variable selection (*IntMon*) editor:

- s:Ucap:0, first submodule, upper arm, phase A
- s:Ucap:1, second submodule, upper arm, phase A
- s:Ucap:10, first submodule, upper arm, phase B
- s:Ucap:12, third submodule, upper arm, phase B
- s:Ucap:20, first submodule, upper arm, phase C

- s:Ucap:30, first submodule, lower arm, phase A
- s:Ucap:40, first submodule, lower arm, phase B
- s:Ucap:50, first submodule, lower arm, phase C

The same is valid for the *gate* signals of the valves. As an example, for a half-bridge MMC with 10 submodules per arm in order to plot the gate signals of the valves the following signals must be defined in the PWM variable selection (*IntMon*) editor:

- s:gate:0, first valve, first submodule, upper arm, phase A
- s:gate:1, second valve, first submodule, upper arm, phase A
- s:gate:2, first valve, second submodule, upper arm, phase A
- s:gate:10, first valve, first submodule, upper arm, phase B
- s:gate:20, first valve, first submodule, upper arm, phase C
- s:gate:30, first valve, first submodule, lower arm, phase A
- s:gate:40, first valve, first submodule, lower arm, phase B
- s:gate:50, first valve, first submodule, lower arm, phase C

Note that the size of the *gate* signals is $2 * 6 * N$ for half-bridge configuration and $4 * 6 * N$ for full-bridge configuration, where N is the number of submodules per arm.

6.9 Built-in Current Controller

The built-in current controller described in section 5.5 is also available during EMT-simulations.

Both the two-level converter and the MMC *Controlled voltage source* models can be configured to behave as a current source. The built-in current controller must be selected and its parameters *Td* and *Tq* must be set to zero. Input *id_ref*, *iq_ref* and (optionally) *i2d_ref* and *i2q_ref* must be provided in this case. The equations describing the behaviour of the model are:

$$
\begin{aligned}
cos2u &= 2 \cdot cosu^2 - 1 \\
sin2u &= 2 \cdot sinu \cdot cosu \\
id &= id\_ref + (i2d\_ref \cdot cos2u + i2q\_ref \cdot sin2u) \\
iq &= iq\_ref + (-i2d\_ref \cdot sin2u + i2q\_ref \cdot cos2u)
\end{aligned}
$$

where *cosu* and *sinu* are calculated according to section 5.1. The possibility to inject a negative sequence current using the input signals *i2d_ref* and *i2q_ref* is available in EMT-simulations only when the PWM converter is modelled as a current source, i.e. *Controlled voltage source* model and the built-in current controller with parameters *Td* and *Tq* set to zero.

6.10 Blocking Mode in EMT-simulations

The *block* signal can be used to switch both the two-level and the MMC *Controlled voltage source* and *Average value* model to a detailed representation of a six-pulse diode rectifier. The diodes are represented as switches with on- and off-resistance (*Ron*,*Goff*).

In the case of the detailed model of a two-level converter, the specified snubber circuit is also included in the diode rectifier representation during blocking.

During blocking of the half-bridge MMC *Controlled voltage source* and *Average value* model, the equivalent capacitor on the DC-side is disconnected.

The full-bridge MMC has the capability to block the DC current during DC-faults. This characteristic is due to the charging of the arm capacitors inserted in the circuit. This blocking characteristic is implemented in the *Controlled voltage source* and *Average value* models of the full-bridge MMC by assuming that two arm capacitors (each charged at the voltage of the equivalent capacitor) are always inserted in the circuit during a DC fault.

The blocking for the MMC *Aggregate arm* model is based on the circuit in Figure 6.2, but the submodules in each arm are represented as in Figure 6.7, instead of a voltage source and an equivalent capacitor. It is noted that for the full-bridge MMC in blocking state, a DC fault causes the blocked submodule capacitors to charge and block the short-circuit current.

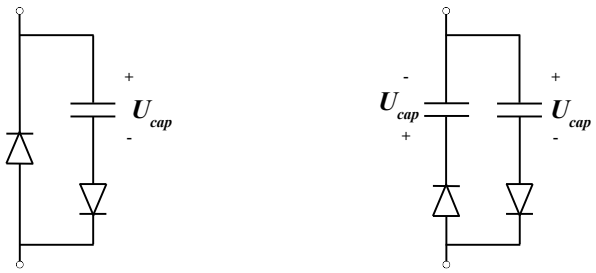


Figure 6.7: Equivalent circuit for half- and full-bridge submodules in blocking state

The blocking for the MMC *Detailed equivalent circuit* is based on representing explicitely each submodule in each block state.

6.11 Independent AC and DC voltage/current source model

This model has been already described in section 5. The following figures show how the voltage and current source are modelled and the corresponding input signals. The impedance parameters can be defined on the RMS or EMT data page. Whenever dq-input are used the input signals *cosref* and *sinref* should also be provided, see section 5.1.

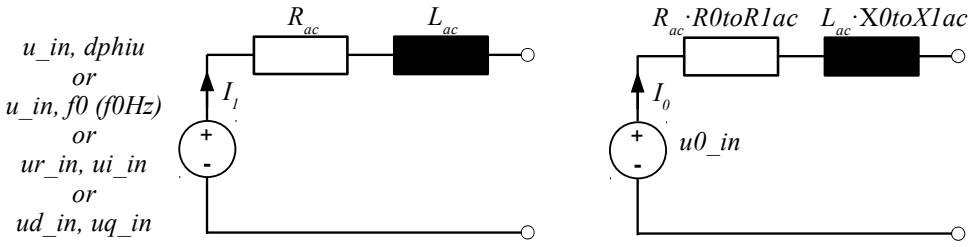


Figure 6.8: EMT alpha-beta-gamma (d-q-0) voltage source model (AC-side)

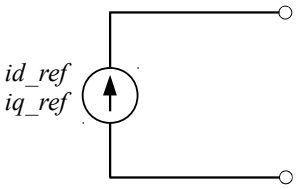


Figure 6.9: EMT current source model (AC-side)

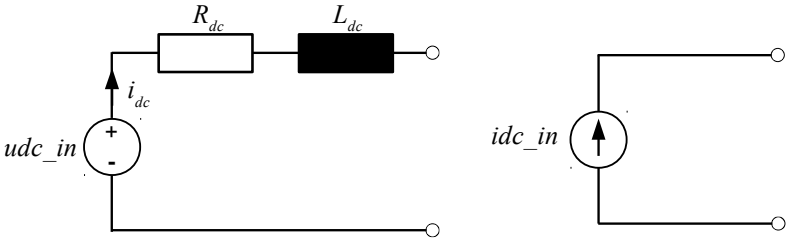


Figure 6.10: EMT voltage and current source model (DC-side)

7 Input/Output Definition of the Dynamic Model

7.1 Stability Model (RMS)

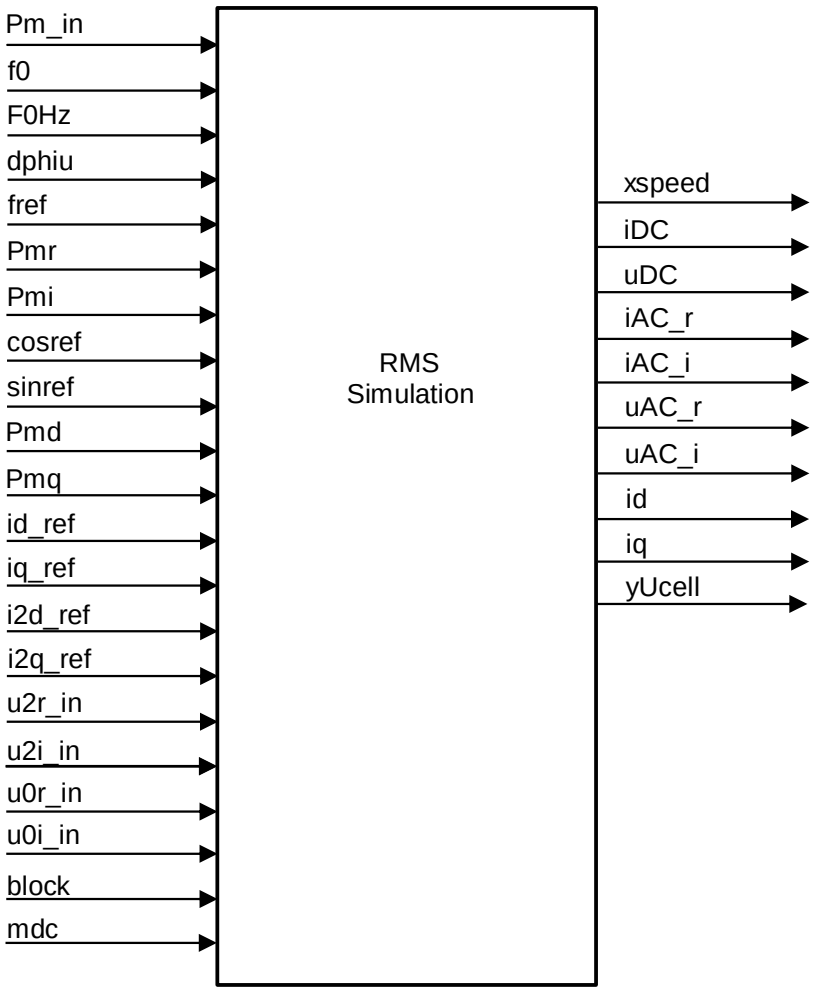


Figure 7.1: Input/Output definition of the PWM-converter model for stability analysis (RMS-simulation). The input $i2d\_ref$, $i2q\_ref$, $u2r\_in$, $u2i\_in$, $u0r\_in$, $u0i\_in$ are available only for unbalanced RMS simulations

7.2 Two-level Converter EMT Model

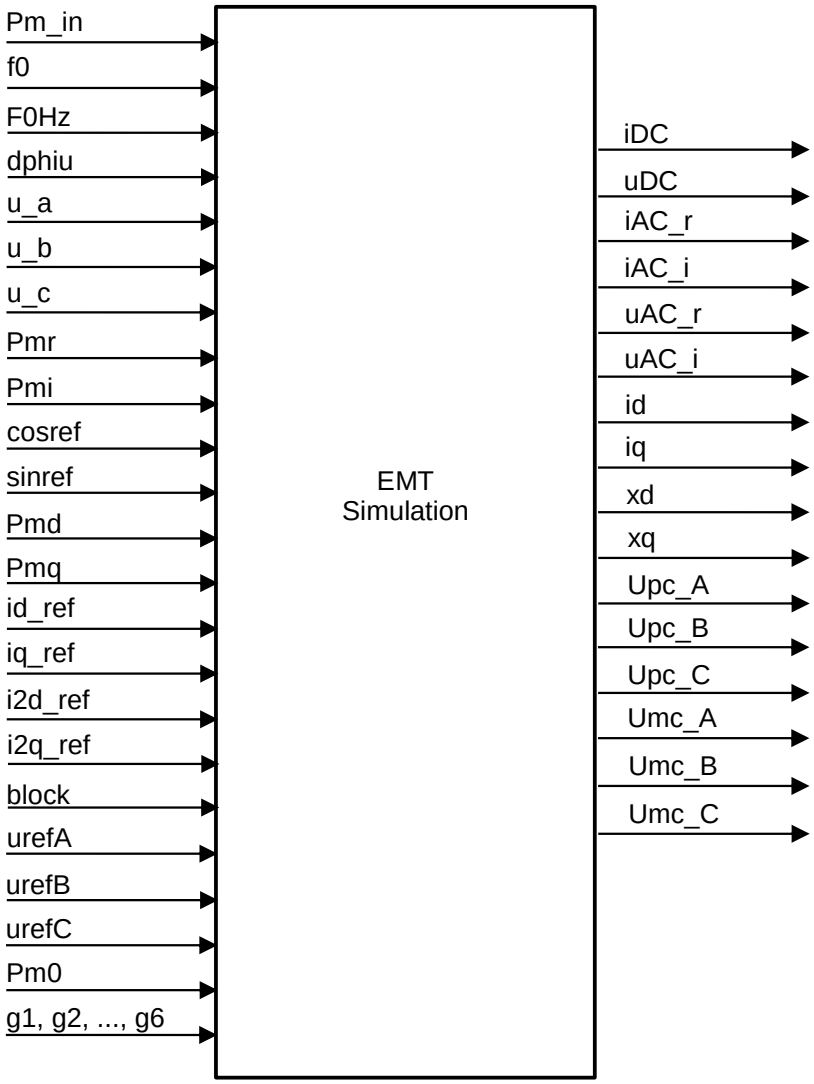


Figure 7.2: Input/Output definition of the two-level converter transient model (EMT-Simulation)

7.3 Modular Multilevel Converter, Average value model, EMT Model

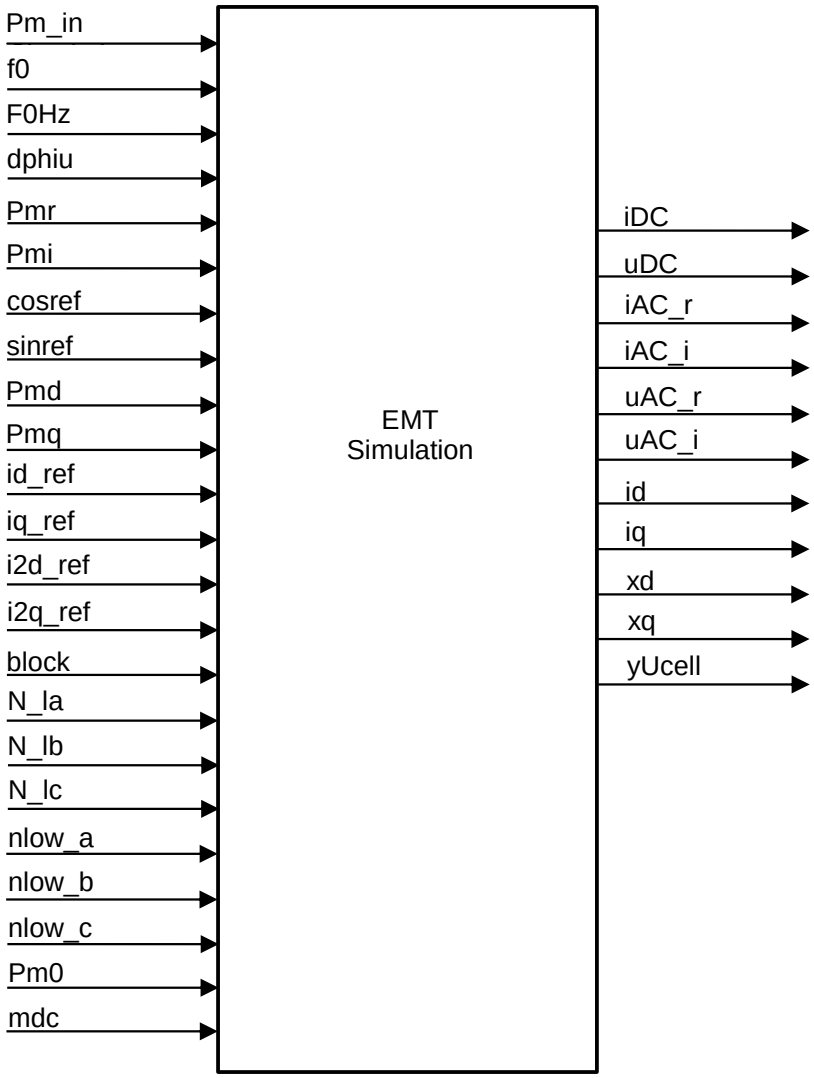


Figure 7.3: Input/Output definition of the MMC Average value model (EMT-Simulation)

7.4 Modular Multilevel Converter, Aggregate arm model, EMT Model

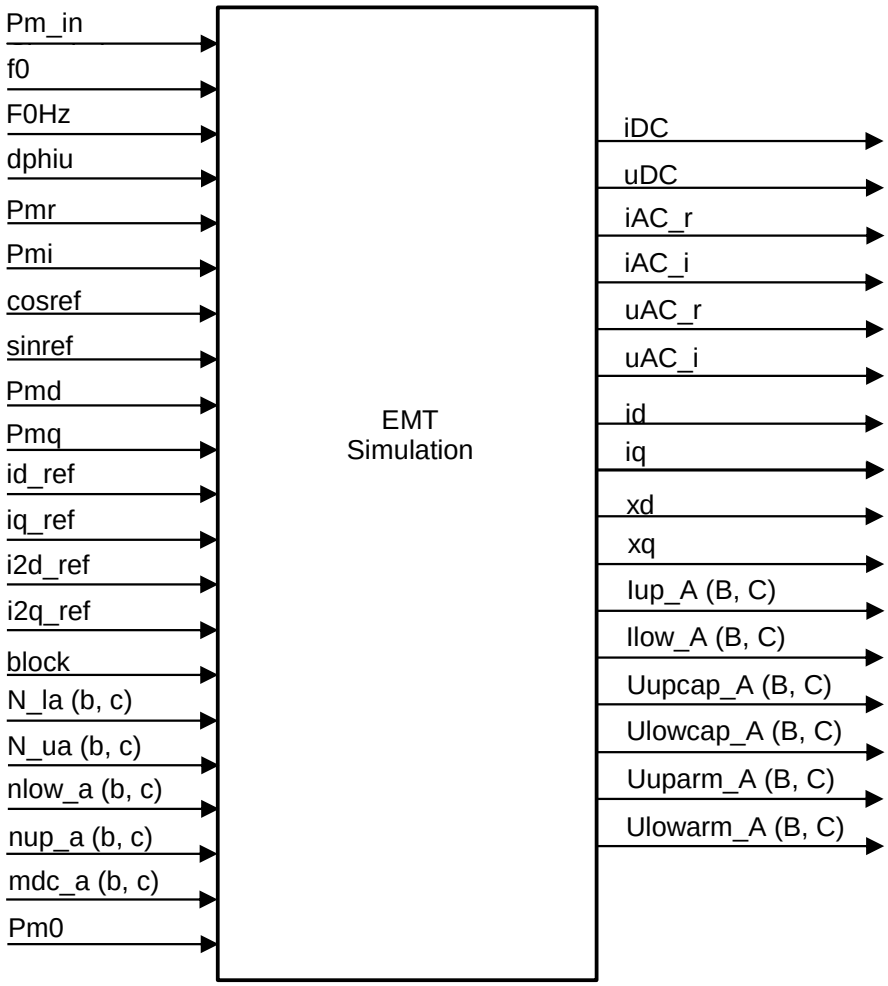


Figure 7.4: Input/Output definition of the MMC Aggregate arm model (EMT-Simulation)

7.5 Modular Multilevel Converter, Detailed equivalent circuit, EMT Model

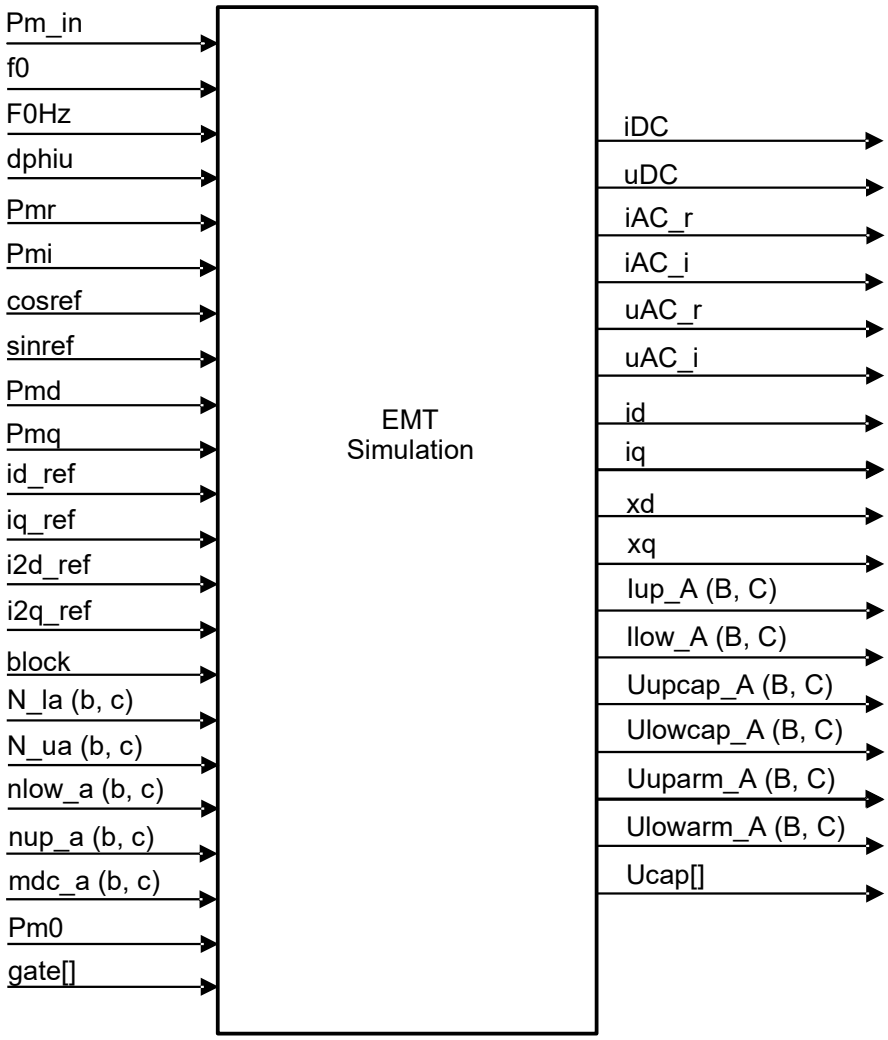


Figure 7.5: Input/Output definition of the MMC Detailed Equivalent circuit (EMT-Simulation)

A Parameters Definitions

Table A.1: Parameters of the PWM Converter

Parameter	Description	Unit
loc_name	Name	
busac	Terminal AC (StaCubic)	
busdp	Terminal DC+ (StaCubic)	
busdm	Terminal DC- (StaCubic)	
outserv	Out of service	
nparnum	Number of parallel converters	
Unom	Ratings: Rated AC-voltage	kV
Unomdc	Ratings: Rated DC-voltage (DC)	kV
Snom	Ratings: Rated power	MVA
uk	Series reactor: Short circuit impedance	%
Pcu	Series reactor: Copper losses	kW
R0toR1	Series reactor: R0/R1 ratio	
X0toX1	Series reactor: X0/X1 ratio	
vsctype	Converter type	
i_mod	Modulation (only two-level converter)	
Rarm	Arm reactor Resistance (only MMC)	Ohm
Larm	Arm reactor inductance (only MMC)	mH
iArmFilt	2nd-Harmonic Filter	
r0	Additional zero sequence impedance: Resistance	p.u.
x0	Additional zero sequence impedance: Reactance	p.u.
c_pmod	Model	
i_acdc	Control mode	
usetp	AC voltage setpoint	p.u.
usetpdc	DC voltage setpoint	p.u.
p_uctrldc	Controlled Node DC (ElmTerm*, StaBar*) (only ElmVscmono)	
pmsetp	PWM factor	p.u.
p_uctrl	Controlled node AC (ElmTerm*, StaBar*, ElmLdfctrl*)	
phisetp	Phase setpoint	deg
p_phictrl	Controlled node (ElmTerm*, StaBar*, ElmLdfctrl*)	
psetp	Active power setpoint	MW
qsetp	Reactive power setpoint	Mvar
pfsetp	Power factor setpoint	
pf_recap	Reactive factor inductive/capacitive	
p_pctrl	Controlled flow (StaCubic*)	
iQorient	Orientation +P/Q flow	
c_pstac	External station controller (StaCtrl*)	
Kpf	Prim. frequency bias	MW/Hz
c_psecc	External secondary controller (SecCtrl*)	
iVacMax	Consider modulation index limit	
Pmmax	Max. PWM factor	
Pnold	Losses: No-load losses	kW
swtLossFactor	Losses: Switching loss factor	kW/A
resLossFactor	Losses: Resistive loss factor	Ohm
iWindGen	Wind generator model	
idroop	DC-voltage dependent P-droop	
K	K	p.u./MW
iPphidrp	Angle difference dependent P-Droop	
Kpphi	Kpphi	MW/degree
p_b1phiu	Remote AC busbar (ElmTerm*)	
p_b2phiu	Local AC busbar (ElmTerm*)	

iPpart	Active power participation	
Kpart	Participation factor	
p_pmeas	P(AC) measured at (StaCubic*,ElmBoundary)	
considerPset	Consider active power setpoint	
pQlimType	Reactive power limits: Capability Curve (IntQlim)	
q_min	Reactive power limits: Min.	p.u.
q_max	Reactive power limits: Max.	p.u.
cQ_min	Reactive power limits: Min.	Mvar
cQ_max	Reactive power limits: Max.	Mvar
scaleQmin	Reactive power limits: Scaling factor (min.)	%
scaleQmax	Reactive power limits: Scaling factor (max.)	%
Pmin_uc	Active power operational limits: Min.	MW
Pmax_uc	Active power operational limits: Max.	MW
r2	Negative sequence impedance: Resistance	p.u.
x2	Negative sequence impedance: Reactance	p.u.
iNoShcContr	No short-circuit contribution	
iconfed	Static converter-fed drive	
Ikss	Fault contribution: Subtransient short-circuit current	kA
rtox	Fault contribution: R to X" ratio	
iShcModel	Fault contribution: short-circuit model	
Iks	Fault contribution: Transient short-circuit current	kA
Kfactor	Fault contribution: K factor	
imax	Fault contribution: Max. current	p.u.
r2shc	Negative sequence impedance: Resistance r2shc	p.u.
x2shc	Negative sequence impedance: Reactance x2shc	p.u.
iAstabint	A-stable integration algorithm	
i_ctrl	Use integrated current controller	
Kd	Current controller: Kd	
Td	Current controller: Td	s
Kq	Current controller: Kq	
Tq	Current controller: Tq	s
Cdc	Cell capacitor (only two-level converter)	uF
Xd	Commutation reactance	Ohm
mmcCmod	Submodule capacitance (only MMC)	uF
MmmcSM	Number of submodules per arm (only MMC)	
i_det	Model (only two-level converter)	
fmod	Modulation frequency (only two-level converter)	Hz
fmodMmc	Modulation frequency (only MMC)	Hz
Tdeadtime	Dead time (only two-level converter)	uS
Ron	Transistor/diode parameter: On-resistance	Ohm
Goff	Transistor/diode parameter: Off-conductance	uS
Cvalve	Transistor/diode parameter: Snubber capacitance (only two-level converter)	uF
Gvalve	Transistor/diode parameter: Snubber conductance (only two-level converter)	S
mmcModel	MMC model (only MMC)	
mmcModType	Modulation method (only MMC)	
iZarmDCside	Consider arm reactor on DC side	
Lfilt	2nd-harmonic filter inductance	
Cfilt	2nd-harmonic filter capacitance	
iVIsource	Independent AC and DC voltage/current source model	
Rac	AC resistance	Ohm
Lac	AC inductance	mH
R0toR1ac	R0/R1 ratio	
X0toX1ac	X0/X1 ratio	
Rdc	DC resistance	Ohm

Ldc	DC inductance	mH
ictrltp	Model	
1:phmc	Harmonic Voltages (TypHmccur)	
icurref	Harmonic Current Injections: Harmonic currents referred to	
r1hmc	Harmonic Current Injections Norton Equivalent: Resistance r1h	p.u.
x1hmc	Harmonic Current Injections Norton Equivalent: Reactance x1h	p.u.
fcharr1	Harmonic Current Injections Norton Equivalent: Frequency-Dependence, r1h(f) (ChaPol, ChaVec, ChaMat)	
fcharx1	Harmonic Current Injections Norton Equivalent: Frequency-Dependence, x1h(f) (ChaPol, ChaVec, ChaMat)	
r2hmc	Harmonic Current Injections Norton Equivalent: Resistance r2h	p.u.
x2hmc	Harmonic Current Injections Norton Equivalent: Reactance x2h	p.u.
fcharr2	Harmonic Current Injections Norton Equivalent: Frequency-Dependence, r2h(f) (ChaPol, ChaVec, ChaMat)	
fcharx2	Harmonic Current Injections Norton Equivalent: Frequency-Dependence, x2h(f) (ChaPol, ChaVec, ChaMat)	
r0hmc	Harmonic Current Injections Norton Equivalent: Resistance r0h	p.u.
x0hmc	Harmonic Current Injections Norton Equivalent: Reactance x0h	p.u.
fcharr0	Harmonic Current Injections Norton Equivalent: Frequency-Dependence, r0h(f) (ChaPol, ChaVec, ChaMat)	
fcharx0	Harmonic Current Injections Norton Equivalent: Frequency-Dependence, x0h(f) (ChaPol, ChaVec, ChaMat)	
pFlicker	Flicker Contribution: Flicker Coefficients (TypFlicker)	
cTypHmc	Harmonic Current Injections: Type of Harmonic Sources	
Inom	Harmonic Current Injections: Rated Current	kA

B Signals Definitions, Two-level Converter

Table B.1: I/O Signals of the Two-level PWM-converter model

Name	Description	Unit	Type	Model
Pm_in	Pulse-width modulation index, Mag.		IN	RMS, EMT
f0	Input frequency		IN	RMS, EMT
F0Hz	Input frequency (in Hz)	Hz	IN	RMS, EMT
dphiu	Voltage angle (input)	rad	IN	RMS, EMT
phiu	Voltage angle	rad	STATE	RMS, EMT
fref	Reference frequency	p.u.	IN	RMS
Pmr	Pulse-width modulation index, Real Part		IN	RMS, EMT
Pmi	Pulse-width modulation index, Imag. Part		IN	RMS, EMT
cosref	cos of reference angle		IN	RMS, EMT
sinref	sin of reference angle		IN	RMS, EMT
Pmd	Pulse-width modulation index, d-axis		IN	RMS, EMT
Pmq	Pulse-width modulation index, q-axis		IN	RMS, EMT
id_ref	Current reference, d-axis	p.u.	IN	RMS, EMT
iq_ref	Current reference, q-axis	p.u.	IN	RMS, EMT
i2d_ref	Negative sequence current reference, d-axis	p.u.	IN	RMS, EMT
i2q_ref	Negative sequence current reference, q-axis	p.u.	IN	RMS, EMT
u2r_in	Negative Sequence Voltage Input, Real Part	p.u.	IN	RMS
u2i_in	Negative Sequence Voltage Input, Imaginary Part	p.u.	IN	RMS
u0r_in	Zero Sequence Voltage Input, Real Part	p.u.	IN	RMS
u0i_in	Zero Sequence Voltage Input, Imaginary Part	p.u.	IN	RMS
Pm0	Pulse-modulation factor (zero sequence)		IN	EMT
u_a	Firing signal, Phase A (only two-level converter)	p.u.	IN	EMT
u_b	Firing signal, Phase B (only two-level converter)	p.u.	IN	EMT
u_c	Firing signal, Phase C (only two-level converter)	p.u.	IN	EMT
urefA	Reference voltage, Phase A (only two-level converter)	p.u.	IN	EMT
urefB	Reference voltage, Phase B (only two-level converter)	p.u.	IN	EMT
urefC	Reference voltage, Phase C (only two-level converter)	p.u.	IN	EMT
g1	Firing signal, T1 (only two-level converter)	p.u.	IN	EMT
g2	Firing signal, T2 (only two-level converter)	p.u.	IN	EMT
g3	Firing signal, T3 (only two-level converter)	p.u.	IN	EMT
g4	Firing signal, T4 (only two-level converter)	p.u.	IN	EMT
g5	Firing signal, T5 (only two-level converter)	p.u.	IN	EMT
g6	Firing signal, T6 (only two-level converter)	p.u.	IN	EMT
block	Blocking	p.u.	IN	RMS, EMT
xspeed	Voltage frequency (output)	p.u.	OUT	RMS
uDC	DC-voltage	p.u.	OUT	RMS, EMT
iAC_r	AC-current, real part	p.u.	OUT	RMS, EMT
iAC_i	AC-current, imag. part	p.u.	OUT	RMS, EMT
uAC_r	AC-voltage, real part	p.u.	OUT	RMS, EMT
uAC_i	AC-voltage, imag. part	p.u.	OUT	RMS, EMT
id	AC-current, d-Axis	p.u.	OUT	RMS, EMT
iq	AC-current, q-Axis	p.u.	OUT	RMS, EMT
xd	Current controller d-axis, state variable	p.u.	STATE, OUT	RMS, EMT

xq	Current controller q-axis, state variable	p.u.	STATE, OUT	RMS, EMT
Ucell	Voltage across cell capacitor	kV	STATE	RMS
Upc_A	Capacitive voltage, TpA	kV	OUT	EMT
Upc_B	Capacitive voltage, TpB	kV	OUT	EMT
Upc_C	Capacitive voltage, TpC	kV	OUT	EMT
Umc_A	Capacitive voltage, TmA	kV	OUT	EMT
Umc_B	Capacitive voltage, TmB	kV	OUT	EMT
Umc_C	Capacitive voltage, TmC	kV	OUT	EMT

C Signals Definitions, MMC Average value model

Table C.1: I/O Signals of the MMC Average value model

Name	Description	Unit	Type	Model
Pm_in	Pulse-width modulation index, Mag.	p.u.	IN	RMS, EMT
f0	Input frequency		IN	RMS, EMT
F0Hz	Input frequency (in Hz)	Hz	IN	RMS, EMT
dphiu	Voltage angle (input)	rad	IN	RMS, EMT
phiu	Voltage angle	rad	STATE	RMS, EMT
fref	Reference frequency	p.u.	IN	RMS
Pmr	Pulse-width modulation index, Real Part		IN	RMS, EMT
Pmi	Pulse-width modulation index, Imag. Part		IN	RMS, EMT
Pm0	Pulse-modulation factor (zero sequence)		IN	EMT
cosref	cos of reference angle		IN	RMS, EMT
sinref	sin of reference angle		IN	RMS, EMT
Pmd	Pulse-width modulation index, d-axis		IN	RMS, EMT
Pmq	Pulse-width modulation index, q-axis		IN	RMS, EMT
id_ref	Current reference, d-axis	p.u.	IN	RMS, EMT
iq_ref	Current reference, q-axis	p.u.	IN	RMS, EMT
i2d_ref	Negative sequence current reference, d-axis	p.u.	IN	RMS, EMT
i2q_ref	Negative sequence current reference, q-axis	p.u.	IN	RMS, EMT
u2r_in	Negative Sequence Voltage Input, Real Part	p.u.	IN	RMS
u2i_in	Negative Sequence Voltage Input, Imaginary Part	p.u.	IN	RMS
u0r_in	Zero Sequence Voltage Input, Real Part	p.u.	IN	RMS
u0i_in	Zero Sequence Voltage Input, Imaginary Part	p.u.	IN	RMS
block	Blocking	p.u.	IN	RMS, EMT
xspeed	Voltage frequency (output)	p.u.	OUT	RMS
uDC	DC-voltage	p.u.	OUT	RMS, EMT
iAC_r	AC-current, real part	p.u.	OUT	RMS, EMT
iAC_i	AC-current, imag. part	p.u.	OUT	RMS, EMT
uAC_r	AC-voltage, real part	p.u.	OUT	RMS, EMT
uAC_i	AC-voltage, imag. part	p.u.	OUT	RMS, EMT
id	AC-current, d-Axis	p.u.	OUT	RMS, EMT
iq	AC-current, q-Axis	p.u.	OUT	RMS, EMT
xd	Current controller d-axis, state variable	p.u.	STATE, OUT	RMS, EMT
xq	Current controller q-axis, state variable	p.u.	STATE, OUT	RMS, EMT
Ucell	Voltage across DC side equivalent capacitor	kV	STATE	RMS, EMT
yUcell	Voltage across cell capacitor, output	kV	OUT	RMS, EMT
N_la	Number of submodules (lower arm), phase A		IN	EMT
N_lb	Number of submodules (lower arm), phase B		IN	EMT
N_lc	Number of submodules (lower arm), phase C		IN	EMT
nlow_a	Insertion index (lower arm), phase A		IN	EMT
nlow_b	Insertion index (lower arm), phase B		IN	EMT
nlow_c	Insertion index (lower arm), phase C		IN	EMT
mdc	Insertion index, DC-bias		IN	RMS, EMT

D Signals Definitions, MMC Aggregate arm model and Detailed equivalent circuit

Table D.1: I/O Signals of the MMC Aggregate arm model and Detailed equivalent circuit

Name	Description	Unit	Type	Model
Pm_in	Pulse-width modulation index, Mag.	p.u.	IN	RMS, EMT
f0	Input frequency		IN	RMS, EMT
F0Hz	Input frequency (in Hz)	Hz	IN	RMS, EMT
dphiu	Voltage angle (input)	rad	IN	RMS, EMT
phiu	Voltage angle	rad	STATE	RMS, EMT
fref	Reference frequency	p.u.	IN	RMS
Pmr	Pulse-width modulation index, Real Part		IN	RMS, EMT
Pmi	Pulse-width modulation index, Imag. Part		IN	RMS, EMT
Pm0	Pulse-modulation factor (zero sequence)		IN	EMT
cosref	cos of reference angle		IN	RMS, EMT
sinref	sin of reference angle		IN	RMS, EMT
Pmd	Pulse-width modulation index, d-axis		IN	RMS, EMT
Pmq	Pulse-width modulation index, q-axis		IN	RMS, EMT
id_ref	Current reference, d-axis	p.u.	IN	RMS, EMT
iq_ref	Current reference, q-axis	p.u.	IN	RMS, EMT
i2d_ref	Negative sequence current reference, d-axis	p.u.	IN	RMS, EMT
i2q_ref	Negative sequence current reference, q-axis	p.u.	IN	RMS, EMT
u2r_in	Negative Sequence Voltage Input, Real Part	p.u.	IN	RMS
u2i_in	Negative Sequence Voltage Input, Imaginary Part	p.u.	IN	RMS
u0r_in	Zero Sequence Voltage Input, Real Part	p.u.	IN	RMS
u0i_in	Zero Sequence Voltage Input, Imaginary Part	p.u.	IN	RMS
block	Blocking	p.u.	IN	RMS, EMT
xspeed	Voltage frequency (output)	p.u.	OUT	RMS
uDC	DC-voltage	p.u.	OUT	RMS, EMT
iAC_r	AC-current, real part	p.u.	OUT	RMS, EMT
iAC_i	AC-current, imag. part	p.u.	OUT	RMS, EMT
uAC_r	AC-voltage, real part	p.u.	OUT	RMS, EMT
uAC_i	AC-voltage, imag. part	p.u.	OUT	RMS, EMT
id	AC-current, d-Axis	p.u.	OUT	RMS, EMT
iq	AC-current, q-Axis	p.u.	OUT	RMS, EMT
xd	Current controller d-axis, state variable	p.u.	STATE, OUT	RMS, EMT
xq	Current controller q-axis, state variable	p.u.	STATE, OUT	RMS, EMT
N_la	Number of submodules (lower arm), phase A		IN	EMT
N_lb	Number of submodules (lower arm), phase B		IN	EMT
N_lc	Number of submodules (lower arm), phase C		IN	EMT
N_ua	Number of submodules (upper arm), phase A		IN	EMT
N_ub	Number of submodules (upper arm), phase B		IN	EMT
N_uc	Number of submodules (upper arm), phase C		IN	EMT
nlow_a	Insertion index (lower arm), phase A		IN	EMT
nlow_b	Insertion index (lower arm), phase B		IN	EMT
nlow_c	Insertion index (lower arm), phase C		IN	EMT
nup_a	Insertion index (upper arm), phase A		IN	EMT
nup_b	Insertion index (upper arm), phase B		IN	EMT
nup_c	Insertion index (upper arm), phase C		IN	EMT
mdc_a	Insertion index, DC-bias, phase A		IN	EMT
mdc_b	Insertion index, DC-bias, phase B		IN	EMT
mdc_c	Insertion index, DC-bias, phase C		IN	EMT
Iup_a	Upper arm current, phase A	kA	OUT	EMT

Iup_b	Upper arm current, phase B	kA	OUT	EMT
Iup_c	Upper arm current, phase C	kA	OUT	EMT
Ilow_a	Lower arm current, phase A	kA	OUT	EMT
Ilow_b	Lower arm current, phase B	kA	OUT	EMT
Ilow_c	Lower arm current, phase C	kA	OUT	EMT
Uuparm_A	Upper arm submodules voltage, phase A	kV	OUT	EMT
Uuparm_B	Upper arm submodules voltage, phase B	kV	OUT	EMT
Uuparm_C	Upper arm submodules voltage, phase C	kV	OUT	EMT
Ulowarm_A	Lower arm submodules voltage, phase A	kV	OUT	EMT
Ulowarm_B	Lower arm submodules voltage, phase B	kV	OUT	EMT
Ulowarm_C	Lower arm submodules voltage, phase C	kV	OUT	EMT
Uupcap_A	Upper arm capacitor voltage, phase A	kV	OUT	EMT
Uupcap_B	Upper arm capacitor voltage, phase B	kV	OUT	EMT
Uupcap_C	Upper arm capacitor voltage, phase C	kV	OUT	EMT
Ulowcap_A	Lower arm capacitor voltage, phase A	kV	OUT	EMT
Ulowcap_B	Lower arm capacitor voltage, phase B	kV	OUT	EMT
Ulowcap_C	Lower arm capacitor voltage, phase C	kV	OUT	EMT
gate	Gate signals (array, only Detailed equivalent circuit)		IN	EMT
Ucap	Submodule capacitor voltages (array, only Detailed equivalent circuit)	kV	OUT	EMT

E References

[1] CIGRE Technical Brochure TB 604 2014, *Guide for the development of models for HVDC converters in a HVDC grid*, WG number: B4-57, 2014.

[2] M. Guan, Z. Xu, *Modeling and Control of a Modular Multilevel Converter-Based HVDC System Under Unbalanced Grid Conditions*, IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 27, NO. 12, DECEMBER 2012.

[3] H. A. Saad, *Modélisation et simulation d'une liaison HVDC de type VSC-MMC*, Ph.D. Thesis, ÉCOLE POLYTECHNIQUE DE MONTRÉAL March 2015.

[4] G. P. Adam ; I. E. Davidson, *Robust and Generic Control of Full-Bridge Modular Multilevel Converter High-Voltage DC Transmission Systems*, IEEE TRANSACTIONS ON POWER DELIVERY, VOL. 30, NO. 6, DECEMBER 2015.

[5] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, T. Jonsson, *VSC-HVDC Transmission with Cascaded Two-Level Converters*, CIGR SC B4 Session 2010, 2010.

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