11 July 2021

PRIMEASIA UNIVERSITY

ELECTRICAL AND ELECTRONIC ENGINEERING DEPARTMENT

BSc in EEE *MID TERM EXAMINATION* *Summer 2021 Semester*

EEE 4136/CSE 404 Regular Batch VLSI LAB

Full Marks: 40 *Time:1 Hr and 30 Mins.*

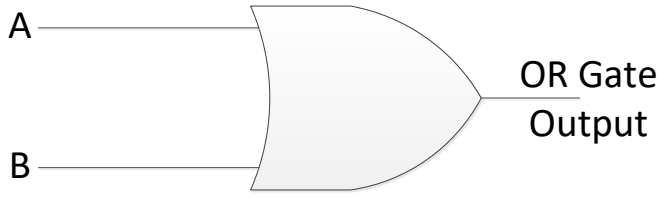
Answer All Questions

(Exam time is 1 hour and 30 minutes, after that you will have 15 minutes to upload the answer script in Orbit OCP, if you have any problem uploading in Orbit OCP, mail the answer script in the given email address: shaiyekbuland@gmail.com

You should save the pdf file as shown using your ID number: **171065051 VLSI EEE 4136 Regular Mid Final LAB Summer 2021**)

All instructions above will be followed strictly.

Design a 2 input CMOS OR gate using Microwind and Dsch Software.



1. Designing in Microwind, you have to show the steps given below: [20 marks]
   - I. Show the 2 input OR gate logic diagram using PMOS and NMOS, also identify and mark in the diagram sourse(S), gate(G) and drain(D).
   - II. Show the Microwind design of 2 input OR gate.
   - III. Show the output result after doing simulation.

2. Designing in Dsch, you have to show the steps given below: [10 marks]
   - I. Show the Dsch design of 2 input OR gate.
   - II. Show the output result for Inputs A=0 and B=0 in Dsch.
   - III. Show the Verilog code for OR gate.

3. Import the Verilog code of OR gate in Microwind. [10 marks]
   - I. Show the 2 input OR gate design created by using the Verilog code.
   - II. Show the simulation result of OR gate.

----------Good Luck----------