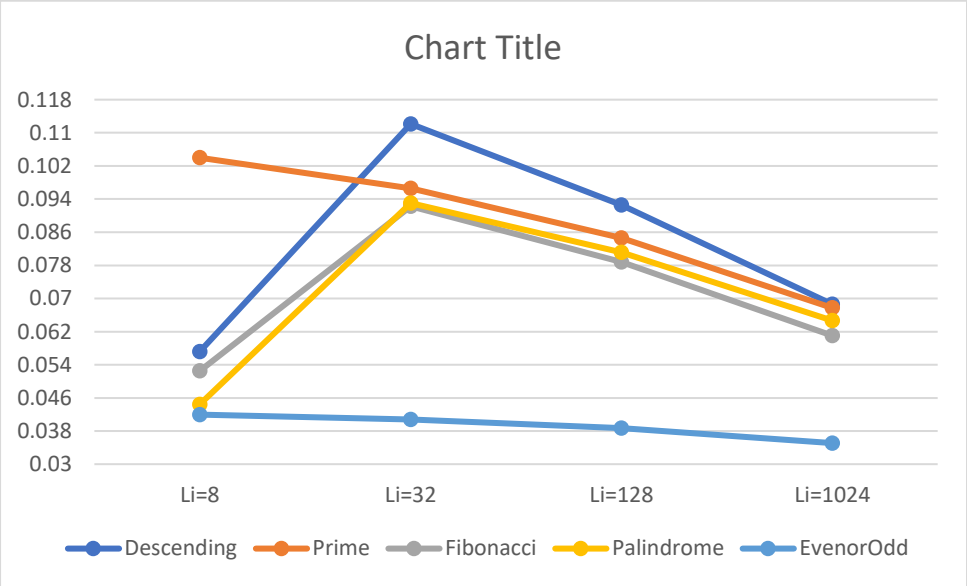
ROLL-200010044,200010020

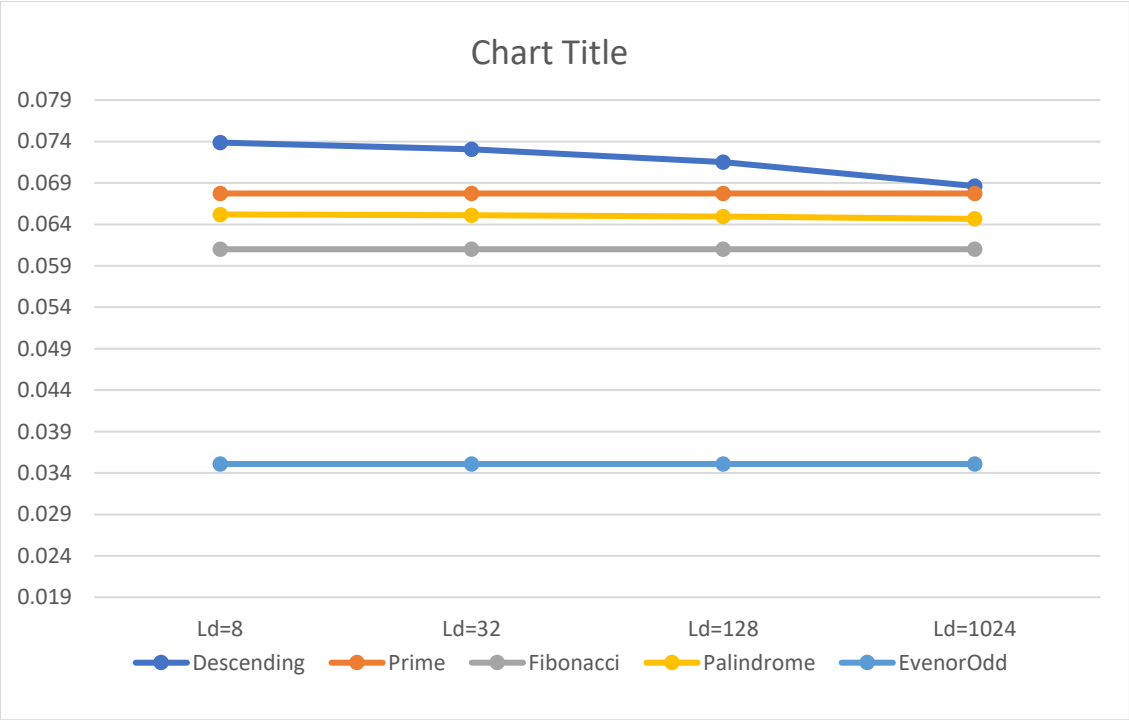
Functionalities Implemented-:

1. L1 Level Caches at IF and MA Stages.
2. Varied various Cache sizes to and plotted the IPC values.

ANALYSIS-1:



ANALYSIS-2:



ANALYSIS-3:

1. When we vary Li cache sizes keeping Ld constant we observe for Evenorodd IPC steadily decreases because the quantity of accesses is limited (fixed) while due to increase in cache size latency increases.
2. In all other cases we observe the IPC improves and peaks at 32 and then decreases, the reason being beyond 32B we don't need more cache since the size is big enough while increase in cache size increases latency which decreases the IPC value.
3. When we vary L1d cache sizes keeping Li constant we observe it almost remains same since our programs are written in such a manner that these don't require much memory accesses.

ANALYSIS-4:

I chose two benchmarks Descending.out and Palindrome.out and compared the Hit Rates for cache sizes of 4 and 32 B.

The observations for descending.out are-:

	Hit Rates (%)
li=32B	**65**
li=128B	**98**

The observations for palindrome.out are-:

	Hit Rates(%)
li=32B	**55**
li=128B	**91**

Clearly, we see, when we increase the sizes of Caches from 32B to 128B in each case, the Hit Rate improves dramatically from 65-98%!!! And 55-91%!!!!

ANALYSIS-5:

Since our original programs do not have much relation with Ld caches, I wrote a simple memory accesses program to look at the hit rate change.

Observations-:

For 32B- 0 hit rate

For 128B- 50% hit rate

The program made accesses to addresses 0,8,16,24, 32,40,48,64, 0,8,16,24, 32,40,48,64,

To simply understand the program,

Let’ say each line of cache is 8B i: e 8 blocks and

For 32B there are 4 lines of cache

-: Here initially there will be 4 misses then another 4 misses. Now the cache has replaced 0,8,16,24 blocks with 32,40,48,64 blocks so there will be additional 4 misses and then finally 4 misses.

So, 0 hits and 16 accesses.

For 128B there are 8 lines of cache

-: After the initial 8 misses, all the rest 8 accesses will be hit only.

So, 50% hit rate!!