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Flip Chip Interconnect Analysis at Millimetre Wave Frequencies

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Abstract: This paper examines the variation of RF performance on a flip chip due to changes in bump height, bump position, bump shape and number of bumps per interconnect. A full 3D electromagnetic simulator is used extensively to compute the scattering parameter response, impedance and electric field distributions. Varying the bump height will change the reflection coefficient and return loss at millimetre wave frequencies significantly. It is found that proper bump positioning could improve the return loss of the structure. Different bump shape also affects the RF performance of the flip chip. Tapered bump shape gives the best return loss and the lowest reflection coefficient.

1. INTRODUCTION

Flip chip interconnection is becoming popular for packaging of microwave and millimetre wave applications. Among the wide range of applications using flip chip technology are wireless LAN and high bandwidth fiber-optic communication systems. In a flip chip process, the chip is flipped over and mounted directly on the substrate using metallic bumps. A typical structure of a flip chip package using coplanar waveguide (CPW) technology is shown in Figure 1.

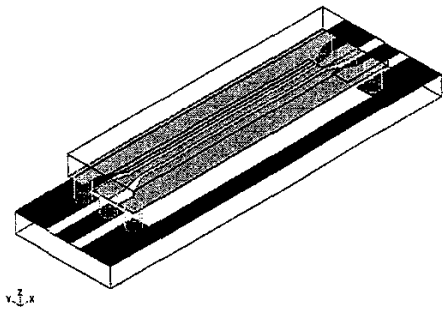

Figure 1: Typical Flip Chip Structure

Flip chip offers several advantages over conventional techniques such as wire bonding. It provides better electrical performance in the millimetre wave range than wire bonding techniques. Flip chip packages also have less parasitic inductance and capacitance, compared to conventional interconnect techniques. The metallic bumps act as heat sinks due to a lower thermal resistance than the substrate, thus improving the power handling capability of the chip [1]. As the bump pads for the interconnections could be provided at

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any location on the die, the mounting area of the package is minimised, allowing higher interconnection density.

Furthermore, the flip chip process is also easier to rework and has many similarities to the SMT (Surface Mount Technology) process. Placement, soldering and cleaning process are identical, providing compatibility with automatic manufacturing [2]. The bonding and connection of flip chips are a one step procedure, and this will lower production costs and increase the volume of production.

Coplanar structure is better than microstrip in implementing designs using flip chip technology. Coplanar design offers better containment of fields close to the chip surface and less interaction of fields with the substrate, as demonstrated in Figure 2. However, modelling of analysis of CPW is more difficult than microstrip as there are less analytical formulas readily available.

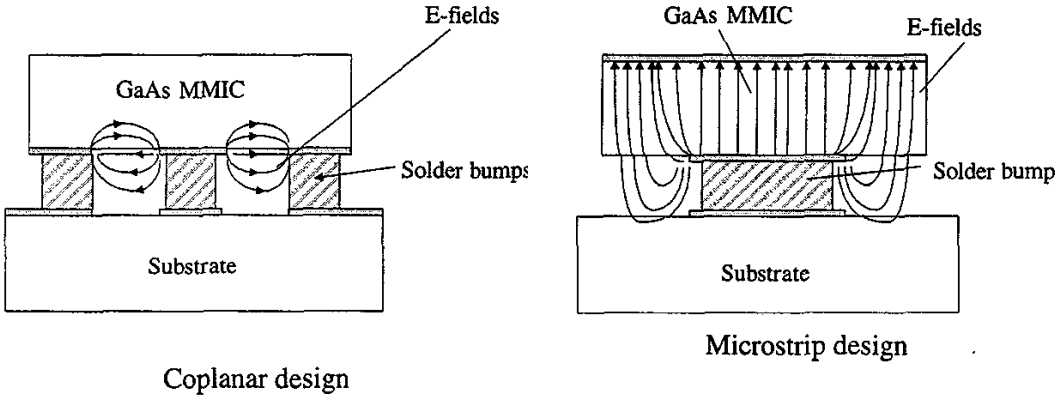

Figure 2: Electric Field Orientation within the Flip Chip Package

Using coplanar technology also has a number of cost advantages in the foundry process. Coplanar structures do not need backside processing or via technology, reducing the cost of production. Applying coplanar structures to the development of flip chip technology is very advantageous for realising low cost millimetre wave applications [3].

2. ASSEMBLY OF FLIP CHIP

The assembly of a flip chip is summarised with a process flow chart shown in Figure 3. There are three options of bumping: bumping the die, bumping the substrate or bumping both. This paper examines on the option of bumping the substrate, as bumping the dice is not always available.

First, preparation of the solder bumps is a critical operation and bump size and diameter must be tightly controlled. Before bumping, a low activity flux is applied on the substrate to provide tackiness and prevent chip movement. There are several bumping methods, namely evaporation, screen printing, ball bonding and plating. Following the bumping step, a reflow process is performed. Flux residues may be cleaned using a solvent. Then, the wafer is cut into individual die in a dicing operation. After that, the chip is aligned to the substrate using a custom built placement machine with split field optics. The module is then reflowed to improve uniformity in bump height. This reflow operation uses

surface tension in the roller ball to provide self alignment. After flip chip bonding the module can be underfilled to improve solder joint reliability [4]. However, at millimetre wave frequencies, underfill would change the effective dielectric constant of the package and have to be compensated by modifying the line lengths appropriately [5].

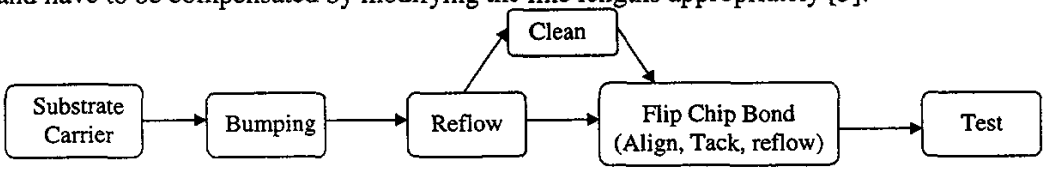

Figure 3: Process Flow Chart for the Flip Chip Process

2.1 Bumping methods

One of the most cost effective bumping methods is plating. This method provides uniform plating heights with relatively good process control. The substrate wafer with devices is metallized such that a current path is provided to the individual bond pads. The blanket metallization is called a seed layer and is deposited on the entire wafer. Metal used would be chrome or TiPtAu. The seed layer would be etched away after the plating step to electrically isolate the bumps. The wafer is patterned with a spun-on photoresist that is compatible with the substrate and the plating process, such that the metallization layer is exposed in the regions where the bump is desired. The wafer is then mounted in a cup plater and a current is applied with the wafer as the cathode. The thickness of the plated bump is determined by the plating current and plating time. Geometry and pitch limitations are determined by the photoresist process [6].

Another alternative to bumping is the ball bonding technique. Gold bumps are deposited directly onto the substrate using a thermosonic bonder. Ball bonding uses gold wire with a small amount of palladium to make the wire brittle so that it snaps off cleanly. The rapidly solidified wire forms a solder ball when it is subjected to an arc discharge in an argon-hydrogen environment. This ball is then bonded directly to a gold bond pad using thermosonic energy. The size and pitch capabilities of ball bonding are limited by the diameter of the wire.

2.2 Substrate material

One of the most important factors in the choice of a flip chip interconnect system is the substrate. The substrate influences the maximum allowable process temperature, the reliability of the interconnect, cost and minimum pitch of the bumps. A good thermal match for the device attached must be obtained in order to minimise thermal and mechanical stresses within the flip chip package. Flexure caused by bad thermal matching could break the bump interconnect. Besides the typical choice of substrate such as alumina (Al_2O_3) and gallium arsenide (GaAs), alternative choice of substrates are available, such as softboard material and silicon.

Softboard is flexible and is soft for wire bonding. However, it is quite difficult to get a CTE (coefficient of thermal expansion) to match that of the GaAs device. Silicon has low resistivity and hence poor isolation and does not make a good microwave substrate.

However, high resistivity silicon is much better with improved isolation. It is flat and can be plated onto, using a seed layer.

3. MODELLING

The modelling of the flip chip structures in this paper is performed using HFSS (High Frequency Structure Simulator). HFSS is a software package for electromagnetic modelling of passive three-dimensional structures using Maxwell's equations to solve for electric and magnetic fields. HFSS employs the finite element method to generate E and H field solutions from which the scattering parameters are computed. Impedance and electric field distributions are also computed using HFSS.

HFSS™ is chosen to be the modelling package as other 2-½D EM simulators such as Momentum™ and Sonnet™ might be insufficient in providing accurate results for more complex 3-D structures. However each simulation is time intensive and the software is relatively difficult to use.

The accuracy of HFSS depends on the setting of adaptive refinement criteria (number of iterations) and mesh seeding values (initial mesh size). Increasing the refinement criteria and mesh seeding values would increase the accuracy, but requires more computing power, and simulation time would also increase dramatically. Thus, there is a trade off between the size of the mesh, the desired level of accuracy and the amount of available computing resource.

For this paper, a tapered CPW structure is flipped onto a carrier substrate transmission line of the same width and spacing as the rf bump pads, as shown in Figure 1. The width and spacing of the 50 Ω CPW tapered transmission line are 30 μm and 15 μm respectively. The carrier substrate transmission line has a width and spacing of 80 μm and 50 μm respectively. GaAs is chosen to be the material of the substrate in the simulations and the bumps are set to be 50 μm in diameter and made of gold. The thickness of the metallization layer of the transmission line is set to be 1.25 μm.

4. RESULTS

The effect of the bumps on the RF performance of the structure is important since the transmission line discontinuity creates undesirable reflections, especially at millimetre wave frequencies. These bumps should be designed such that the induced reflections are minimum. The objective is to have low series resistance and still maintain the transmission line impedance across the bump transition. The variation of RF performance due to bump height, bump geometry and number of bumps are examined.

Cylindrical bumps of 50 μm in diameter are chosen for the simulation of various bump heights. Figure 4 shows the variation of the magnitude of S_{11} with bump height. It can be seen via HFSS that varying bump height does not change the S-parameter values significantly at low frequencies. However, higher bumps provide a better reflection coefficient at millimetre wave frequencies. This might be because the field distribution would be more confined to the chip surface. Note that having a bump that is above 200 μm high is impossible to fabricate, as it is very difficult to produce a photoresist of such large thickness. Also, it is known that the minimum distance between the chip and the

substrate needs to be at least the ground to ground distance of the CPW line in order to avoid the interaction of fields with the substrate [7].

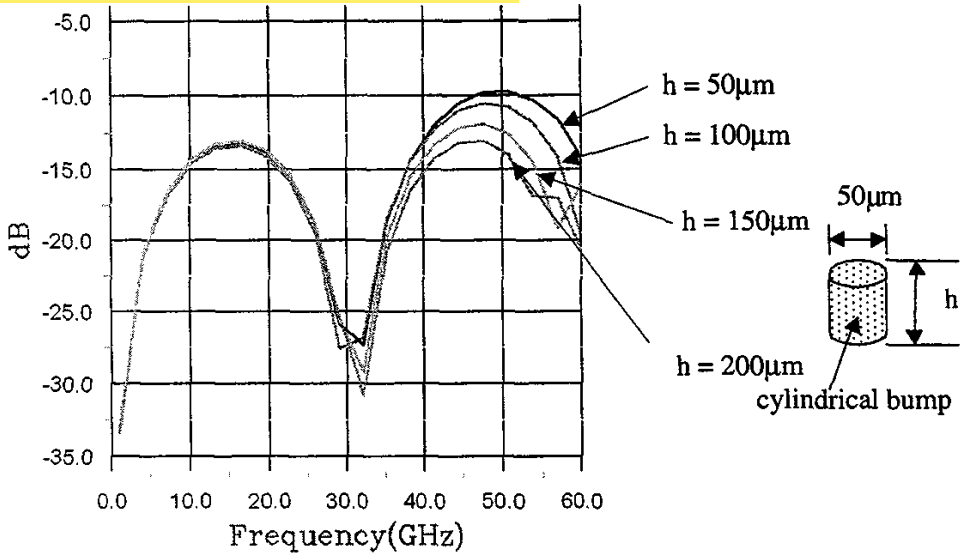

Figure 4: Variation of S_{11} (dB) due to bump height

The variation of RF performance due to bump geometry, i.e. having bumps of different shapes will also affect the performance of the structure. A series of bump shapes are investigated, and are shown in Figure 5. Results show that the performance variation with different bump geometry is more pronounced at higher frequencies. It is found that the concave bump shape gives the best return loss and the lowest reflection coefficient (Figure 6). It is also found that thinner bumps also produce a much better performance than thicker bumps of the same shape and height.

The variation of the number of bumps is also examined. One large bump is used to fill the width of the transmission line and compared with a series of smaller bumps may be used to spread the interconnection and thus reduce the discontinuity at the transition. This technique may also be used to minimise the series resistance of the metal bump, especially for power devices. This is currently under investigation and initial simulations show that having more bumps increases the transmission loss of the structure slightly. Careful design can improve the return loss by properly matching the interconnection to the transmission line on the substrate.

5. CONCLUSIONS

Proper design of the flip chip interconnects is fundamental to improving the flip chip transition performance. The effect of the bumps on the RF performance of the structure is important since the discontinuity on transmission line creates undesirable reflections, especially at millimetre wave frequencies. Different height and geometry of the bumps would influence the rf performance of the flip chip at millimetre wave frequencies significantly. Reducing the return loss due to interconnections within the structure is important in order to allow for the fabrication of millimetre wave circuits that are not possible because of large internal reflection problems. One method that might further reduce loss is with staggered or tilted bumps.

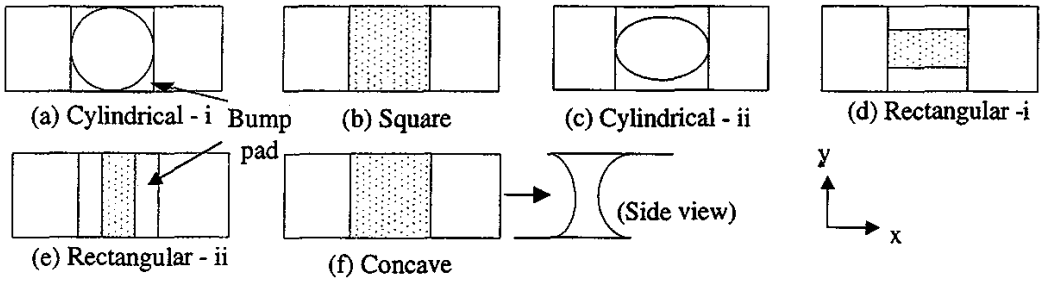

Figure 5: Variation of bump geometry (top view)

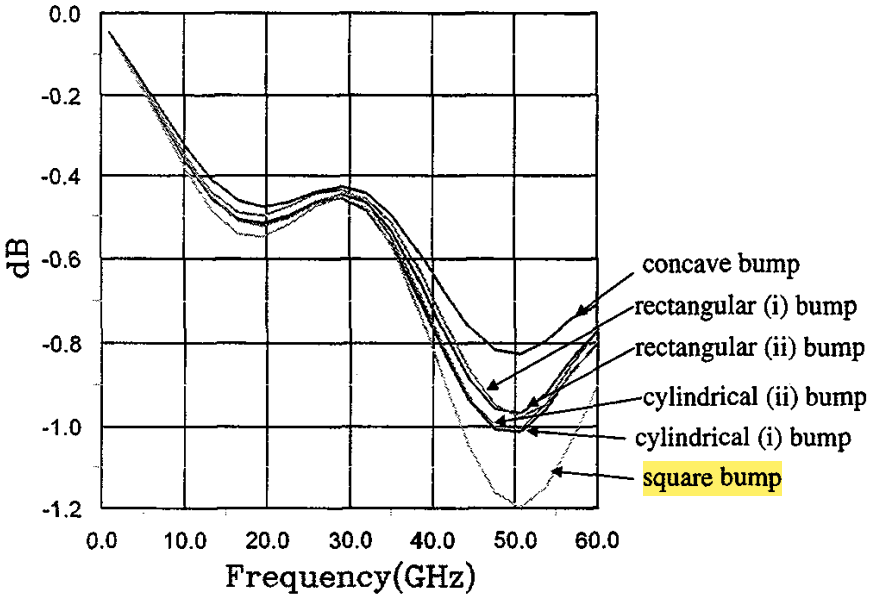

Figure 6: Variation of S_{12} (dB) due to bump geometry

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