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Design, Processing, and Characterization of High Frequency Flip Chip Interconnects

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CHALMERS

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Abstract

The demands for high frequency interconnect techniques for microwave integrated circuits (ICs) are growing with increasing operating frequencies of wireless communication systems. Interconnects have significant effect and impact on the overall system performance at high frequencies. To provide good performance in high frequency packaging, flip chip interconnect is one of the most attractive candidates compared to other schemes with low reflection and low insertion loss due to the lower parasitics involved. The widely used bond-wire interconnect suffers from serious parasitics when operating frequency reaches the gigahertz range. The tolerances such as the wire length and loop are very tight to enable an acceptable transition. At high frequencies, however, it still encounters stronger parasitics no matter how well it is controlled.

This thesis deals with the design, processing, and characterization of flip chip interconnects at high frequencies. The main issues of the flip chip interconnect are described before the design criteria of the conventional flip chip interconnect are reviewed. In the following, the work of the hot-via transition is presented. It is a solution to the detuning effect of the microstrip (MS) flip chip assembly. The designs of the hot-via transition for the MS-to-CPW (coplanar waveguide) are presented; the results presented are currently world record for this technique to our knowledge. Another part of work in this thesis is the coaxial transition developed for the CPW-to-CPW flip chip interconnects. The coaxial-type transition was successfully fabricated in-house and demonstrated excellent transition performance up to 60 GHz. The entire fabrication processes for all demonstrated flip chip interconnect structures have been in-house developed and are described in details. All the design rules regarding to the different architectures for the flip chip interconnects are described and verified with the measured results. The main contributions of this thesis work are the innovative designs and the developments of both the hot-via transition and coaxial transition for the flip chip interconnects.

Keywords: flip chip, interconnect, high frequency, microwave, packaging, coaxial, hot-via, transition, microstrip, coplanar waveguide.

List of Publications

Appended papers

The thesis is based on the following papers:

[A] Wei-Cheng Wu, Li-Han Hsu, Edward Yi Chang, Camilla Kärnfelt, Herbert Zirath, J. Piotr Starski, and Yun-Chi Wu, ”60 GHz broadband MS-to-CPW hot-via flip chip interconnects,” *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 11, pp. 784-786, Nov. 2007.

[B] Wei-Cheng Wu, Edward Yi Chang, Ruey-Bing Huang, Li-Han Hsu, Chen-Hua Huang, Camilla Kärnfelt, J. Piotr Starski, and Herbert Zirath, “Design, fabrication, and characterization of novel vertical coaxial transitions for flip chip interconnects,” *IEEE Transactions on Advanced Packaging.*, Vol. 33, pp. 30-36, 2010

[C] Wei-Cheng Wu, Edward Yi Chang, Li-Han Hsu, Chen-Hua Huang, Herbert Zirath, and J. Piotr Starski, ”Novel coaxial transitions for CPW-to-CPW flip chip interconnects,” *Electronics Letters*, vol. 43, no. 17, pp. 929-930, August 16 2007.

[D] Wei-Cheng Wu, Ruey-Bing Huang, Heng-Tung Hsu, Edward Yi Chang, Li-Han Hsu, Chen-Hua Huang, Yin-Chu Hu, and Ming-Iu Lai, “Design of flip-chip interconnects with vertical coaxial transitions and its fabrication,” *2005 Asia-Pacific Microwave Conference Proceedings*, vol. 2, pp 965-968, 4-7 Dec. 2005.

[E] Wei-Cheng Wu, Li-Han Hsu, Edward Yi Chang, J. Piotr Starski, and Herbert Zirath, “60 GHz broadband 0/1-level RF-via interconnect for RF-MEMS packaging,” *Electronics Letters*, vol. 43, no. 22, October 25 2007.

Published papers not included in this thesis:

[a] Wei-Cheng Wu, Cheng-Shih Lee, and Edward Yi Chang, "Microstructural evolution of Cu/Ta/GaAs multilayers with thermal annealing," *Materials Research Society Fall Meeting*, Boston, MA, December 1-5, 2003.

[b] Wei-Cheng Wu, Heng-Tung Hsu, Edward Yi Chang, Cheng-Shih Lee, Chen-Hua Huang, Yin-Chu Hu, Li-Han Hsu, and Yi-Chung Lien "Flip-chip packaged $In_{0.52}Al_{0.48}As$/InGaAs metamorphic HEMT device for millimeter wave application," *2005 CS-MAX, Compound Semiconductor Manufacturing Expo*, pp 94-97, 30 Oct.-2 Nov. 2005.

[c] Wei-Cheng Wu, Li-Han Hsu, Edward Yi Chang, Yin-Chu Hu, Yun-Chi Wu, and Yu-Min Teng, "DC and RF characterizations of flip chip packaged low-noise GaAs PHEMT towards multi-chip modules (MCMs) for microwave applications," *2007 Mediterranean Microwave Symposium*, Budapest, Hungary, 14-16 May 2007.

[d] Li-Han Hsu, Wei-Cheng Wu, Edward Yi Chang, Yin-Chu Hu, Chin-Te Wang, and Guo-Wei Huang, "Chip-scale packaged 30 GHz GaAs microstrip and coplanar waveguide MMIC amplifiers using flip chip interconnects," *2007 Mediterranean Microwave Symposium*, Budapest, Hungary, 14-16 May 2007.

[e] Camilla Kärnfelt, Wei-Cheng Wu, and J. Piotr Starski, "Proximity effect, resonances and modeling of microstrip flip chip assemblies," submitted to *IEEE Transactions on Advanced Packaging*.

[f] Shang-Wen Chang, Edward Yi Chang, Dhrubes Biswas, Cheng-Shih Lee, Ke-Shian Chen, Chao-Wei Tseng, Tung-Ling Hsieh, and Wei-Cheng Wu, "Gold-free fully Cu-metallized InGaP/GaAs heterojunction bipolar transistor," Jpn. J. Appl. Phys., vol. 44, no. 1A, pp.8-11, 2005.

[g] Y. C. Wu, E. Y. Chang, Y. C. Lin, H. T. Hsu, S. H. Chen, W. C. Wu, L. H. Chu and C. Y. Chang, "SPDT GaAs switches with copper metallized interconnects," *IEEE Microwave and Wireless Components Letters*, vol. 17, 2, pp. 133-135, 2007.

[h] Yueh-Chin Lin, Edward Yi Chang, H. Yamaguchi, Wei-Cheng Wu, and Chun-Yen Chang, "A δ-doped InGaP/InGaAs PHEMT with different doping profiles for device linearity improvement," *IEEE Transactions on Electron Devices*, vol. 54, 7, pp. 1617-1625, 2007.

Abbreviations

ACA	Anisotropic Conductive Adhesive
BCB	BenzoCycloButene
C4	Controlled Collapse Chip Connection
CPW	Coplanar Waveguide
CSP	Chip Scale Packaging
CST	Computer Simulation Technology
CTE	Coefficient of Thermal Expansion
DBIT	Direct Backside Interconnect Technology
DC	Direct Current
EM	ElectroMagnetic
FC	Flip Chip
FGCPW	Finite Ground Coplanar Waveguide
FR-4	Flame Retardant 4, a type of material used for making a printed circuit board (PCB)
GND	Ground
GSG	Ground-Signal-Ground
HEMT	High Electron Mobility Transistor
HF	High Frequency
HFSS	High Frequency Simulation Software
LNA	Low Noise Amplifier
IC	Integrated Circuit
ICA	Isotropic Conductive Adhesive
ICP-RIE	Induced Coupled Plasma Reactive Ion Etcher
IMCs	Inter Metallic Compounds
I/O	Input/Output
MCM	Multi Chip Module
MEMS	Micro Electro Mechanical Systems
MIC	Microwave Integrated Circuits
MMIC	Monolithic Microwave Integrated Circuits
MS	Microstrip
NCA	Non Conductive Adhesive
PCB	Printed Circuit Board
PNA	Power Network Analyzer
PRs	Photoresists
PTFE	Polytetrafluoroethylene

RF	Radio Frequency
SEM	Scanning Electron Microscope
SoC	System on Chip
SiP	System in Package
TAB	Tape Automated Bonding
TC	Thermo-Compression
TL	Transmission Line
TS	Thermo-Sonic
TSM	Top Surface Metallurgy
UBM	Under Bump Metallurgy

Contents

Chapter 1

Introduction

1.1 High frequency interconnect

The rapid growth of the commercial wireless communications, such as 40 GHz WLAN and 77 GHz automotive radar systems, has driven the development of the interconnect techniques towards high performance and low cost solutions for the microwave packaging in order to achieve the size, weight, and cost reduction of the final products [1]. Interconnect technique plays a key role in the packaging for the microwave circuits and other components; it can have significant effect and impact on the final performance of the assembled chip particularly at millimeter wave frequencies. Basically, the requirements of the interconnect technique for microwave packaging are low reflection, low insertion loss and low-cost fabrication [1].

In general, the three main interconnect techniques to connect the bare chip to the first level package are wire bonding, tape automated bonding (TAB), and flip chip bonding. In the case of the conventional wire bonding technique, interconnect suffers severe the parasitic inductances induced by long bond wires at high frequencies. In contrast, the most promising interconnect technique in the microwave packaging is flip chip technology using the short bump transition to connect the chips to the package, where the parasitic effects at high frequencies can be effectively minimized. However, wire bonding still dominates the packaging markets in RF field at lower frequencies because it is a mature, widely-used and well-proven technique [1]. Nevertheless, when the wireless communications steps into higher frequencies applications, flip chip technique has to be adopted in order to avoid the parasitic effect.

Actually, there are still many uncertain problems prevent designers and/or producers from adopting the flip chip approach for the realistic production [1]. For instance, which bonding methods should be used, soldering or thermocompression? Which is the better bump material, Au or lead-free solder for environmental protection issue? Which substrate material gives the best compromise between the cost and performance, ceramic or polymer? Whether to use the underfill and, if any, which material to be used? What about the structure reliability and the electrical

performance? The answers can differ and depend on the specific applications. The lack of the experience and the proven design data delays the popularity of the flip chip approach to the microwave productions and requires more research efforts in this field [1].

1.2 Outline of the thesis

The motivation of this research work is the developments of the high frequency flip chip interconnect technique and the novel transition scheme for the flip chip interconnect to achieve low reflection and low insertion loss with broadband performance.

The thesis is organized as follows. Chapter 2 outlines the packaging functions and the interconnect techniques at the chip level package. The conventional flip chip interconnect is reviewed with emphasis on the high frequency performance. Chapter 3 summarizes the present bumping and bonding methods in the flip chip technology and ends up with the development of the in-house bumping and bonding process. In chapter 4, the hot-via transition, an alternative approach avoiding the detuning effect associated with flip chip technology, is presented. The experimental results obtained for the hot-via technique are currently state-of-the-art in the field. Chapter 5 deals with the novel work, coaxial transition for flip chip interconnect. The effects of the key parameters on the interconnect performance are described and discussed; the fabrication process of such structure is presented as well. Further, with the use of the BCB dielectric, an extended design, the perfect coaxial transition, is presented and demonstrates excellent interconnect performance. The last chapter presents the conclusions of this thesis work and some suggestions for the future work.

Chapter 2

Flip Chip Interconnect for Microwave Packaging

Flip chip technology means to flip the chip onto the substrates, circuit boards, or any carriers forming the electrical connections from the chip to the substrate by means of the conductive bumps standing between the bond pads. The basic concept of the flip chip scheme is shown in Fig. 1, where the MMIC chip (simplified to CPW line on chip) is face-down mounted on a carrier substrate by using the conductive bumps as the interconnects. Flip chip technology can be traced back to the C4 technology, Controlled Collapse Chip Connection technology, which was introduced by IBM for the mainframe computer applications in 1960s [2]. Since then, the flip chip technology has found its way in the low-frequency applications. In the RF field, it is still rarely used even if it shows great potential and superior performance over other interconnect techniques. This is mainly because the typical flip chip technique can not be simply transferred to the microwave frequencies applications. The bumping technique, *e.g.* the bump diameter pitch and the bump metallurgy have to be modified to be compatible with the millimeter-wave and broadband chips [1]. This chapter starts with a brief introduction of the packaging functions and the various fist-level interconnect techniques. The properties of the commonly used materials in flip chip architectures are subsequently surveyed. Finally, the key factors affecting the flip chip interconnect performance at high frequencies are presented and discussed according to a careful review on the relevant literatures.

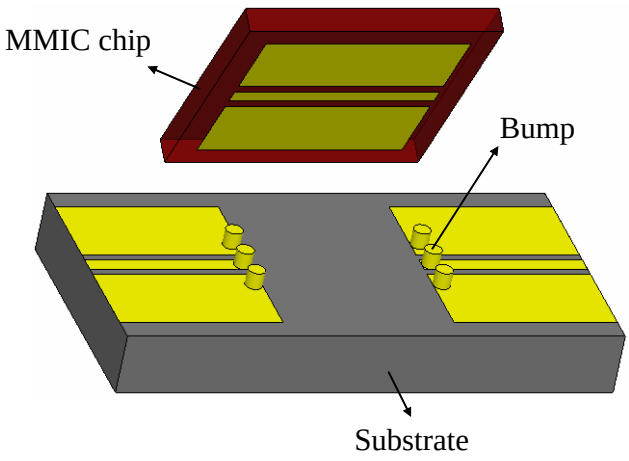


Fig. 1. Illustration of flip chip concept for mounting a MMIC chip (represented by CPW line) onto a substrate by means of bumps.

2.1 Functions of electronic packaging

Electronic packaging is a key enabling technology to achieve the desired functionalities of the final products. It deals with the interconnection between the semiconductor ICs and the intended application environment in a possibly compact and efficient way with a minimum degradation in performance. It also acts as the determining factor in cost and size of the final product.

Electronic packaging mainly has three principal functions: power and signal delivery, heat dissipation, and support/protection. First and foremost, the package provides conductive paths out/into the ICs for delivering the external power supplies and signals through the I/O pads on the ICs' surface. To ensure reliable and predictable signal transmission after packaging, the power and signal delivery paths in the package have to be designed in advance by considering numerous electrical constraints, such as the parasitics, the electromagnetic properties, the signal degradation and distortion, *etc*. A good packaging design keeps the degradation of the signal transmission to a minimum.

Electrical energy is consumed and converted into heat during IC operation. The heat accumulation increases the operating temperature of the chip and may trigger the temperature-activated failures. So another purpose of the electronic packaging is to dissipate the heat generated by the chip. The third important function of the package is to protect the components and their interconnections against the outside harsh environments during handling and/or operation. In most cases, the main concern is the protection against the moisture and mechanical damage. Moisture is one of the major corrosion sources in semiconductor devices. The presence of moisture can induce the IC failures by electro-oxidation and metal migration. Therefore, sensitive components are generally encapsulated or sealed with a hermetic package.

2.2 First-level interconnect (chip-level interconnect)

Electronic packaging starts from individual chips and finishes at system level. The conventional packaging hierarchy consists of three packaging levels. At the first-level packaging, bare chips are mounted and electrically interconnected onto a packaging

support. The chip and packaging support are then encapsulated in a plastic molding or with ceramic/metal caps for mechanical and environmental protection with the terminals like pins, leads, or bumps for incorporation into the next level of packaging. At the second-level packaging, the system functionality is generally achieved, where the first-level-packaged ICs are integrated with the passive or other active components on a circuit board which consists of wiring metal traces serving as the grounds and transmission routes for power and signal distribution. Circuit board manufacturing is the key technology for the second-level packaging. When dealing with a larger system, *e.g.*, workstation or mainframe, a third-level packaging may apply, in which several assembled circuit boards are interconnected on a main motherboard to achieve greater system functionality. This thesis deals with the high frequency interconnect performance at the first-level packaging. Therefore, more details on the first-level package are presented in the following.

At the first-level packaging, the chip electrically interconnects with the packaging substrate through I/O pads, which are commonly realized by one of the two common methods, bond-wire interconnect or flip chip interconnect. Fig. 2 shows the concepts of these two interconnect methods.

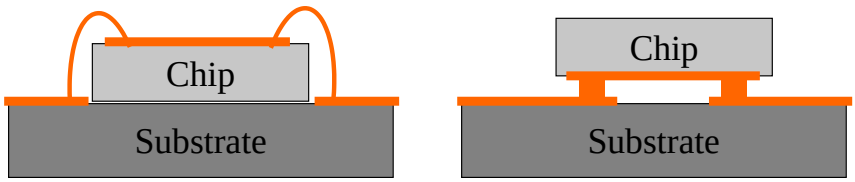


Fig. 2. The concepts of the two different first-level interconnect, bond-wire interconnect on the left side and flip chip interconnect on the right side.

Wire bonding technology is the most mature process and has been dominant technique in the conventional ICs packages. In this scheme, a fine metal wire typically about 20-25 μm in diameter is connected between the pads of the chip and the substrate. The wire is welded to the pads at two ends by ultrasonic (US), thermosonic (TS), or thermocompression (TC) bonding methods. The bonding technology is a time consuming process because the connection between chip and substrate is made sequentially. For chips with many I/Os, the process time can become relatively long. The I/O density of the chip is limited as well because it is a peripheral packaging scheme. Another main drawback of bond wire interconnect is the degradation of performance at high frequencies due to the serious parasitics. This is a key issue for packaging at millimeter waves. The main parasitic effect is the bond wire inductance, which increases in proportion to the interconnect length. With a Au

wire of 25 μm diameter, a bond wire interconnect generally introduces about 1 nH/mm of inductance.

On the other hand, as the first-level interconnect, flip chip interconnect provides numerous advantageous over bond-wire interconnect, particularly for the applications of packaging high-frequency and/or high-power ICs. For flip chip technology, the active side of the chip is face-down and is interconnected to bonding pads on the packaging substrate by means of the conductive bumps. The connections between the numerous bumping pads can be achieved simultaneously, leading to a considerably time-saving process for chips with many I/Os. Furthermore, higher I/O density can be provided in packaging because it allows the I/Os to be distributed all over the chip surface rather than confined to the periphery as in wire bonging technology. With higher density connections, the short bumps also provide a thermal path for heat dissipation. Most important of all, due to the short electrical path, the parasitics induced by the interconnect are significantly smaller compared to bond-wire interconnect scheme, making flip chip interconnect very attractive for high frequency packaging applications. More details about the issues of the flip chip interconnect for high frequency packaging applications are discussed and presented in Section 2.4.

2.3 Materials in flip chip structure

Fig. 3 shows the schematic of the flip chip interconnect structure, which consists of three essential elements: chip, substrate, and bump. With different joining method, the chip is face-down mounted and electrically connected to the substrate by means of the bump. From the material aspect, it is important to know the intrinsic material properties of those before they are assembled together. Table 1 and 2 show the various materials for the chip and the substrate. As can be clearly seen from the tables, the three possible ceramic materials for the substrate show tolerable coefficient of thermal expansion (CTE) with all the possible chip materials while the other three polymer substrates have quite high CTE constants. The thermal stress resulting from the CTE mismatch will cause a serious reliability problem to the flip chip structure. Besides, the polymer substrates have higher values of tangent loss than the ceramic substrates do. These two reasons make the ceramic substrate widely used for the microwave packaging applications.

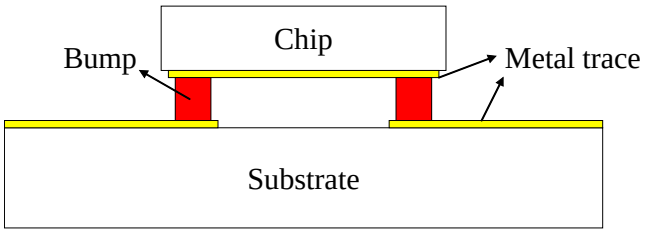


Fig. 3. Schematic side view of flip chip structure.

Table 1. The properties of various chip materials.

Chip materials	Dielectric constant	Loss tangent	CTE (ppm/^{o}C)
Si	11.7	0.001	2.6
GaAs	12.9	0.0005	5.8
InP	12.4	0.0005	4.5

Table 2. The properties of various substrate materials.

Substrate materials	Dielectric constant	Loss tangent	CTE (ppm/^{o}C)
Al_2O_3	9.8	0.0002	6.7
AlN	9.7	0.0005	4.5
BeO	6.6	0.0003	7.5
FR-4	4.4	0.0015	15
Polyimide	4	0.0014	50
PTFE	2.2	0.001	80

There are two main systems for bump materials. One of them is to use solder alloys as the bump materials, which means the bumps have to be melted (also called reflow) to form balls with an uniform alloy composition. The other one system for the bumping process is to use a single metal material as the bump material. Several metals have been attempted, such as Au, Cu, and Ni. No further melting is needed in this case and the bumps can sustain higher temperature processing.

For the solder bump materials, the investigations are currently towards use of lead-free solder alloys because of the environment protection issues. The aim is to find alternative alloys with similar characteristics to those of lead-based solders so that they are compatible with existing manufacturing processes, components, and end-use environments [6]. Table 3 lists the viable alternatives of the lead-free solders recommended to take place of tin-lead (Sn-Pb) solders in the melting temperature range of 183 ^{o}C to 232 ^{o}C. They are identified as tin-based binary to quaternary alloy systems. Indium-containing lead-free alloys were found to have a higher fatigue resistance (ability to withstand repeated and varying loads) due to the ductility of

indium metal. 88.5Sn/3.0Ag/0.5Cu/8.0In, 91.5Sn/3.5Ag/1.0Bi/4.0In and 92.8Sn/ 0.7Cu/0.5Ga/6.0In are high-fatigue resistant materials with a melting point below 215 ^{o}C. They are expected as the possible candidates as lead-free solder bumps for highly reliable flip chip assembly [6]. From the aspect of application, however, so far in the literatures very few researches reported the demonstrated data using lead-free solder as the bump materials for the microwave flip chip assembly. Only Sn95/Au5 solder alloy has been used for flip chip interconnect at microwave frequencies [7-9].

Table 3. The comparison of viable lead-free alloys and eutectic lead-tin solder, [6]

Alloy	Melting temperature (^{o}C)	Fatigue resistance
85.2Sn/4.1Ag/2.2Bi/0.5Cu/8.0In	193~199	10,000~12,000
88.5Sn/3.0Ag/0.5Cu/8.0In	195~201	>19,000
91.5Sn/3.5Ag/1.0Bi/4.0In	208~212	10,000~12,000
93.5Sn/3.1Ag/3.1Bi/0.5Cu	209~212	6,000~9,000
92.8Sn/0.7Cu/0.5Ga/6.0In	210~215	10,000~12,000
95.4Sn/3.1Ag/0.5Cu	216~217	216~217
96.5Sn/3.5Ag	221	4186
99.3Sn/0.7Cu	227	1125
63.0Sn/37.0Pb	183	3650

One single metal material is another good option for the bumps. Compared with the solder bumps, non-melting metal bumps have a wider temperature range for processing, which can maintain the higher chip-to-substrate gap in subsequent high temperature processes. Additionally, the mechanical shear strength of soft metals (like Au and Cu) are higher compared to the lead solders, which helps alleviate thermal stresses resulted from the CTE mismatch of the chip and substrate materials and therefore strengthens the bumps connections [6]. Overall, Au bumps are the most commonly used metal bumps today. Cu bump is a new emerging bump material for flip chip assembly. Compared with Au, Cu is of course a low-cost metal; it also offers comparable electrical and heat-dissipation performance because of its low electrical resistivity and high thermal conductivity. However, the oxidation of the Cu surface is an issue during the process or the later bonding.

About the materials used in this thesis work, a brief summary is given here. Most chips for microwave applications are of GaAs because of its superior intrinsic properties over Si, such as higher electron mobility (GaAs: 8500 $cm^2V^{-1}s^{-1}$, Si: 1350 $cm^2V^{-1}s^{-1}$), making it better for high frequency operation than Si. GaAs is also an intrinsic semi-insulating material; the intrinsic reisistivity of GaAs is higher than Si.

Therefore, in the entire thesis work, GaAs is used as the chip material for the demonstration samples. Besides, alumina (Al_2O_3) is used as the substrate material to fabricate the circuits and bumps on it, which is widely used at microwaves and has a close CTE constant to that of GaAs. Since Au is the metallization metal for most GaAs-based devices or circuits, Au electroplating bumping is chosen as the first developing bumping process in this thesis work, which also can be used for other flip chip assembly work of GaAs MMICs in some relevant projects.

2.4 Flip chip interconnect at high frequencies

The bond-wire interconnect suffers from serious parasitics when the operating frequency reaches the microwave range because of its long interconnect path. In contrast, the flip chip approach is expected as a low cost alternative for high frequency packaging with better RF interconnect performances. Flip chip interconnect has the advantages of the shorter conducting path and therefore lower parasitic effects. It can also achieve the size-reduction and high I/O density packaging. It is generally believed that flip chip approach is a solution for broadband interconnect at high frequencies. The RF performance of the flip chip interconnect are affected by two factors: the detuning effect, the reflection and insertion loss at the bump transition. The effects of these two factors on the flip chip interconnect performance are discussed in the following subsections. Further, to achieve the broadband flip chip interconnect performance, the optimized design using the high impedance line section for compensation is presented as well.

2.4.1 Detuning effect (or proximity effect)

Flip chip bonding makes the chip upside down mounted on the substrate. As a result, the active surface of the chip is close to the substrate, which is separated only by a distance equal to the bump height. The substrate has a significant influence on the electrical characteristics of the chip. This influence is called the detuning effect [10], or the proximity effect [12]. The detuning effect can result in change of electrical characteristics of the circuit elements on the chip, such as the shift in resonant frequency of an oscillator due to the dielectric loading. The transmission line and spiral inductor are sensitive to the detuning while transistors and small-size components do not show noticeable influence [1]. The detuning extent can vary with

the transmission line type on the MMICs chip and the chip-to-substrate spacing [10-13]. Fig. 4 shows the different electrical field distribution of microstrip and coplanar chips mounted on the substrate. Fig. 5 shows the deviation of the quantitative data for 50 Ω MS line and CPW line as a function of chip-to-substrate spacing (bump height) at 50 GHz. If there is metallization underneath the chip, the detuning effect becomes even stronger, as shown in Fig. 6 [10]. To avoid strong detuning effect, two general criteria for the suggested minimum value of the bump height are given in the further detailed study. The first one is for microstrip case that the bump height is suggested to be higher than half the thickness of the chip. Second, for coplanar chips, the bump height is suggested to be higher than one third of the ground-to-ground spacing [1]. Generally, higher bump height gives less detuning effect on the chip; and the metallization on the substrate underneath the chip should be avoided to lower the detuning effect. Besides, if underfill is injected into the gap, the detuning effect is even more pronounced due to the larger permittivity of the dielectric material contacts directly to the chip surface.

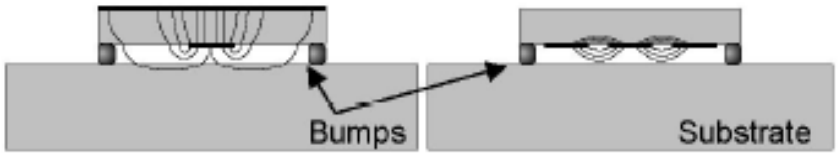


Fig. 4. The electric field distributions of microstrip and coplanar waveguide MMICs chips mounted on the substrate, [13].

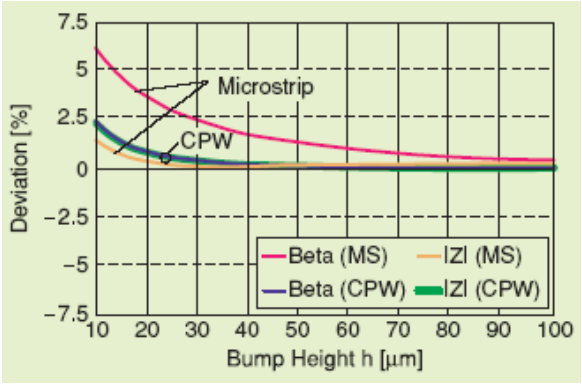


Fig. 5. Detuning effect. The deviation of phase constant beta and characteristic impedance as a function of bump height for a 50 Ω MS line and CPW line at 50 GHz, [1].

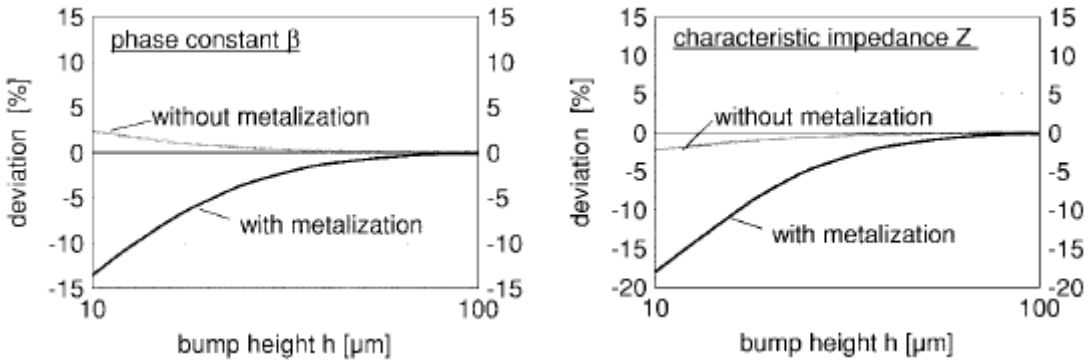


Fig. 6. Detuning effect. The deviation of CPW transmission line parameters as a function of bump height with and without metallization underneath the chip. [10]

Another effective option to avoid the detuning effect is that the MMIC chip is face-up mounted to the substrate. In this way, the signal transmission path has to go through the chip by via technique. This approach is called hot-via technique [14], or direct backside interconnect technology (DBIT) [15]. The hot-via technique is also part of study in this thesis work, which is presented and discussed in detail in Chapter 4.

2.4.2 Reflection and insertion loss at bump interconnect

The geometric parameters at the bump transition have influences on the RF interconnect performance. The geometric parameters include the bump height, diameter, shape, and the pads overlap. In the various studies, the design rules for the optimum parameters have been developed to achieve the low-loss interconnect performance.

The MMIC chip is mounted upside down onto the substrate carrier by means of the metallic bumps as the mechanical, physical and electrical connections. By using the different bonding methods, the consequent shape of the bump may differ after bonding. In the case of the thermo-compression method, the bump is compressed and a maintaining constant volume of the bump results in a convex shape of the bump. Fig. 7 shows an example of Au bump in a convex shape after thermo-compression bonding. On the other hand, by soldering joining, the shape of bump is determined by the surface tension phenomenon of the bump. The bump shape varies with UBM (Under Bump Metallurgy) size and the chip-to-substrate distance. For instance, when the distance between the chip and substrate is fixed during bonding, the bump ends up with a concave shape. In another situation, the shape of the solder bump can be in a convex shape as well. The simulated results of various bump shapes are shown in Fig.

8 [16]. The performance variation with different bump geometry is more pronounced at higher frequencies. The concave bump shape gives the best return loss and the lowest reflection coefficient. But the variation of the insertion loss is only with 0.4 dB for the different bump shapes.

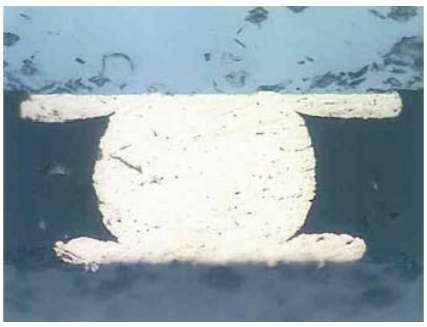


Fig. 7. The Au bump shape after thermo-compression bonding, [1].

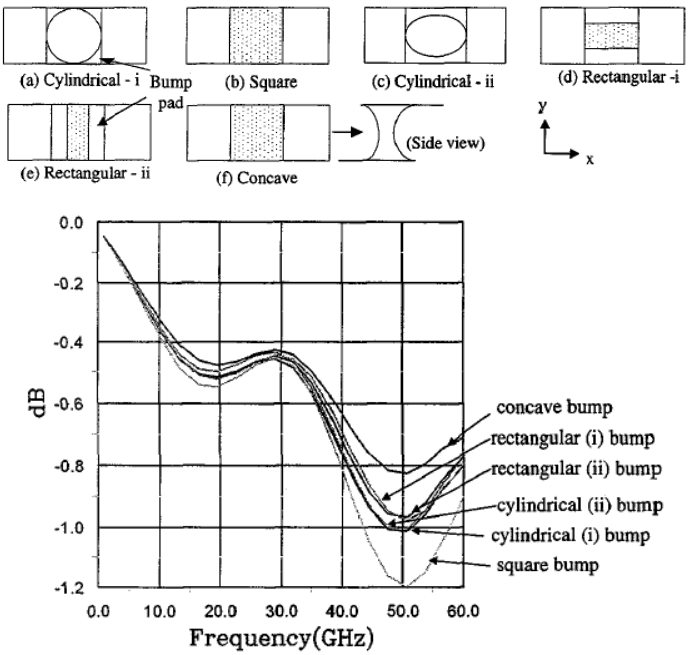


Fig. 8. The simulated results of the insertion loss vs. frequency for the different bump geometric shapes, [16].

Fig. 9 illustrates the CPW-to-CPW flip chip interconnect and indicates the related dimensional parameters. By performing the DOE (Design of Experiments) technique with a factorial experiment, the parameters having strong influence on the interconnect performance are found to be the pad overlap, the bump diameter, and the CPW signal width [17, 18]. In contrast, the other parameters have minor influence on the interconnect performance. The evidence can be found as well in the other reports [1, 10-11, 19]. The wider pad overlap deteriorates the reflection, as shown in Fig. 10

(a); the higher bump height improves the reflection slightly, as shown in Fig. 10 (b) [10].

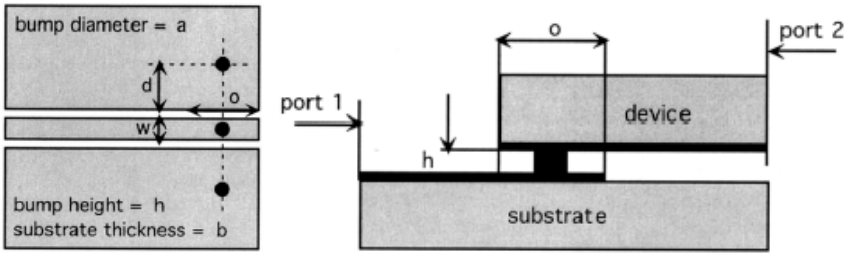


Fig. 9. The CPW-to-CPW flip chip interconnect and the related dimension parameters. The bump height (h), the bump diameter (a), the pad overlap (o), the CPW signal width (w), the ground bump position (d), the substrate thickness (b), [17].

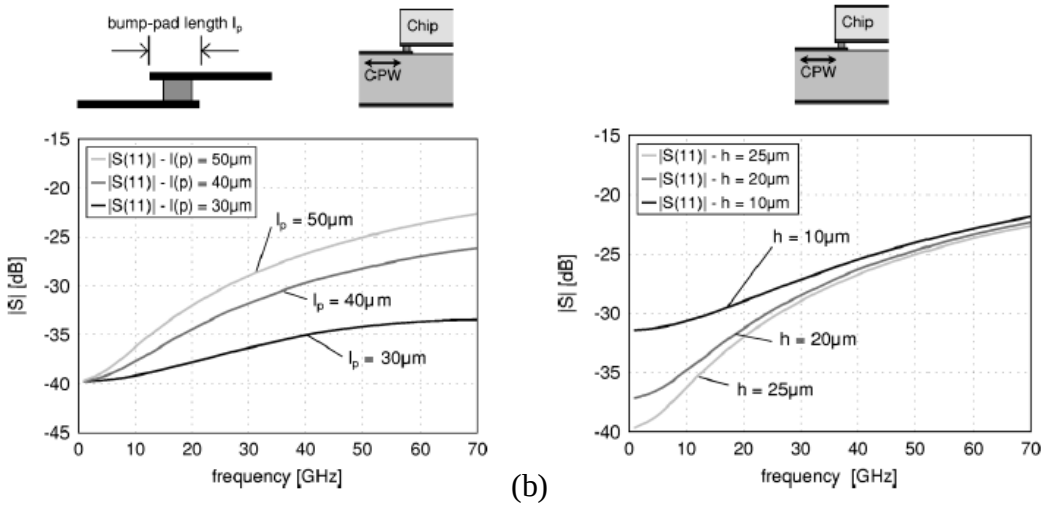


Fig. 10. Reflection of a single CPW-to-CPW transition as a function of frequency for the two parameters. (a) The pad overlap. (b) The bump height, [10].

The general design rules for the flip chip interconnect can be summarized as follows [1, 10-13, 18, 20-21].

a. The bump height affects the detuning effect of the chip; the larger bump height improves the interconnect performance slightly. It is suggested that the bump height should be large enough to avoid the detuning effect. Quantitatively, the value *h*/*d* should be larger than 0.3 for coplanar chips, where *h* represents the bump height and *d* represents the ground-to-ground spacing of the CPW line on the chip.
b. The bump diameter and the pad overlap should be kept as small as possible to achieve the minimum reflection at the bump interconnect. It causes the dielectric loading of the transition, which is identified as the main source of

the reflection. In practice, however, the limit is given by the bump diameter plus the margin required for the bump placement. And the bump diameter together with the bump height is limited by the bumping process capability.

c. The extended edge area of the chip outside the pads should be kept as small as possible, which means one should only leave the minimum edge enough for the dicing tolerance.

2.4.3 Further compensation design to achieve broadband interconnect performance

Flip chip interconnect is a combination of the inductive and capacitive effects [1]. Fig. 11 shows the two different contributions. The inductive contribution comes from the change in the current flow because of the vertical interconnect. Also, the three bumps (ground-signal-ground bumps or G-S-G bumps) in the air form a short transmission line section, which has relatively high impedance and definitely gives an inductive contribution. On the other hand, the interconnect section with the pads connecting the chip and substrate causes dielectric loading and therefore gives a capacitive contribution. Both contributions exist, but for the typical dimensions of the microwave flip chip structure, the capacitive effect dominates because the capacitance exceeds the inductive part.

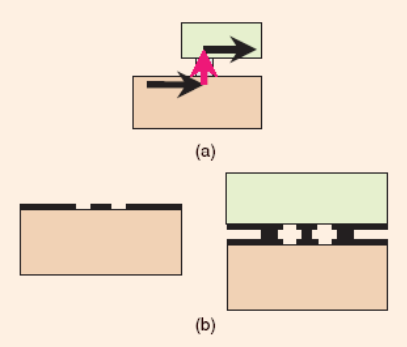
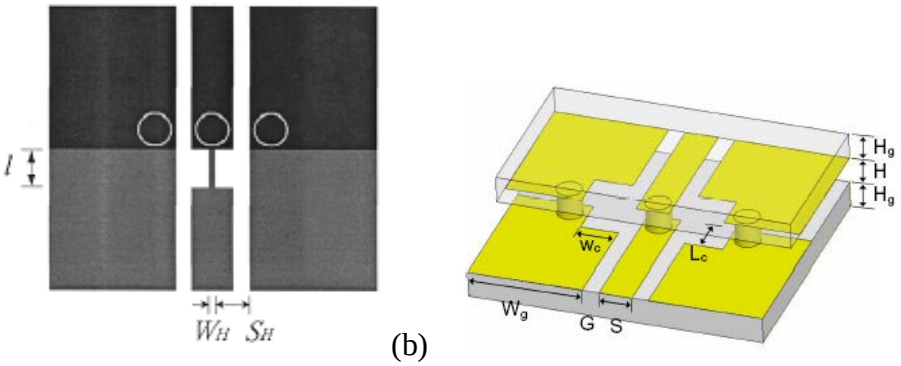


Fig. 11. The inductive and capacitive contributions of the flip chip interconnect. (a) The inductive effect. (b) The capacitive effect, [1].

To lower the reflection at the interconnect to get a broadband performance, two main ways have been attempted to compensate the capacitive effect. One is by introducing a high impedance line section exhibiting the inductive effect at the interconnect for compensation, as shown in Fig. 12 (a) [22, 24-25, 27]. The other one is modifying the ground pads layout to make the transition less capacitive and enhance the inductive

part, shown in Fig. 12 (b) [19, 22-26]. Fig. 13 shows the broadband flip chip interconnect performance after the compensation design, showing the return loss better than 15 dB from DC up to 100 GHz.



(a) (b)

Fig. 12. Two different compensation designs. (a) A high impedance transmission line section, [22]. (b) Modification of the ground pads, [23].

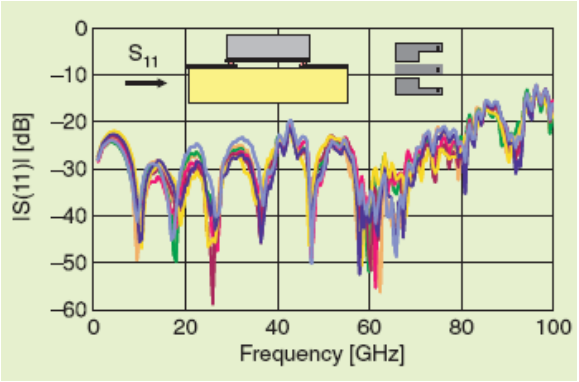


Fig. 13. The broadband flip chip interconnect performance, [27].

Another way to compensate the capacitive behavior of the flip chip interconnect is the use of the staggered bumps [19, 25, 28-30]. Fig. 14 shows the staggered bump scheme and the effective improvement on the reflection property. Because the signal line is elevated in advance and the ground lines still lie on the substrate, the main part of the field is concentrated in the air, acting like a high impedance line section and counteracting the exceeding capacitance to minimize the reflection at the interconnect.

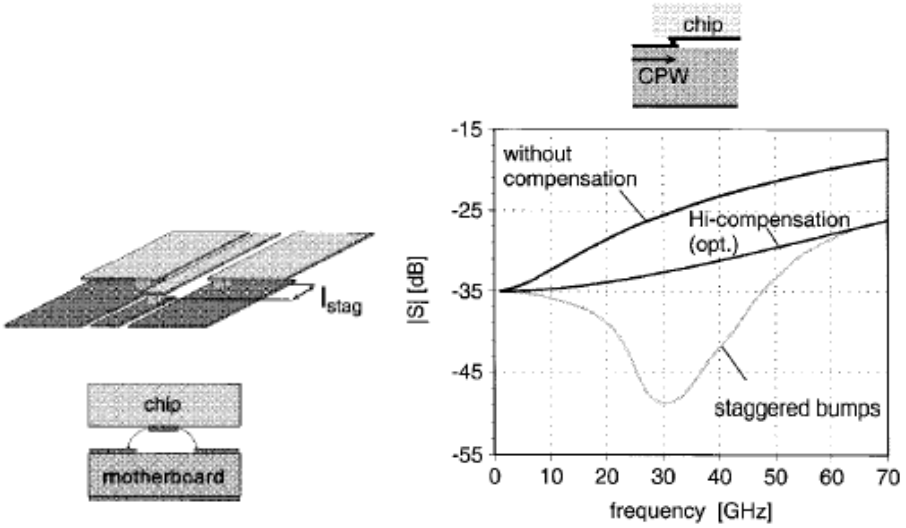


Fig. 14. The stagger bumps scheme and its effective improvement on the reflection property, [19].

2.4.4 Underfill impact on the interconnect performance

Underfill can help relieve the thermal stress caused by the CTE mismatch between the different materials in the flip chip structure during the temperature variation to ensure the bump joints reliability [31]. Underfill also protects the chip from the moisture, the ionic contaminants, and the mechanical damage in the various operating environments. However, it affects the electrical performance of the flip chip assembly especially at high frequencies, resulting from the higher dielectric constant (usually 3~4) and the higher dissipation factor (approximately 0.05 at 10 MHz) as compared to the air. Fig. 15 shows a comparison of the measured S parameters of the CPW flip chip assembly with and without underfill. The underfill mainly induces additional transmission loss to the final assembly and changes the effective dielectric constant of the transmission line on the MMICs [32-36]. So does the glob top encapsulation affect the signal transmission in the CPW flip chip assembly, as shown in Fig. 16 [37]. The effects of the underfill and the glob top encapsulation should be taken into consideration in advance at the circuit design stage if the MMICs were assembled in such environments. One efficient way to alleviate the underfill impact on the electrical performance is to coat a low-*k* and low-loss dielectric layer such as BCB on the chip surface with a sufficient thickness before flip chip assembly so that the EM fields of the transmission lines confines in the dielectric layer and the chip [38].

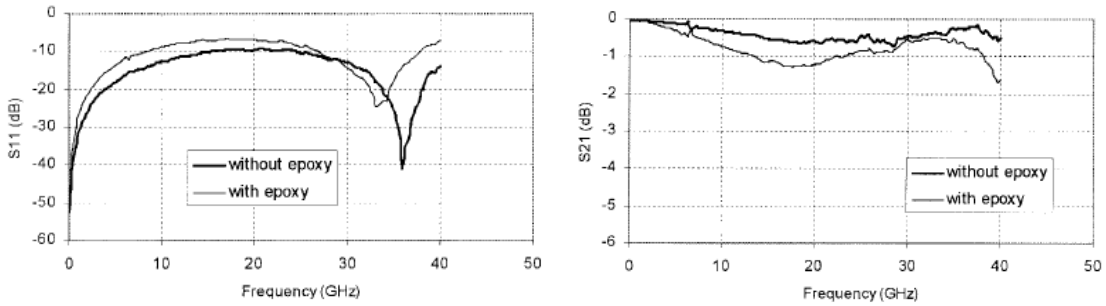


Fig. 15. Comparison of the measured S parameters of the flip chip assembly with and without underfill, [32].

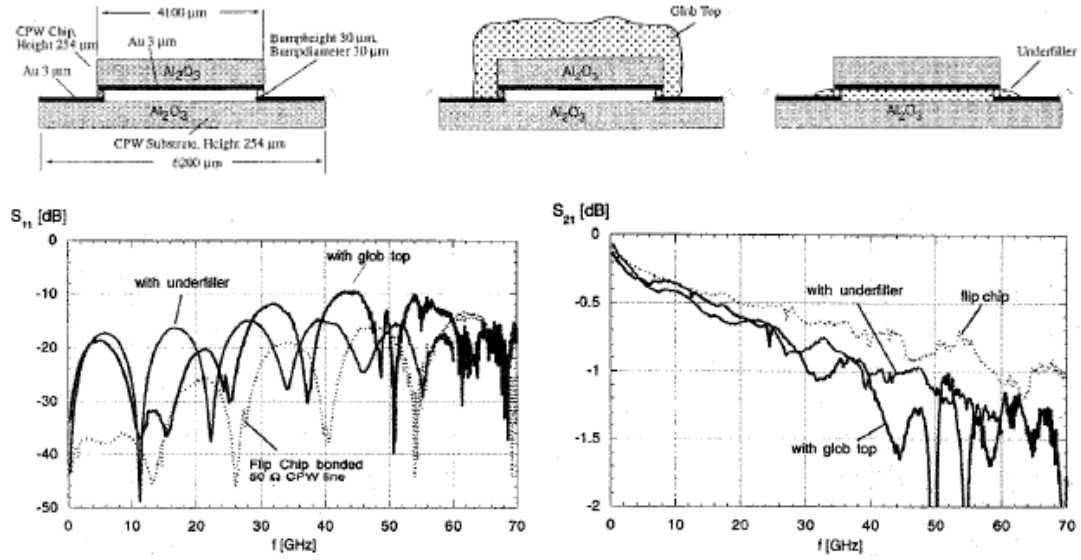


Fig. 16. The comparison of the flip chip bonded CPW transmission line with the the glob top encapsulation and the underfill, [37].

2.5 Summary

To ensure the long-term reliability of the flip chip structure, the substrate materials and the bumping materials should be carefully chosen for the corresponding chip and pad materials before carrying out the assembly process. CTE mismatch is a big concern in this regard. In the conventional flip chip architecture, in order to achieve good interconnect performance, the bump height should be high enough to avoid the chip detuning effect, and the pad overlap must be kept as small as possible to lower the capacitance effect dominating at the interconnect. The use of the compensation, the high impedance line, helps attain broadband flip chip interconnect performance. Underfill causes impact on the flip chip interconnect performance by changing the

effective dielectric constant of the transmission line and inducing additional insertion loss. It should be taken into consideration in advance before the flip chip assembly.

Chapter 3

Flip Chip Bumping and Bonding Process

Flip chip assembly contains three major processing steps. The first step is bumping, to deposit the conductive bumps on the chip or substrate pads. The second one is bonding, to perform a face-down connection of the chip to the substrate by the bumps. The final step is the underfill injection, to fill the gap between the chip and the substrate with an underfill material for protection and thermo-mechanical management. The third step may be omitted in some processes, especially for packaging applications at high frequencies. There are different methods for bumping and corresponding bonding process. In the following, the diverse processing techniques are reviewed first, and the standard Au bumping and flip chip thermo-compression bonding processes which have been developed in-house are briefly described.

3.1 Bumping methods

Previously, two main systems for the bumps materials have been addressed. They are solder bumps and metal bumps. For solder bumps, the bumps are melted to form balls with a uniform alloy composition. For metal bumps, no further melting is needed. The different bumping processes for these two different bump-material systems are summarized in the following subsections.

3.1.1 Solder bumping method

Most of the solder bumping are batch fabrication process. Mostly bumps are fabricated on IC wafers. Prior to bumping, the wafer needs successive depositions of under-bump metals (UBM) on the bonding pads of ICs. The purpose of UBM is to provide a platform for connecting the wafer metallurgy to the solder bump metallurgy. Fig. 17 shows the illustration of the solder bumping on the chip pad via UBM metal. UBM preparations involve several sequential dry and wet processes, for example, wet etching, sputtering, electroplating or electroless-plating [39]. The bumps are

fabricated on the UBM in cylinder or mushroom shapes and then reflowed into smooth balls before the subsequent process of solder bonding. Fig. 18 shows the SEM image of the reflowed solder bumps on the chip pads. Electroplating and stencil printing are the most frequently used deposition techniques for solder bumping. Bumping by electroplating allows closer spacing between bumps, making it superior to achieve high-density bump arrays. However, this bumping method requires a careful and accurate control of plating conditions to avoid variations in alloy compositions. On the other hand, stencil printing of solder pastes gives a better control of the bump compositions for all alloy systems. The minimum bump pitch with current stencil printing technique is about 120 μm [6]. To realize fine-pitch bumping, the solder pastes require further development.

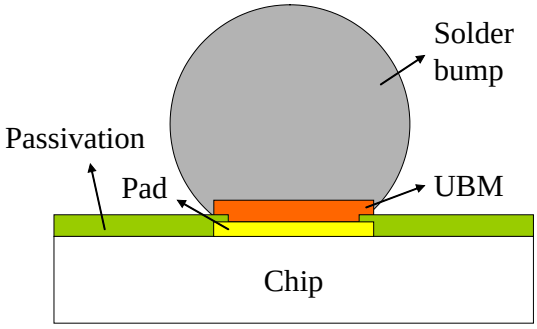


Fig. 17. The schematic of a solder bump on the chip pad via UBM metal.

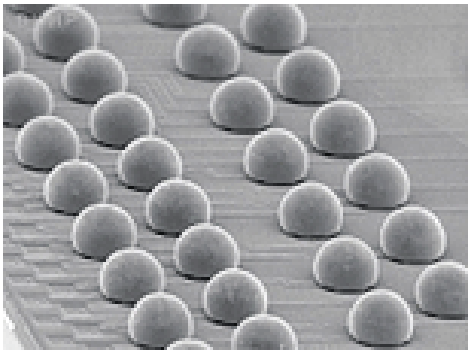


Fig. 18. The SEM image of the reflowed solder bumps on the chip pads. (Source: www.samsung.com)

3.1.2 Metal bumping method

Two ways to form metal bumps are stud bumping and electroplating. Stud bumping is an extended technique of the classic Au wire bonding to form metal bumps. It is a widely adopted method to fabricate Au bumps. The process starts with ball bonding the Au wire to a chip pad. After the Au ball is bonded to the pad, the Au wire is cut off

then, leaving a Au stud attached to the pad. To get a uniform bump height, the studs may be flattened (or called “coined”) by pressing any remaining wire tail to the ball or shearing it off. Fig. 19 shows the SEM images of the stud Au bump and the flattened Au stud bumps. Unlike the solder ball bumping technique, Au stud bumping requires no UBM on the chip pads. Any wire-bondable chip can be applied for flip chip assembly at either the individual chip level or wafer level without any additional wafer processing, making the bumping process highly flexible. Just like wire bonding, however, stud bumping suffers from being a sequential process, a time-consuming process. Therefore, it is really not an efficient way to bump chip with high I/Os.

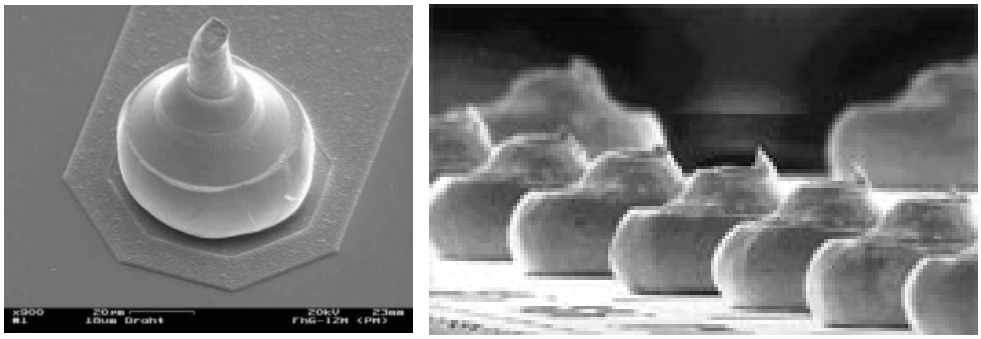


Fig. 19. The SEM images of the gold stud bump and the flattened gold stud bumps. (Source: www.pb.izm.fhg.de and www.kns.com)

For the chips with high I/O density, electroplating is a more practical way for bumping. Bumping by electroplating requires patterned photoresist as a template mask on top of a successive and conductive seed layer. Electroplating is performed in the regions which are not covered by the photoresist. The photoresist mask and the surrounding seed layer are then removed, finalizing metal bumping process. Fig. 20 shows the in-house electroplated Au pillar bump. The process flow of Au bumping by electroplating will be described later in the in-house developed standard Au bumping process. With the suitable plating bath and carefully controlled plating conditions, the plated Au bumps show comparable mechanical and electrical properties with those of wire bonded Au studs. In many applications, however, cost is always the constraint. Both the material cost and processing cost must be taken into consideration. Au is a very high cost metal; consequently, Au bumping is limited to the applications with low I/O density.

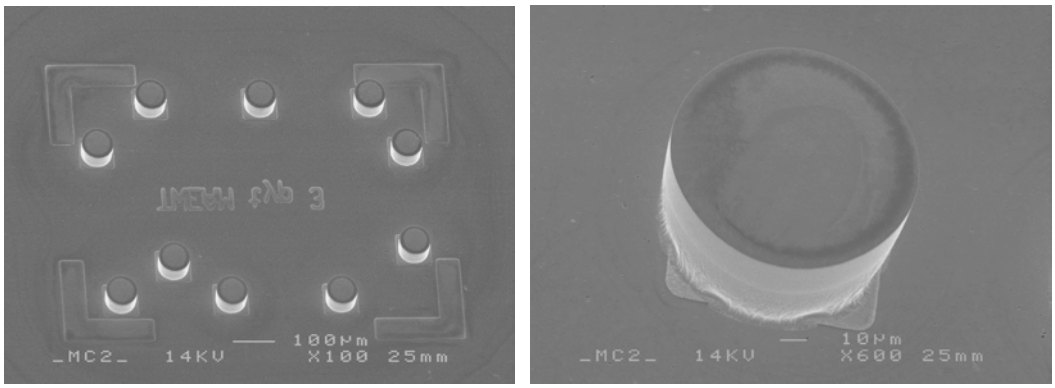


Fig. 20. SEM images of the electroplated Au pillars (in-house fabricated and photographed at MC2).

Compared with Au, Cu is of course a low-cost metal; it also offers the comparable electrical and heat-dissipation performance because of its low electrical resistivity and high thermal conductivity. Like Au bumping, Cu bumping by electroplating can have precise control of the bump dimensions to achieve high aspect ratio bumps for some special applications. Fig. 21 gives an example of the Cu bumping by electroplating with a very high aspect ratio (about 5). To prevent the Cu bump surface from oxidization in air and to facilitate the subsequent flip chip bonding process, the Cu bumps were coated with solder caps. Fig. 22 shows the plated Cu bumps with the reflowed eutectic solder caps, proposed and proven by TLMI Corp. The amount of solder must be carefully controlled to give the required thickness of solder for final soldering assembly. A thin layer of Au over the Cu was suggested to provide a long-lasting oxidation-free surface. On the other hand, Cu stud bumping has been demonstrated as well [40]. Cu studs can be directly bonded to the Al bonding pads by using a thermosonic wire bonding machine. However, the ultrasonic power and bonding force are generally higher than for the Au stud bumping due to the hardness of Cu. Besides, a forming gas (8% hydrogen in nitrogen) must be blown over the end of the Cu wire during the formation of the ball to prevent Cu from oxidation. Cu stud bumping is relatively new in the flip chip industry; and further investigation on the bonding chemistry and optimization of the bumping parameters are required.

Overall, Cu bumping has many advantages over solder and Au bumping such as better electrical and mechanical properties and reduction of cost, but more research in this area are required before it can be prevailed in the flip chip assembly technology.

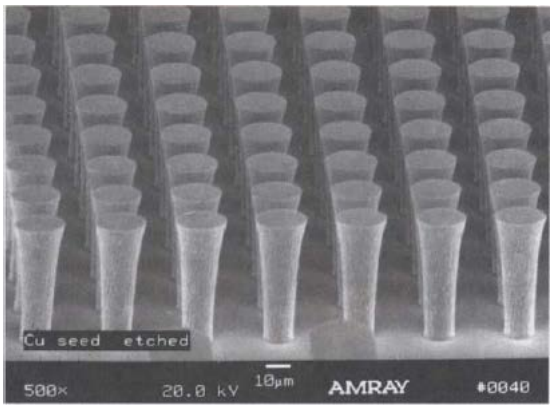


Fig. 21. SEM image of the plated copper bump on silicon chip with a high aspect ratio (around 5) and in a face-area pitch of 30μm. (Source: Fujitsu Computer Packaging Technologies, Inc.)

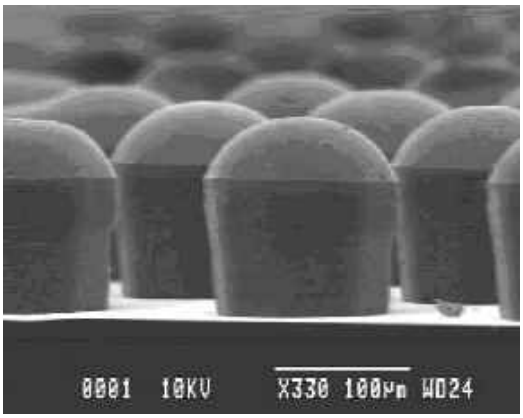


Fig. 22. Plated copper bumps with the reflowed eutectic solder caps. (Source: TLMI Corporation.)

3.2 Flip chip bonding methods

There are many different flip-chip bonding methods. The flip chip bonding methods varies with the bump materials and the different applications. Table 4 lists the various bonding methods corresponding to the bump materials that have been reported or suggested [6]. Fig. 23 shows the illustrations of the different bonding methods [2].

Table 4. The various bonding methods corresponding to the different bump materials, [6].

Bump materials	**Flip chip bonding methods**
Solder bump	Soldering
Gold bump	Adhesive joining (isotropic conductive adhesive, anisotropic conductive adhesive, non conductive adhesive) Thermo-compression bonding Thermo-sonic bonding Soldering
Copper bump	Soldering Adhesive joining

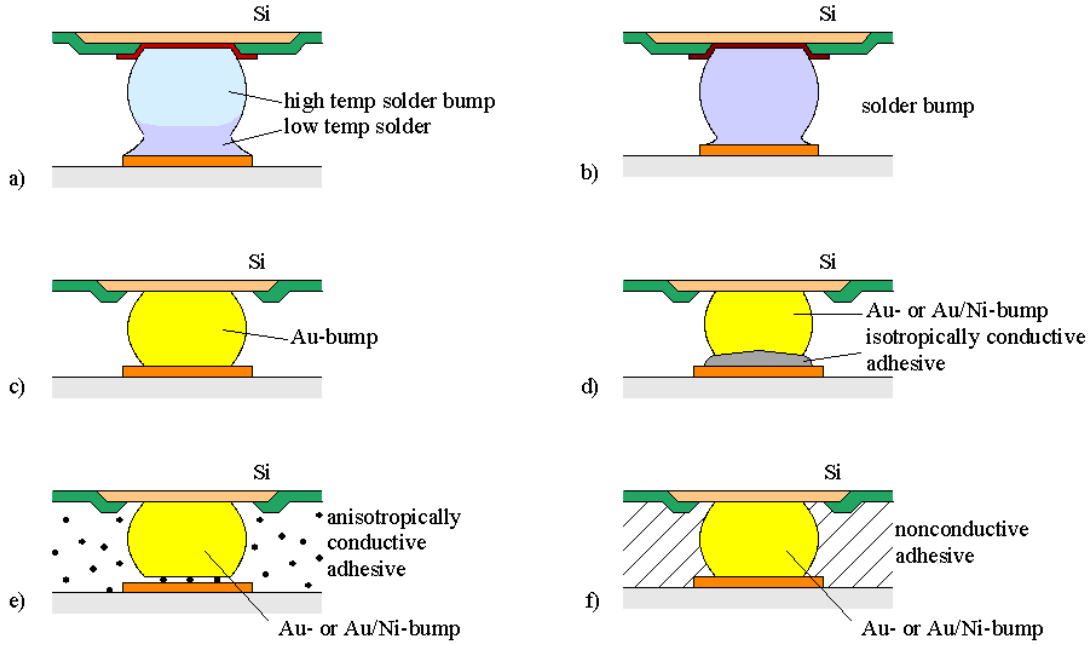


Fig. 23. Examples of some flip chip bonding methods, (Source: extra.ivf.se).

3.2.1 Soldering

Soldering is a commonly used process for direct joining of the solder bumps to the opposing bond pads. During soldering bonding, the joint between the solder bump and the bonding pad (perhaps the metal bump on the pad) is formed by reflow when the bonding temperature is maintained above the solder melting point. From the aspect of

the materials engineering, the soldering is a complex interfacial reaction, where the intermetallic compounds (IMCs) is formed for the mechanical joint. The volume and composition of the IMCs have to be controlled properly. Too much IMCs make the bonding weak and brittle, leading to the failure of the joint. UBM and TSM play important roles in the soldering process, which includes three main metal layers, the adhesion layer, the diffusion barrier, and the wetting layer [41]. The metal and thickness for each layer should be carefully considered because of the reliability issues.

In addition, soldering is also less popular with Au bumps. It can be attributed to the fast inter-diffusion of Au into the Sn alloy, which soon consumes the soft solder and forms brittle IMCs at the solder joint [42]. Due to the brittle intermetallics (IMCs), the solder joint is very weak and has to be protected by the underfill epoxy.

Generally, prior to soldering process, flux is applied onto the bonding pads or solder bumps to clean oxidized surfaces which are going to be joined together to enhance the wetting property of the solder in the molten state [43-44]. To achieve this, the flux must be able to deoxidize metal surfaces at high temperatures without decomposing. Consequently, flux residues, the reaction products of flux and metal, have to be removed. Otherwise the residues left on the components, especially when ionic, can cause electrical shorts or corrosion of the microcircuit and give rise to the long-term reliability problems. Some flux residues are water soluble, while some have to be removed by aggressive solvents. Post-cleaning of the flux residues has always been a big concern in solder-based flip chip bonding, and at present the technique about flux is still under development.

3.2.2 Adhesive bonding

There are three types of adhesives, isotropic conductive adhesive (ICA), anisotropic conductive adhesive (ACA), and non conductive adhesive (NCA). For different purposes and applications, different type of adhesive is chosen. The different conductive properties of these adhesives lead to the different final bonding results, as shown in Figs. 23 (d)-(f). Adhesive bonding shows several advantages. No post-cleaning is required to remove flux residues because adhesive needs no fluxing. Compared with the soldering process, the process steps are relatively simplified, for example, the elimination of UBM fabrication process and solder bump fabrication process. In ACA and NCA applications, the adhesive film also acts as underfill

material, which is simultaneously formed in the bonding process providing thermal and mechanical managements. Adhesive bonding is usually accompanied with the Au bumps, which can be easily accomplished just by stud bumping technique without further special preparation for bumping.

ICA is composed of an adhesive binder and conductive particles such as Ag flakes, providing a low electrical resistance in all directions. The adhesive has to be placed locally on the bonding pad by stencil printing or coated onto the bump surface by dipping the bumps into a thin layer of the adhesive. The bumps and their corresponding bonding pads are joined together while heat curing of the ICAs. A non-conductive underfill resin is generally required to reduce the thermal stress at ICA joints and ensure the reliability of the connections.

ACA consists of epoxy resins and small conductive particles approximately about a few microns in size, for example, Au-coated polymer spheres. The adhesive is dispensed on the whole substrate prior to chip bonding. When the chip is forced to the substrate, the adhesive fills all the space between chip and substrate and surrounds the bumps. The conductive connection is achieved by the small conductive particles trapped in the small gap of the bumps and the opposing pads. In other regions between the chip and substrate, the small conductive particles separate apart in the adhesive and isolate electrically. After curing the adhesive, the bonding process and underfill process are accomplished simultaneously. This greatly simplifies the assembly process. The big drawback is that the ACA joints have variations in electrical conductivity due to the different amount of the small conductive particles trapped at the connections, which limits the applications of ACA bonding.

NCA bonding functions in some ways are similar to ACA bonding. After dispensing the adhesive, the bumps are forced to the substrate pads under a sufficient pressure to ensure no adhesive remains between the bumps and pads. After curing the adhesive, the epoxy resin shrinks and holds the chip and substrate tightly and makes the direct bump-to-pad metal connections. The bonding and underfilling processes are done simultaneously just like ACA bonding works. The strong compressive force due to the shrinkage of the epoxy resin allow some difference of CTE between the chip and substrate, which provides good resistance against the thermal shock environment.

3.2.3 Thermo-compression and thermo-sonic bonding

Thermo-compression (TC) bonding is mainly found in the Au bump flip chip

applications. The Au bumps are formed on the substrate by electroplating or stud bumping techniques. During bonding, the bumps are forced to the pads with intimate contact simultaneously under the thermal treatment. The bonding temperature is generally higher (*e.g.* 400 ^{o}C) compared to other bonding processes. The purpose is to soften the material and enhance the atoms diffusion to form bonds. The bonding force and temperature have to be well controlled to achieve good bonding results. Too much force can cause the cracks to the chip passivation and sometimes the bump bridging (*e.g.* short circuits) in a fine-pitch case due to the over-deformation of the bumps. To avoid this, the bonding force is suggested not over 1 N for an 80 μm diameter bump and should be applied with a gradient.

TC bonding can be modified to thermo-sonic (TS) bonding with the aid of ultrasonic energy which helps and speeds up the welding process. The introduction of the ultrasonic energy lowers the bonding temperature and force and shortens the bonding time as well. Therefore, TC bonding is suitable for the chips that are thin, brittle, or intolerant of high temperature, which is of particular importance for the assembly of the temperature sensitive elements or the brittle elements such as GaAs devices and MEMS devices. Additionally, the ultrasonic energy can help break the surface oxides on the Al pads, enabling the welding between Au and Al. Therefore, TS bonding serves more options of the bond pad and bump metallurgy for the flip chip assembly, especially for the case of the Al pads. In a word, TS can offer a flux-free, adhesive-free, and low-temperature bonding process for the flip chip assembly. However, the bonding process actually is a series of complex interactions between the pressure, temperature, and ultrasonic energy, making this technique challenging before it can be widely adopted.

3.3 Bumping and bonding techniques adopted in this research

In this thesis work, metal bumping by electroplating is adopted for the fabrication of the Au bumps on the Al_2O_3 substrate; thermo-compression bonding method is adopted for joining and mounting the chips to the substrates.

The Au bumping process has been successfully developed at both NCTU in Taiwan and Chalmers in Sweden. The successful development of the Au bumping process can

provide the reliable and uniform cylindrical Au pillars on the ceramic substrates for flip chip packaging the microwave chips. This section briefly summarizes the bumping and bonding process procedures of the in-house work. The process details and recipes are attached in the appendixes.

3.3.1 Gold bumping process

Fig. 24 presents the work of the Au bumping process established both at NCTU, Taiwan and MC2, Chalmers, Sweden. The development of the Au bumping process was the major work in the early stage of the PhD study, intending to provide the reliable and repeatable bumped substrates for the flip chip assembly by in-house fabrication. In the first place, Au bumping process has been developed at NCTU, where lots of efforts have been made on testing the process conditions of the thick photoresists. The process established at MC2 has been completed together with Ms Camilla Kärnfelt, and Mr. John Halonen. The report for the details of the fabrication and the process recipes at Chalmers has been written by Mr. Sten Gunarsson, attached in the appendix. The entire fabrication developed in this study and the recipes details are attached in the appendix as well. Fig. 25 shows the results of the successfully fabricated thick photoresists and the Au bumps standing on the substrate.

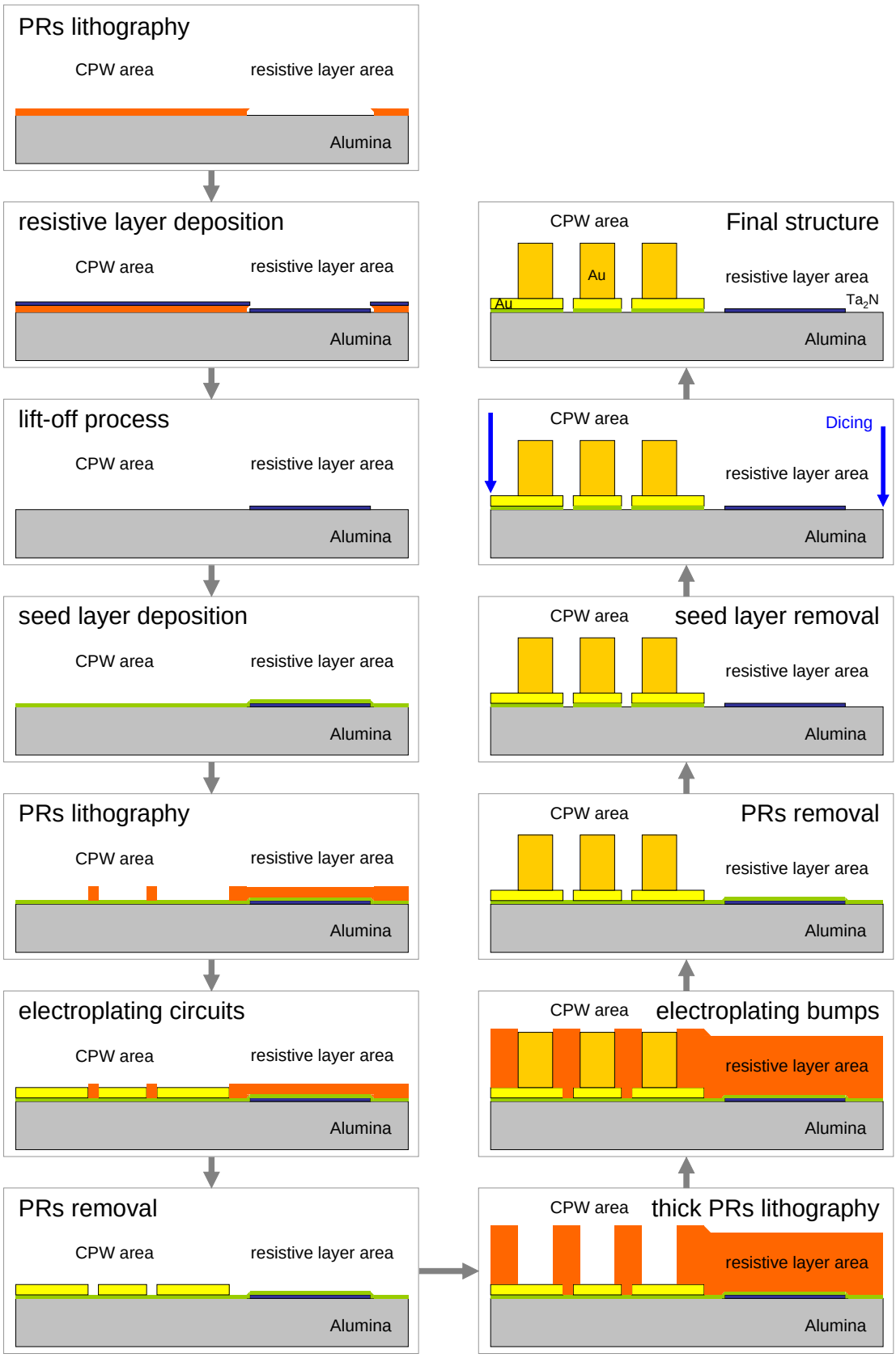


Fig. 24. The fabrication process developed in MC2, Chalmers, with the resistive layer and bumps on the alumina substrate.

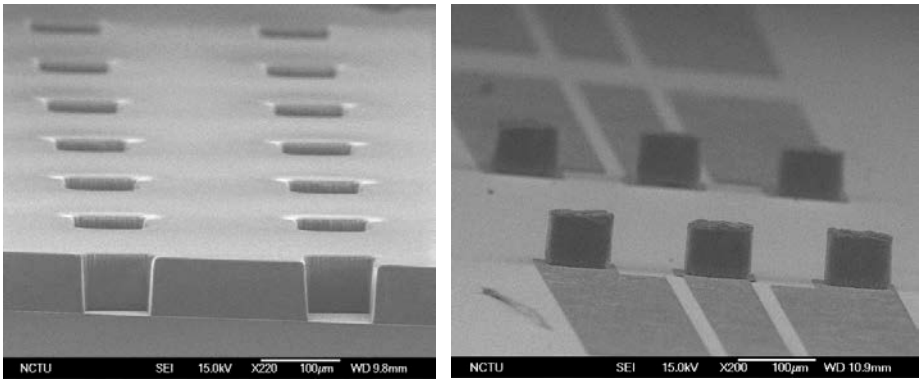
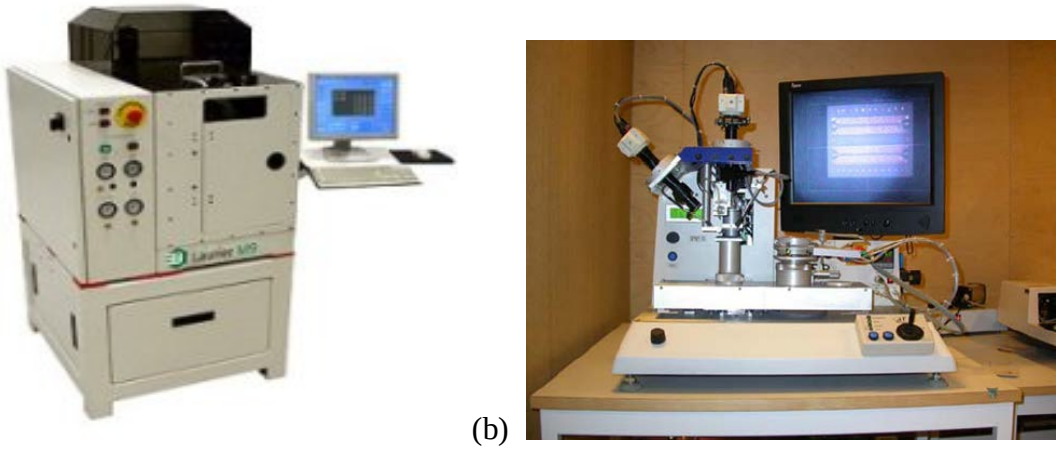


Fig. 25. The SEM images of the fabricated thick photoresists and the gold bumps on the substrate.

3.3.2 Flip chip thermocompression bonding process

Au-to-Au thermocompression bonding is used as the joint technique for the flip chip assembly in this thesis work. Fig. 26 shows the bonding machines respectively at NCTU and Chalmers. The manufacturer of the bonder at NCTU is Laurier Inc. in USA; the manufacturer of the bonder at Chalmers is Céfori ingenierie in France.

The bonding conditions are optimized in order to avoid over-pressure on the Au bumps and achieve less deformation of the bumps with good contact to the pads. The bonding force for a 60 μm-diameter bump is about 10 g. Sometimes in the re-bonding process the bonding force increases a little for the cases of bumped substrates with bad uniformity. The bonding temperature is commonly 300 ^{o}C for the passive structures. For the assembly of the active circuits, the temperature of the chip-side chuck is lowered down to 180 ^{o}C while the temperature on the substrate side is still 300 ^{o}C. The time for bonding is normally 1 min while for certain situations it increases to 2 or 3 minutes. The details of the bonding conditions for different work in this thesis are attached respectively in the appendix. Fig. 27 shows an example of the OM image of the flip chip bonded GaAs MMICs chip.



(a) (b)

Fig. 26. Flip chip bonding machines performing thermocompression for gold-to-gold bonding. (a) The bonder at NCTU. (b) The bonder at Chalmers.

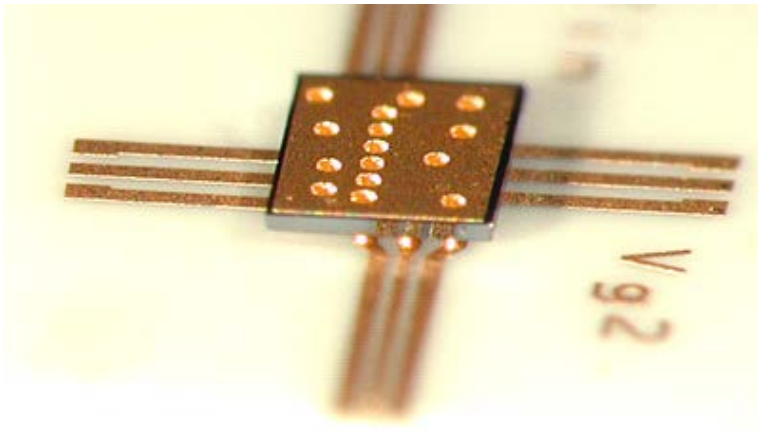


Fig. 27. OM picture of flip-chip bonded GaAs MMIC chip by thermocompression method.

Chapter 4

Hot-Via Transitions for MS-to-CPW Flip Chip Interconnects

This chapter presents an optimized design of hot-via transitions for MS-to-CPW flip chip interconnects, including the full wave EM simulation, the fabrication of the demonstrated structures, and the RF characterizations. The hot-via approach can be applied to the packaging of the microstrip type MMICs without inducing the detuning effect on the chip circuits. The characterized results demonstrated excellent interconnect performance for this approach from DC at least up to 60 GHz. This is the best result, the broadband interconnect performance, at the moment ever reported in the literature, extending the potential of the hot-via approach to higher frequencies for microstrip packaging applications.

4.1 Background of the hot-via transitions

Flip chip architecture is believed to be more compatible with the coplanar chip designs [13] over the microstrip ones because of the occurrence of the detuning effect due to the proximity of the chip to the substrate carrier in the microstrip case. Besides, most existing chip designs are of microstrip type, which is of particular importance for power applications [14]. Therefore, a modified architecture so-called “hot-via” [14] or “direct backside interconnect technology” (DBIT) [15] was proposed to be a good alternative for the flip-chip procedures, showing the compatibility with the microstrip designs. Fig. 28 shows the details of the hot-via transition for the MS-to-CPW flip chip interconnect structure, where the signal passes by the via hole through the chip to the chip backside and by the bump to the substrate transmission line. Because of this, the approach is called hot-via technique.

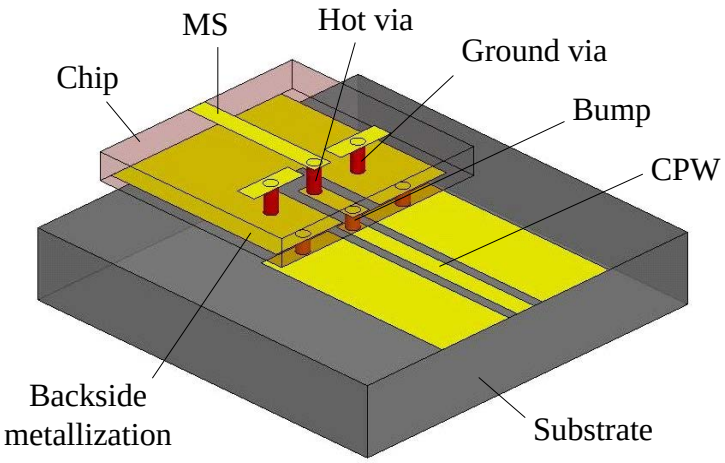
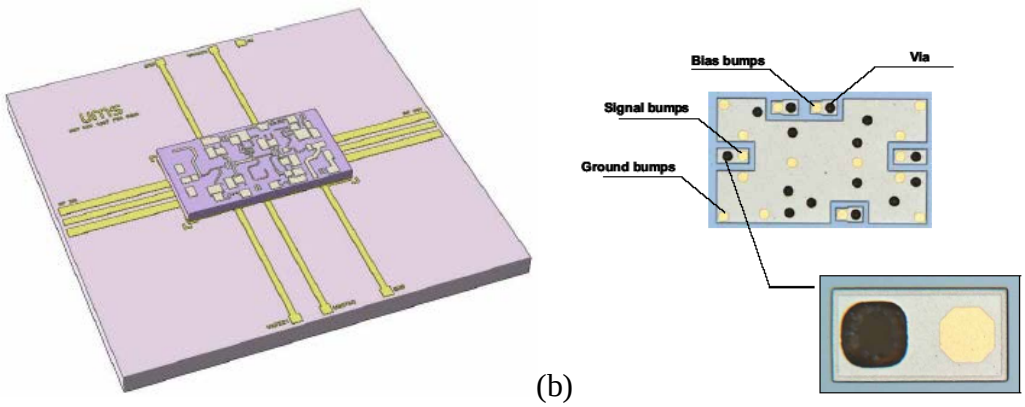


Fig. 28. The details of the hot-via flip chip interconnect structure.

In the MS-to-CPW hot-via architecture, because the chip is face-up mounted to the substrate, the detuning effect due to chip flipping is eliminated; meanwhile, the chip can be optically inspected after bonding. Besides, the backside metallization of the microstrip line acts as a shield against the structure underneath the chip [14]. Like flip chip technique, it also allows the chip to be surface mountable (chip scale packaging, CSP) directly to the motherboard towards the goals of the easy assembly and cost reduction for the packaging [49-50]. Fig. 29 gives an example of a MS MMICs chip mounted to a motherboard using hot-via technique and the backside patterns of the metallization. However, there are some compromises when using the hot-via approach. As compared to the conventional MMICs process, one has to add a step of patterning the backside metallization, which increases the complexity in the process a little. Also, the size of the chip due to the patterned backside metallization is a little larger than the chip size without hot-via approach.



(a) (b)

Fig. 29. (a) An example of a MS MMICs mounted on a motherboard using the hot-via approach. (b) The patterned backside metallization of the MMIC chip, [49].

To date, the hot-via approach with the broadband performance over 40 GHz has not been experimentally proved and reported. Among the reported literatures, one reported MS-to-CPW hot-via interconnect measurement data showed a bandwidth of 5 GHz at 38 GHz with reflection loss beyond 20 dB [14]. Another report demonstrated a good performance from DC to 20 GHz with reflection loss lower than 15 dB using silver coated polymer bumps [15]. A chip-scale packaged LNA MMIC using the hot-via transitions was reported to operate from 13 to 32 GHz with the insertion gain of 15 dB; the input and output return loss was about 10 dB [49-50]. Besides, only a few design data were reported [51-52]. Overall, very little work have been reported on the hot-via technique. More efforts still need to be made for the hot-via approach to improve its transmission properties to achieve broadband interconnect performance for the microwave and millimeter-wave packaging applications.

4.2 Design and parametric simulation

The design of the hot-via flip chip interconnects were performed using the two simulation tools, HFSS and CST microwave studio for the three dimensional electromagnetic field analysis. Fig. 30 shows the simulated model of the hot-via interconnect structure, where the microstrip line on the MMIC chip is connected to the CPW line on the substrate by the hot-via transition and the bump transition.

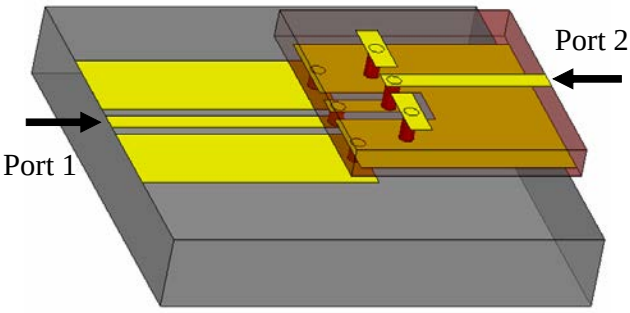


Fig. 30. The simulated model of the MS-to-CPW hot-via flip chip interconnect structure.

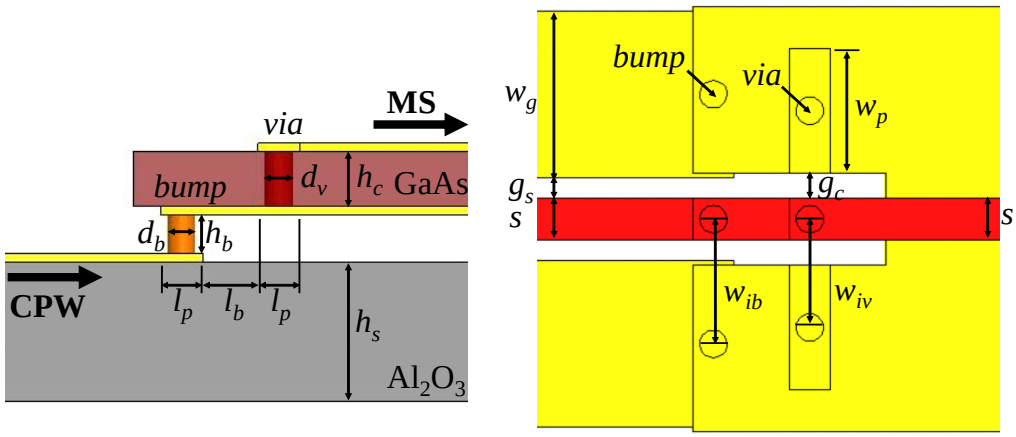


Fig. 31. The physical parameters of the hot-via transition.

Fig. 31 shows the physical parameters of the hot-via transition. The material of the substrate was Al_2O_3, and the material of the chip was GaAs; the thicknesses of the substrate (h_s) and chip (h_c) were 254 μm and 100 mm respectively. The conductor metal was 3 μm Au. The microstrip (signal width, s = 76 μm) on the chip and CPW (s = 76 μm, g_s = 38 μm) on the substrate were with the characteristic impedances (Z_0) equal to 50 Ω. In the following parametric study on the reflection property at the transition, some physical parameters were fixed in the simulation. The width of the ground pads on the chip (w_p) was set at 228 μm, and the gap (g_c) was 46 μm. The signal length on the chip backside (l_b) was 100 μm. In the design, finite-ground coplanar (FGC) waveguide was actually employed on the substrate instead of the conventional CPW with large ground planes to effectively suppress the parallel plate and higher order modes. To eliminate coupling of CPW mode into slotline mode, the symmetry was always kept along the signal transmission lines [53].

By using the full wave EM simulation, the parametric study was performed to explore the effect of each physical parameter of the transition on the reflection property. The parameters of interest investigated here were the via hole diameter (d_v), the pads overlap (l_p), the bump height (h_b), and the bump diameter (d_b).

Fig. 32 shows the simulation results of the return loss *versus* frequency for different via hole diameters (d_b = 30 to 70 μm). From the figure, it is observed that the smaller via hole diameter (d_v), lower the return loss is achieved. Due to the process consideration, however, the parameter d_v can not be too small. The capability of etching process limits the dimension of the via hole, the aspect ratio of the via hole. As can be seen from the figure, when d_v decreases from 50 to 30 μm, the return loss improves about 2 dB at 40 GHz. The wider diameter of the via hole gives the worse

reflection at the interconnect.

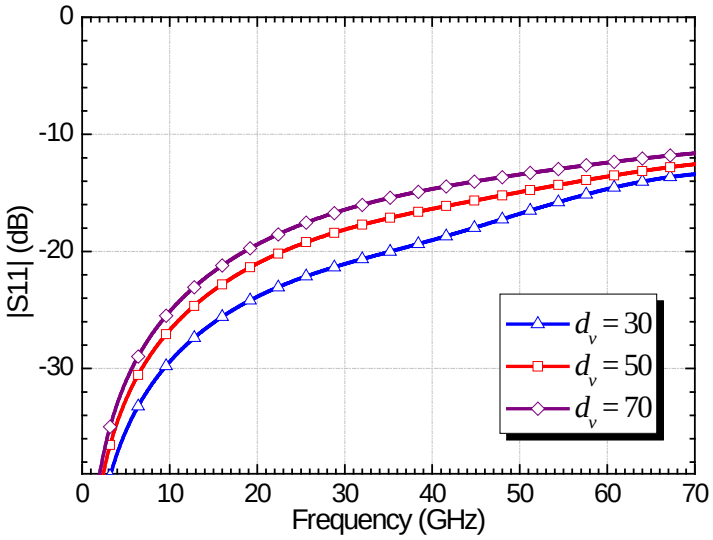


Fig. 32. The simulation data of CPW input return loss versus frequency. The parameter is the via hole diameter (d_v).

Fig. 33 and Fig. 34 show the simulation results of the return loss *versus* frequency for the bump-related parameters, the bump diameters (d_b = 10 to 50 μm) and the bump heights (h_b = 10 to 70 μm). The simulation results in Fig. 33 show that the decrease in the bump diameter (d_b) gives the better return loss. The return loss is improved by 1.7 dB at 40 GHz when d_b decreases from 50 to 10 μm. In Fig. 34, it is obvious that the higher bump height, the better return loss is achieved. The increase in h_b from 10 to 70 μm improves the return loss by 3.2 dB at 40 GHz. From the bump-related simulation results, it can be concluded that the high aspect ratio of the bump is better for the reflection property of the transition at the interconnect.

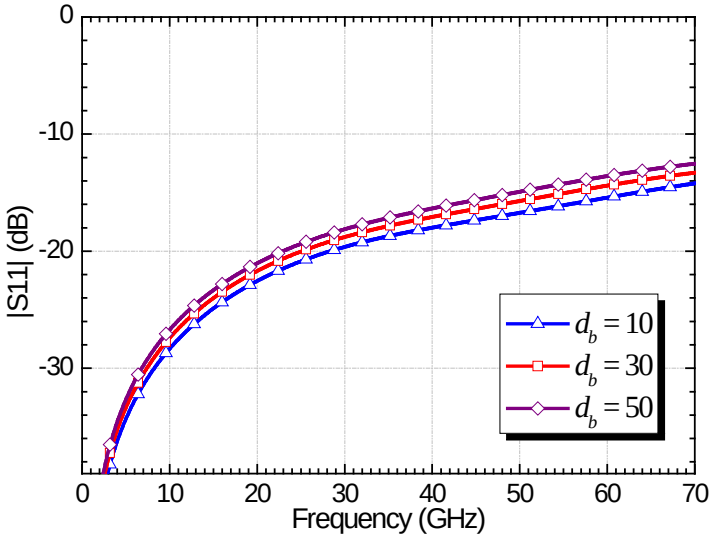


Fig. 33. The simulation data of CPW input return loss versus frequency. The parameter is the bump diameter (d_b).

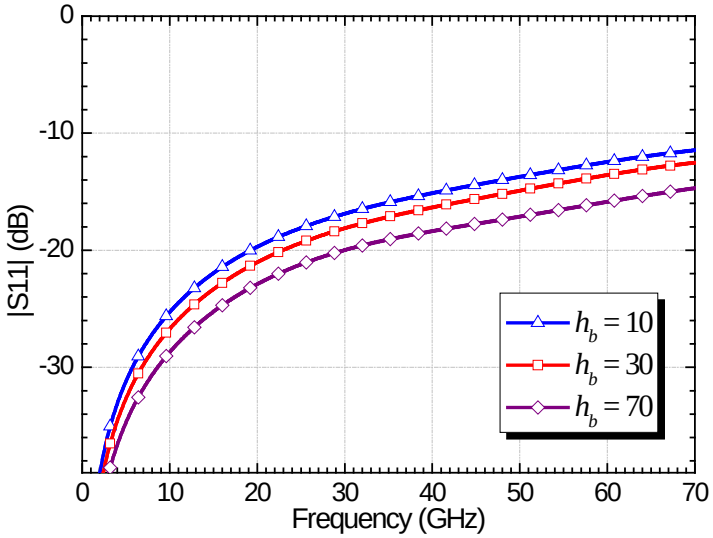


Fig. 34. The simulation data of CPW input return loss versus frequency. The parameter is the bump height (h_b).

The next parameter in the investigation is the pad-related parameter, the pad length (l_p) at the via's side and the bump's side. Fig. 35 and Fig. 36 show the simulation results for different pad overlap lengths (l_p) at the via's side and the bump's side, respectively. The simulation results indicate that the increase in l_p worsens the return loss in both cases. At the via's side, the return loss degrades by 3.8 dB when l_p increases from 76 to 228 μm. At the bump's side, the return loss is worse by 4.4 dB when l_p increases from 76 to 228 μm. It is conclusive that the pad overlap should be kept as small as possible to achieve low reflection for the transition.

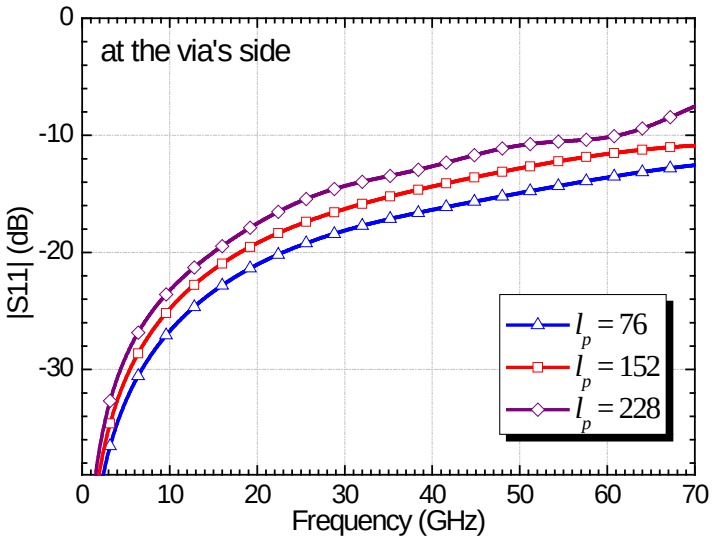


Fig. 35. The simulation data of CPW input return loss versus frequency. The parameter is the pads overlap (l_p) at the via's side.

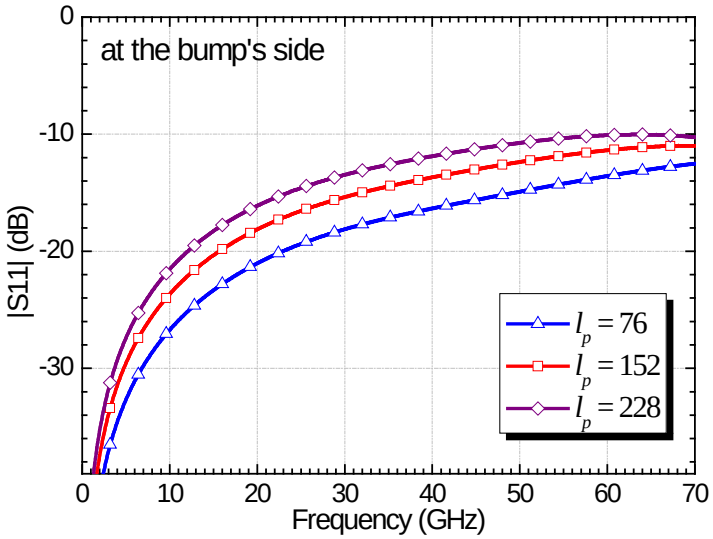
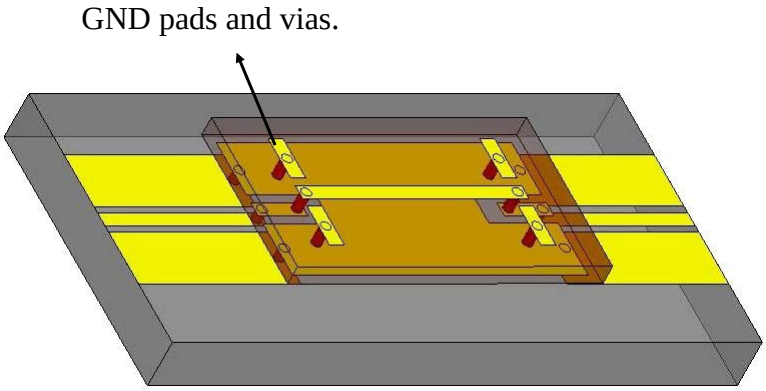


Fig. 36. The simulation data of CPW input return loss versus frequency. The parameter is the pads overlap (l_p) at the bump's side.

From the previous parametric simulations and discussions, the design rules were derived for of the hot-via transition. The diameter of the via hole (d_v) and the bump (d_b), if applicable and practicable, should be as small as possible in order to get the lower reflection at the interconnect. The higher bump height (h_b) reduces the reflection as well. For the pad dimension (l_p) at the transition, one should avoid using large pad but keep the pad as small as possible to minimize the return loss at the transition.

4.3 The demonstrated structures and compensation design

Based on the design rules of the hot-via transition developed in the previous section, the practical situations and the process capability were also further taken into consideration for the demonstrated interconnect structures. Fig. 37 to Fig. 39 show the three different designs of the MS-to-CPW hot-via flip chip interconnect structure for demonstration. Fig. 40 shows the details of the physical values of the transition structures of the three demonstration designs. The total length of the three demonstrated MS-to-CPW hot-via interconnect structure was 3000 μm, including the microstrip line on the chip (1000 μm) and the CPW line on the substrate (750 μm). The diameters of the via holes (d_v) and bumps (d_b) were both 50 μm; the bump height (h_b) was 30 μm. The width of the ground pads on the chip (w_p) was set at 228 μm, and the gap (g_c) was 46 μm. The length of the pads (l_p) was 76 μm; the signal length on the chip backside (l_b) was 100 μm. The locations of the via holes and bumps were optimized by simulation, where w_{iv} = 198 μm and w_{ib} = 228 μm.

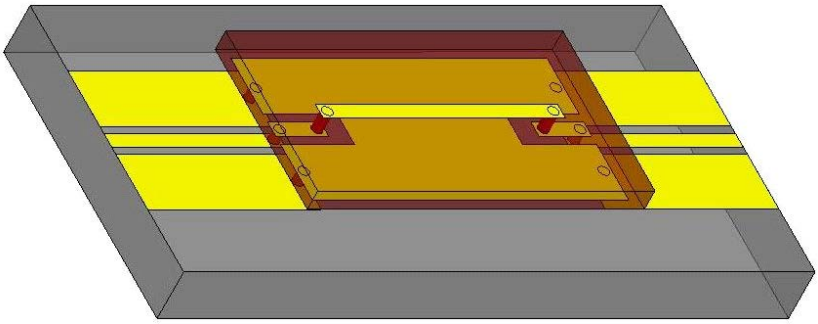


Design I.

Fig. 37. The schematic of the demonstrated MS-to-CPW hot-via interconnect structure having the ground pads and vias on the chip, designated as Design I.

Conventionally, microstrip MMICs have the ground pads and vias at the ends of the microstrip lines to enable on-wafer measurements with the GSG probes. However, this might induce some parasitics in the interconnects. Therefore, in Design II, the ground pads and vias on the chip were removed in the fabricated structure to investigate the parasitic effects due to the existence of the ground pads and vias, as shown in Fig. 38.

No GND pads and vias.

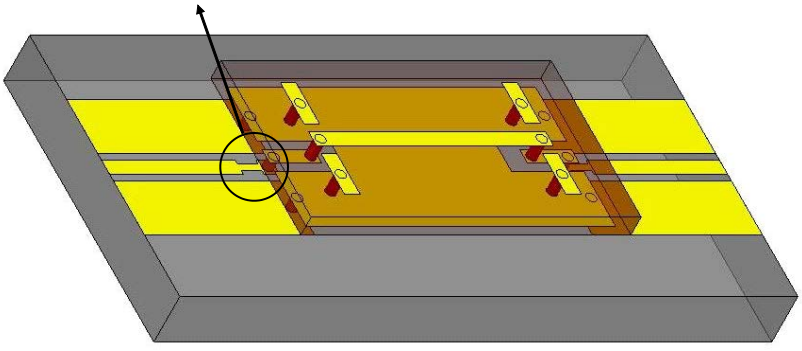


Design II.

Fig. 38. The schematic of the demonstrated MS-to-CPW hot-via interconnect structure without the ground pads and vias on the chip, designated as Design II.

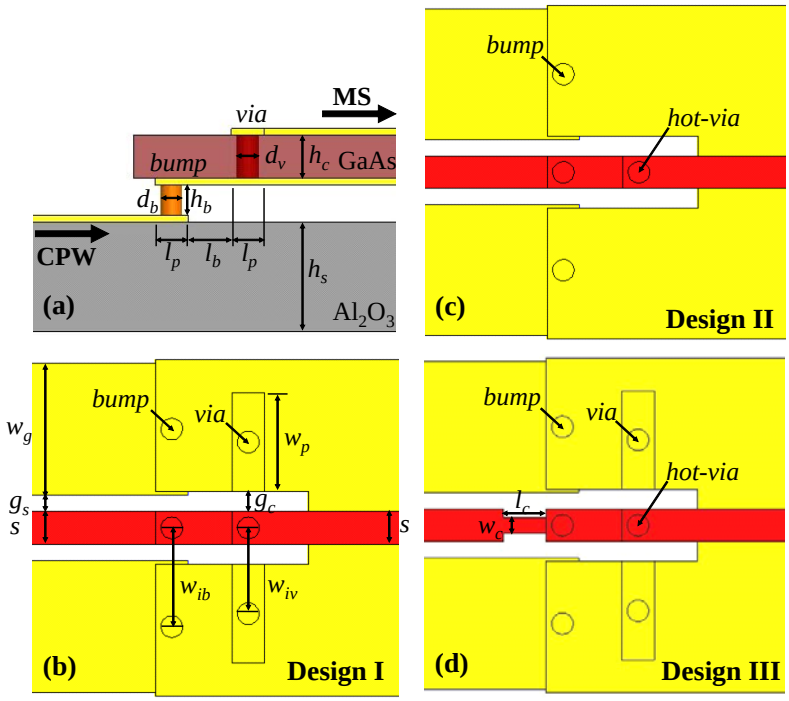
For the typical dimensions of the flip chip interconnects, the bump transition shows a strong capacitive behavior resulting from the dielectric loading due to the presence of the chip and substrate dielectrics [25]. It degrades the reflection property at high frequencies. It was suggested that the bump pads should be as small as possible to lower the capacitance. However, this always causes great concerns in the real fabrication. To achieve low reflection at the bump transition, one efficient way was adopted here by implementing the high impedance line in front of the bump transition; the design is designated as Design III as shown in Fig. 39. The high impedance line exhibits an inductive effect to compensate the capacitive part in the reactance. The location and dimensions, w_c = 16 μm and l_c = 50 μm, of the compensated patterns were determined by EM simulations, as shown in Fig. 40 (d).

Compensation



Design III.

Fig. 39. The schematic of the demonstrated MS-to-CPW hot-via interconnect structure with compensation design at the CPW circuit in front of the bump transition on the substrate, designated as Design III.



Designed parameters in Design I and II (μm)

$s=76$	$w_g=304$
$g_s=38$	$g_c=46$
$w_{ib}=228$	$w_{iv}=198$
$w_p=228$	$l_p=76$
$l_b=100$	$d_b=50$
$d_v=50$	$h_b=30$
$h_c=100$	$h_s=254$

High impedance line in Design III

$w_c=16$

$l_c=50$

Fig. 40. The details of the physical values of the transition structures of the three designs for demonstration. (a) Side-view. (b) Top-view of the structure Design I with each parameter indicated. (c) Top-view of Design II. (d) Top-view of Design III with the high impedance compensation design.

The demonstrated MS-to-CPW hot-via interconnect structures were then fabricated with the in-house developed process. The detailed process steps will be described in the following section. The substrate circuits with Au bumps were fabricated by using the in-house developed standard Au bumping process as presented in Chapter 2. The Au-to-Au thermo-compression process was performed to bond the chip samples to the substrate samples. The three different structures were then RF characterized up to 67 GHz to test the interconnect performance.

4.4 In-house developed fabrication process

The in-house process was developed to fabricate the optimum-designed MS-to-CPW hot-via flip chip interconnect structures. The backside process for the chip fabrication was modified to provide the signal transmission from the front side to the back side of the chip, for which the signal via holes at the transmission line was etched, and the backside metallization of the chip was patterned. Fig. 41 shows the diagrams of the front-side process steps for the chip samples.

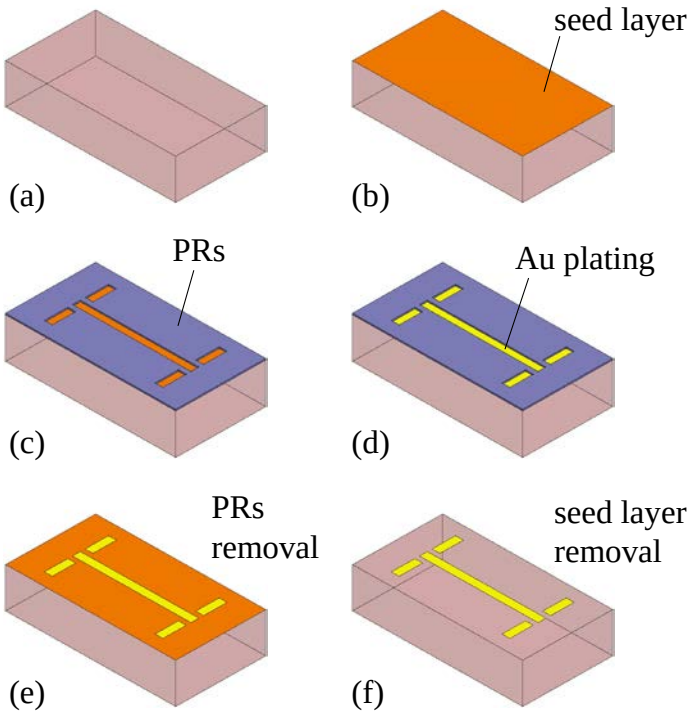


Fig. 41. The front-side process steps of the chip samples.

First, metal Ti and Au (300 Å and 500 Å) were successively deposited using E-gun evaporator onto the GaAs chip to form continuous seed layers for the following Au electroplating of the circuits. The plating bath was cyanide based solution. Ti was used as an adhesion layer to improve the adhesion of Au to the GaAs material, and Au was used as a seed layer to electroplate Au onto the matrix. Thin photoresists from Shipley Company were then patterned on the chip to electroplate the circuits of the test structure. After the electroplating of the Au circuits, the thin photoresists were then removed. The seed layers were removed with KI/I_2 solution for Au and HF dilute solution for Ti to complete the front-side process.

After the front side processes were completed, the chip samples went for the backside process with the added backside patterning step. Fig. 42 describes the in-house backside process steps for the demonstrated chip samples. The chip wafer was first mounted on the sapphire carrier and thinned down to a thickness of 100 μm. The thinned chip was then patterned with the photoresists, opening the regions of the via holes. The via holes etching was performed by using the ICP etcher with the BCl_3 and Cl_2 gas mixture. The etching conditions such as the gases mixture ratio, pressure, and etching power were optimized to achieve high etching rate, high etching selectivity,

and good etching profiles [54]. The optimized etching condition is summarized in Table 5. Fig. 43 shows the etching profile of the via hole. The “hot-via” was formed at the same time when the ground via was formed in the etching process. After finishing the via holes etching, the backside of the chip was electroplated with Au and patterned by etching the unwanted regions with the KI/I_2 solution. When the backside metallization of the chip was finished, the wafer was then de-mounted and diced into the discrete samples and was ready for bonding on the substrate.

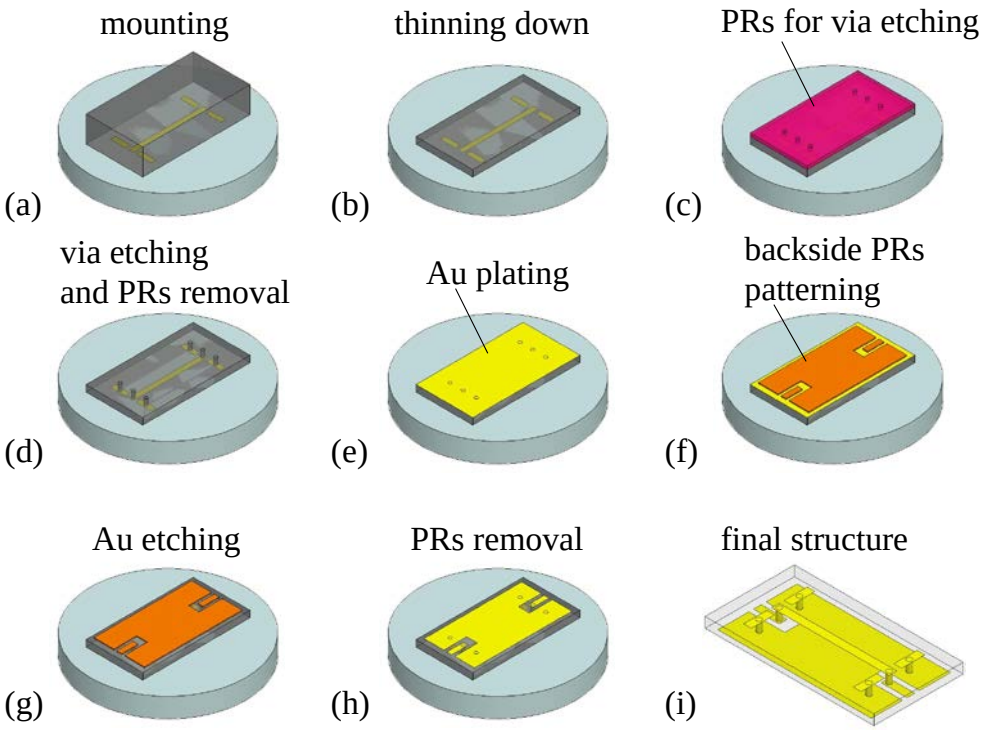


Fig. 42. The back-side process steps of the chip samples with the added backside patterning step.

Table 5. The optimized etching condition by using ICP-RIE etcher, [54].

Pressure	Coil power	Platen power	Gas ratio	Etching rate
10 mTorr	600 W	200 W	BCl_3/Cl_2=75/25 (sccm)	~1.3 μm/min

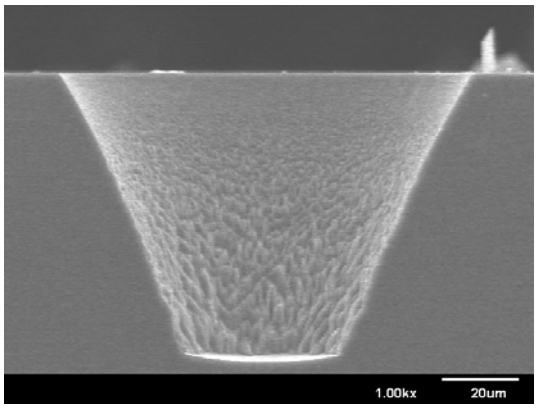


Fig. 43. The SEM image of the etched via hole, [54].

The bumps transitions were electroplated on the substrate. The Au bumps were electroplated on the substrate circuit patterns using the in-house developed standard Au bumping process, which was described in Chapter 3.

After the chip and substrate samples were fabricated, the chip samples were flip-chip bonded to the substrate using the flip chip bonder to form the final hot-via interconnect structures. The flip chip bonding process was performed using the Au-to-Au thermo-compression. Fig. 44 shows the image of the bonded hot-via interconnect structure. The bonded samples with different designs were RF tested.

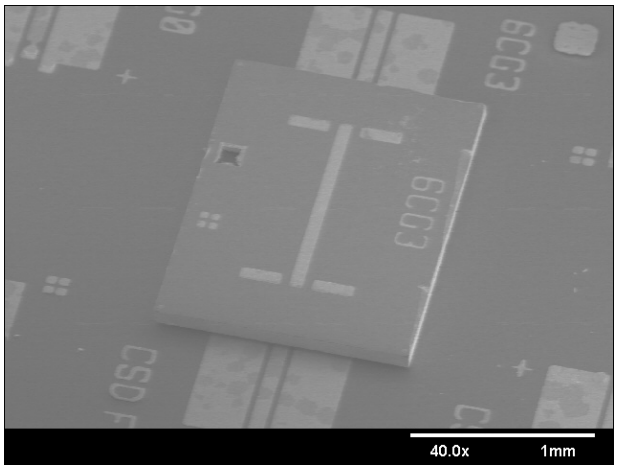


Fig. 44. The SEM image of the fabricated MS-to-CPW hot-via interconnect structure.

4.5 RF characterization results of the demonstrated structures

The scattering parameters of the fabricated MS-to-CPW hot-via flip chip interconnect structures were characterized by using the on-wafer probe measurement system. During the measurements, a 10 mm thick layer of Rohacell 31 (ε_r = 1.04 at 26.5 GHz) was placed between the samples and the metal chuck of the probe station to avoid the grounded backside under the substrate. Fig. 45 shows the measured transmission coefficients of the three hot-via interconnect structures. From the measured results, Design I and Design II showed small variation both in the reflection and insertion properties, indicating the ground pads and vias had minor influence on the interconnect performance. From DC to 20 GHz, the return loss was less than 25 dB; from 20 to 50 GHz, the return loss was less than 15 dB. Above 50 GHz, the reflection became worse but was less than 12 dB. The insertion loss was 0.4 dB at 40 GHz and 0.8 dB at 60 GHz. Both the insertion and reflection characteristics were much better than the results reported in the previous literatures [14-15, 49-52]. The best results reported so far showed the insertion loss of 2 dB from DC to 40 GHz and return loss of 10 dB up to 25 GHz [49].

To further improve the transmission performance of the proposed hot-via architecture, the high impedance line was adopted on the circuits in Design III. From the results in Fig. 45, further improvements of the insertion and reflection properties in the interconnect structure were achieved in this design. At 60 GHz, the return loss was improved from 12 dB to 19 dB, and the insertion loss was also improved from 0.8 dB to 0.5 dB. The compensation design improved both the transmission characteristics and the bandwidth. From DC to 67 GHz, the return loss was less than 18 dB, and the insertion loss was within 0.5 dB. Because of the overall capacitive effect of the transition, the return loss became worse as the frequency increased. The high impedance line was calculated to have an inductance about 34 pH, which compensated the capacitive effect of the transition to match close to 50 Ω and therefore gave a broadband interconnect performance.

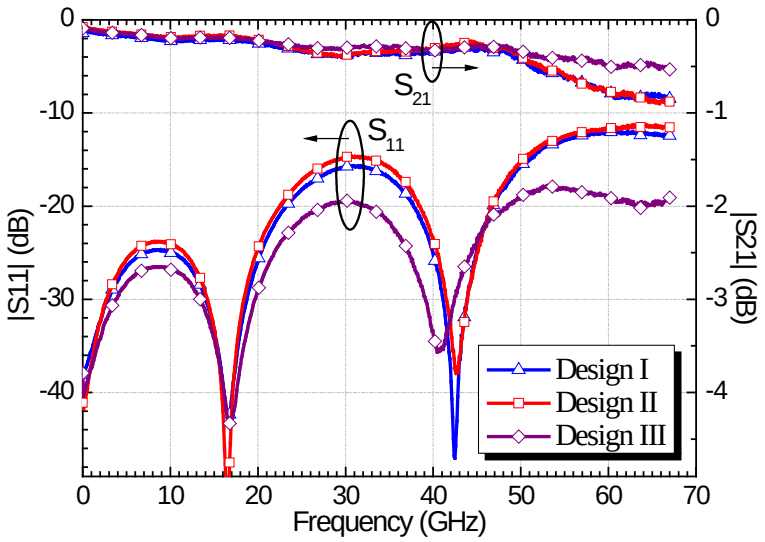


Fig. 45. Comparison of the measured transmission coefficients between the three different designs of the hot-via interconnect structures. The triangle line (-△-) indicates the design of the microstrip line with the ground pads and ground vias on the chip. The square line (-□-) indicates the design of the microstrip line without the ground pads and ground vias on the chip. The rhombus line (-◇-) indicates the design with the high-impedance compensation pattern at the transition.

Fig. 46 shows the comparison of the measured insertion loss *versus* frequency of the CPW transmission line on the Al_2O_3 substrate and the two interconnect structures, Design I and Design III. The CPW transmission line was equal in length to the two interconnect structures. The insertion loss of the two interconnect structures in both cases was a little higher than that of the CPW thru line. Compared with the thru line structure, the hot-via flip chip interconnect structure had four more vertical transitions including two hot-via transitions at the chip side and two bump transitions at the substrate side. At 60 GHz, the insertion loss of Design I was 0.8 dB, which was 0.5 dB worse than the CPW thru line. However, the compensated hot-via interconnect structure, Design III, just exhibited the insertion loss about 0.5 dB at 60 GHz, which was only 0.2 dB higher than that of the CPW thru line. Table 6 shows the calculated losses of the hot-via and bump transitions (Design III) at 20, 40, and 60 GHz. It should be noticed that the four vertical transitions (2 hot-vias and 2 bumps) induced only 0.23 dB in the insertion loss at 60 GHz. The results were much better than the data reported in [15] and [49].

It was demonstrated that with the compensated design the hot-via architecture can achieve low reflection and low insertion loss with a very broad bandwidth over 60 GHz. To our knowledge, this is the best result ever reported in the literature, which

reveals the potential of the hot-via approach for microstrip packaging solutions up to at least V band.

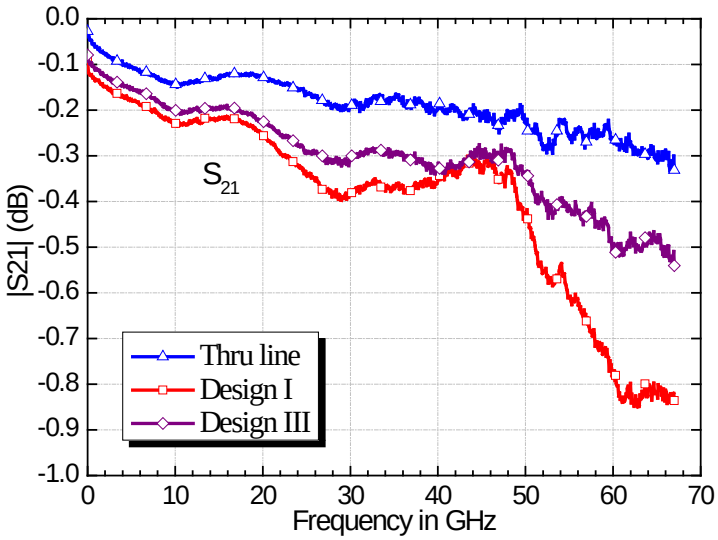


Fig. 46. Comparison of the measured transmission coefficients between the three different designs of the hot-via interconnect structures. The triangle line (-△-) indicates the design of the microstrip line with the ground pads and ground vias on the chip. The square line (-□-) indicates the design of the microstrip line without the ground pads and ground vias on the chip. The rhombus line (-◇-) indicates the design with the high-impedance compensation pattern at the transition.

Table 6. Losses.

Frequency (GHz)	20	40	60
Loss of the interconnect structure (dB)	0.22	0.32	0.49
Loss of the transmission line (dB)	0.13	0.19	0.26
Loss of the transitions (dB)	0.09	0.13	0.23

The loss of the transitions included the hot-vias and bumps.

Chapter 5

Coaxial Transitions for Flip Chip Interconnects

This chapter presents the novel design of coaxial transitions for the vertical transitions in the flip chip interconnects intended to replace the conventional three-bumps G-S-G transitions. The coaxial transition has the advantage of better field confinement over the conventional one. However, this novel approach encounters difficulty and complexity in the fabrication process. The details of the in-house developed fabrication process are presented, and the design and the RF performance of the coaxial approach are described and discussed throughout this chapter.

This chapter starts with the presentation and the discussion of our first proposal, in which the coaxial transition consists of the center cylinder signal bump and two C-shaped ground bumps forming the coaxial structure as the vertical transition for the flip chip interconnects. The design criteria of such transition are described in details and its fabrication process is presented as well. The major goal is to achieve broadband interconnect performance for the flip chip interconnects when using the proposed coaxial transition. In the following, the further design of the perfect coaxial transition is realized for the flip chip interconnects with the use of BCB dielectric as an interlayer on top of the circuits. To realize such a perfect coaxial transition structure onto the flip chip interconnects, lots of efforts were made in the development of the in-house fabrication process. The interconnect performance is excellent using this novel approach, showing the feasibility and the potential of the coaxial transition for the flip chip interconnects. To our best knowledge, this novel approach is unique and advanced for microwave packaging applications.

5.1 Background

Flip-chip interconnects are more compatible with coplanar configurations, which are frequently used for very high frequency designs to minimize undesired parasitics [1, 10, 19]. Conventionally, solder or Au bumps are grown on the ground and signal paths of the CPW structure at the vertical transition region to maintain the continuity in the current flow. Fig. 47 shows the conventional flip chip interconnect structure with

three bumps (G-S-G bumps) for CPW-to-CPW transitions.

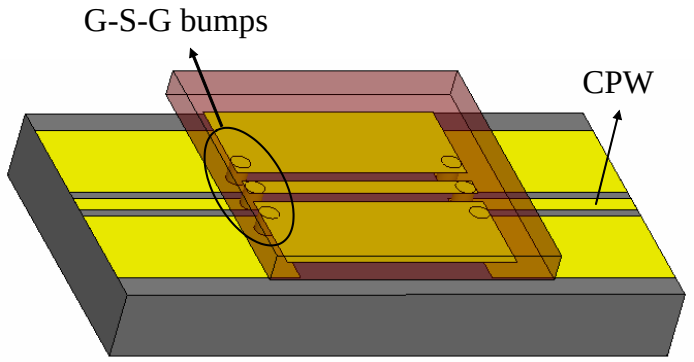


Fig. 47. The conventional vertical transitions of three bumps for CPW to CPW interconnects.

The proposal of the coaxial transition for the flip chip interconnects comes from the idea that the coaxial transmission line shows the advantage of the good shielding property, which is helpful for the transition property such as better field confinement and good isolation. In [55], it proposed to use multiple ground bumps at the vertical transition for the flip chip interconnects. Fig. 48 shows the configurations of the multiple ground bumps presented in [55]. The arrangement of the multiple ground bumps was of the radial type, which formed a pseudo-coaxial vertical transition. It gave a rough concept of the coaxial transition although it was not a real coaxial transition at the vertical interconnect. From this point, the first idea of the two C-shaped ground bumps surrounding the signal bump was proposed, which formed a real coaxial structure. The coaxial transition structure will be described in the following section.

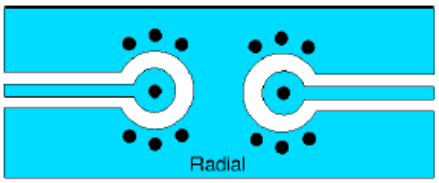


Fig. 48. The configurations of the multiple ground bumps presented in [55].

5.2 The coaxial transition structure and the EM field properties

Fig. 49 shows the flip chip interconnect structure with the proposed vertical coaxial transitions. The transition has two C-shaped ground bumps as the shield ground of the coaxial structure. Fig. 50 shows the coaxial transition structures on both sides of the chip and substrate. It can be seen that the C-shaped ground bumps are formed on the ground metal at the end of the CPW circuits and as well as the signal bumps are formed on the signal path of the CPW circuits. The open ends of the two C-shaped bumps were arranged in opposite directions. Once the chip sample is bonded to the substrate sample, the coaxial transition is formed. The two C-shaped ground bumps together with the center cylindrical signal bump form a coaxial structure.

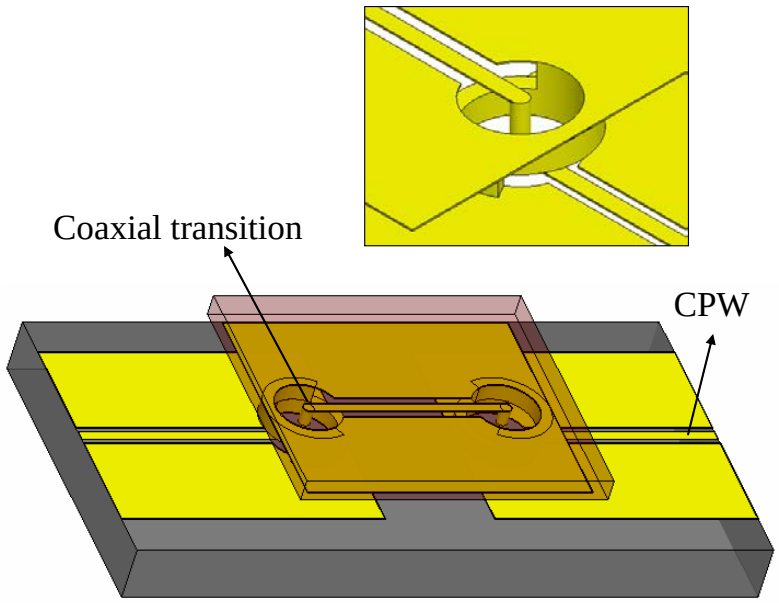


Fig. 49. The “coaxial transitions” for the vertical transitions of the CPW-to-CPW flip chip interconnect structure.

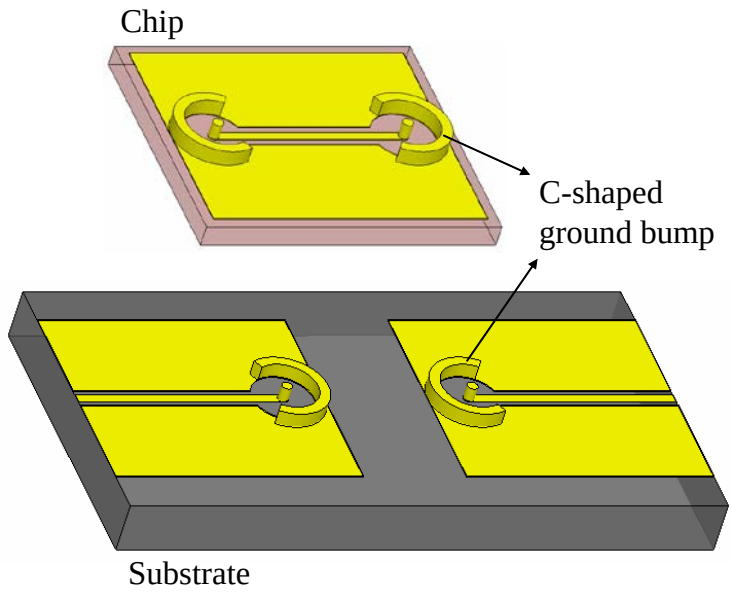


Fig. 50. Schematic of the coaxial transitions on the CPW circuits of the substrate and chip, where the signal cylinder bump and C-shaped ground bump form the coaxial transition.

The tool for the three dimensional electromagnetic field analysis of the interconnect structure with the vertical coaxial transitions is CST Microwave Studio. In our design, the material of the substrate is Al_2O_3, and the material of the chip is GaAs. The thickness of the alumina substrate and GaAs chip are 254 μm and 100 μm, respectively. The conductor metal is Au of 3 μm. The transmission lines on both the chip and substrate are of CPW type. Fig. 51 shows the graphs of the electric field and magnetic filed at the vertical transition. From the plot, the coaxial transition shows better field confinement as compared to the conventional structure with three bumps at the CPW-to-CPW transitions.

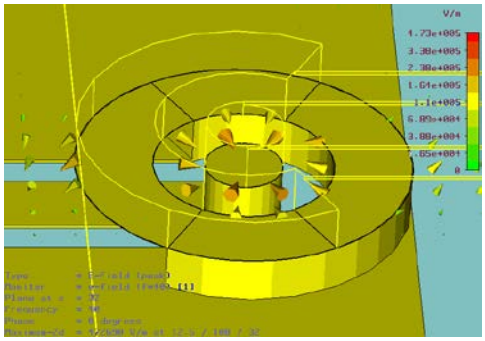
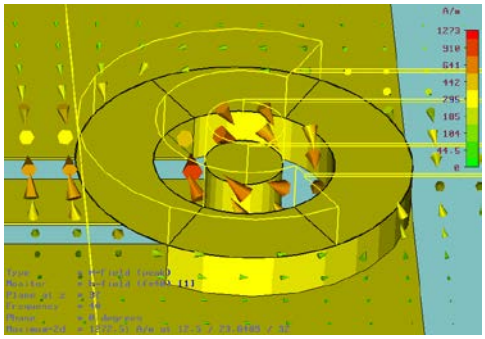
(a)  (b) 

Fig. 51. (a) The electric field view at the coaxial transition. (b) The magnetic field view at the coaxial transition.

5.3 Parametric study and simulation

The design and simulation of the coaxial transitions were performed using the simulation tool CST microwave studio. Fig. 52 shows the simulated model of the coaxial transition structure for CPW-to-CPW flip chip interconnect.

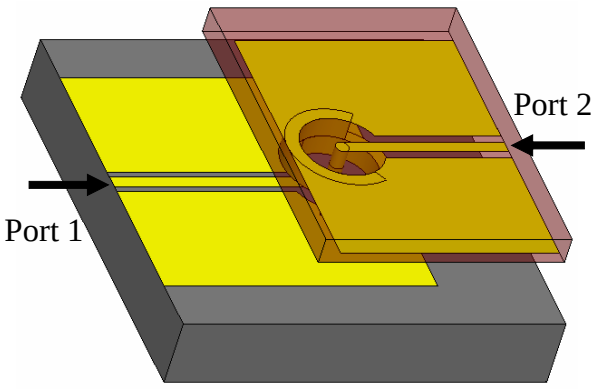


Fig. 52. The simulated coaxial transition model for flip chip interconnects in the simulator.

The effects of the physical parameters and their dimensions on the transition properties were studied by the EM simulator. Fig. 53 shows the definitions of the main parameters of the coaxial transition. The characteristic impedances (Z_0) of CPWs on the substrate and chip were 50 Ω. The signal widths on the chip (w_{chip}) and substrate (w_{sub}) were 50 μm. Thus, the spacing between the signal and ground on the chip (g_{chip}) and substrate (g_{sub}) were 34 μm and 24 μm, respectively. For the vertical coaxial transition structure, the effective physical parameters under investigation are the chip-side bump height (h_c), the substrate-side bump height (h_s), the C-shaped ground bumps wall thickness (t_{Cg}), the ratio (R) of outer conductor radius (r_o) to inner conductor radius (r_i) of the coaxial transition ($R = r_o/r_i$).

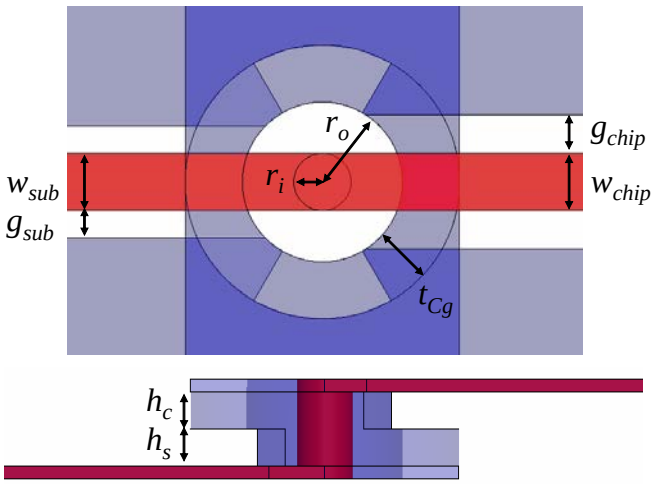


Fig. 53. Main parameters in the vertical coaxial transition are chip-side bump height (h_c), substrate-side bump height (h_s), C-shaped ground bumps wall thickness (t_{Cg}), and ratio of outer conductor radius to inner conductor radius at the coaxial transition ($R=r_o/r_i$).

Fig. 54 shows the simulation results of the return loss *versus* frequency for different chip-side bump heights (h_c = 10 to 50 μm) while h_s, t_{Cg}, and R are 30 μm, 50 μm, and 2.5 (r_i = 25 μm, r_o = 62.5 μm). The results indicate that the increase in h_c from 10 to 30 μm significantly improves the return loss by 1.6 dB at 40 GHz. However, further increase in h_c from 30 to 50 μm does not have much effect on the return loss. In Fig. 55, a similar trend as the parameter h_c was also observed for the different substrate-side bump heights (h_s).

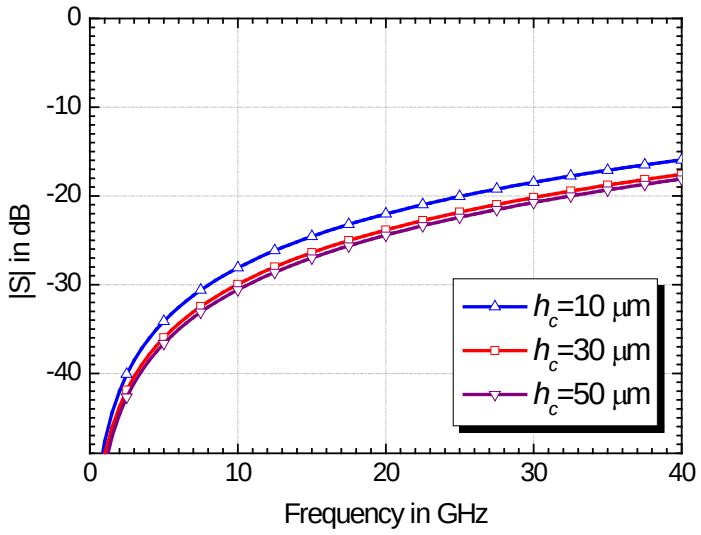


Fig. 54. Simulation results of return loss versus frequency. The parameters are the various chip-side bump heights (h_c = 10, 30, 50 μm) while h_s equals 30 μm, t_{Cg} equals

50 μm, and R equals 2.5 (r_i = 25 μm, r_o = 62.5 μm).

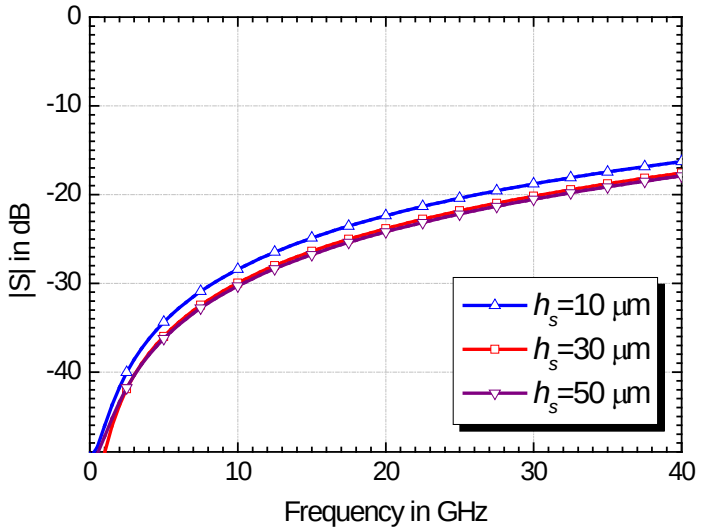


Fig. 55. Simulation results of return loss versus frequency. The parameters are the various substrate-side bump heights (h_s = 10, 30, 50 μm) while h_c equals 30 μm, t_{Cg} equals 50 μm, and R equals 2.5 (r_i = 25 μm, r_o = 62.5 μm).

The simulation results of return loss *versus* frequency with the same values of the substrate-side height and the chip-side bump height (h_c = h_s) are shown in Fig. 56. The results indicate that the increase in h_c and h_s from 10 to 30 μm improves the return loss by 2.6 dB at 40 GHz. Further increase in h_c and h_s from 30 to 50 μm has only a small improvement of 1.2 dB at 40 GHz on the return loss.

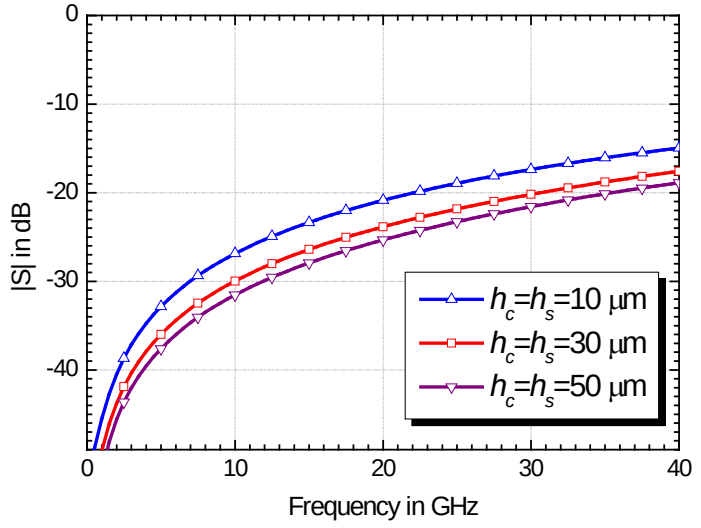


Fig. 56. Simulation results of return loss versus frequency. The parameters are the various chip-side and substrate-side bump heights (h_c = h_s = 10, 30, 50 μm) while t_{Cg}

equals 50 μm, and R equals 2.5 (r_i = 25 μm, r_o = 62.5 μm).

Fig. 57 shows the simulation results of the return loss *versus* frequency of the third parameter, C-shaped ground bumps wall thickness (t_{Cg}). The other parameters h_c, h_s, and R are 30 μm, 30 μm, and 2.5 (r_i = 25 μm, r_o = 62.5 μm). From the figure, it is observed that the smaller thickness (t_{Cg}) of the C-shaped bumps wall, the lower return loss at the interconnect is achieved. As the two C-shaped ground bumps together with the center signal bump form a coaxial structure; they both go across the signal lines of the substrate and chip. In this way, the C-shaped ground bump gives a capacitive effect to the signal line and acts as a shunt capacitance. The thinner ground wall thickness (t_{Cg}) alleviates the capacitive effect and therefore helps improve the reflection property of the coaxial transition. Due to the process consideration, however, the parameter t_{Cg} can not be too small. The process limitation comes from the aspect ratio of the thick photoresist and the mask resolution. In this study, the masks are of film type, which limits the line width on the mask. The dimension of the C-shaped ground bumps wall thickness (t_{Cg}) is set to be 50 μm for the real fabricated coaxial structure in this study.

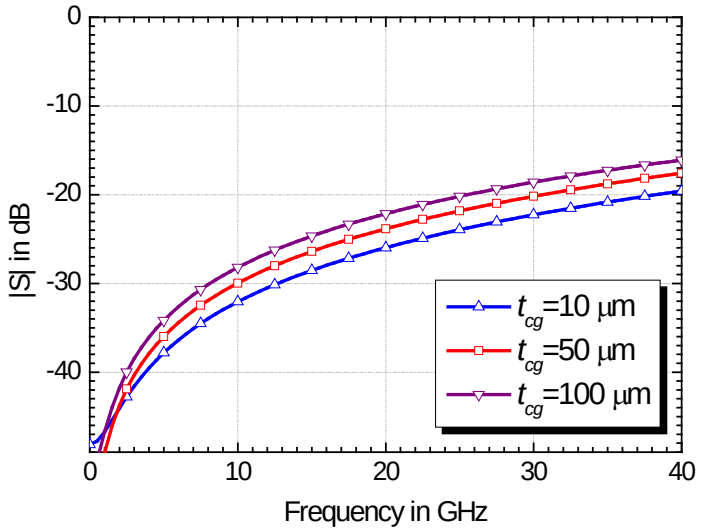


Fig. 57. Simulation results of return loss versus frequency. The parameters are various C-shaped ground bumps wall thickness (t_{Cg} = 10, 50, 100 μm) while h_c equals 30 μm, h_s equals 30 μm, and R equals 2.5 (r_i=25 μm, r_o=62.5 μm).

The most important parameter for the proposed coaxial transition is the ratio (R=r_o/r_i) of the outer conductor radius (r_o) to the inner conductor radius (r_i). Fig. 58 shows the simulation results of the return loss *versus* frequency of the parameter R ranging from 2.5 to 8 while the other parameters h_c, h_s, and t_{Cg} are 30 μm, 30 μm, and 50 μm,

respectively. From the figure, when R increases from 2.5 to 3, there is a small improvement in the return loss about 1.8 dB at 40 GHz. Further increase in R to 5 improves the return loss significantly. The return loss for single transition is much less than 20 dB at 40 GHz when the parameter R equals 5, which shows very good interconnect performance. However, the return loss becomes worse when R increases further. In the case of R = 8, the return loss greatly degrades. From the results, it is suggested that there is an optimum value of R giving the lowest reflection at the transition.

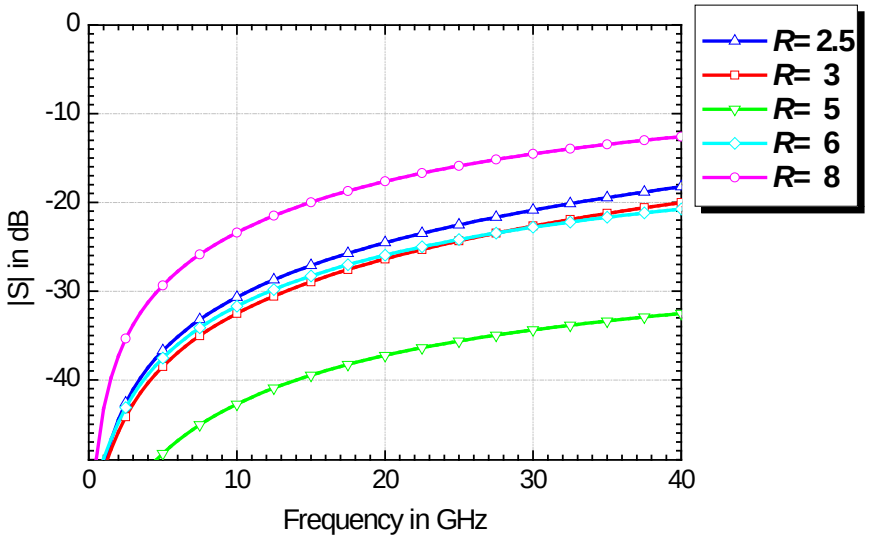


Fig. 58. Simulation results of return loss versus frequency. The parameters are various ratio of outer conductor radius to inner conductor radius of coaxial transitions ($R=r_o/r_i$ = 2.5, 3, 5, 6, 8 while r_i = 25 μm) while h_c equals 30 μm, h_s equals 30 μm, and t_{Cg} equals 50 μm.

For better understanding of the coaxial transition structure and the effect of the key parameter R, it is helpful to develop an equivalent circuit model for the coaxial transition structure. Fig. 59 shows the schematic of the coaxial transition and the developed equivalent circuit model. The associated equivalent circuit model of the coaxial transition consists of three physical transmission lines and two capacitors. The three transmission lines describe the two CPW transmission lines inside the area of the coaxial structure and the coaxial structure itself. The two capacitors are used to account for the induced capacitances of the C-shaped ground bumps to the signal lines. Table 7 lists the model parameters of the coaxial transition structure for the case of R = 5 after simulation and optimization. The shunt capacitances in the model were found to be $C_{sub} = C_{chip}$ = 14 fF. The impedances of the two CPW transmission lines were calculated to be $Z_{CPW\text{-}TL1}$= 66 Ω and $Z_{CPW\text{-}TL2}$= 60 Ω, and the impedance of the

coaxial transmission line was Z_{coax}= 96 Ω. The high-impedance transmission lines, exhibiting an inductive effect, compensate the capacitive effect induced by the C-shaped ground bumps, which results in the low reflection property of the coaxial transition. When the parameter *R* is small, *e.g.* 2.5, the transition still shows an overall capacitive property because of the lower impedances (i.e. lower inductive effect) of the both CPW transmission lines and the coaxial transmission line and the excess capacitance. It explains why the increase of *R* from 2.5 to 3 just gives small improvement in the return loss of the transition. The further increase of *R* to 5 leads to higher impedance transmission lines, which enhances the inductive effect and makes the overall effect of the coaxial transition match to 50 Ω. In this case, it therefore gives the low return loss for the transition. However, when the value of *R* increases to 8, it results in too much inductive effect and causes an overall inductive property of the transition, which degrades the return loss.

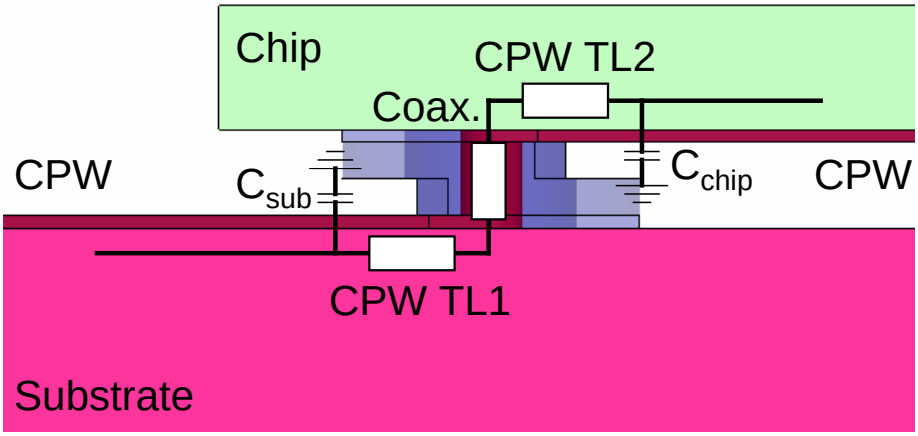


Fig. 59. Schematic of vertical coaxial transition with equivalent circuit model (TL: transmission line).

Table 7. Vertical coaxial transition model parameters (R = 5).

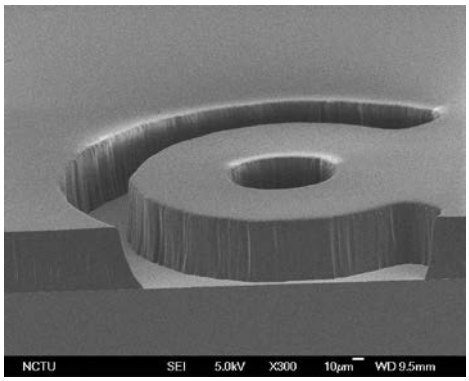
Transmission lines		
CPW TL1	Z = 66 Ω	length = 125 μm
Coaxial TL	Z = 96 Ω	length = 60 μm
CPW TL2	Z = 60 Ω	length = 125 μm
Lumped element		
$C_{sub} = C_{chip}$ = 14 fF		

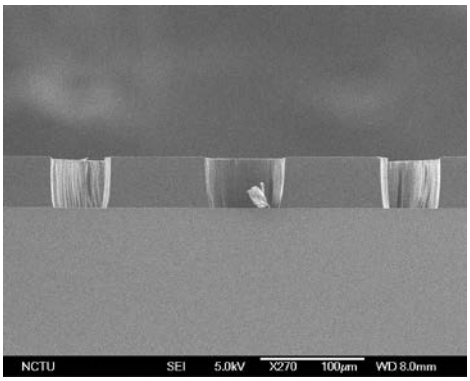
From the simulation results, several rules for the design of the coaxial transition are concluded and summarized as follows. The higher bump height gives the lower return

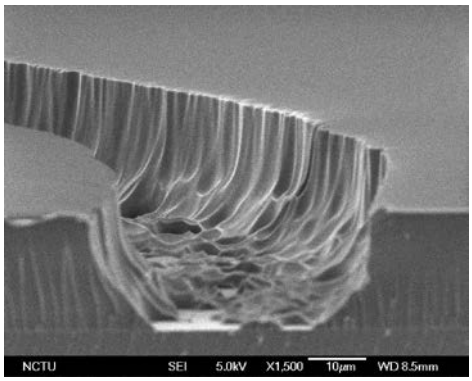
loss at the interconnect. The thinner C-shaped ground wall thickness also gives the lower return loss. However, these two parameters of the coaxial transition only show small improvement on the reflection property. The key parameter of the coaxial transition is the ratio *R*, which greatly affects the interconnect property. It is suggested that there is an optimum value of *R*, which gives the lowest reflection at the transition. With proper design, the proposed coaxial transition can provide good interconnect performance for the flip-chip interconnects with low return loss and low insertion loss over a broad bandwidth at high frequencies up to 40 GHz.

5.4 Fabrication process

To demonstrate the proposed idea, flip-chip interconnect structures with the vertical coaxial transitions were fabricated. Thick photoresist with high aspect ratio was used. The key process for the vertical coaxial transition structure is the thick photoresist formation. A double coating technique for the photoresist was developed to achieve thick photoresist with flat surface on the whole sample. At each coating step, the sample was baked on the hot plate at a temperature of 120 ^{o}C for 15 minutes to remove the solvents. A photoresist of 60 μm thickness was obtained. The samples were then exposed using Karl-Suss MJB-3 aligner with a broadband exposure. The masks were of film type, which was an approach with acceptable accuracy in the dimensions. Fig. 60 shows the SEM pictures of the photoresists profiles with different exposure and development conditions. Fig. 60 (a) and Fig. 60 (b) show the profiles of the thick photoresists with the best exposure and development conditions after fine tuning. The SEM pictures show excellent profiles with a smooth side wall. However, if the exposure time was insufficient, serious residues remained at the bottom of the exposed areas after development. Fig. 60 (c) shows the SEM image of the serious residues. Fig. 60 (d) shows the SEM image of the over-developed profile. An over development time caused a sloped side wall.

(a) 

(b) 

(c) 

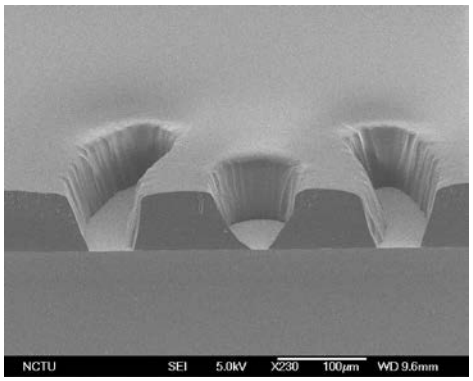
(d) 

Fig. 60. The SEM images of the thick photoresists with different testing conditions. (a), (b) Exposure time: 9 minutes; development time: 6 minutes. (c) Exposure time: 6 minutes; development time: 6 minutes. (d) Exposure time: 9 minutes; development time: 9 minutes.

The back-to-back flip chip interconnect structure with the proposed coaxial transitions were then fabricated. Fig. 61 shows the diagrams of the process procedures. Al_2O_3 and GaAs were the materials for the substrate and the chip. The thickness of the Al_2O_3 substrate and GaAs chip were 254 μm and 100 μm, respectively. The Al_2O_3 substrate was 2 inch square, and the GaAs was a 3 inch wafer. The interconnect metal was Au and was formed by electroplating.

First, metal Ti and Au (300 Å and 500 Å) were successively deposited using E-gun evaporator onto the GaAs chip and Al_2O_3 substrate to form continuous seed layers for the following Au electroplating. The plating bath was cyanide based solution. Ti was used as an adhesion layer to improve the adhesion of Au to the Al_2O_3 and GaAs material, and Au was used as a seed layer to electroplate Au onto the matrix. Thin photoresists from Shipley Company were then patterned on the chip and substrate to electroplate the circuits of the test structure. After the electroplating of the Au circuits, the thin photoresists were then removed. Thick photoresists from TOK was coated on both the chip and the substrate. The positions and dimensions of the coaxial transitions bumps were then patterned both on the chip and substrate with the

previously established conditions. Then, the electroplating of Au coaxial transitions was performed. By controlling the electroplating current density and electroplating time, the bump of required heights were achieved. Finally, the seed layers were removed with KI/I_2 solution for Au and HF dilute solution for Ti.

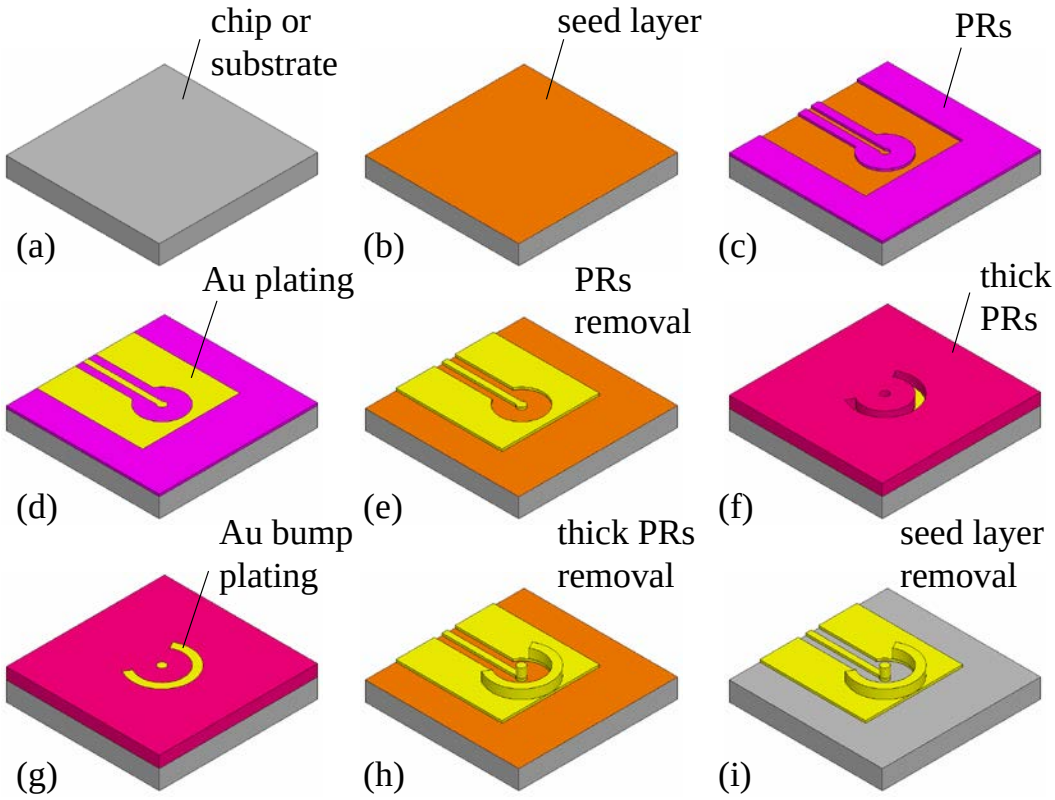


Fig. 61. The fabrication process steps of the coaxial transition on the CPW circuits.

After thin metal etch, the test interconnect structure was successfully fabricated. The plated coaxial transition test structure is shown in Fig. 62. The test chip structures were then flip chip bonded to the substrate to form the final flip-chip interconnect structures with the vertical coaxial transitions. Fig. 63 shows one of the flip-chip bonded interconnect structures. After bonding the chips onto the substrates, RF characterizations were then performed on the bonded test structures.

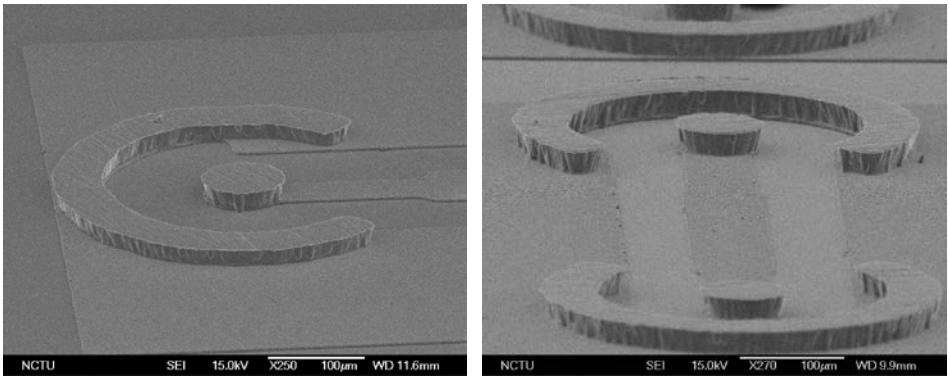


Fig. 62. The SEM images of the fabricated test structure.

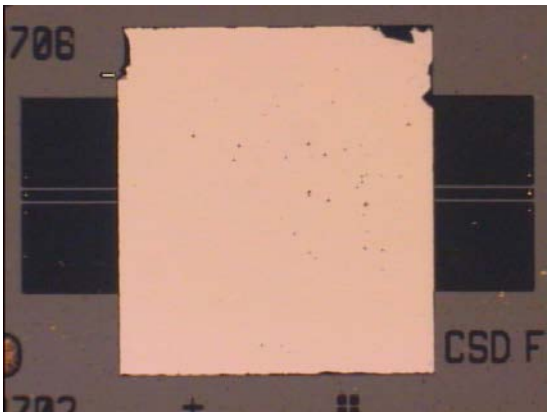


Fig. 63. The top-view photo of one final demonstrated structure.

5.5 Characterization results

According to the discussion in the previous section, the geometric parameters of the vertical coaxial transition are the bump height (h), the C-shaped ground wall thickness (t_{Cg}), and the ratio (R) of the outer conductor radius to the inner conductor radius at the coaxial transition, where R is the key design parameter. To demonstrate the proposed coaxial transition for the flip-chip application and verify the design rules, we have fabricated the back-to-back flip-chip interconnect structures with the vertical coaxial transitions for the various ratios (R) by using the in-house developed fabrication process, which has been presented and described in detail in the previous section. The thermo-compression method was used to flip-chip bond the demonstrated samples. The compression during the bonding operations would bring some small changes to the original geometry of the coaxial transition. The bonding conditions were tested and optimized to avoid too much deformation of the bumps. However, it should be noticed that the best thermo-compression bonding conditions still caused

little deformation of the bumps, including the reduction in the bump height and the shift in the parameter *R* of the coaxial transition. The scattering parameters of the test structures were then measured up to 40 GHz by the on-wafer probing measurement system with the Anritsu 37369C vector network analyzer.

For the demonstrated structures, the designed signal width of 50Ω-CPW was 70 μm both on Al_2O_3 substrate and on GaAs chip. The inner conductor radius (r_i) at the coaxial transition was 35 μm. The C-shaped ground bump wall thickness (t_{Cg}) was 50 μm. The height of the coaxial-type bump (h_c and h_s) was 30 μm both on the chip and substrate before flip-chip bonding. The interconnect structures with the various designed ratios (*R*) ranging from 3 to 6 were fabricated and RF characterized. Fig. 64 shows the measurement results of the insertion loss *versus* frequency of the CPW transmission line on the Al_2O_3 substrate and the flip-chip interconnect structure with the coaxial transitions where the designed R = 3. These two structures have equal length. Compared with the CPW transmission line on the Al_2O_3 substrate, there are two more vertical coaxial transitions for the case of the flip-chip interconnect structure. Even so, from DC to 30GHz, it shows no additional insertion loss. Above 30 GHz, the insertion loss increases less than 0.1 dB.

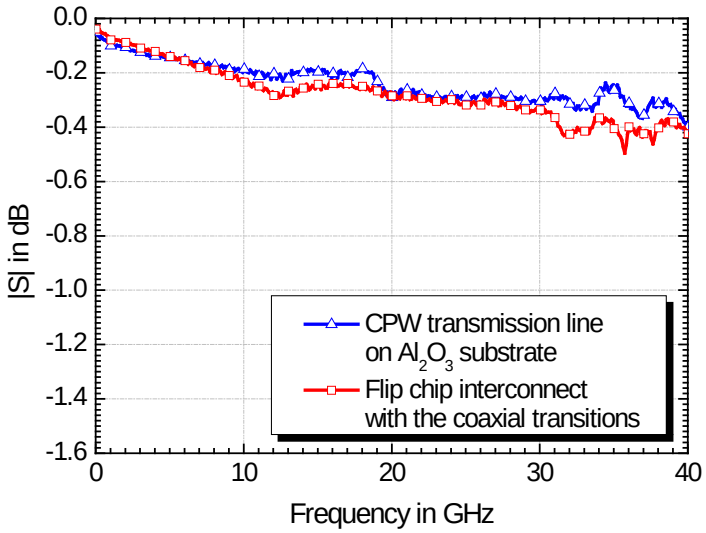


Fig. 64. Measurement results of insertion loss *versus* frequency. Comparison between the CPW transmission line and the flip chip interconnect structure with the coaxial transitions (R = 3).

Fig. 65 shows the measurement results of the return loss and the insertion loss *versus* frequency of the designed parameter *R*. In the figure, the measurement data show a similar trend as the simulation results. It can be seen that the best performance with a

very low return loss was achieved for the designed parameter R=6. From DC to 40 GHz, the return loss was less than 25 dB. The idea of the proposed coaxial transition for the flip-chip interconnects is clearly verified. However, it should be noticed that in reality the designed R shifted a little to the lower-value range because the thermo-compression bonding changed the originally designed parameter R. By SEM examination and calculation, for the case of the designed R=6, it could be verified the designed parameter R was shifted to the value about 5. The designed coaxial transition structure was different from the real situation of the fabricated structure. This explains the phenomenon that the simulation and measurement results indicate the different optimum values for the parameter R. This should be taken into consideration in advance at the design stage.

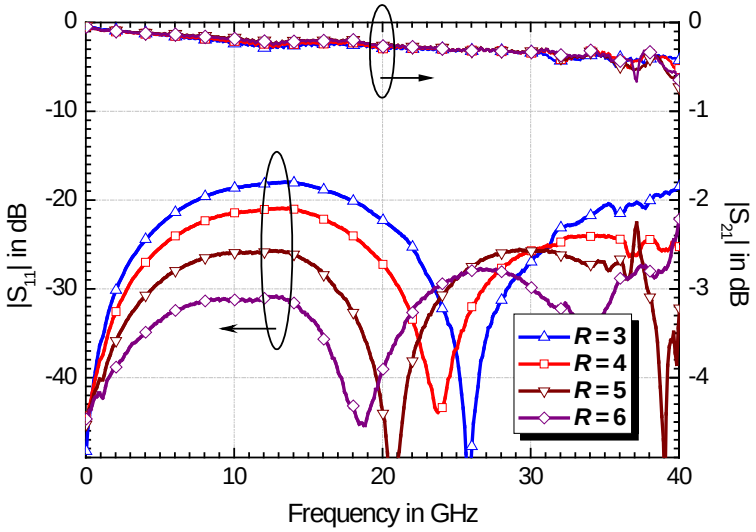


Fig. 65. Measurement results of return loss versus frequency. The parameters are various ratios of outer conductor radius to inner conductor radius of coaxial transitions ($R = r_o/r_i$ = 3, 4, 5, 6) while h_c equals 30 μm, h_s equals 30 μm, t_{Cg} equals 50 μm.

About the performance comparison between the conventional three-bump (G-S-G) flip-chip interconnect structure and the proposed coaxial interconnect structure, there is actually no fair starting point to do the comparison because the proposed coaxial interconnect structure is completely different from the conventional one. Without compensation design, the return loss of the conventional flip chip interconnect was only about 18 dB from DC to 40 GHz [17, 19]. However, with high impedance compensation design at the transition, the return loss of the conventional one was further improved, which could be below 20 dB from DC to 40 GHz as indicated in [19]. In this study, the flip-chip interconnect structure using the proposed coaxial

transition demonstrates an excellent reflection property below 20 dB from DC to 40 GHz as well. However, for the dimensional comparison with the conventional flip-chip structure, the coaxial approach requires a little more area in order to form the coaxial structure at the vertical transition.

After thermo-compression bonding, the designed parameters of the coaxial transition structure have changed. Therefore, we used the CST simulator to re-simulate the coaxial transition structure with the consideration of the reality. The coaxial transition model data were then exported from the CST simulator and inserted into the Agilent ADS circuit simulation tool to simulate the full back-to-back flip-chip interconnect structure. Fig. 66 shows the modeling circuits of the flip-chip interconnect structure with the vertical coaxial transition for the case of the designed parameter R = 3. The same modeling circuits were also used to simulate the interconnect structures with the different designed ratios R. The dimensions for the CPWs on the chip and the substrate are also shown in the figure.

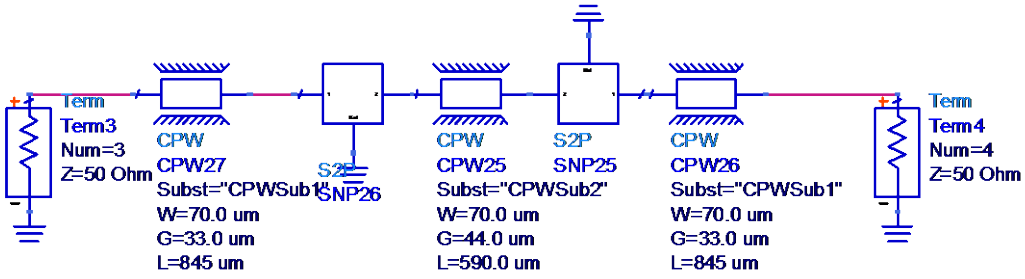


Fig. 66. Modeling of the back-to-back interconnect structure with the EM simulated transition model inserted.

The comparisons between the simulated and the measured data for different R are shown in Fig. 67 to Fig. 70. For the cases of R = 3, 4, and 5, the modeled and simulated curves show almost the same profiles. In the case of R = 6, the simulated and measured curves show only a little difference. The simulated and measured results show excellent agreement, which validates the accuracy of the transition data exported from the EM wave simulation tool. In this way, designers can predict the final performance of the assembled circuits in the system. It also means that one can take the vertical coaxial transitions and interconnects into consideration in advance at the design stage to anticipate the circuit performance after packaging and have beforehand optimization.

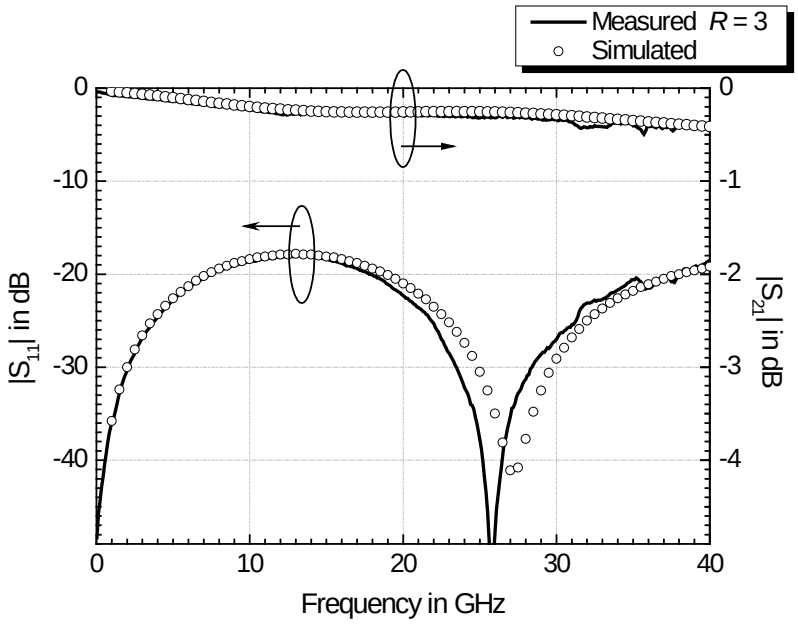


Fig. 67. Simulated and measured results of the flip chip interconnect structure with the coaxial transitions where R = 3.

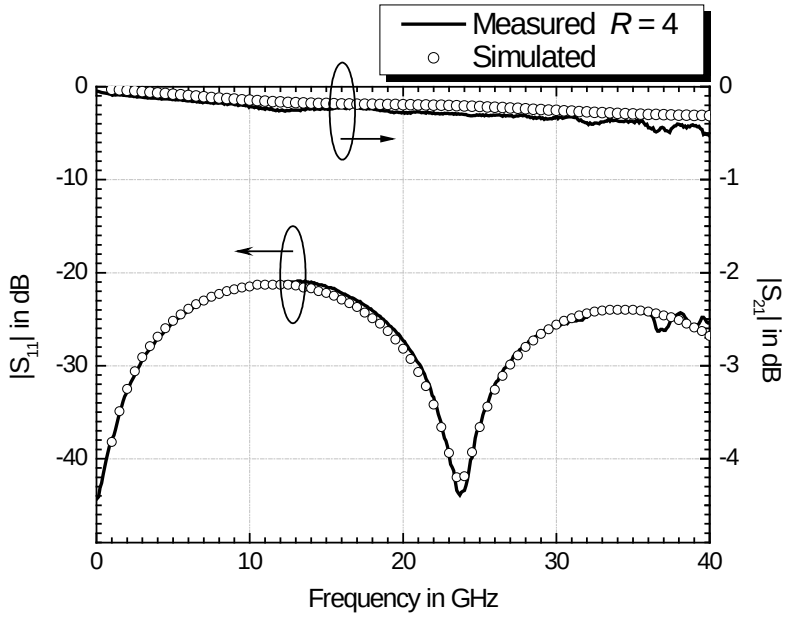


Fig. 68. Simulated and measured results of the flip chip interconnect structure with the coaxial transitions where R = 4.

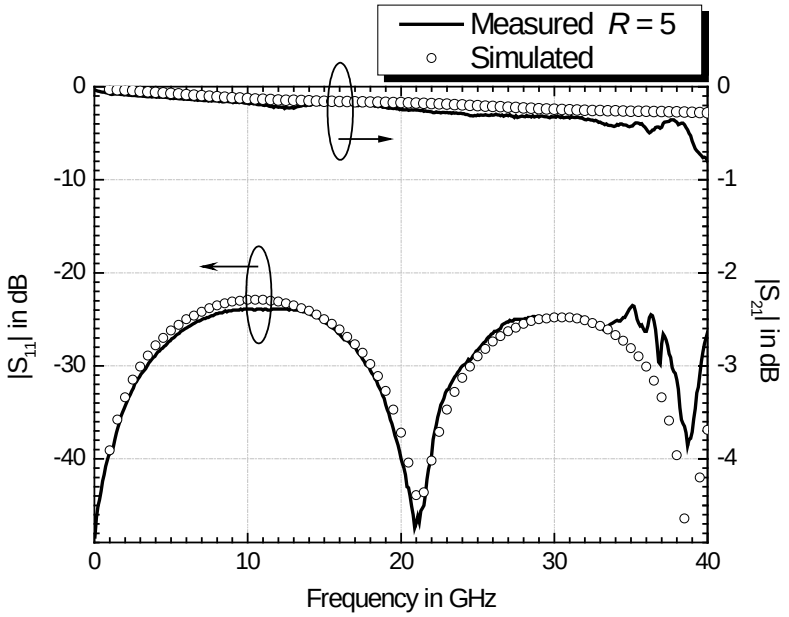


Fig. 69. Simulated and measured results of the flip chip interconnect structure with the coaxial transitions for $R = 5$.

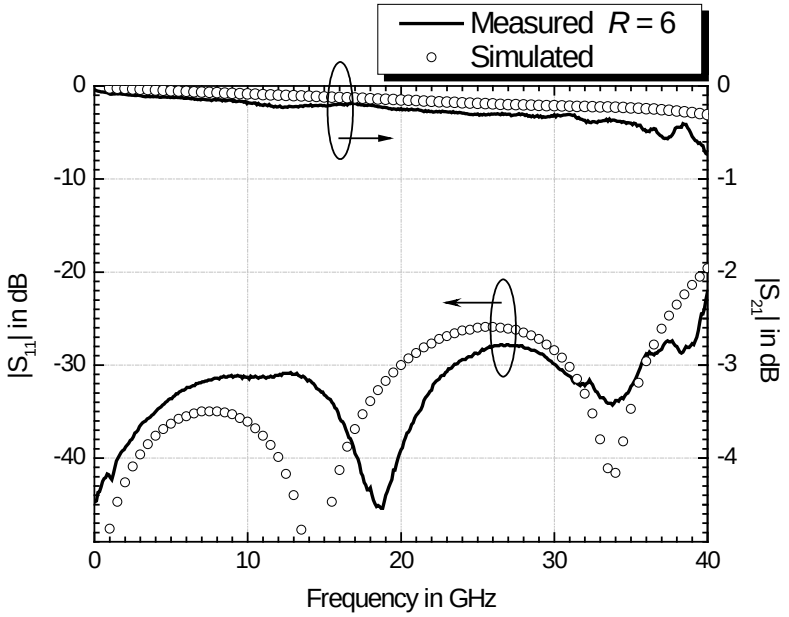


Fig. 70. Simulated and measured results of the flip chip interconnect structure with the coaxial transitions where $R = 6$.

5.6 Perfect coaxial transition using BCB dielectric

In this section, a perfect coaxial transition for CPW-to-CPW flip chip interconnect is further presented and demonstrated. To realize this perfect coaxial transition on the CPW circuit, benzocyclobutene (BCB) was used as the interlayer dielectric between the vertical coaxial transition and the CPW circuit. The coaxial interconnect structure was successfully fabricated and RF characterized up to 67 GHz. The structure showed excellent interconnect performance from DC up to 55 GHz with return loss better 20 dB and insertion loss less than 0.5 dB even when the underfill was applied to the structure.

5.6.1 Idea and advantages of the perfect coaxial transition

Fig. 71 shows the coaxial transitions for the CPW-to-CPW flip chip interconnect structure using BCB dielectric. For the idea of the proposal, the ring-shaped ground bump together with the center signal bump forms a perfect coaxial transition structure. It has the advantage of better field confinement and can therefore achieve good isolation property at the vertical transition when compared with the conventional G-S-G transition architecture. In other words, it can provide good electric shielding for the vertical signal transmission. The detailed view of the perfect coaxial transition is shown in Fig. 71 (d).

Underfill is generally needed for flip chip structure to ensure the joints reliability during the temperature cycling by reducing the thermal stress due to the CTE (coefficient of thermal expansion) mismatch of different materials. However, it degrades the performance of the flip chip assembly [32-37], because of the higher dielectric constant (usually 3~4) and the higher dissipation factor (approximately 0.05 at 10 MHz) compared to air. The underfill mainly induces additional transmission loss to the final assembly and changes the effective dielectric constant of transmission lines on the MMICs. However, with the proposed perfect coaxial transition, the impacts of the underfill on the flip chip interconnects can be effectively reduced. With the ring-shaped ground wall the injected underfill stays outside of the coaxial structure, it can provide good isolation and prevent the perturbation of the underfill for the signal transmission in the coaxial structure.

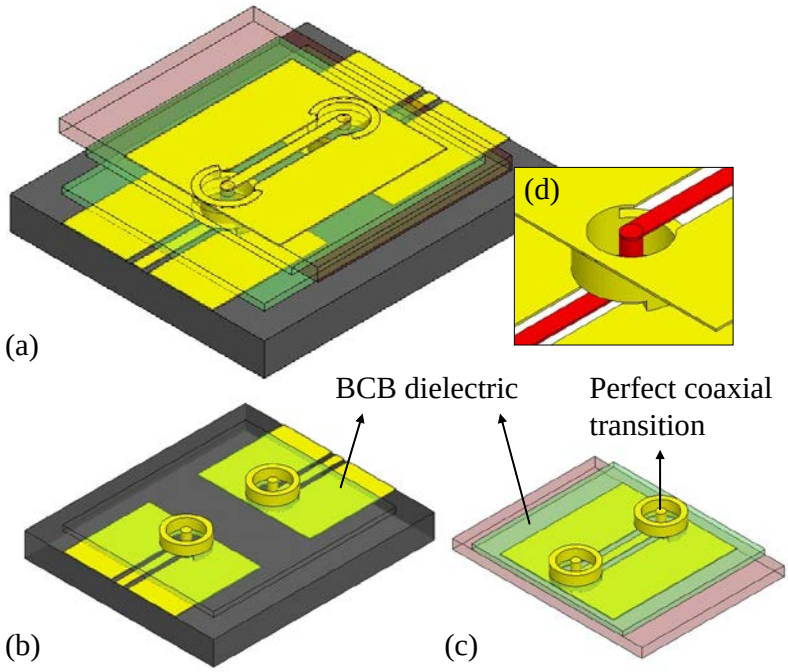


Fig. 71. The perfect coaxial transition structure for the CPW-to-CPW flip chip interconnects with the use of the BCB dielectric.

5.6.2 Design of the perfect coaxial transition

The perfect coaxial transition structure was designed using the simulation tool CST for the 3-D electromagnetic field analysis. The goal of the design was to achieve low reflection below 20 dB at the interconnect with a bandwidth from DC to 60 GHz. The thickness of the Al_2O_3 substrate and GaAs chip were 254 μm and 100 μm, respectively. The characteristic impedances (Z_0) of the Au CPW lines on the chip and the substrate were 50 Ω (w_{sub} = w_{chip} = 80 μm, g_{sub} = 44 μm, and g_{chip} = 59 μm). The CPW length on the chip was 900 μm, and the CPW length on the substrate was 700 μm. The total length of the interconnect structure was 2300 μm. Fig. 72 shows the final optimized design details of the coaxial transition structure, where r_i = 40 μm, t_g = 50 μm, r_o = 155 μm, h_{BCB} = 10 μm, and h_{coax} = 20 μm. After design, the interconnect structures were fabricated for demonstration using the in-house developed process.

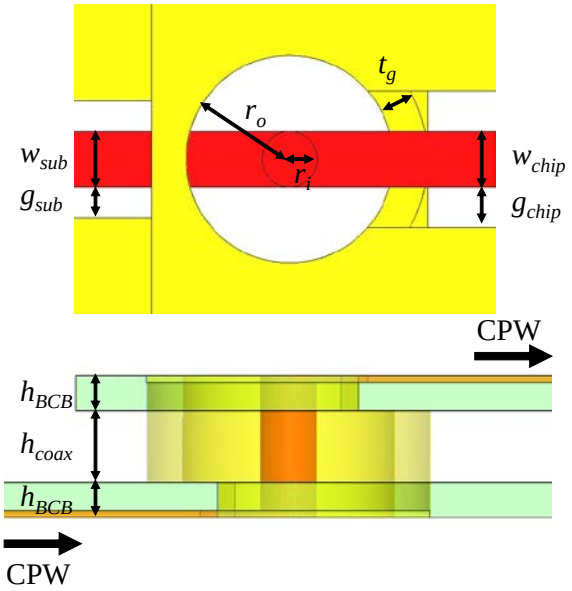


Fig. 72. The physical parameters at the designed perfect coaxial transition.

5.6.3 In-house developed fabrication process

For the proposed perfect coaxial transition in the flip chip structure, the fabrication of the coaxial bumps is of critical importance. In order to realize the perfect coaxial transitions between the CPW circuits on the chip and on the substrate, a dielectric layer must be used to support the ring-shaped ground bump and prevent the coaxial ground bump from touching the CPW signal line. BCB was chosen here as the dielectric layer because of its superior performance at high frequencies. Fig. 73 shows the whole fabrication process steps. Al_2O_3 and GaAs were the materials for the substrate and the chip, respectively. The interconnect metal was Au and formed by electroplating. After the Au CPW lines of 3 μm were electroplated, as shown in Fig. 73 (f), BCB were coated as the dielectric layer. The photoresists were then patterned on the BCB layer as the etching mask for the following dry etching process. After RIE etching with the CF_4 and O_2 gas mixture, the BCB film was patterned and then cured at 250^{o}C for 1 hour to achieve the polymerization, as shown in Fig. 73 (j). The optimized BCB dry etching condition is summarized in Table 8. Fig. 74 shows the SEM images with the good etching results of the BCB dielectric layer using the optimized etching condition. Ti (300 Å) and Au (500 Å) layers were deposited using E-gun evaporator as the seed layer for the electroplating of the vertical coaxial bumps. To define the positions and dimensions of the coaxial transitions bumps, thick photoresists were patterned, as shown in Fig. 73 (l). By controlling the electroplating current density and time, the Au coaxial bumps of the required height were attained.

After electroplating, the thick photoresists and the seed layer were then removed to form the final structure, as shown Fig. 73 (o). The coaxial bump transitions were fabricated on both the Al_2O_3 substrate and the GaAs chip. Fig. 75 shows the SEM image of the fabricated chip with the fabricated coaxial bumps. The fabricated chip sample was then bonded to the substrate sample using the thermo-compression method to accomplish the final interconnect structure.

Table 8. The optimized BCB dry etching condition by using RIE etcher [56].

Pressure	RF Power	Gas ratio	Etching rate
80 mTorr	250 W	CF_4/O_2 = 14/35 (sccm)	~ 0.65 μm/min

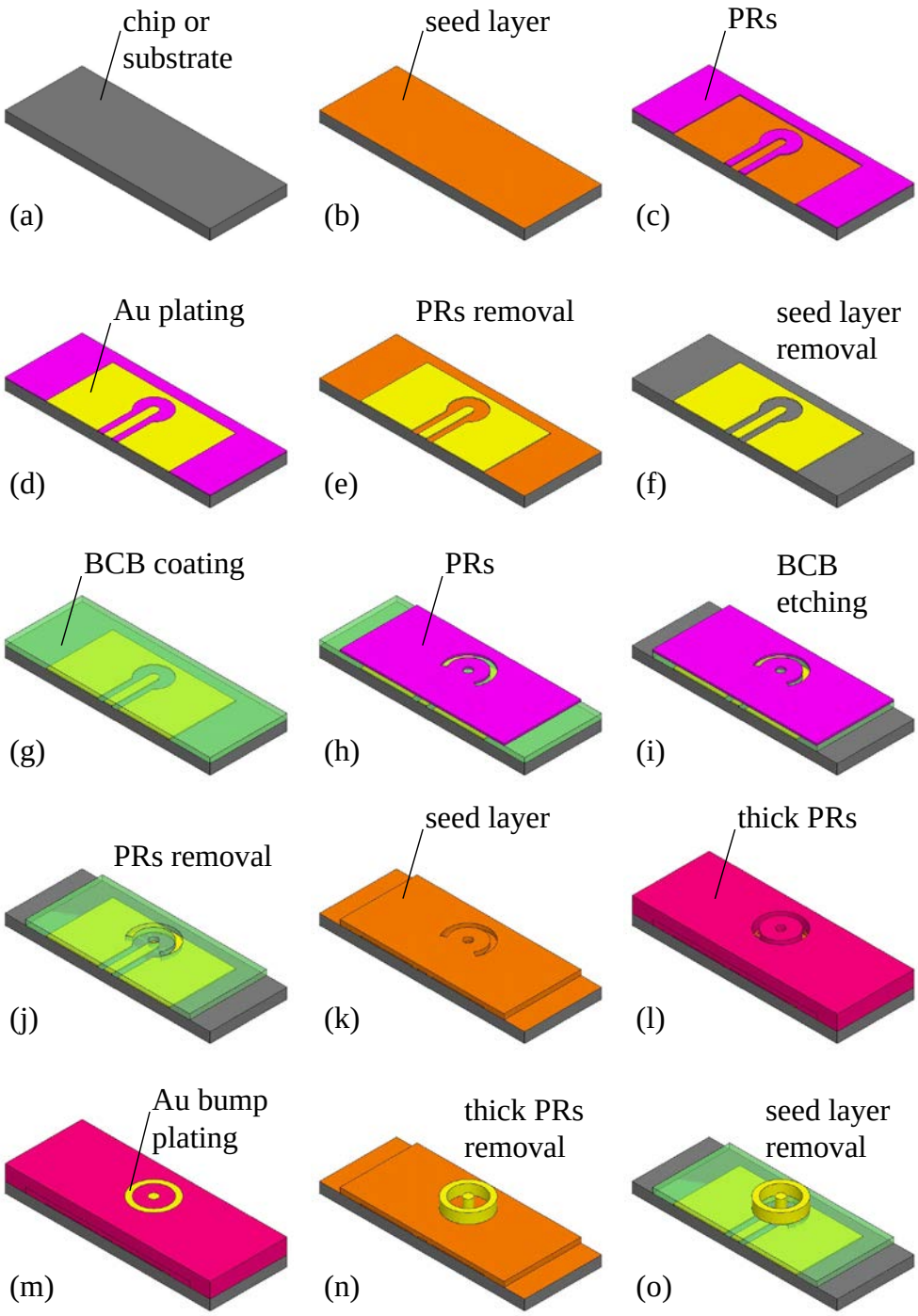


Fig. 73. The whole process steps to fabricate the perfect coaxial transition.

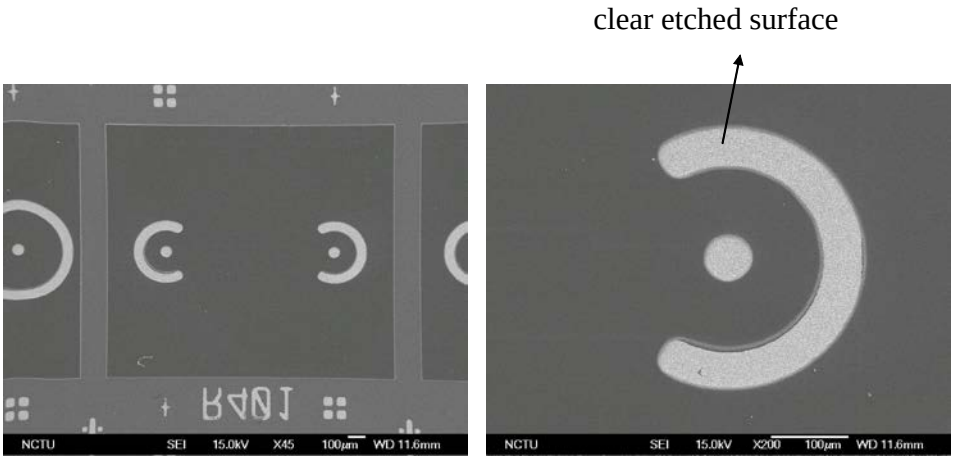


Fig. 74. The SEM images of the BCB dielectric layer with the good etching results.

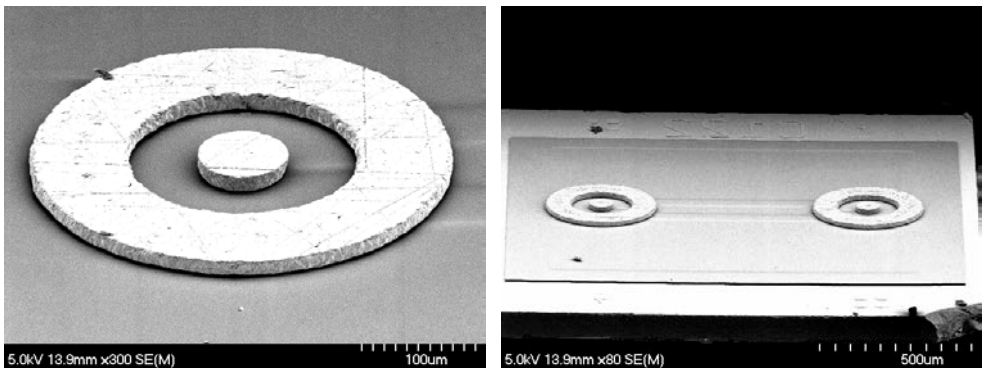


Fig. 75. The SEM images of the fabricated coaxial transition and the chip sample.

5.6.4 RF characterization results

The demonstrated flip chip interconnect structure using the perfect coaxial transitions was RF characterized up to 67 GHz by the on-wafer probing measurement system with the Agilent PNA (Performance of Network Analyzer). Fig. 76 shows the simulated and measured transmission coefficients of the demonstrated structures with and without the underfill injected (ε_r = 3.5 and $\tan\delta$ = 0.02 at 10 MHz). The simulated and measured results show good agreement. The flip chip interconnect structure with the perfect coaxial transitions demonstrates excellent performance up to 67 GHz. In the case without underfill injection, the return loss was less than 20 dB and the insertion loss was within 0.7 dB from DC to 67 GHz, which clearly demonstrates the feasibility and potential of the perfect coaxial transition for the flip chip interconnects. In the case with the epoxy-based underfill injection, the return loss was still less than 20 dB from DC to 55 GHz. Above 55 GHz, the return loss and insertion loss became worse; however the return loss was still less than 10 dB at 67 GHz. The shift in the

frequencies of the minimum reflection resulted from the change of the effective dielectric constant of the CPW line due to the existence of the underfill. The return loss slightly increased because of the impedance mismatch induced by the change in the effective dielectric constant. The two structures with and without underfill injection showed comparable insertion loss from DC to 55 GHz. Above 55 GHz the sample with the underfill injection showed an increase in the insertion loss, and the return loss also increased. At 60 GHz, the return loss was 13.7 dB, and the insertion loss was 0.9 dB. The measured results demonstrated excellent potential for the perfect coaxial transition to be used for the flip chip interconnects up to 60 GHz.

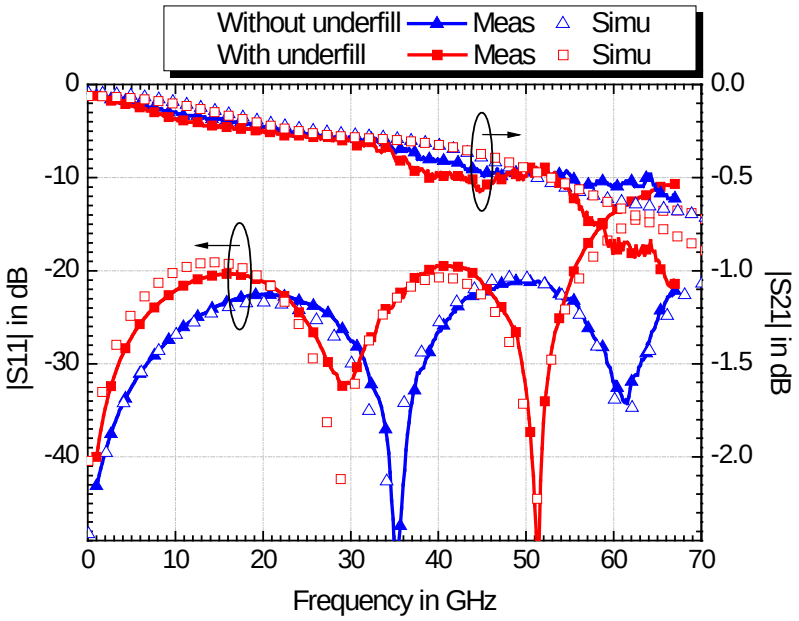


Fig. 76. Comparison of the simulated and measured S-parameters of the demonstrated structures with and without underfill injection

Chapter 6

Conclusions

6.1 Conclusions

This thesis work contributes to the flip chip interconnect techniques for microwave packaging. A complete Au bumping and bonding process has been developed for fabrication of flip chip assembly. Hot-via transition for microstrip type packaging has been investigated and demonstrated to offer broadband interconnect from DC up to 60 GHz. A novel concept using coaxial transitions has also been proposed and successfully demonstrated. It shows excellent performance and great potential for high frequency interconnects.

The hot-via approach provides the microstrip MMIC chips with a non-flipping interconnect technique, which can avoid the detuning effect to the front-side circuits of the chips. However this approach requires a few additional steps to the backside process to pattern the backside metallization, which is rarely seen in a conventional foundry process and of course leads to a little complexity to the process. From the parametric simulations and discussions, the design rules were derived for of the hot-via transition. The diameter of the via hole (d_v) and the bump (d_b), if applicable and practicable, should be as small as possible in order to get the lower reflection at the interconnect. The higher bump height (h_b) reduces the reflection as well. For the pad dimension (l_p) at the transition, one should avoid using large pad but keep the pad as small as possible to minimize the return loss at the transition. To fabricate the demonstrated hot-via interconnect structures in this study, the process has been fully in-house developed. It has been demonstrated that the hot-via architecture exhibits excellent performance for flip chip interconnects with very low transition loss over a very broad bandwidth from DC up to at least 60 GHz. From the experimental results, the GND pads and vias of the MMICs chips had minor influence to the signal transmission properties, *e.g.* return loss and insertion loss. By adopting the compensation design, the hot-via flip chip interconnect structure showed excellent interconnect performance with the return loss better than 18 dB and insertion loss within 0.5 dB from DC to 60 GHz, where the hot-via and bump transitions accounted only for 0.23 dB of loss. This is the best result reported so far to our knowledge. The

work explored the promising results for the use of the hot-via approach as the packaging solutions for the microstrip design based MMICs at high frequencies at least up to 60 GHz.

A whole new idea for flip chip interconnects, the concept of the coaxial transition, has been proposed and demonstrated in this study. To realize the coaxial transition for the flip chip interconnects, the complete fabrication process has been successfully developed. The physical parameters of the coaxial transition structure are well indicated; their effects on the interconnect performance are also well investigated. The design parameters of the coaxial transition are the bump height, the ground wall thickness, and the ratio of the radius of the outer conductor to the radius of the inner conductor. Several rules for the design of the coaxial transition are concluded and summarized as follows. The higher bump height gives the lower return loss at the interconnect. The thinner C-shaped ground wall thickness also gives the lower return loss. However, these two parameters of the coaxial transition only show small improvement on the reflection property. The key parameter of the coaxial transition is the ratio *R*, which greatly affects the interconnect property. It is suggested that there is an optimum value of *R*, which gives the lowest reflection at the transition. The design concepts of the coaxial transition have been validated through the realization of the coaxial transition on the flip chip interconnects. The characterized results of the interconnect structures showed excellent performance, where no additional insertion loss was observed and the return loss was better than 25 dB from DC up to 40 GHz. The coaxial transition has been well modeled and extracted from the EM simulator; the simulated data showed good agreement with the measured data.

Further, by using BCB dielectric the perfect coaxial transition has been realized and experimentally fabricated for the flip chip interconnects, which exhibits excellent transition performance with low return and insertion loss from DC to 67 GHz at least. Even with the underfill injection, the flip chip interconnect structure using the perfect coaxial transition still showed excellent interconnect performance. The novel approach using the coaxial transition for the flip chip interconnects has been proved to show great potential for high frequency packaging applications; this study also reveals the possibility for the application of the coaxial transition as the various interconnect transitions at high frequencies, such as the transition from inverted MS to CPW.

6.2 Suggestions for future work

This thesis deals with the high frequency flip chip interconnect techniques including the design, fabrication, and RF characterization and mainly concentrates on the hot-via approach and the coaxial transition approach. Although both approaches have demonstrated excellent interconnect performance, substantial further development is required to have more knowledge of each approach and evaluate the feasibility of the realization on the active circuits assembly. Some suggestions for the continuous work are given below.

For the continuous work about the hot-via approach, it can be further evaluated for the packaging applications even at frequencies above 60 GHz to reveal the frequency limit of this architecture. On the other hand, for demonstration of the packaging active circuits using the hot-via approach, so far only up to 40 GHz was the CSP MMICs demonstrated. This approach should be further applied and realized on packaging the microstrip type MMICs at higher frequencies to have more evidences and results proving its potential in very high frequency packaging applications. Besides, it requires more work on the equivalent electrical circuit modeling for the hot-via transition.

For the coaxial approach, further evaluation for packaging applications at frequencies above 60 GHz is required to explore how high frequency this approach is applicable for. More efforts are needed to push this approach towards higher frequency applications, such as the use of the compensation design. Besides, the coaxial approach can be further applied and realized as the packaging solution for active circuits; however, it may complicate the design of the circuits and the fabrication process. The equivalent electrical circuit model for the coaxial transition is still not fully developed; there is room for more research here.

The underfill degrades RF performance of flip chip assembly in some ways, such as the change of the effective dielectric constant and the additional losses. However, underfill is generally required for the flip chip assembly to attain long-term reliability, particularly important for the direct assembly to the motherboard with the high CTE or the use of lead-free solder. Very few give attention to this issue because gold bumping and ceramic packaging are prevalent in the microwave packaging and underfill is not so necessary in this case. When it goes towards low cost, underfill will show its necessity and importance to the flip chip assembly. However, it requires

more knowledge and efforts for underfill to be used in the RF-field packaging, such as what kind of underfill material should be used, new material development for low-k and low-loss underfill, or finding solutions to lower the influence from underfill.

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Appended papers

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