CPW: the RF interconnect for photonics

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CADFEM

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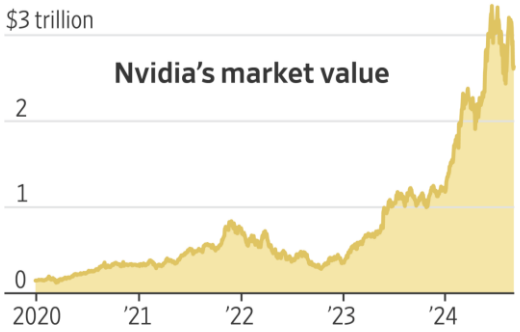
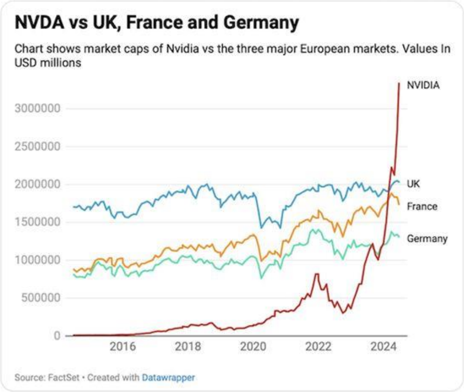
Agenda

- The rise of datacenters, the need for photonics
- The hidden devil: coplanar wave guide
- Tips and tricks for CPW simulation
- Summary

The rise of datacentres

- Everyone is using AI now!
- AI need loads of data centers



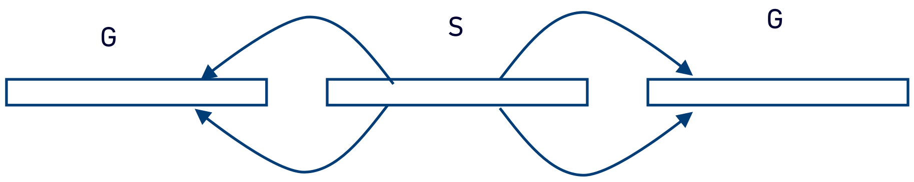


- These data centres are energy hungry
- Many attempts are done to reduce energy consumption and increase data rate
- Go from copper to fiber optics will dramatically increase data throughput and decrease losses hence decreasing energy usage

However,.....

- As the rest of the system is electric, we need electro-opto modulator, RF packaging and interconnects
- At these frequencies 10-300 GHz, Co planar wave guide is the interconnect of choice
- BUT CPW is super tricky

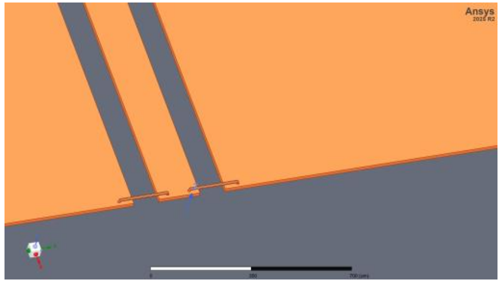
How does CPW work and not

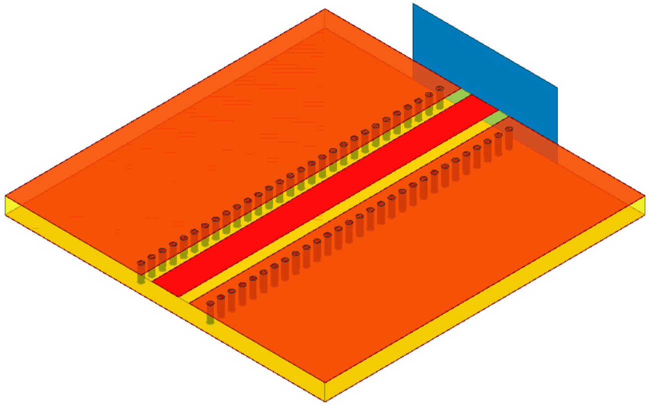


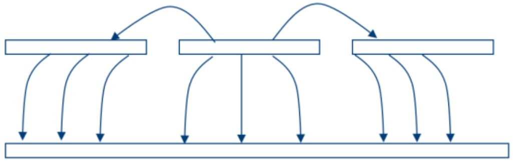
- Really difficult to keep CPW structures balanced and free from overmoding
- Anything in the structure of the filter itself, or near the filter on the substrate could influence how the current balanced itself, leading to structures that didn't behave correctly

Bridges or tunnels

- air bridges every 1/8 wavelength or less to keep the grounds at even potential or the line itself could become unbalanced and even start to radiate
- at every cross or tee junction, you have to put in air bridges to connect grounds on both sides to keep the current distribution balanced
- Grounded-backside CPW had strong parallel plate mode tendencies, and you have to throw so many stitching vias into the structures that you nearly ended up with substrate-integrated waveguides (SIW) that were stitched to keep the substrate modes below cutoff



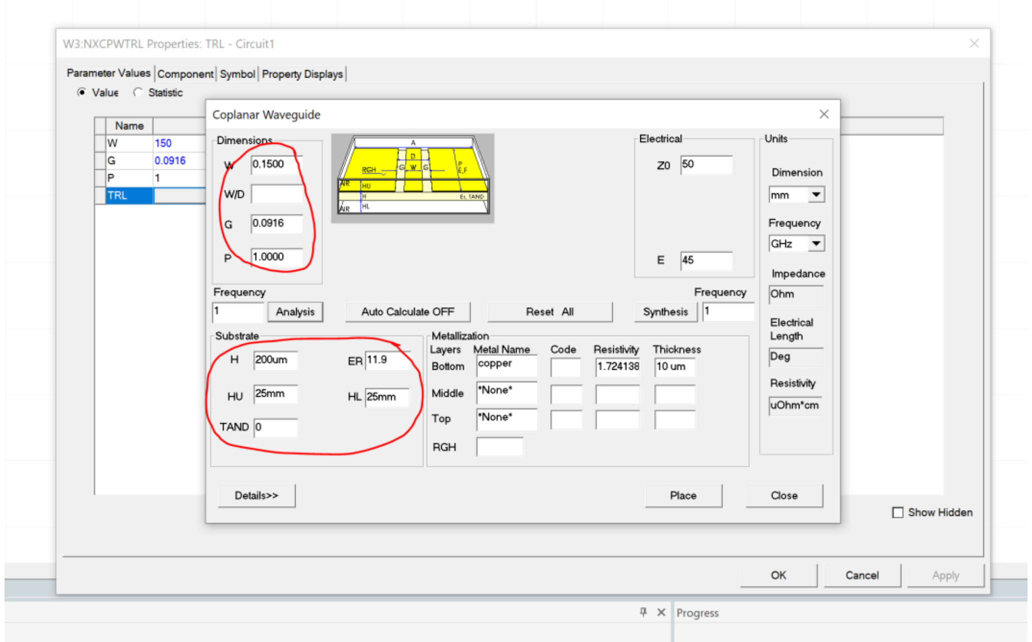




Tips and tricks for CPW simulation

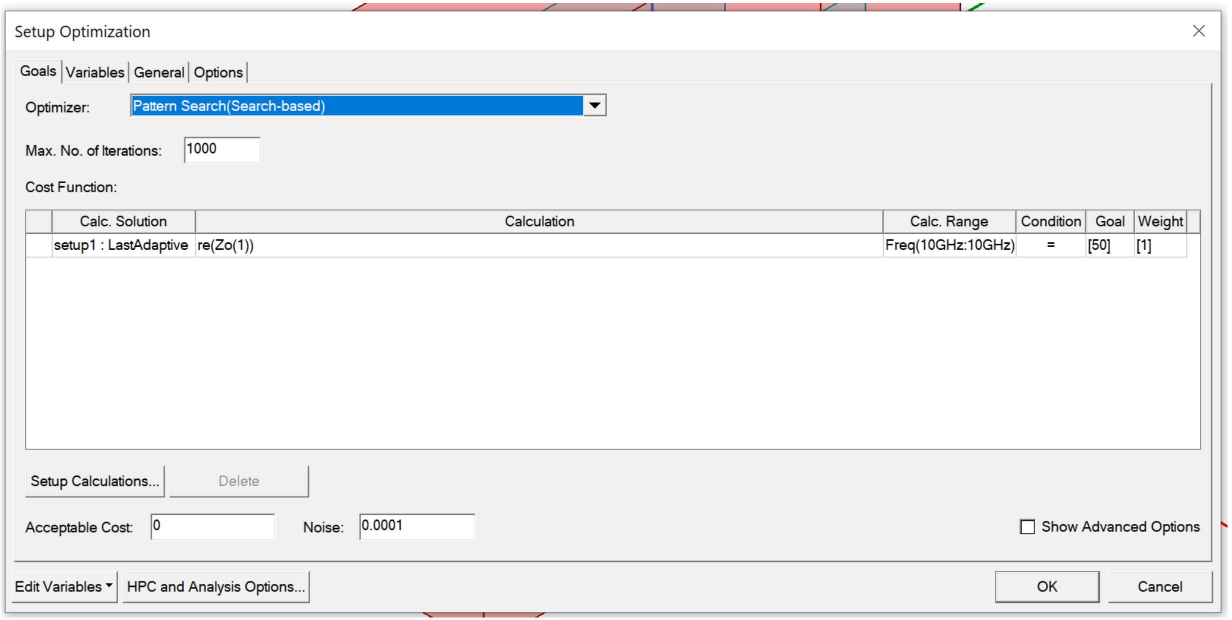
CPW on high resistivity Si

– First use TRL tool for synthesis. Instantaneous *mathematical* synthesis
– Example below for Si, 200 um substrate height,



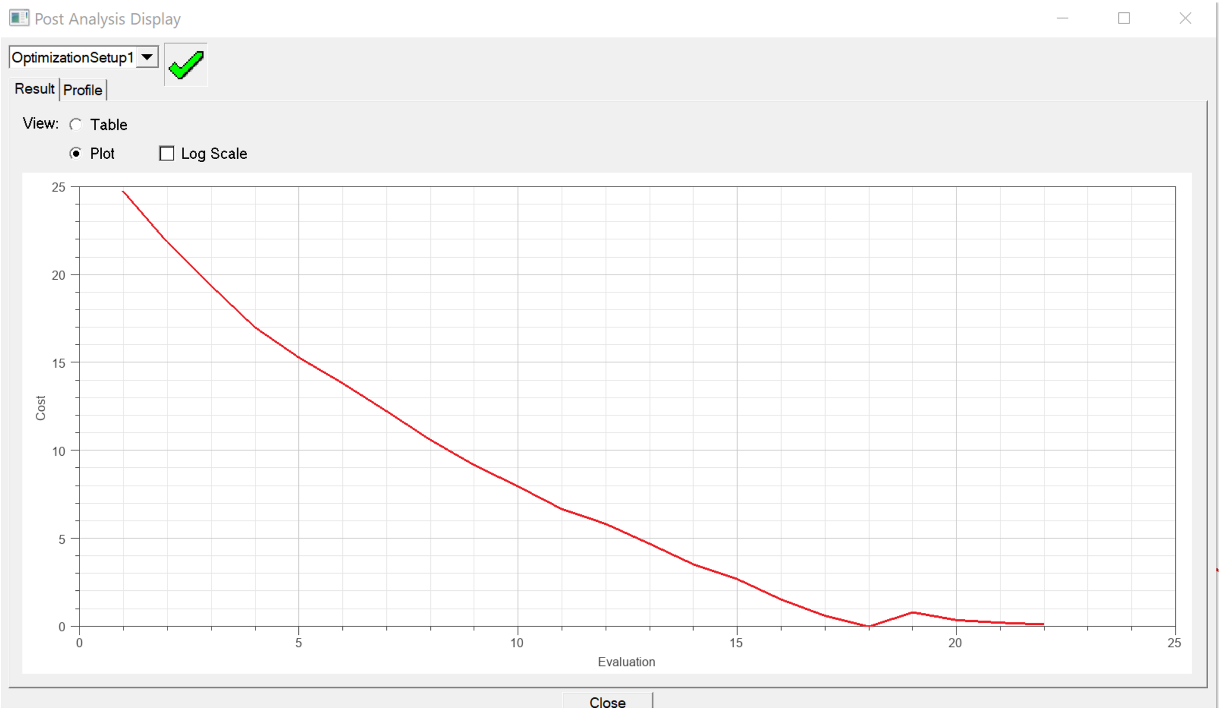
CPW in Fullwave

- The values (centre trace width and gaps) are only good as starting points. Further FEM analysis needed +optimization
- Using HFSS built in optimizer



Cost function evaluation

Cost= abs(current impedance-50)



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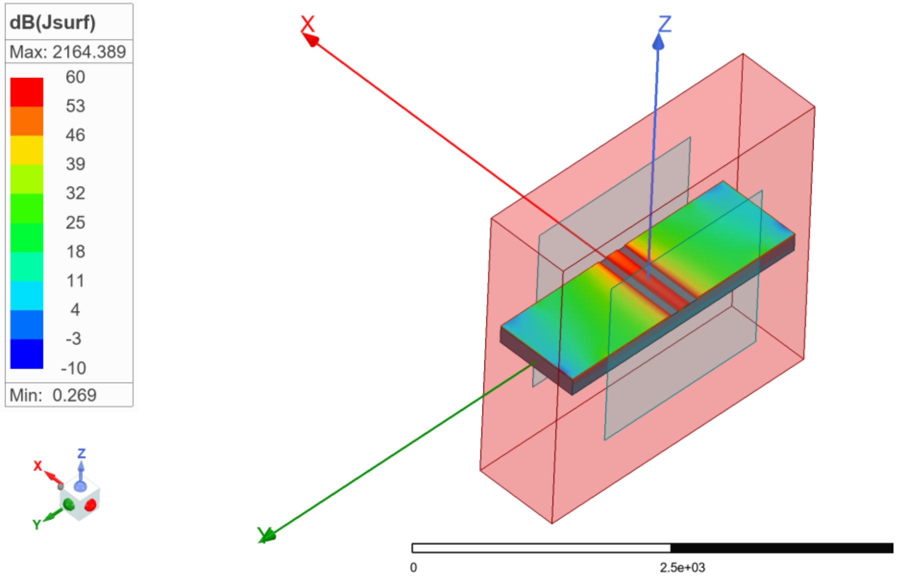
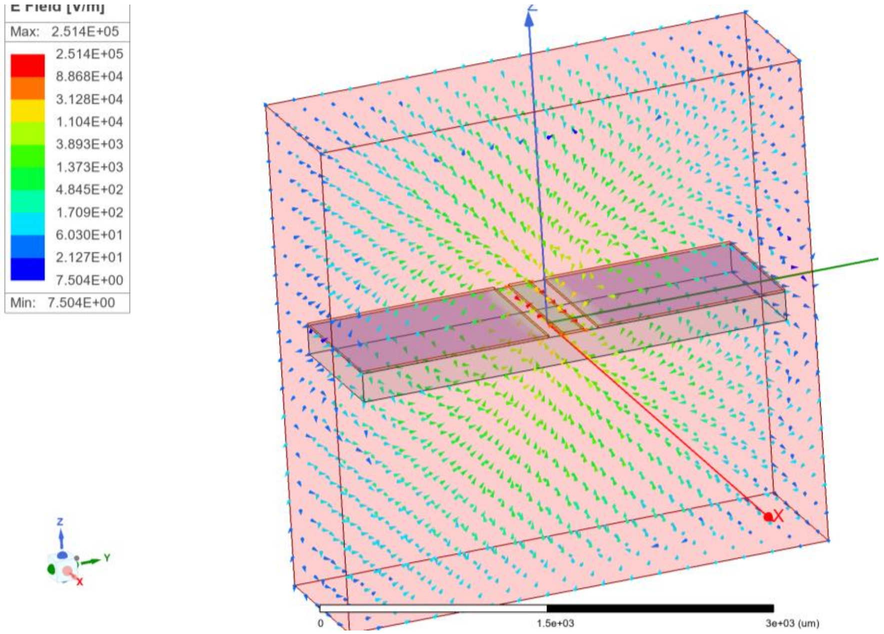
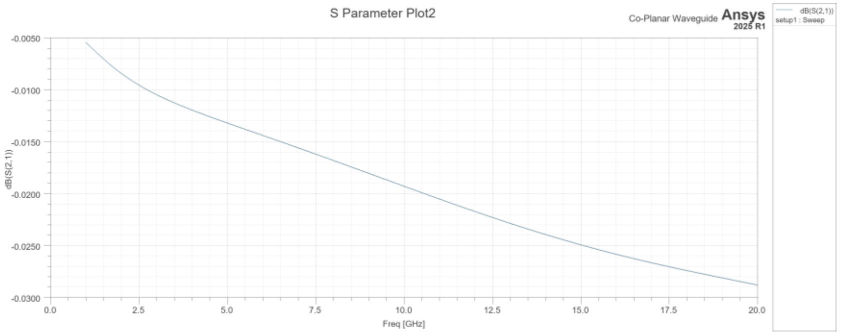
Current distribution

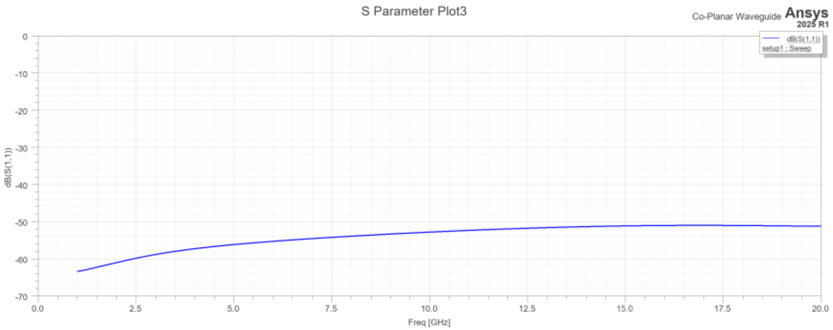




S parameters

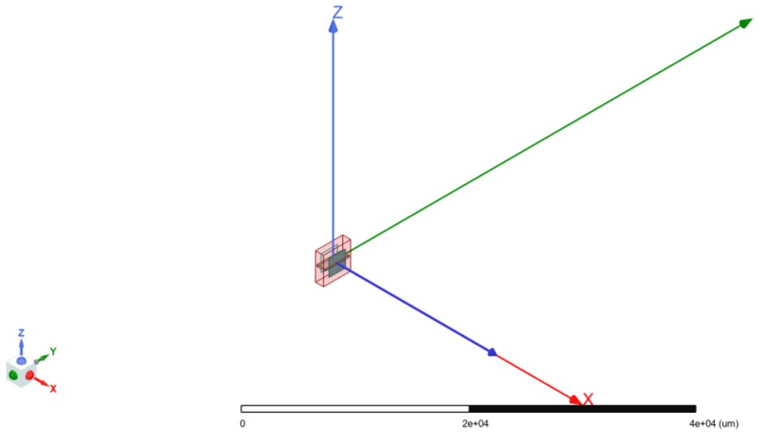
- Very high dynamic range

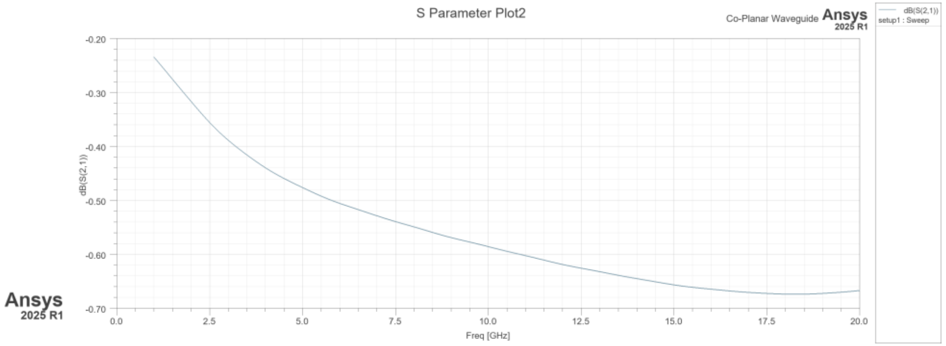


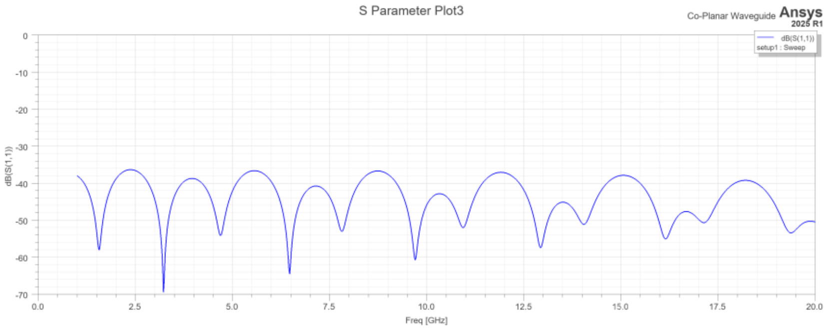


Can go further if wanted

Deembedding as postprocessing

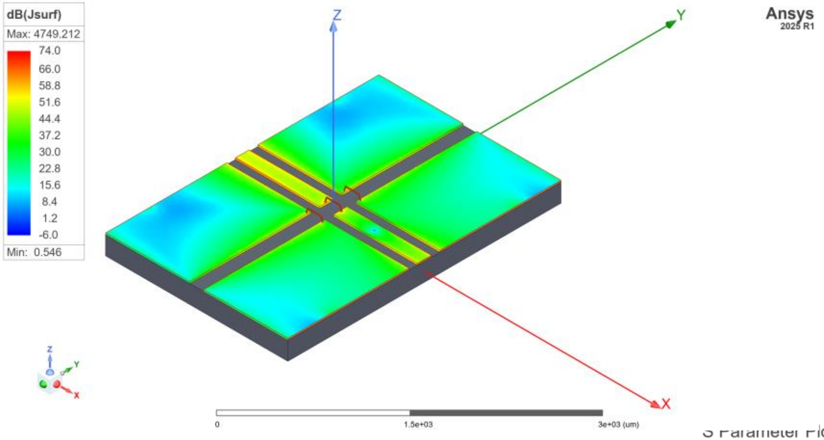


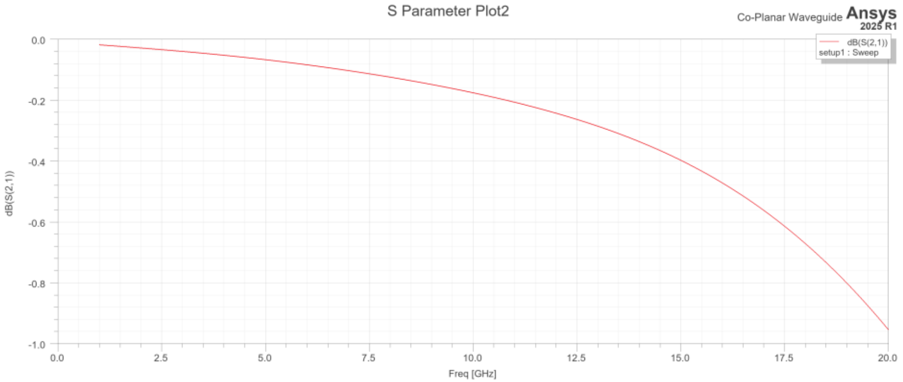


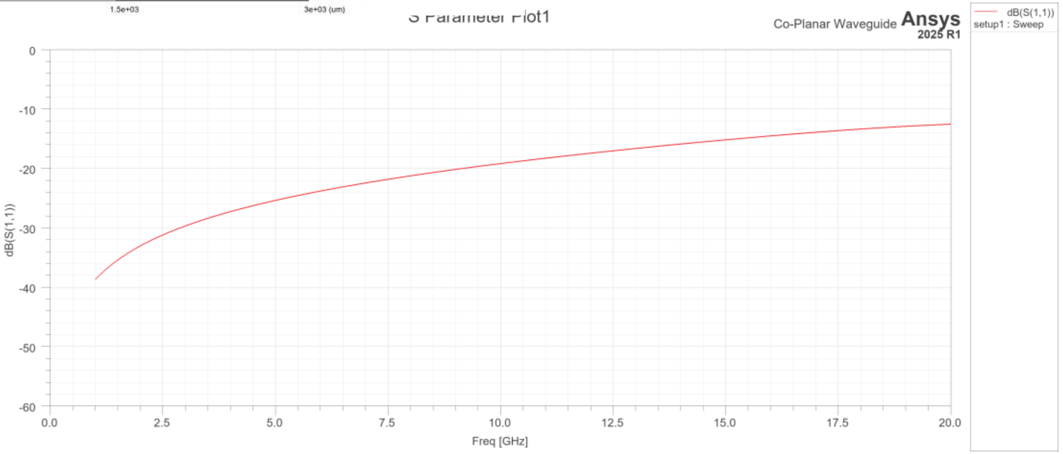


Bondwire transition

- Bondwire diameter = 10 um
- Bondwire height = 50 um
- Very high inductance







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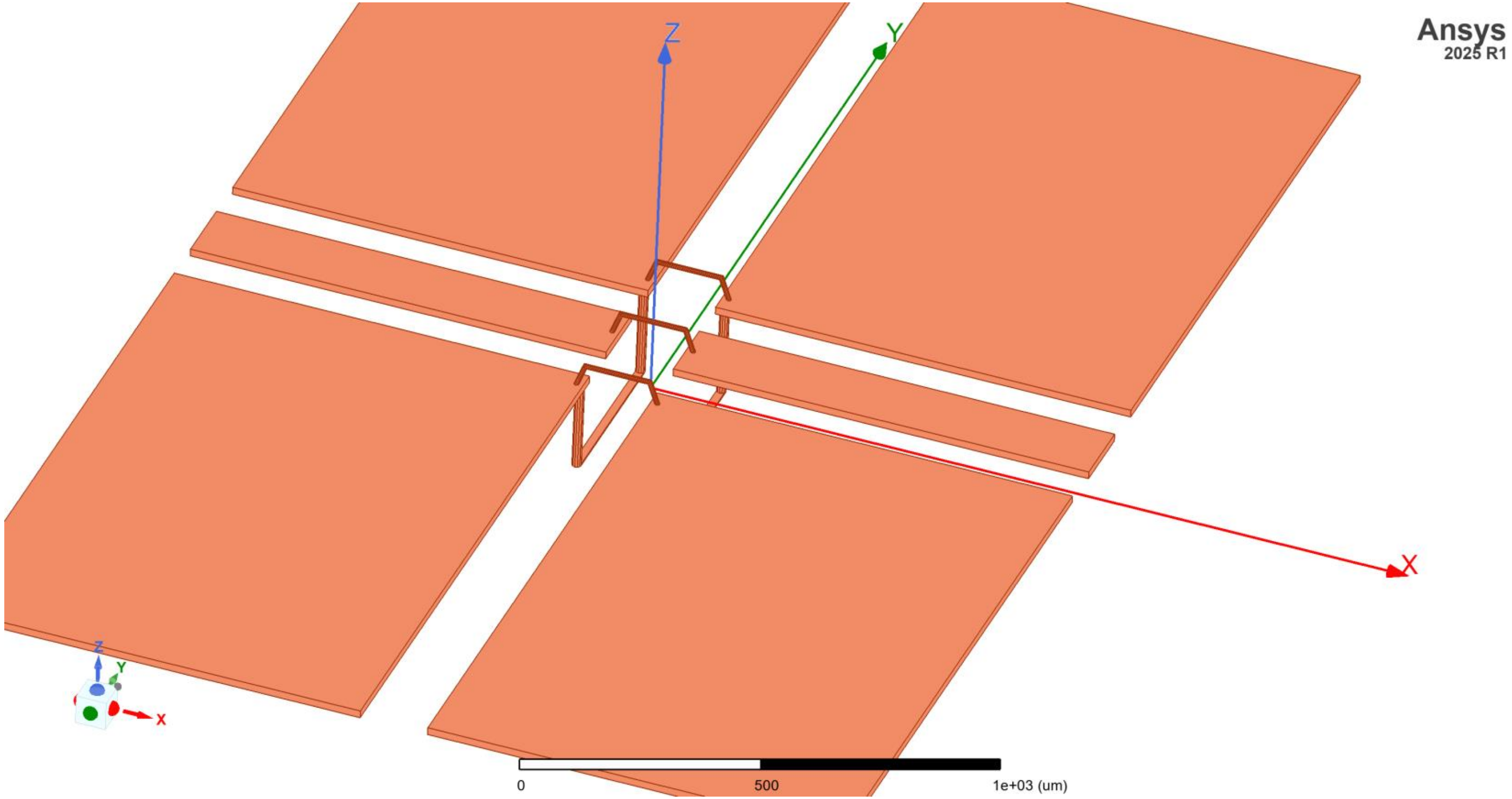
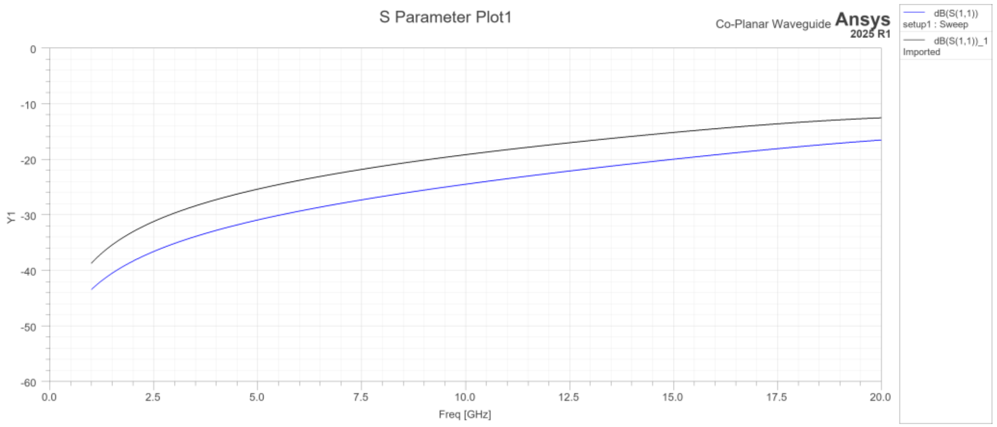
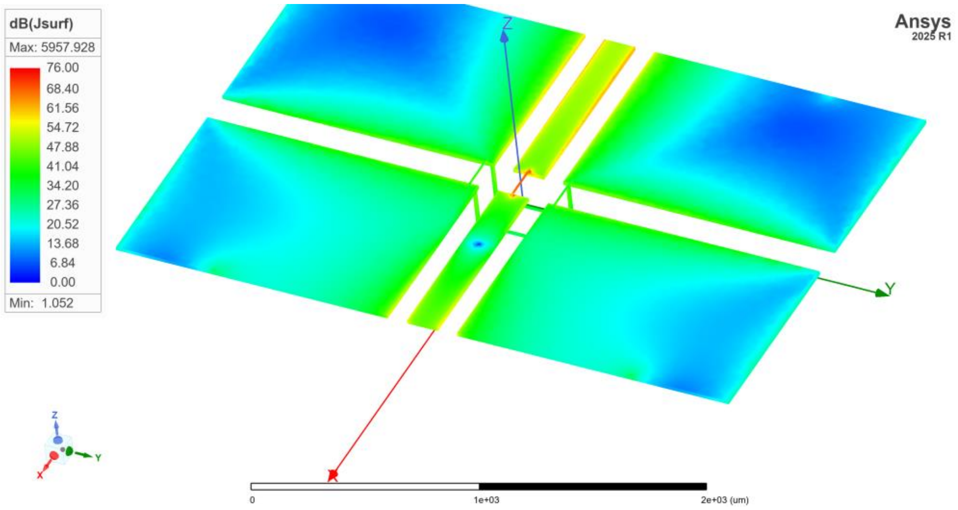
Adding bridges and tunnels to suppress parasitic modes



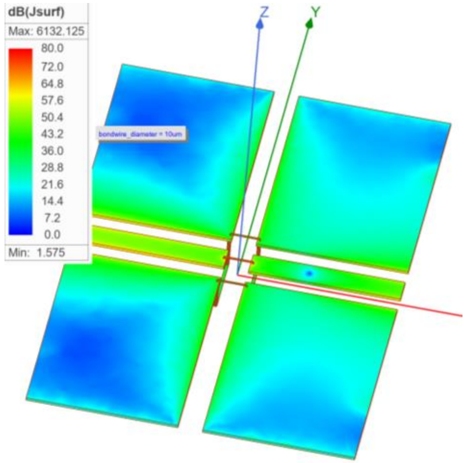
Reducing the bond wire inductance

- Reducing height from 50 um to 10 um

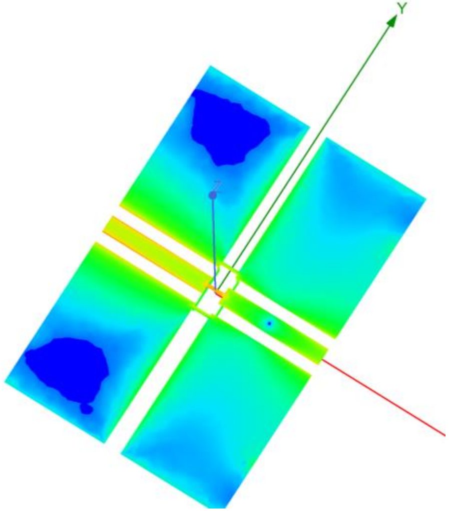




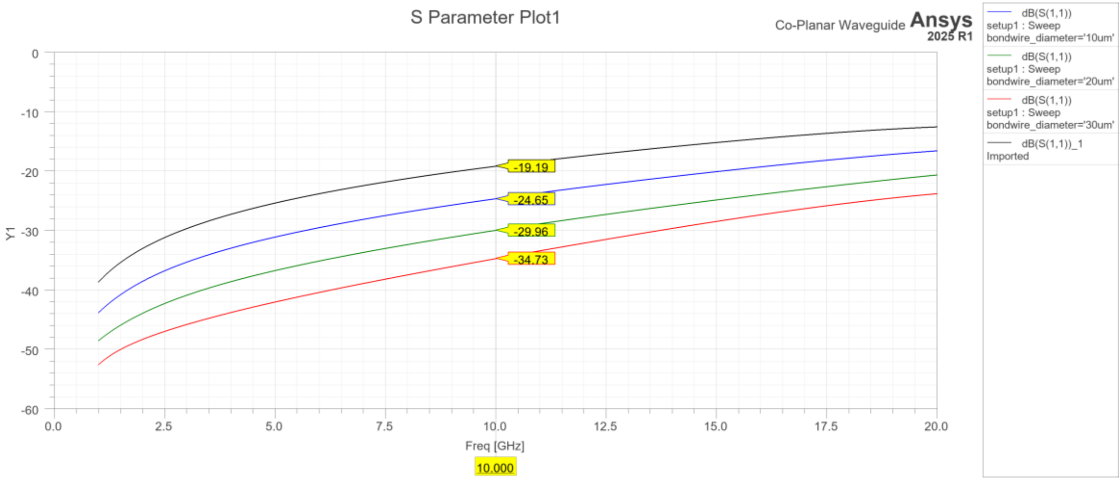
Sweeping the wire diameter from 10 um to 30 um



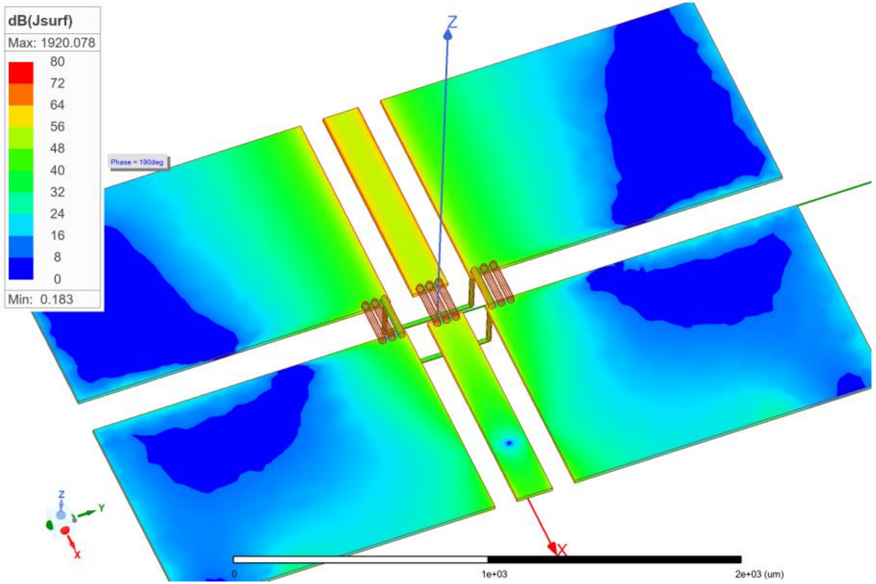
10 um

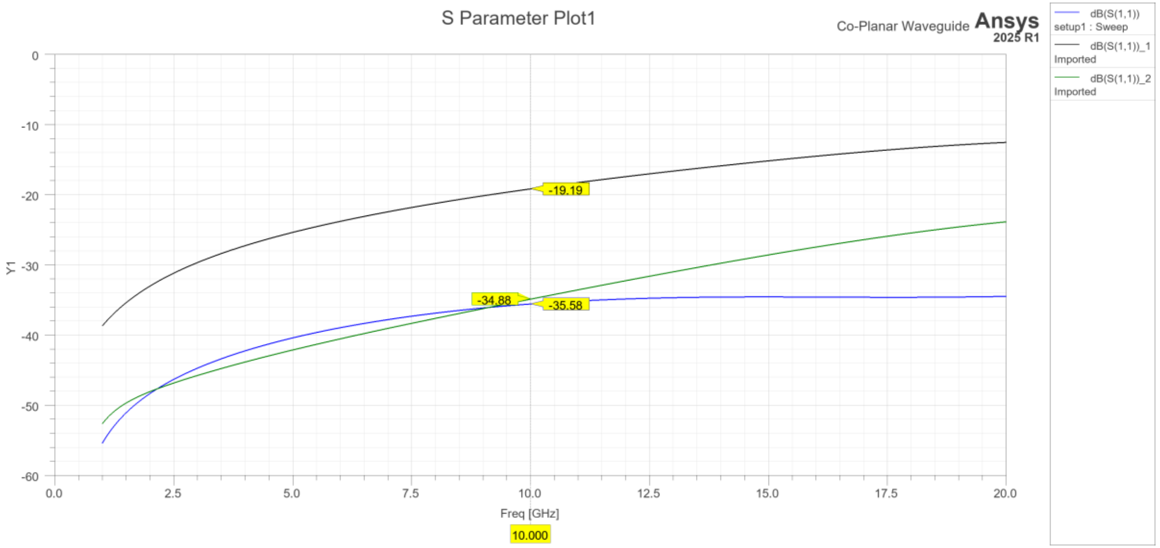


30 um

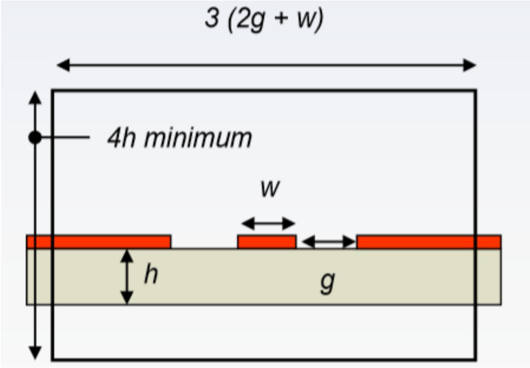


Adding more bond wires





CPW ports



Wave Port Location
•The wave port should be centered horizontally on the CPW trace.

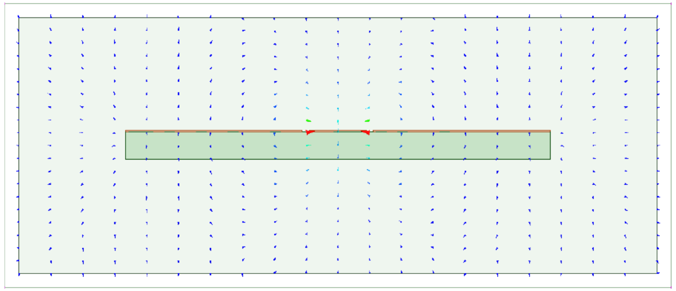
•**Wave Port Restrictions**
•**The wave port outline must contact the side grounds (all CPWs).**
•**The wave port size should not exceed lambda/2 in any dimension, to avoid permitting a rectangular waveguide modal excitation.**

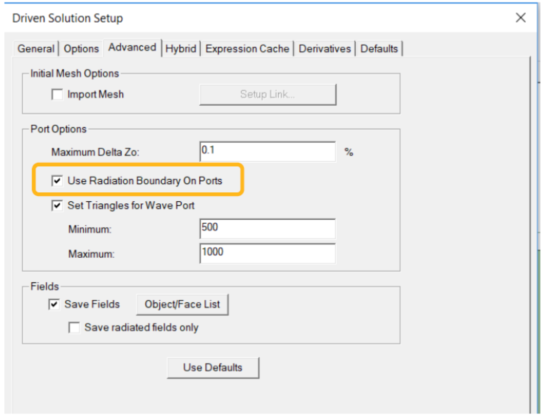
Port touching ground

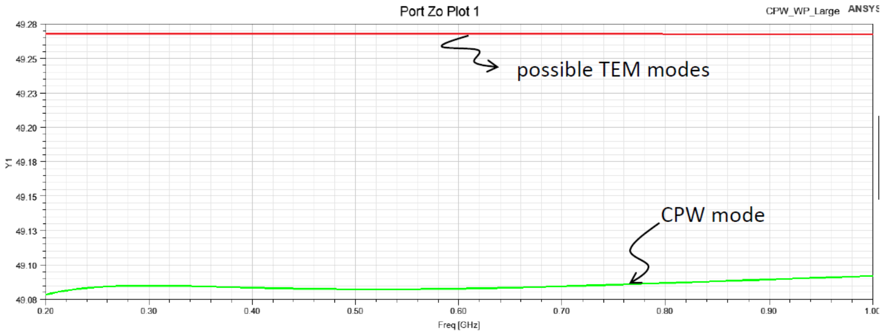
Port Recommendations : Wave Port …

Why must port outline touch side grounds?

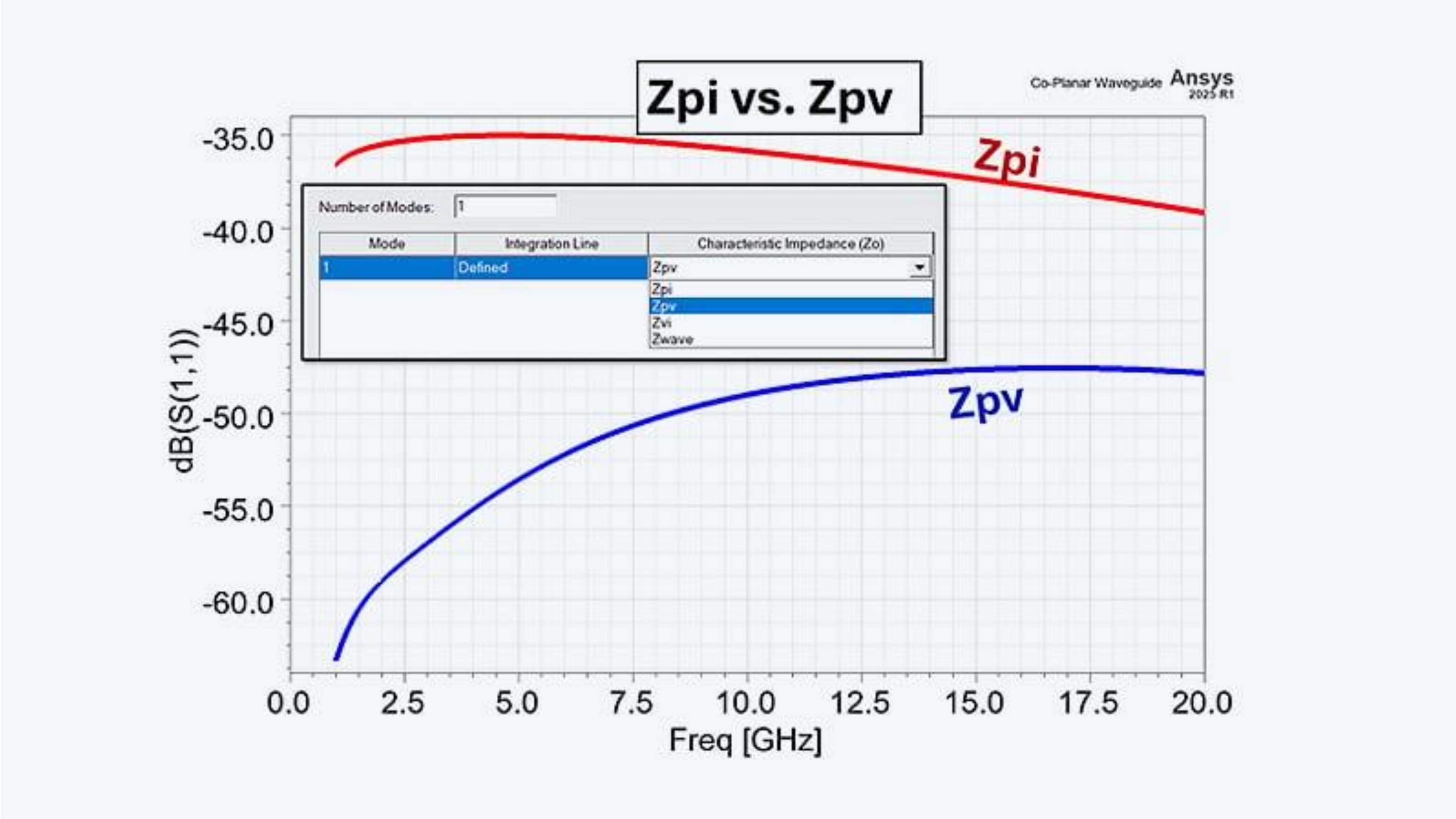
- If port outline does not contact side grounds, the port ‘window’ sees three possible signal traces inside the ‘ground reference’ of the port perimeter.
- Mode solved will be ‘even’ or first mode of 3 possible TEM modes in this system, not that of CPW excitation.







Charachtersitic impedance definition



Ohmic losses

- Remember skin depth? $\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$.
- It causes increasing losses as the frequency increases
- Skin depth decreases with √f
- RF resistance increases with √f
- Power losses due to skin effect increase with √f
- Now lets examine three cases low, medium, high frequency

Skin depth

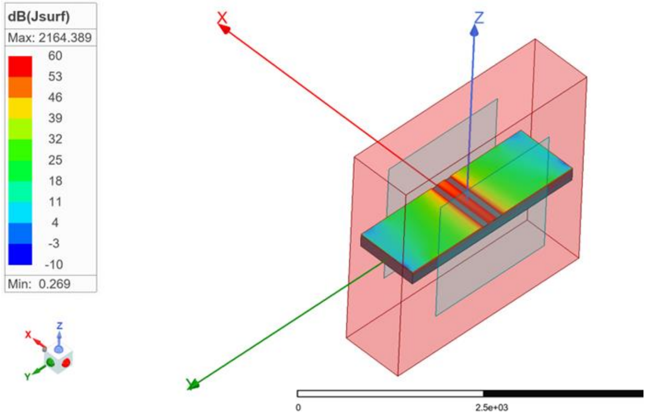
- At lower frequency (skin depth is much larger than conductor thickness) current density is almost constant in conductor so no need to mesh inside conductor

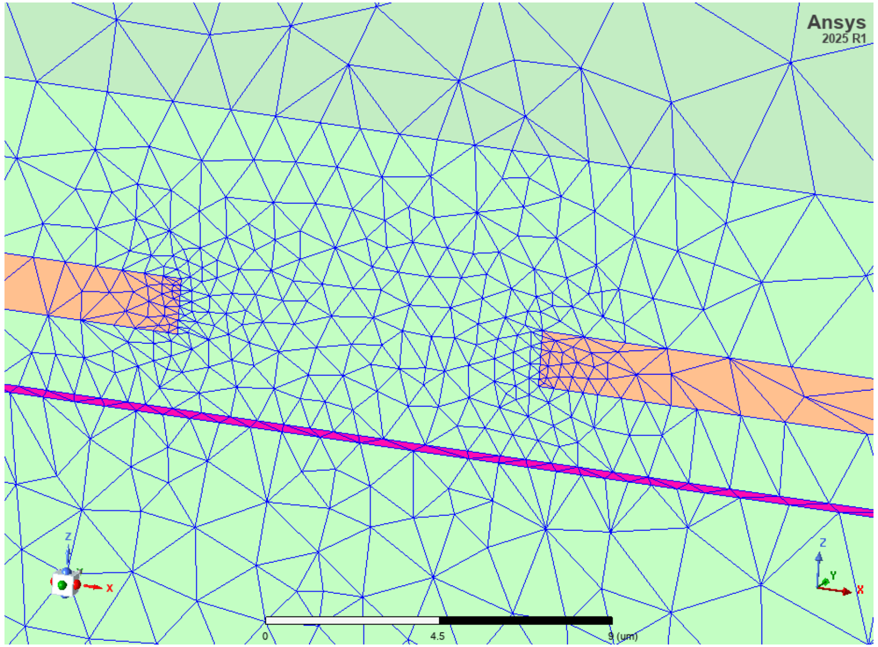
- At very higher frequencies : thickness ~ 10 deltas we can use thick metal formulation; we don’t need to mesh inside the conductor

- At intermediate frequencies (skin depth is comparable to skin depth) where delta = 0.5 um and conductor thickness = 1.5 um it becomes tricky to get conductor loss

port solution

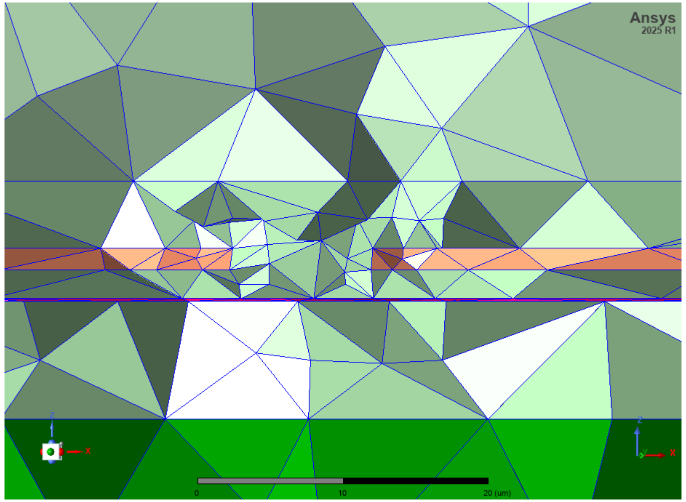
- Is very accurate because the mesh is great, and it captures the current decay very well hence capturing ohmic losses very well too





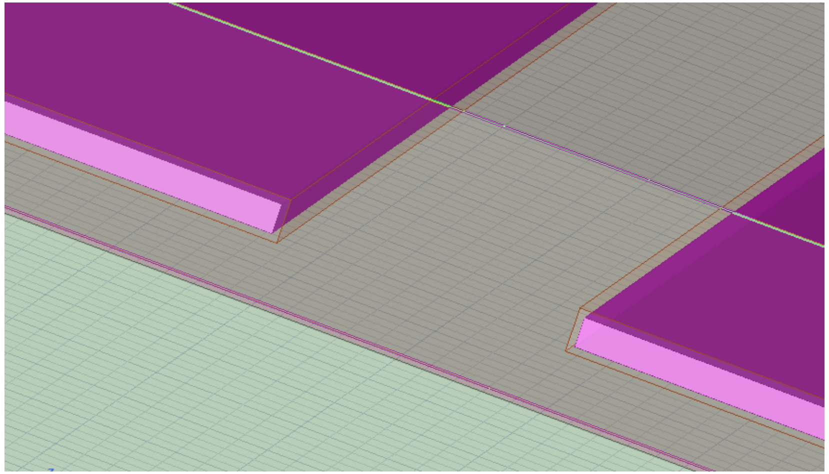
3D solution

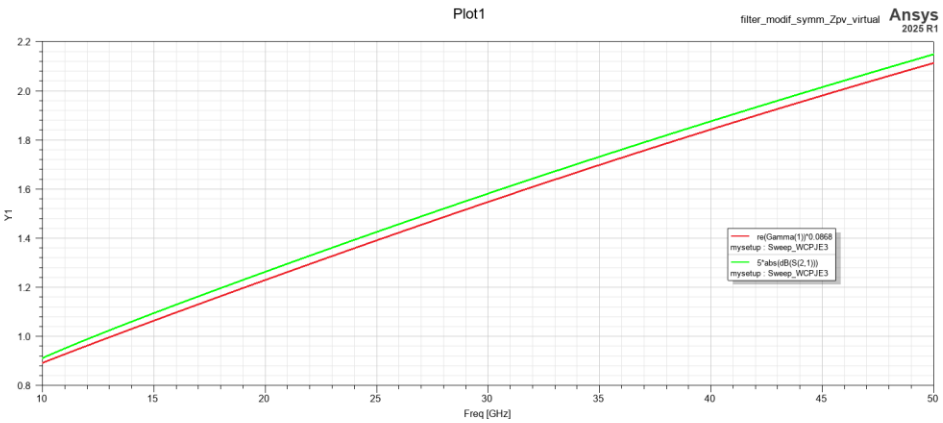
- We need to activate **solve inside** to start with
- not needed if current density in Z is constant i.e. conductor thickness is less than delta or larger than 10 deltas
- however, the internal automatic mesh is not good enough

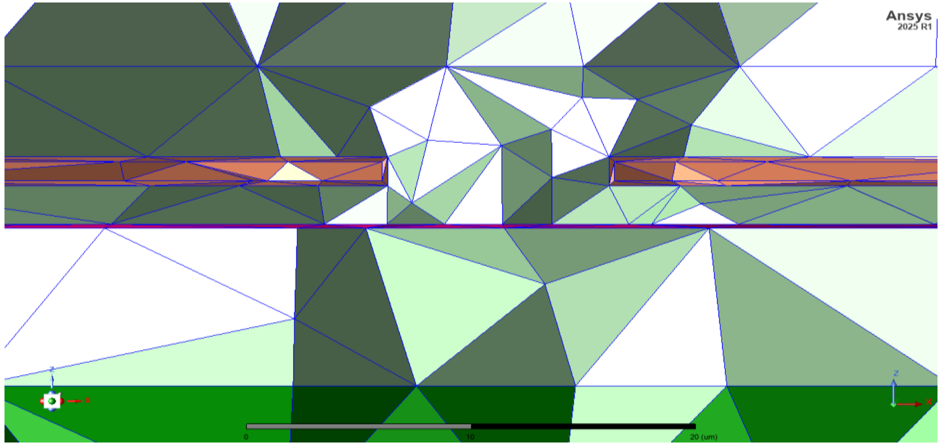


solution for 3D

- For such a corner case, you manually mesh to mesh more ***inside*** the conductor**. And do smaller frequency intervals**
- Then both curves, are almost identical







Summary

- Enormous increase in AI usage and hence need for massive datacenters
- These data centres would use opto electric interfaces to manage the huge data rates needed
- Like it or not, CPW is the interconnect of choice
- CPW is tricky, yet could still be done right both in simulation and design
- This guide has some tricks
- For any further help, please get in touch
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