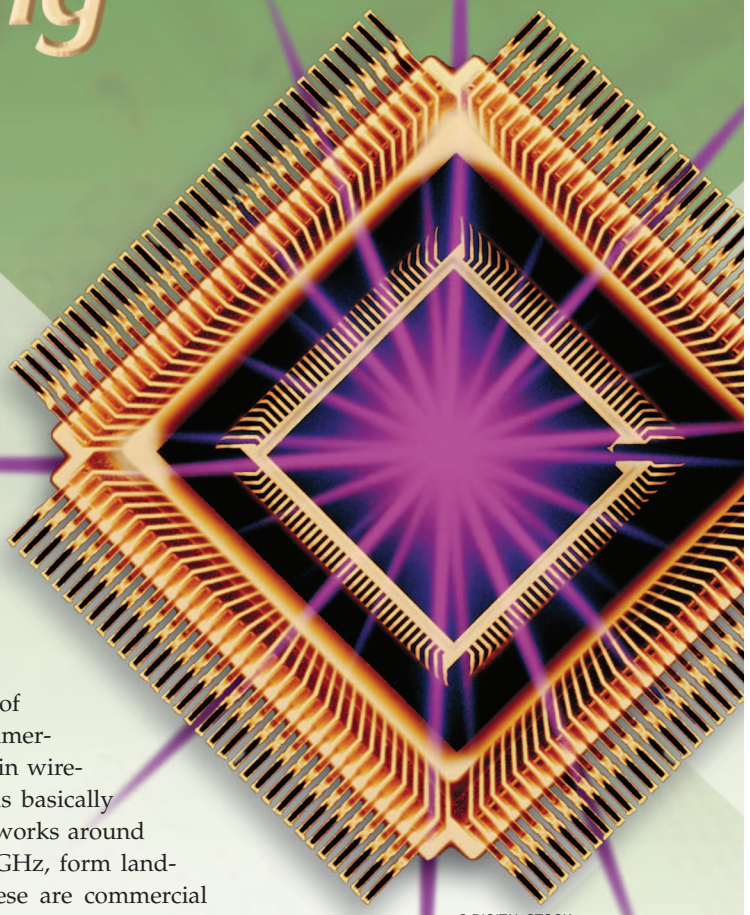
The Flip-Chip Approach for Millimeter-Wave Packaging

Wolfgang Heinrich



Until recently, the millimeter-wave frequency range has been the domain of some specialized and mostly noncommercial applications. Following the boom in wireless communications, this situation has basically changed. Broadband radio links and distribution networks around 40 GHz, as well as automotive radar systems at 77 GHz, form landmarks for new markets above 30 GHz. Because these are commercial applications, which follow the rules of the market, cost and volume have become crucial parameters for system development.

A particularly critical issue in this regard is module packaging, i.e., the way to assemble and connect several monolithic microwave integrated circuits (MMICs) in a multichip environment in order to build the millimeter-wave front-end. The requirements on the packaging scheme are obvious: the interconnects should provide good millimeter-wave performance (primarily meaning: low reflections and low insertion loss) and, at the same time, they should allow for low-cost fabrication. Among the multichip packaging techniques available, the flip-chip approach is considered to be the most promising candidate to meet these requirements.

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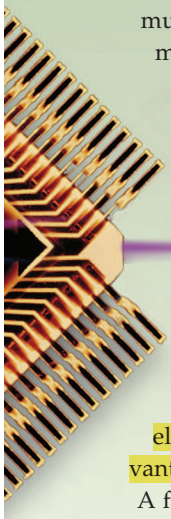
 1527-3342/05/$20.00©2005 IEEE

A similar situation is found in broadband electronics operating at 40 Gb/s and more. In contrast to the classical millimeter-wave systems, such as radio links and radars, which are essentially of the narrow-band type, high bit-rate optoelectronics demand for broadband solutions covering the entire range from almost dc to frequencies of 50 GHz and beyond. This puts constraints on the interconnect, which are much more challenging than in the conventional millimeter-wave world.



Is the flip-chip approach the solution to this demand for an interconnect, which shows low parasitics, is broadband, and cheap as well? This has been discussed now for some time, and there are a lot of arguments around. The purpose of this article is to shed some light on the technical background and to highlight the key issues. This will be done from the designer's point of view. Accordingly, the article will discuss flip-chip technology only briefly but concentrate on the electromagnetic effects and the design issues relevant for the higher gigahertz range.

A further aspect needs to be clarified before going into the details: RF module packaging commonly includes several levels of interconnects. The first level (sometimes one prefers to start counting these levels with zero) denotes the interconnect directly linked with the semiconductor chip. In many cases, the chip is mounted on an intermediate carrier substrate, which leads to a chip-scale package (CSP). These CSPs are then assembled on a multichip board, where several chips are grouped to form a multichip module (MCM). This connection between CSP and multichip boards is named the second interconnect level. There may be additional levels as well as an arrangement where the chips are mounted directly on the multichip board, which means that first and second interconnect levels merge to a single one. In order to keep the scope as general as possible and to highlight the principal effects, the following considerations focus on the first-level interconnect.

The article is organized as follows. After a brief description of the flip-chip technique and the competing approaches, the main body of results and discussions is grouped around the two key parts of any high-frequency packaging scheme: 1) the interconnect, which is of the flip-chip type in our case, and 2) the package environment in which the chip is mounted and to which it is connected. The article closes with a brief discussion of some specific topics of interest such as compatibility of the flip-chip technique with microstrip MMICs and power handling issues.

RF Flip-Chip Basics

The basic flip-chip scheme is illustrated in Figure 1. The MMIC chip is mounted upside down on a carrier substrate by using metallic bumps as interconnects. To simplify discussion, this carrier substrate will be referred to as a motherboard in the following whether it is only an intermediate carrier or a multichip board.

The flip-chip technique is well proven for lower frequencies. In fact, IBM introduced it in 1964 with its 360-mainframe generation. The process was called C4, which stands for Controlled Collapse Chip Connection. Since then, the flip-chip has found its way into mainstream electronics. In the RF field, however, it is still rarely used. This is because the conventional technique cannot be transferred to microwave frequencies simply. Bump diameter and pitch have to be shrunk, and the bump metal-composition has to be modified in order to become compatible with millimeter-wave and broadband chips. High-frequency effects add further constraints.

Regarding technology, two different methods are in use for RF flip-chip.

- *Soldering:* the bumps consist of an appropriate alloy, e.g., AuSn. The bumps are heated, they melt, and after bonding they form a mechanically stable connection between chip and board.
- *Thermocompression:* the chips are bonded applying pressure and heat simultaneously. Bumps can be deposited, for instance, by electroplating or as stud bumps by a suitable wire bonder. While the first version lends itself to high-volume production, the stud-bump method is well suited for prototyping or small lots.

As a consequence of the different bonding methods, the resulting shape of a bump after bonding differs. In the thermocompression case, the bump is squeezed while maintaining the volume, which leads to a convex shape. Figure 2 shows an example. When using the soldering variant, the shape is controlled by surface tension. The bump will assume a concave form if the height of the chip above the carrier is fixed during bonding.

Both methods, thermocompression and soldering, result in structures with similar dimensions, which do not differ significantly in terms of their electromagnetic properties. However, the soldering version is better suited for high-volume production, because soldering can be done for many chips in one step, and it provides self-alignment since the surface tension of the bumps centers the chip during the soldering step. The IBM C4 process is of the solder type as is the vast majority of classical flip-chip process versions. On the other hand,

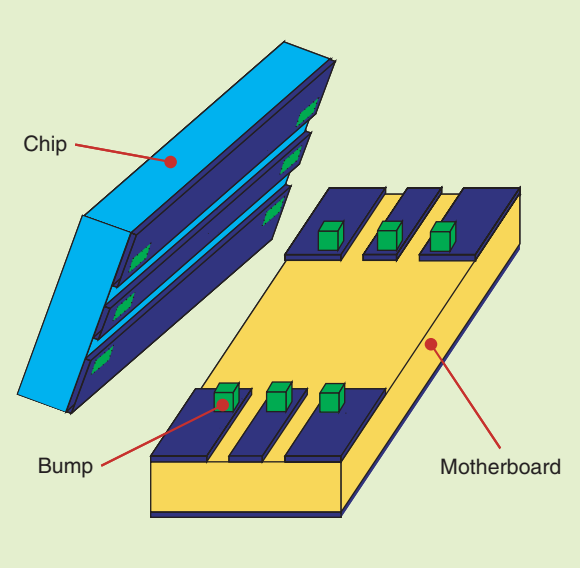


Figure 1. *The flip-chip approach: mounting a flipped chip onto a motherboard using bump interconnects (simplified coplanar geometry with thru-line on chip).*

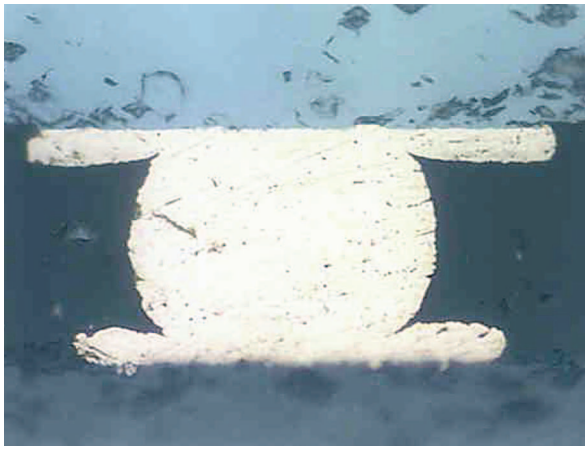


Figure 2. *Au bump after thermocompression bonding (cross-sectional view).*

solder bumps consist of an alloy, in the RF case, mostly AuSn, the thermal conductivity of which is lower than that of pure Au as used in the thermocompression process. Therefore, soldering leads to poorer thermal resistance of the bumps, which deteriorates heat-sinking capabilities.

Independent of the technology, a flip-chip interconnect looks more or less like the structure depicted in Figure 3. The most important dimension is the bump diameter (usually bumps are of approximately circular cross-section). This parameter also determines the necessary pad size as well as the possible bump height, which is limited to values slightly smaller than the diameter for technological reasons. Thus, bump diameter, height, and the size of the corresponding upper and lower pads are not independent.

Regarding the RF characteristics, the actual bump shape does not play an important role as long as the bump dimensions are small enough. For common RF bumps with diameters in the range below 100 μm, the average bump diameter and its height are sufficient for electrical description.

What Makes Flip-Chip Attractive

From the electrical point of view, the flip-chip interconnect has two distinct advantages.

1) It is small in terms of dimensions as well as electrical size.
2) Its relevant parameters can be well controlled.

Common bump diameters are in the 20–80-μm range. They can be realized with good control of height and average diameter, which results in an electrically small interconnect and a module with reproducible performance. Figure 4 presents a schematic view. Note that both horizontal alignment of the chip as well as vertical positioning, i.e., the bump height, which denotes the distance between chip and motherboard, can be controlled accurately within some tens of microns or less.

Due to its small dimensions, the flip-chip interconnect differs significantly from the classical mounting technique using wire bonding, where the bond wire causes a relatively large parasitic inductance. Moreover, wire length and, particularly, spacing between chips or chip and motherboard (see Figure 5) give rise to high tolerances in the electrical characteristics, which become more important at higher frequencies of operation.

A further alternative in microwave packaging is to embed the chips into a carrier substrate and to connect them by thin-film transmission lines. This leads to interconnect structures smaller than wire bonds and with better control of impedance. Figure 6 explains the basic idea. However, the gap between the chip and the motherboard (green section in Figure 6) causes trouble because of the impedance mismatch. This gap is relatively large, with significant variations, because the

outer dimensions of a chip result from dicing and are not usually well controlled. This makes it difficult to fabricate well-defined thin-film structures with small dimensions bridging the gap, as required for an impedance-matched millimeter-wave interconnect. The flip-chip concept offers inherently smaller interconnects and better control of the dimensions. These benefits make flip-chip an attractive candidate for high-performance, high-frequency, and broadband modules.

But, this is not the whole story. Besides the electrical aspects, there are two further important issues to be accounted for.

- The thermal characteristics, which comprise both heatsinking of the chip, i.e., question of which value thermal resistance can be realized with a flip-chip assembly, and the mismatch in thermal expansion coefficient (CTE mismatch) between chip and carrier substrate. The CTE mismatch becomes critical during thermal cycling and determines reliability.

  While heatsinking properties can be improved by adding thermal bumps, which have only a thermal and no electrical function, the CTE mismatch can be avoided by a careful selection of the substrate materials used. Also, an underfiller can be applied, which distributes the shear forces, thus protecting the bump interconnects. Experience from flip-chip assemblies at lower frequencies shows that underfiller greatly improves reliability.
- Last, but most important, manufacturability and cost.

We will not elaborate on these issues in the following since this article focuses on electrical aspects. Accordingly, the next sections are devoted to the electromagnetic characteristics. In a first part, the flip-chip interconnect is studied, followed by considerations on the package environment.

The Flip-Chip Interconnect

The flip-chip interconnect influences RF behavior in a threefold way:

- detuning of the chip
- reflections and insertion loss at the interconnect
- excitation of parasitic modes.

These three effects will be treated in detail in the following subsections.

Chip Detuning

Flip-chip mounting the chip brings the motherboard or carrier substrate in close vicinity to the active surface of the chip, separated only by an air gap as thick as the bump height. This can significantly influence the electrical properties of the chip, an effect called detuning. The circuit elements on the chip may change their electrical characteristics due to the presence of the carrier substrate, which, for example, can shift the frequency of an oscillator away from its specified value due to dielectric loading. Figure 7 illustrates the relevant cross-sections for both coplanar and microstrip chips.

The actual amount of detuning depends on the element type and size and the spacing between chip and substrate, which is controlled by the bump height. Large bump heights minimize detuning. Particularly sensitive to detuning effects are transmission lines and spiral inductors, while transistors and small-sized components do not show a noticeable influence.

The flip-chip technique is well proven for lower frequences.

Figure 8 shows quantitative data for typical 50-Ω transmissions lines in the coplanar and microstrip case. The curves refer to a frequency of 50 GHz, but the results do not change significantly within the range up to 100 GHz. Overall, the necessary minimum bump heights h are quite small. Allowing for 1% of maximum deviation in either beta or impedance bump heights down to 15 μm in the coplanar and 50 μm in the microstrip case can be tolerated. One should note that the coplanar data refer to a motherboard without metalization on the surface [see Figure 7(a)]. Otherwise,

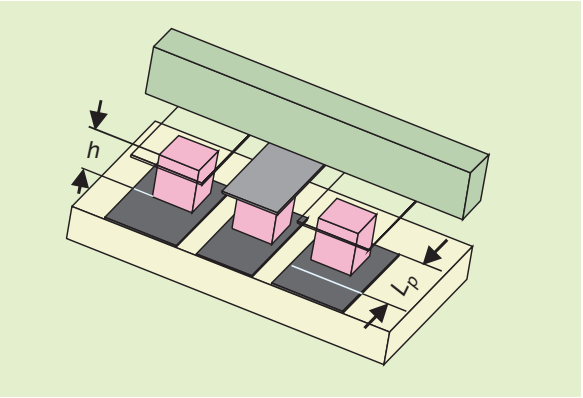


Figure 3. *The flip-chip interconnect and its most important dimensions: bump height h, pad size L_P, and bump diameter d (whether the bumps have circular or rectangular cross section does not influence electrical characteristics significantly).*

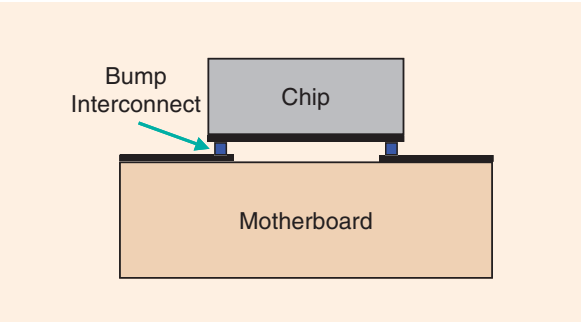


Figure 4. *The flip-chip structure (cross section).*

detuning is significantly increased, and parasitic parallel-plate moding in the gap between chip and motherboard occurs.

A more detailed study yields the following minimum values for bump height h given the typical chip environments:

The interconnects should provide good millimeter-wave performance and should allow for low-cost fabrication as well.

- half the chip-substrate thickness for GaAs microstrip chips; e.g., 50 μm for 100-μm thick chips
- 30% the ground-to-ground spacing for coplanar chips, e.g., 15 μm for a 50-μm wide coplanar waveguide (CPW)
- down to 10 μm for the typical millimeter-wave Si chips with thin-film microstrip lines.

Using an underfiller, of course, the detuning effect is more pronounced since then the dielectric material is in direct contact with the chip surface. One can tackle this problem by including the detuning in chip design a priori or by having a relatively thick dielectric layer (e.g., BCB) on top of the chip so that the influence of the underfiller is more or less negligible.

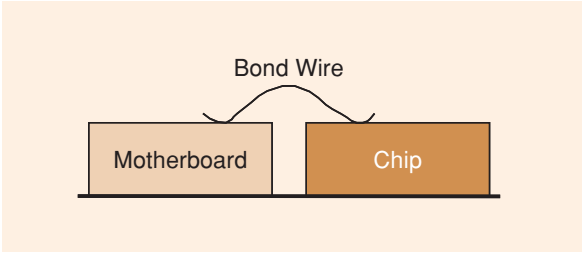


Figure 5. *The classical technique: chip interconnect using bond wire.*

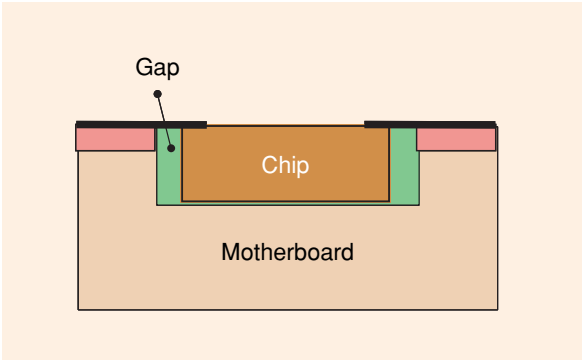


Figure 6. *An example of the packaging approach using embedded chips and thin-film interconnect.*

Reflections and Insertion Loss at the Interconnect

In the ideal case, the interconnect should be transparent to the electrical signals. In reality, however, each interconnect causes reflections. The generic flip-chip interconnect is shown in Figure 3. As mentioned earlier, the bump cross-section does not play an important role for electrical characteristics and is assumed to be of rectangular shape here. The feeding transmission lines are coplanar both on the chip and on the motherboard. Simulation results on the reflection factor S_{11} at a typical flip-chip interconnect with 80-μm bumps is plotted in Figures 9 and 10. These data as well as the other simulation data in the following figures were obtained by using the finite-difference method in frequency domain (FDFD). The code was developed at the Ferdinand-Braun-Institut für Höchstfrequenztechnik (FBH) and has been in routine use with packaging problems for many years (e.g., [1], [5], [6]).

In Figure 9, the bump height is varied, and in Figure 10, the influence of pad size is studied. Generally, one finds that reflections are relatively low, given the broad frequency range and the fact that the raw interconnect without any optimization is treated. For the 80-μm pad, reflections remain below -10 dB up to 100 GHz.

Furthermore, as can be seen from Figures 9 and 10, increasing bump height from 20 to 100 μm causes only negligible deviations in $|S_{11}|$, while varying pad size only from 80 to 110 μm leads to significant changes in reflection. Thus, it is not the bump height which determines reflection to first order but the bump-pad size. The pads on the motherboard and on the chip (or the overlap of the two metalizations when referring to Figure 3) cause dielectric loading of the transition, which can be identified as the main source of reflections. One concludes as a first step that the pads have to be kept as small as possible in order to achieve a maximum of return loss at the interconnect. In practice, this lower limit of pad size is given by the bump diameter plus the margin required for bump placement and bonding. Bump height, on the other hand, is important only with regard to the detuning effects.

But the reflection values in Figures 9 and 10 do not represent the limiting performance. The resulting return loss can be considerably improved by layout optimization and suitable compensation techniques, which are well known from wire-bonding structures. Already simple compensation measures yield excellent broadband behavior over tens of gigahertz.

Excitation of Parasitic Modes

Low reflections at the interconnect and low insertion loss are necessary for good high-frequency characteristics but are not at all sufficient. It is not only the bump transition that determines millimeter-wave characteristics but also the transmission-line environments on

chip and motherboard that play an important role. For the chip, this refers to the decision between microstrip and coplanar. On the motherboard side, a variety of solutions are available, from the conventional ceramics substrate to low-temperature cofired ceramics (LTCC) substrates with multilevel wiring or thin-film transmission lines.

A critical issue is substrate moding, i.e., the existence of parasitic modes in the chip and particularly in the motherboard substrate. These modes cause crosstalk between different interconnects and housing feedthroughs of a module, which reduces isolation and degrades the stability of amplifiers. Naturally, this is especially important when dealing with high-gain units.

As an example, Figure 11 presents a simple flip-chip configuration with a conductor-backed CPW on the motherboard. Note that such a conductor backing is the standard situation in any metallic housing, even if the substrate itself does not contain a metalized backside. This configuration supports not only the desired CPW mode but also parasitic parallel-plate (PPL) mode, the fields of which resemble the parallel-plate case and are concentrated in the motherboard substrate between the upper- and lower-ground metalization. In other words, they represent the floating potential between the two ground metalizations on the front and back side of the motherboard.

In Figure 12, the coupling coefficients between the coplanar and the PPL wave modes are plotted against frequency. One should note that they are all in the range between −20 and −30 dB, which is the same order of magnitude as the reflection factor. Moreover, this means that the maximum isolation between two interconnects is about twice this value, i.e., 40–60 dB. This gives an idea which isolation levels, and, consequently, which stable gain values, can be realized in such a module without further measures. And it makes clear that careful design of the entire structure, including the motherboard and housing, not only the interconnect, is mandatory to achieve a proper package.

Interconnect Modeling and Optimization

Basically, a flip-chip interconnect has both an inductive and a capacitive contribution (see Figure 13). The fringing of the current from the motherboard surface to the chip causes an inductive effect. Also, the bumps form a short vertical transmission-line section consisting of the three bumps (one signal and two ground ones). This transmission line is embedded in air or a low-ε_r dielectric, which yields a relatively high characteristic impedance, which can be understood as an inductive contribution. On the other hand, the interconnect section with the pads, which connects both motherboard and chip substrates, causes dielectric loading and, consequently, adds capacitance.

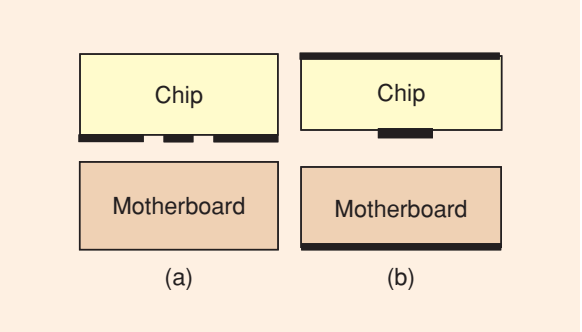


Figure 7. *Detuning: how the presence of the motherboard changes the transmission-line cross section for (a) coplanar and (b) microstrip chips.*

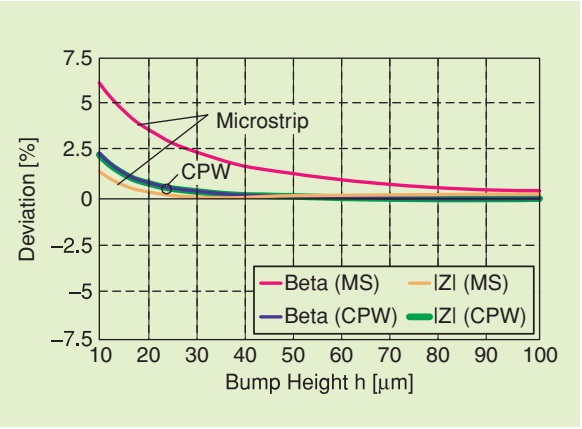


Figure 8. *Detuning: percentage deviation of phase constant beta and characteristic impedance as a function of bump height for a 50-Ω coplanar and microstrip transmission line at 50 GHz (100-μm thick GaAs chip on 254-μm thick conductor-backed Al_2O_3 motherboard, see Figure 7; CPW with 20-μm center conductor and 50-μm ground-to-ground spacing; microstrip with 72-μm strip width).*

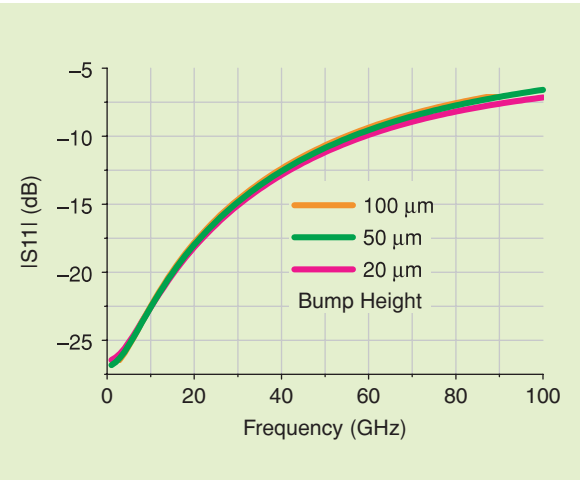


Figure 9. *Influence of bump height (80-μm bumps, 100-μm pad size): reflections at the flip-chip interconnect against frequency with bump height as parameter (em simulation data, FDFD).*

Since both contributions are present, the question is which one, if any, is dominating the characteristics. We found that for the typical millimeter-wave geometries, it is, in almost any case, capacitance that exceeds the inductive part and governs the behavior. Thus, a first-order equivalent circuit description of the flip-chip interconnect should consist of a shunt capacitance. For small bump heights, and, thus, small parasitics, this type of model holds with good accuracy up to W-band frequencies.

Moving to flip-chip requires some basic changes, which will be implemented only if the prospective benefits are high enough.

This finding also enables one to develop optimized layouts for the flip-chip interconnect applying the well-known compensation methods: since one is dealing with a capacitive discontinuity, the reflections can be reduced by adding inductance at the interconnect. This can be realized by a short inductive line section next to the bump transition or by simply modifying the pad layout so that it becomes less capacitive. Such measures might require some additional space so it is recommended to place the structures not on the chip, where real estate is expensive, but on the motherboard. Our investigations show that, in many cases, quite simple layout changes yield excellent results, as will become clear also in the following section.

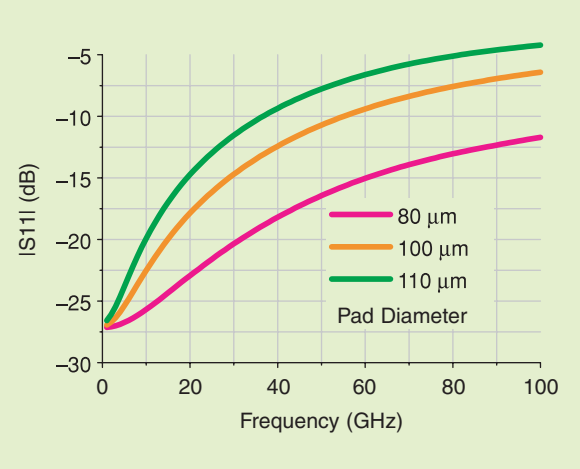


Figure 10. *Influence of pad size (80-µm bump height, 100-µm pad size): reflections at the flip-chip interconnect against frequency with pad size as parameter (em simulation data, FDFD).*

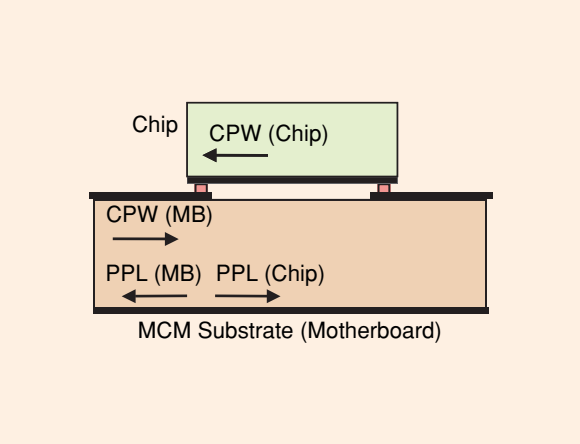


Figure 11. *Basic structure of a chip flip-chip mounted on a motherboard with a conducting backside and the corresponding wave modes present at the interconnect: incident CPW modes on motherboard (MB) and chip excite parallel-plate (PPL) modes in the motherboard substrate in two directions (MB and chip, respectively).*

Measurement Verification

As an example of broadband performance, Figure 14 provides measured data of several samples of a passive flip-chip test structure. It consists of a GaAs chip with a coplanar thru-line and an Al_2O_3 motherboard with coplanar feeding lines and pads for on-wafer measurements. The flip-chip process used electroplated bumps together with thermocompression bonding, the resulting bump diameter is about 25 µm (see Figure 2 for a cross-sectional view). The layout of the interconnect was optimized by increasing the gaps of the coplanar line at the bumps, thus adding inductance (see inset of Figure 14). The test structures are measured up to 110 GHz. For the back-to-back configuration with two interconnects, one obtains a return loss beyond 20-dB broadband from dc to 80 GHz [1]. Also, the scattering of measured data over the different samples is impressively low,

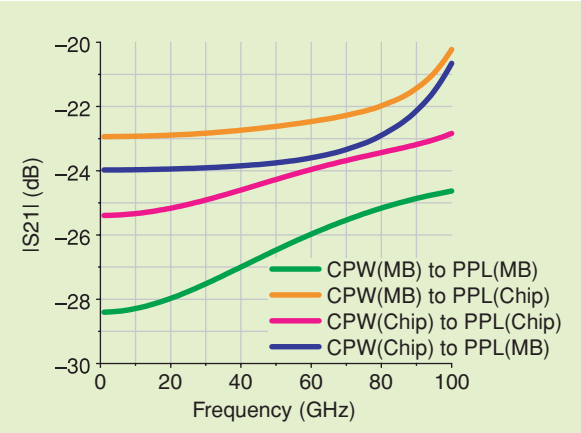


Figure 12. *Excitation of substrate modes (structure according to Figure 11): transmission coefficients S_{21} from CPW modes into the PPL modes as a function of frequency (for mode definitions see Figure 11, bump diameter 30 µm, bump height 20 µm, pad size 50 µm, em simulation data).*

which is due to the small dimensions of the bump interconnect and the good control of the critical parameters, such as bump height.

In the case shown in Figure 14, relatively small bumps with 25-μm diameter are used. However, similar results can be achieved for larger bump diameters in the range 50–80 μm when applying appropriate compensation techniques. The resulting bandwidth then still spans 20–30 GHz, which is sufficient for most applications. Published data (e.g., [2]–[5]) supports the excellent performance of flip-chip-mounted chips up to W-band frequencies.

Some Specific Topics

After having looked into the basic characteristics of a flip-chip interconnect, in the final part of this article we will now broaden the scope and discuss some specific topics of interest. Three issues will be addressed: flip-chip and thin-film, flip-chip and microstrip chips, and flip-chip for power modules.

Flip-Chip and Thin-Film

Flip-chip is a surface-oriented interconnect, which works best with surface-oriented transmission lines on both chip and motherboard, as coplanar lines are. However, coplanar lines are not the only type of surface-oriented transmission lines in use. The thin-film microstrip line, for instance, belongs to this category as well, with both ground and signal conductors being realized on top of the substrate, separated by a thin dielectric layer (see Figure 15 for a principal sketch view). Such a line structure is ideally suited for high-speed silicon processes, which provide a stack of metal wiring-layers separated by a SiO or SiN dielectric, on top of the low-resistivity substrate. More generally, almost any chip design on low-resistivity semiconductor material uses a surface-oriented line environment and, thus, is well compatible with flip-chip. Hence, one may conclude that the entire silicon IC world works well with flip-chip.

Flip-Chip and Microstrip Chips

The majority of today's ICs for the microwave and millimeter-wave frequency range is realized on GaAs as a microstrip chip. This makes implementation of a flip-chip assembly more difficult than in the coplanar case since flip-chip is surface oriented, and, in a microstrip environment, vias have to be introduced to provide the ground connection.

But one can avoid this by modifying the flip-chip scheme. The result is the so-called hot-via structure (see Figure 16), where the microstrip chip is mounted face-up with the interconnect at the backside. One needs a via to connect the signal conductor, which led to the name "hot-via" (e.g., [6]). The resulting structure is similar to that of the so-called direct-backside interconnect technology [7].

The hot-via version is well compatible with a microstrip chip environment. Moreover, because the chip is in an upright position, it can be inspected optically after mounting, and the backside metalization prevents detuning. There are two main drawbacks compared to the conventional flip-chip approach.

The flip-chip technique is well proven for lower frequencies.

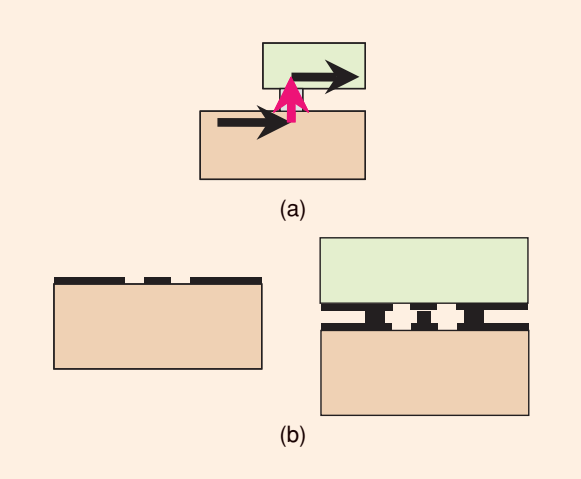


Figure 13. *Inductive and capacitive contributions at a flip-chip interconnect. (a) inductive effect due to changes in current flow. (b) capacitive effect: transmission-line section on chip or motherboard (left) and interconnect part with dielectric loading (right).*

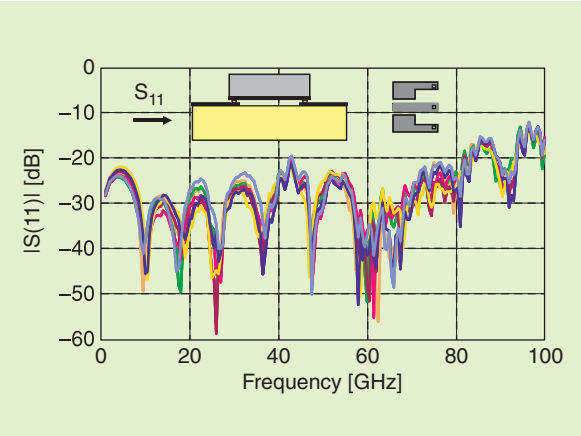


Figure 14. *Excellent broadband performance with 25-μm bumps (measurements of a back-to-back structure as shown involving two interconnects and a coplanar thru-line on the chip; the data of seven samples is plotted, the interconnect is compensated by reducing capacitance in the transmission-line section next to the bumps—see inset).*

- Backside metalization needs to be structured to form the opening and the pad for the signal bump. This requires some effort, but is not a great issue since usually backside metal is structured anyway to free the dicing streets from metalization.

Interconnects should provide good millimeter-wave performance and should allow for low-cost fabrication as well.

- Due to the via in the signal path, parasitics of the interconnect are higher than for the conventional coplanar flip-chip interconnect. In our experience, the frequency limit for the typical dimensions and materials can be extended to frequencies beyond 60 GHz when sacrificing bandwidth.

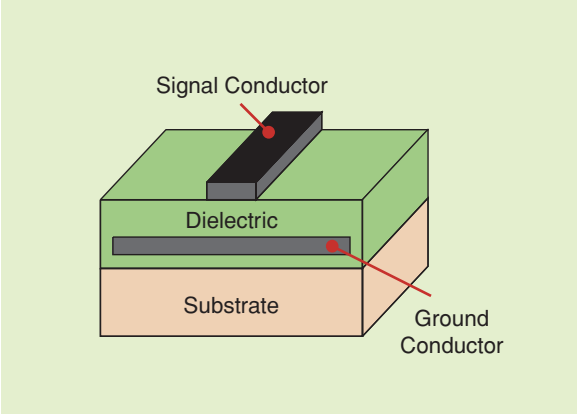


Figure 15. *The thin-film microstrip line (TFMSL): both signal and ground conductors are realized on top of the substrate (e.g., silicon); a thin dielectric layer stack, e.g., formed by oxides or polyimide, supports the microstrip transmission-line structure.*

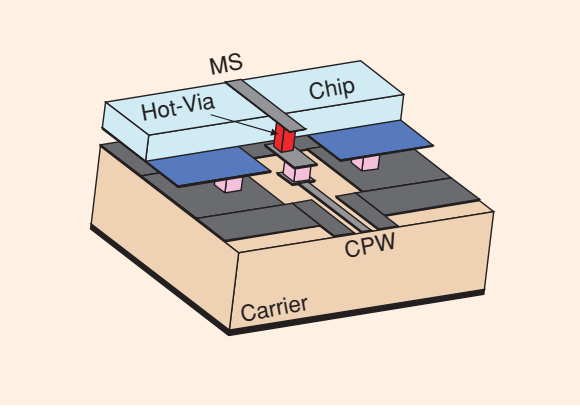


Figure 16. *The so-called hot-via approach (chip is mounted face-up, MS denotes microstrip, CPW).*

Flip-Chip for Power Modules

What is special about power modules is the heat-sinking issue. Of course, it may also play an important role in other applications, e.g., in high-speed dividers dissipating powers in the order of 1-W per chip.

Commonly, heat sinking is performed through the chip backside. In the flip-chip case, this is not possible because the backside of the flipped chip is free. Thus, heat has to be removed from the front-side. For this purpose, thermal bumps can be used, placed near the heat sources. Such bumps do not have electrical functions but act only as heat sink to the motherboard surface. This, of course, is a very effective means, because it removes the heat at the point where it is generated, i.e., near the device at the front-side of the chip.

In addition, when placing thermal bumps, one has to realize a good heat path from the motherboard surface through the substrate to the backside, which is mostly in direct contact with the base plate of the housing. This can be achieved by choosing a substrate with good thermal conductivity, such as AlN or even diamond, by inserting metal blocks beneath the chip, or by employing via arrays that act similarly to a solid metal block, both thermally and electrically (see Figure 17).

One should note at this point that, for substrates with low thermal conductivity, such as GaAs, flip-chip even offers advantages in heat sinking (for practical examples, see [8]–[10]). However, there is still some work to do to have flip-chip power modules fully developed. Looking into the present practical realizations, one finds that an overwhelming majority use backside mounting.

Conclusions

Despite the advantages of flip-chip, at present, the major part of millimeter-wave and broadband

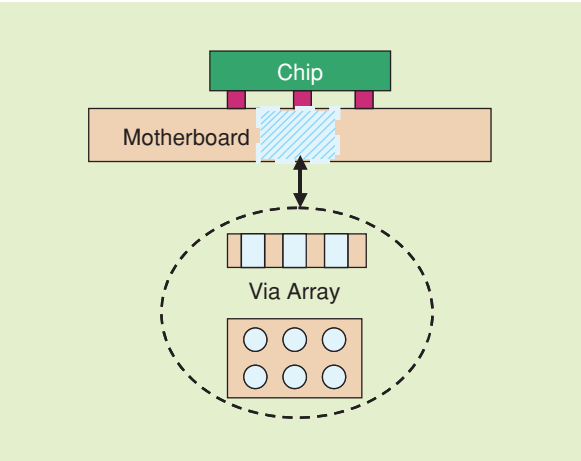


Figure 17. *Heat sinking through the motherboard and electrical grounding using a via array, which acts similar to a solid metal block.*

modules is still packaged using backside mounting, wire bonding, and related approaches. What are the reasons? First of all, wire bonding is the classical solution, well proven in production and well known by many designers. Moving to flip-chip requires some basic changes, which will be implemented only if the prospective benefits are high enough. The main road blocks are:

- There are still many open questions about flip-chip for which research results are available but which still await final answers, taking into account a realistic production environment, e.g., whether to use thermocompression or soldering, which underfiller material (if any) should be used, which motherboard-substrate materials give best cost-performance trade off, what about reliability, and what is the final cost advantage. Moreover, the answers differ depending on the individual specifications. A solution well suited for power modules will probably not work with high-gain, small-signal applications and vice versa. This lack of experience and proven design data requires additional efforts before embarking on a specific approach.
- Today, the bulk of the commercial chips for millimeter-wave frequencies are GaAs microstrip MMICs. A decision to use flip-chip implies a basic change in design strategies as well, moving towards coplanar or related concepts. For most companies, this requires building up a new knowledge base, which is risky and costly.
- At the foundry side, introducing flip-chip requires the addition of a bump fabrication step to the process flow on the wafer level. Otherwise, the efforts for handling diced chips and for aligning the bumps to the layout are too high. So, in a flip-chip world, foundries are to provide bumped chips—an extended service, which will be offered only if the demand is large enough. And, at this point, one encounters the chicken-and-egg problem.

What will be the future? Flip-chip clearly offers excellent potential in realizing high-frequency interconnects at moderate processing efforts. Hence, for high-performance circuits, such as broadband modules, the flip-chip technique is a must. Furthermore, the increasing market share of millimeter-wave Si chips with their surface-oriented wiring will exert a push towards flip-chip equally. The same is true for high pin-count digital ICs, which demand flip-chip mounting with miniaturized bump interconnects not because of their high-frequency properties but because of the necessity to accommodate a large number of interconnects on a given chip size.

Flip-chip clearly offers excellent potential in realizing high-frequency interconnects at moderate processing efforts.

So, this author expects to see more and more flip-chip solutions. On the other hand, there will not be a single flip-chip approach but many different versions adapted to fit the special needs. Some of them may even come without the classical bump, as surface-mount device-like approaches.

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