

Started on Wednesday, 6 April 2022, 12:10 PM

State Finished

Completed on Wednesday, 6 April 2022, 12:14 PM

Time taken 4 mins 14 secs

Marks 3.00/4.00

Grade 7.50 out of 10.00 (75%)

Question 1

Complete

Mark 1.00 out of 1.00

Dynamic pipeline scheduling chooses which instructions to execute next, possibly reordering them to avoid stalls?

- a. Branch prediction
- b. Dynamic pipeline
- c. Prediction branch
- d. Dynamic branch prediction

Question 2

Complete

Mark 0.00 out of 1.00

For Dynamic Scheduling, select the correct option.

- a. The hardware determines the order in which instructions execute
- b. The DMA determines the order in which instructions execute
- c. The software determines the order in which instructions execute
- d. None of the mentioned

Question 3

Complete

Mark 1.00 out of 1.00

Consider the following code:**CODE:****Load R1,Loc1; Load R1 from memory location Loc1****Load R2,Loc2; Load R2 from memory location Loc2****Add R1,R2,R1; Add R1 and R2 and save result in R1****Dec R2; Decrement R2****Dec R1; Decrement R1****Mpy R1,R2,R3; Multiply R1 and R2 and store in R3****Store R3, Loc3; Store r3 in Memory Location Loc3****What is the number of cycles needed to execute the above code assuming each instruction takes one cycle to execute?**

- a. 10
- b. 9
- c. 5
- d. 7

Question 4

Complete

Mark 1.00 out of 1.00

For the Software Pipelining, select the correct option.

- a. select order of instructions from different iterations to pipeline
- b. All of the mentioned
- c. unroll loop body with an unroll factor of n
- d. "paste" instructions from different iterations into the new pipelined loop body

[◀ CS-208 MidSem Online Test-11-03-2022](#)

Jump to...

[CS-208-Assessment-4_13-04-2022 ►](#)

Started on Wednesday, 13 April 2022, 12:11 PM

State Finished

Completed on Wednesday, 13 April 2022, 12:15 PM

Time taken 3 mins 5 secs

Marks 3.00/4.00

Grade 7.50 out of 10.00 (75%)

Question 1

Complete

Mark 1.00 out of 1.00

Which of the following processor uses static in nature?

a. Superscalar(speculative)

b. VLIW/LIW

c. Superscalar(static)

d. Superscalar(dynamic)

Question 2

Complete

Mark 1.00 out of 1.00

Which of the following processor uses Dynamic in nature

a. Superscalar(dynamic)

b. All of the mentioned

c. Superscalar(speculative)

d. Superscalar(static)

Question 3

Complete

Mark 1.00 out of 1.00

Which of the following processor uses primarily static in nature?

- a. Superscalar(static)
- b. Superscalar(dynamic)
- c. EPIC
- d. Superscalar(speculative)

Question 4

Complete

Mark 0.00 out of 1.00

The tightly coupled set of thread execution working on a single task is as?

- a. Multiprocess
- b. Parallel Processing
- c. Serial Processing
- d. Multithread

[◀ CS-208-Assignment-3_06-04-2022](#)

Jump to...

[CS-208-Assignment-5_20-04-2022 ►](#)

Started on Wednesday, 20 April 2022, 12:10 PM

State Finished

Completed on Wednesday, 20 April 2022, 12:15 PM

Time taken 4 mins 54 secs

Marks 4.00/5.00

Grade 8.00 out of 10.00 (80%)

Question 1

Complete

Mark 1.00 out of 1.00

For virtual memory address translation, select the correct option.

- a. Hardware converts virtual addresses to virtual addresses and OS-managed lookup table
- b. Hardware converts virtual addresses to physical addresses and OS-managed lookup table
- c. Hardware converts physical addresses to virtual addresses and OS-managed lookup table
- d. None of the mentioned

Question 2

Complete

Mark 1.00 out of 1.00

For the Virtual Memory Design Issues, select the right option.

- a. All of the mentioned
- b. Page faults need not be handled by hardware
- c. Write through approach cannot be used
- d. Page size should be large enough to try to amortize the high access time

Question 3

Complete

Mark 1.00 out of 1.00

Making Address Translation Faster, Choose the correct option.

- a. Each memory access requires two memory reads
- b. All of the mentioned
- c. A special address translation cache called Translation Lookaside is required
- d. The page tables are stored in the main memory

Question 4

Complete

Mark 1.00 out of 1.00

For 32 bit data/4 blocks, 32 bit address is given for the CACHE of 32 KB(data part only). Calculate the size of the CACHE?

- a. None of the mentioned
- b. 314 KB
- c. 316 KB
- d. 314 B

Question 5

Complete

Mark 0.00 out of 1.00

What is miss penalty for the parameters given below.

1. One clock to send the address.
- 2.10 clocks for each DRAM access.
- 3.1 clock for send the memory word to CACHE from DRAM.
4. CACHE width is 4W and DRAM width is 1W

- a. 46 Clock Cycles
- b. 45 Clock Cycles
- c. None of the mentioned
- d. 44 Clock Cycles

Jump to...

Started on Friday, 18 February 2022, 1:55 PM

State Finished

Completed on Friday, 18 February 2022, 2:02 PM

Time taken 7 mins 9 secs

Marks 5.00/5.00

Grade **10.00** out of 10.00 (**100%**)

Question **1**

Complete

Mark 1.00 out of 1.00

The two numbers given below are multiplied using Booth's algorithm.

Multiplicand : 0101 1010 1110 1110

Multiplier: 0111 0111 1011 1101

How many additions/Subtractions are required for ?

- a. **3 subtractions and 4 additions**
- b. **4 subtractions and 4 additions**
- c. **4 subtractions and 3 additions**
- d. **3 subtractions and 3 additions**

Question **2**

Complete

Mark 1.00 out of 1.00

When both integer are +ve i.e. (+ve) x (+ve) = (+ve) and Multiply 7 with 3 and register size is 4 bit. Choose the correct option?

- a. 4 Cycles are required to complete the multiplication
- b. 3 Cycles are required to complete the multiplication
- c. 5 Cycles are required to complete the multiplication
- d. 7 Cycles are required to complete the multiplication

Question 3

Complete

Mark 1.00 out of 1.00

Using Booth's Algorithm for multiplication, the multiplier -57 will be recorded as? a. **0 -1 0 0 1 1 1 -1** b. **None of the mentioned** c. **0 -1 0 0 1 0 0 -1** d. **0 -1 0 0 1 0 1 -1****Question 4**

Complete

Mark 1.00 out of 1.00

for B= 0 0 0 1 1 1 0 0 0 1 1 what will be the arithmetic shift right ?

 a. 0 0 0 0 1 1 1 0 0 0 0 0 b. 0 0 0 0 1 1 1 0 0 0 1 c. 1 0 0 0 1 1 1 0 0 0 1 d. **0 0 0 1 1 1 1 0 0 0 1****Question 5**

Complete

Mark 1.00 out of 1.00

For A= 0 0 1 0 1 0 1 0 0 what will be arithmetic shift right ?

 a. A= 0 1 1 1 0 1 0 1 0 b. A= 0 0 0 1 0 1 0 1 0 c. A= 1 1 1 1 0 1 0 1 1 d. A= 0 0 0 1 0 1 0 0 0

[◀ Assignment 1-18-02-2022](#)

Jump to...

[Assignment 3-25-02-2022 ►](#)

Started on Friday, 25 February 2022, 1:50 PM

State Finished

Completed on Friday, 25 February 2022, 1:56 PM

Time taken 5 mins 41 secs

Marks 4.00/4.00

Grade **10.00** out of 10.00 (**100%**)

Question 1

Complete

Mark 1.00 out of 1.00

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using full adders. What is the total propagation time of this 4-bit binary adder in microseconds.

a. **19.5 ms**

b. **19.8 ms**

c. **19.2 ms**

d. **20 ms**

Question 2

Complete

Mark 1.00 out of 1.00

What is true for the look ahead carry adder?

- a. All of the mentioned
- b. To reduce the computation time, there are faster ways to add two binary numbers by using carry lookahead adders
- c. The carry propagator is propagated to the next level whereas the carry generator is used to generate the output carry ,regardless of input carry.
- d. They work by creating two signals P and G known to be Carry Propagator and Carry Generator.

Question 3

Complete

Mark 1.00 out of 1.00

Two 1's with a carry-in of 1 are added using a ripple carry adder. What are the outputs?

- a. 0,1
- b. 0,0
- c. 1,0
- d. 1,1

Question 4

Complete

Mark 1.00 out of 1.00

For $X = (A \oplus B) C + (A \oplus B) C$ & $Y = AB + (A \oplus B) C$, choose the correct option.

- a. None of the mentioned
- b. Are the expressions for the Full subtractor
- c. Are the expressions for the carry look ahead adder
- d. Are the expressions for the ripple carry adder

[◀ Assignment 2-18-02-2022](#)

Jump to...

[Assignment 4-04-03-2022 ►](#)

Started on Friday, 4 March 2022, 1:50 PM**State** Finished**Completed on** Friday, 4 March 2022, 1:55 PM**Time taken** 5 mins 41 secs**Marks** 3.00/5.00**Grade** **6.00** out of 10.00 (**60%**)**Question 1**

Complete

Mark 1.00 out of 1.00

For the of RISC pipeline. Choose the correct option.

- a. All operands are in registers
- b. All of the mentioned
- c. all instructions are the same size
- d. The only operations that affect memory are loads and stores

Question 2

Complete

Mark 1.00 out of 1.00

For Implementing Instruction Pipeline ?

- a. Cycle time is determined by the longest stage
- b. None of the mentioned
- c. Cycle time does not dependent on stages of the pipeline
- d. Cycle time is determined by the smallest stage

Question 3

Complete

Mark 0.00 out of 1.00

For the single instruction pipeline (code given below). The two stalls are provided as a part of the program. Choose the correct option?

Begin: add t0, t1, t2

nop

nop

.end Begin

- a. For the given program two more stalls are required
- b. For the given program one more stall is required
- c. For the given program three more stalls are required
- d. For the given program no stalls are required

Question 4

Complete

Mark 1.00 out of 1.00

The Ideal RISC pipeline may have?

- a. Successive instructions are independent of one another
- b. All of the mentioned
- c. Instructions can be divided into independent parts, each taking nearly equal time
- d. Instructions are executed in sequence one after the other in the order in which they are written

Question 5

Complete

Mark 0.00 out of 1.00

A four stage pipeline has the stage delays as 150, 120, 170 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate. The total time taken to process 1000 data items on the pipeline?

- a. 170.5 us
- b. 165.3 us
- c. 165.5 us
- d. 180.3 us

[◀ Assignment 3-25-02-2022](#)

Jump to...

[Assignment 5-25-03-2022 ►](#)

Started on Friday, 25 March 2022, 2:50 PM**State** Finished**Completed on** Friday, 25 March 2022, 2:58 PM**Time taken** 7 mins 54 secs**Marks** 3.00/5.00**Grade** **6.00** out of 10.00 (**60%**)**Question 1**

Complete

Mark 0.00 out of 1.00

For the given code (MIPS processor), the total number of stalls required with scheduling?

Original code:

L.D F0, 0(R1)

ADD.D F4,F0,F2

S.D F4, 0(R1)

DADDUI R1,R1, #-8

BNE R1,R2,Loop

 a. 4 b. 5 c. 2 d. 3

Question 2

Complete

Mark 1.00 out of 1.00

Consider the unpipelined machine with 10ns clock cycles. It uses four cycles for ALU operations and branches where as five cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40% respectively. Let due to clock skew and set up pipelining, the machine adds 1 ns of overhead to the clock. How much speed in instruction execution rate will we gain from pipeline ?

- a. 5 times
- b. 6 times
- c. None of the mentioned
- d. 4 times

Question 3

Complete

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with their execution delays in ns i.e. IF (60), ID(50), IE(90) and WB(80).

The clock duration is calculated based on ?

- a. IE(90ns)
- b. IF (60ns)
- c. WB(80ns)
- d. ID(50ns)

Question 4

Complete

Mark 1.00 out of 1.00

For the given code (MIPS processor), the total number of stalls required ?

Original code:

L.D F0, 0(R1)

ADD.D F4,F0,F2

S.D F4, 0(R1)

DADDUI R1,R1, #-8

BNE R1,R2,Loop

a. 5

b. 3

c. 4

d. 2

Question 5

Complete

Mark 0.00 out of 1.00

For the given code (MIPS processor), the total number of stalls required with loop unrolling 4 copies along with scheduling implementation?

Original code:

L.D F0, 0(R1)

ADD.D F4,F0,F2

S.D F4, 0(R1)

DADDUI R1,R1, #-8

BNE R1,R2,Loop

a. 4

b. 0

c. 2

d. 1

[◀ Assignment 4-04-03-2022](#)

Jump to...



[Assignment 6_01-04-2022 ►](#)

Started on Friday, 1 April 2022, 2:50 PM

State Finished

Completed on Friday, 1 April 2022, 2:54 PM

Time taken 4 mins 44 secs

Marks 3.00/4.00

Grade **7.50** out of 10.00 (**75%**)

Question 1

Complete

Mark 1.00 out of 1.00

A branch-prediction cache that stores the predicted address for the next instruction after a branch is called a

- a. Data cache
- b. branch-target cache
- c. None of the mentioned
- d. Memory cache

Question 2

Complete

Mark 0.00 out of 1.00

Code:**DIV.D F0,F2,F4****ADD.D F6,F0,F8****S.D F6,0(R1)****SUB.D F8,F10,F14****MUL.D F6,F10,F8****How many name-dependencies are available in the given code?**

- a. 4
- b. 3
- c. 2
- d. 1

Question 3

Complete

Mark 1.00 out of 1.00

Branch predictors that use the behavior of other branches to make a prediction are called?

- a. **multi-level predictors**

- b. **non-correlation predictors**

- c. **correlating predictors**

- d. **one-level predictor**

Question 4

Complete

Mark 1.00 out of 1.00

Probability of branch in buffer, but actually not taken is 0.09 and probability of branch not in buffer, but actually taken is 0.10. then find the Branch penalty

- a. **0.32**
- b. **0.48**
- c. **0.38**
- d. 0.18

[◀ Assignment 5-25-03-2022](#)

Jump to...

[CS-268 II 15% Mid Term Online Test II 09-04-2022 ►](#)

Started on Saturday, 9 April 2022, 11:00 AM

State Finished

Completed on Saturday, 9 April 2022, 11:48 AM

Time taken 48 mins 9 secs

Marks 26.00/35.00

Grade 7.43 out of 10.00 (74%)

Question 1

Complete

Mark 0.00 out of 1.00

In 2 bit ripple carry adder, used XOR, AND, and OR gates propagation delay are 15ns, 10ns and 5ns, respectively. What is the required time for a valid answer?

- a. 60ns
- b. 50ns
- c. 70ns
- d. 30ns

Question 2

Complete

Mark 1.00 out of 1.00

For the Stages of Datapath and control(Execution sequence) for instruction MOV 20(R1),R2. Select the correct option?

- a. Add 20 to value in register R1
- b. All of the mentioned
- c. Decode to find that it is an MOV instruction, then read registers R1 and R2
- d. Fetch the instruction, and increment PC

Question 3

Complete

Mark 1.00 out of 1.00

Consider a ideal pipeline having 5 phases with duration 30, 10, 40, 10 and 30 ns. Given latch delay is 5 ns. What is the Non-pipeline execution time in ns?

- a. 110
- b. 120
- c. 130
- d. 100

Question 4

Complete

Mark 1.00 out of 1.00

Among ripple carry adder and carry look ahead, in which time delay is independent of a number of bits of operand.

- a. **None**
- b. **Both**
- c. **Ripple carry adder**
- d. **carry look ahead**

Question 5

Complete

Mark 1.00 out of 1.00

What is the two times arithmetic shift right (ASR) of the binary stream 0 1 0 1 1 1 0 1?

- a. 0 0 0 1 0 1 1 1
- b. 0 1 0 1 1 1 0 1
- c. 1 0 0 1 0 1 1 0
- d. 0 1 0 1 1 1 1 0



Question 6

Complete

Mark 0.00 out of 1.00

The role of sign extension hardware in data path architecture?

- a. All of the mentioned
- b. To convert the 8 bit to 32 bit binary number
- c. To convert the 16 bit to 32 bit binary number
- d. To convert the 12 bit to 32 bit binary number

Question 7

Complete

Mark 1.00 out of 1.00

Code:**DIV.D F0,F2,F4****ADD.D F6,F0,F8****S.D F6,0(R1)****SUB.D F8,F10,F14****MUL.D F6,F10,F8**

How many possible hazards are available in the given code?

- a. 4
- b. 5
- c. 2
- d. 3



Question 8

Complete

Mark 1.00 out of 1.00

In 4 bit ripple carry adder, carry propagation delay is 10ns, and sum propagation delay is 20ns. What is the required time for a valid answer?

- a. **50ns**
- b. **40ns**
- c. **30ns**
- d. **20ns**

Question 9

Complete

Mark 1.00 out of 1.00

A four stage pipeline has the stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, what is the total time (micro second) taken to process 1000 data items on the pipeline?

- a. 165.1
- b. 165.3
- c. 165.4
- d. 165.5

Question 10

Complete

Mark 0.00 out of 1.00

The 2bits ripple carry adder is made by 3 input XOR, OR and 2 input AND gate. All 3 input gates have a propagation delay of 5ns, and 2 input gates have a propagation delay of 1ns. What is the required time for a valid answer?

- a. **13ns**
- b. **11ns**
- c. **10ns**
- d. **16ns**



Question 11

Complete

Mark 1.00 out of 1.00

The first and second address sent by the PC to the memory and their corresponding content will be stored into

- a. Instruction register and PC register
- b. Both into instruction register
- c. Instruction register and data register
- d. None of the mentioned

Question 12

Complete

Mark 1.00 out of 1.00

Any condition that causes a processor to stall is called as _____

- a. **Page fault**
- b. Pipeline error
- c. **Hazard**
- d. **System error**

Question 13

Complete

Mark 1.00 out of 1.00

Pipelining of a MIPS-like Processor, select the right option

- a. All ALU operations are performed on register operands
- b. Only instructions which access memory are load and store instructions
- c. All of the mentioned
- d. Separate Instruction and data memory is required



Question 14

Complete

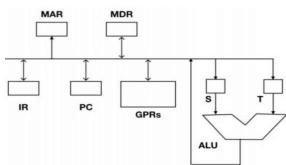
Mark 1.00 out of 1.00

Consider the following data path of a CPU. The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR. The instruction "call Rn, sub" is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is

$$Rn \leftarrow PC + 1; Rn \leftarrow PC + 1;$$

$$PC \leftarrow M[PC]; PC \leftarrow M[PC];$$

How many minimum number of CPU clock cycles needed during the execution cycle of this instruction?



- a. 2 cycle
- b. 7 cycle
- c. 3 cycle
- d. 5 cycle

Question 15

Complete

Mark 1.00 out of 1.00

In the MIPS architecture, data transfer takes place between ?

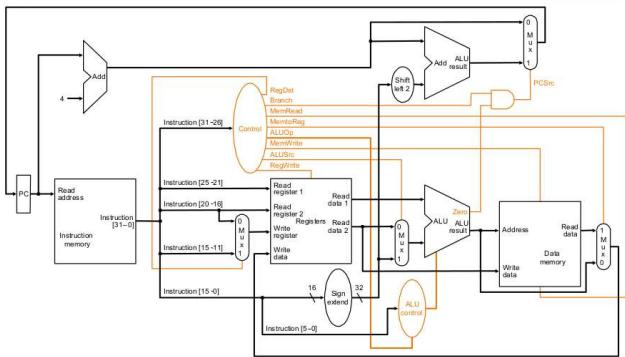
- a. All of the mentioned
- b. Register to memory
- c. Memory to register
- d. Register to register

Question 16

Complete

Mark 1.00 out of 1.00

For the figure given below, select the correct option ?



- a. I-type instruction can not be executed
- b. R-type instruction can not be executed
- c. None of the mentioned
- d. J-type instruction can not be executed

Question 17

Complete

Mark 0.00 out of 1.00

Which one is not the pipeline performance parameter?

- a. Speed up ratio
- b. Pipeline cycle time
- c. Throughput
- d. Pipeline overlapping factor

Question 18

Complete

Mark 0.00 out of 1.00

Consider a pipeline having 4 phases with duration 10, 20, 30 and 40 ns. Given latch delay is 10 ns. The pipeline may produce wrong output data if the minimum clock cycle time (ns) is less than

- a. 40
- b. 30
- c. 20
- d. 10

Question 19

Complete

Mark 1.00 out of 1.00

How many types of pipelining exist?

- a. 2
- b. 3
- c. 4
- d. 1

Question 20

Complete

Mark 1.00 out of 1.00

The contention for the usage of a hardware device is called _____

- a. Control hazard
- b. None of the Mentioned
- c. **Structural hazard**
- d. **Data hazard**

Question 21

Complete

Mark 0.00 out of 1.00

The features of the RISC processor ?

- a. Small number of addressing modes
- b. Small number of the instructions
- c. Instruction execute in one or two clock cycle
- d. All of the mentioned

Question 22

Complete

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 20 ns. What is Pipeline cycle time in ns.

- a. 110
- b. None of the mentioned
- c. 90
- d. 100

Question 23

Complete

Mark 1.00 out of 1.00

Consider the unpipelined machine with 10ns clock cycles. It uses four cycles for ALU operations and branches where as five cycles for memory operations. Assume that the relative frequencies of these operations are 40%,20% and 40% respectively. Let due to clock skew and set up pipelining, the machine adds 1 ns of overhead to the clock. What is the average instruction execution time(ns)?

- a. 32
- b. 42
- c. None of the mentioned
- d. 40

Question 24

Complete

Mark 1.00 out of 1.00

Which of the following is not a pipeline conflict?

- a. Timing variation
- b. Load balancing
- c. Data Dependency
- d. Branching

Question 25

Complete

Mark 0.00 out of 1.00

The full 32 bit target address is computed by concatenating?

- a. 26 bit immediate field of the jump instruction
- b. All of the mentioned
- c. Bits 00 in the lowest positions
- d. Upper 4 bits of PC+4

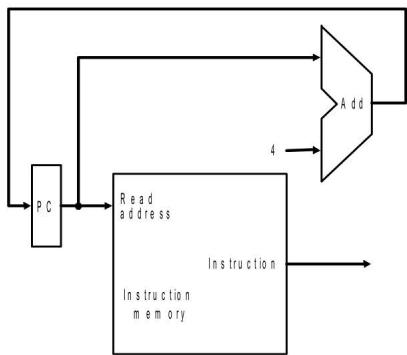


Question 26

Complete

Mark 0.00 out of 1.00

For the figure given below, select the correct option



- a. $PC = PC + 0$ for the first address
- b. All of the mentioned
- c. $PC = PC + 4$ for the second address
- d. Address will be the multiple fo 4

Question 27

Complete

Mark 1.00 out of 1.00

In which one of the following addressing modes, the content of the program counter is added to the address part of the instruction in order to obtain the effective address?

- a. Indexed addressing mode
- b. Absolute addressing mode
- c. Register indirect addressing mode
- d. Register addressing mode

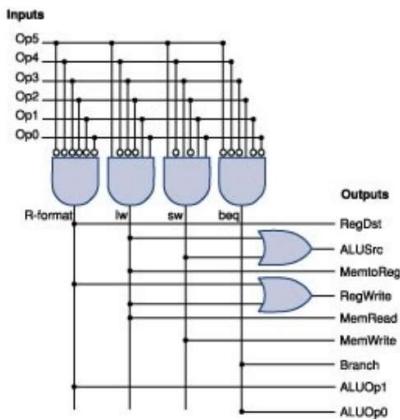


Question 28

Complete

Mark 1.00 out of 1.00

The figure given below is the example of ?



- a. Branch control unit
- b. ALU control unit
- c. RAW hazard control unit
- d. CPU Main control unit

Question 29

Complete

Mark 1.00 out of 1.00

Which one of the following about the MIPS rating of a computer is FALSE?

- a. MIPS rating of a processor is independent of the program is being executed.
- b. MIPS rating of computer depends on the computer being used
- c. None of the mentioned
- d. MIPS rating of a computer can very based on which instruction of a processor are being considered



Question 30

Complete

Mark 1.00 out of 1.00

Out-of-order execution introduces the possibility of ____ hazards a. **RAW and RAR** b. **WAR and RAW** c. **WAR and WAW** d. **RAR and WAR****Question 31**

Complete

Mark 1.00 out of 1.00

The processor speed has been increased over the last five decades due to the ?

 a. None of the mentioned b. Charl's law c. Moore's Law d. Krammar's Law

Question 32

Complete

Mark 1.00 out of 1.00

The two numbers given below are multiplied using Booth's algorithm.

Multiplicand : 0101 1010 1110 1110

Multiplier: 0111 0111 1011 1101

How many additions/Subtractions are required for the multiplication of the above two numbers?

- a. 9 additions/Subtractions are required
- b. 5 additions/Subtractions are required
- c. 8 additions/Subtractions are required
- d. None of the mentioned

Question 33

Complete

Mark 0.00 out of 1.00

Carry look adder is better than ripple carry adder because of _____

- a. **Both**
- b. **Complex architecture**
- c. **Less propagation delay**
- d. **None**

Question 34

Complete

Mark 1.00 out of 1.00

A booth's multiplier circuit needs to inspect at most how many LSB bits to determine whether to add the multiplier, subtract the multiplier or leave the partial result unchanged during any step in the sequence of multiplication steps?

- a. 3 bits
- b. 2 bits
- c. 1 bit
- d. None of the mentioned

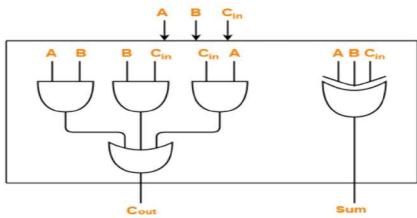


Question 35

Complete

Mark 1.00 out of 1.00

Following figure shows the implementation of full adders in a 16-bit ripple carry adder realized using 16 identical full adders. The propagation delay of the XOR, AND and OR gates are 20 ns, 15 ns and 10 ns respectively. The worst case delay (ns) of this 16 bit adder will be?



- a. 396
- b. 394
- c. 393
- d. 395

[◀ Assignment 6_01-04-2022](#)

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Started on	Friday, 18 February 2022, 1:40 PM
State	Finished
Completed on	Friday, 18 February 2022, 1:47 PM
Time taken	6 mins 36 secs
Marks	5.00/7.00
Grade	7.14 out of 10.00 (71%)

Question **1**

Complete

Mark 0.00 out of 1.00

A machine (31-bit architecture, with 1-word long instructions) has 64 registers, each register is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, what is the maximum value of the immediate operand?

- a. 26383
- b. 16383
- c. 16333
- d. None of the mentioned

Question **2**

Complete

Mark 1.00 out of 1.00

_____ register specifically holds the _____ and provides it to instruction decoder circuit

- a. **Memory and instruction**
- b. **Instruction and instruction**
- c. **data and instruction**
- d. **instruction and data**

Question **3**

Complete

Mark 1.00 out of 1.00

The components to design the data path architecture ?

- a. Control unit and MUX
- b. ALU, MUX, Registres
- c. None of the mentioned
- d. ALU, Control unit, program counter

Question **4**

Complete

Mark 0.00 out of 1.00

Which unit is responsible for directing the operations of computer arithmetic and logical unit?

- a. Control Unit
- b. Multiplexer
- c. ALU by itself
- d. Program Counter

Question **5**

Complete

Mark 1.00 out of 1.00

An instruction register is the part of a CPU's control unit that holds the _____ currently being executed

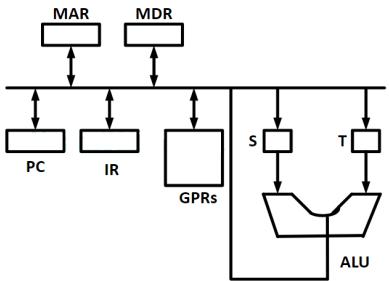
- a. **instruction**
- b. **address**
- c. **data**
- d. None of the mentioned

Question 6

Complete

Mark 1.00 out of 1.00

Consider the following data path of a cpu:



In the above data path size of bus, ALU and all registers are equal. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU.

Two clock cycles are needed for memory read operation- one is for loading address in MAR and one for loading data from memory but into MDR.

The instruction "call Rn,sub" is a two word instruction. Assume that program counter is incremented during the fetch cycle of the first word of the instruction, it's register transfer interpretation is

Rn <= PC + 1;

PC <= M[PC];

The no. of minimum number of CPU clock cycles required in the execution cycle of this instruction?

- a. 3
- b. 1
- c. 4
- d. 2

Question 7

Complete

Mark 1.00 out of 1.00

In a system, which has 32 registers the register id is _____ long?

- a. 4 bit
- b. 5 bit
- c. 6 bit
- d. 16 bit

◀ Announcements

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Started on Friday, 11 March 2022, 10:00 AM

State Finished

Completed on Friday, 11 March 2022, 11:05 AM

Time taken 1 hour 4 mins

Marks 40.00/45.00

Grade 8.89 out of 10.00 (89%)

Question 1

Complete

Mark 1.00 out of 1.00

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The number of and gates required to design full adders are?

- a. Nine
- b. Twelve
- c. Eight
- d. Ten

Question 2

Complete

Mark 1.00 out of 1.00

Consider the following instruction sequence five-stage pipeline,

ADD R1, R2, R1 --- I1

LW R2,0(R1) --- I2

LW R1,4(R1) -- I3

OR R3, R1, R2 -- I4

Select the correct option.

- a. RAW hazards is present in instructions I1-I2
- b. RAW hazards is present in instructions I2-I3
- c. RAW hazards is present in instructions I3-I4
- d. All of the mentioned

Question 3

Complete

Mark 1.00 out of 1.00

Pipelining of a MIPS-like Processor, select the right option

- a. Only instructions which access memory are load and store instructions
- b. All of the mentioned
- c. All ALU operations are performed on register operands
- d. Separate Instruction and data memory is required

Question 4

Complete

Mark 1.00 out of 1.00

In pipelining, which of the following operation is used to enhance the memory access speed?

- a. Cache
- b. Registers
- c. Stack
- d. Queue

Question 5

Complete

Mark 1.00 out of 1.00

Forwarding can be implemented in 5-stage and 6-stage MIPS pipeline --

- a. Using one multiplexer
- b. Using three multiplexers
- c. Using two multiplexers
- d. Using two multiplexers with extra latch

Question 6

Complete

Mark 1.00 out of 1.00

If multiplicand (M) is 0111, the AC register is initialized with zero. What will be the content of the AC register after operation $AC = AC - M$?

- a. 1111
- b. 1010
- c. 1001
- d. 1100

Question 7

Complete

Mark 1.00 out of 1.00

Instruction pipeline improves the CPU performance due to which one of the following reasons?

- a. Efficient utilization of the processor hardware
- b. Use of additional functional units
- c. Reduced memory access time
- d. Use a larger Cache

Question 8

Complete

Mark 0.00 out of 1.00

Overcoming control dependence is done by ____ on the outcome of branches?

- a. None of the mentioned
- b. speculating
- c. Out of order scheme
- d. Scoreboard

Question 9

Complete

Mark 1.00 out of 1.00

A computer has a word size of 16-bit and has 16 programmer visible registers. each instruction has two sources and one destination operands and uses only register direct addressing mode. what is the maximum number of op-codes that this processor can have?

- a. 32
- b. 64
- c. 8
- d. 16

Question 10

Complete

Mark 1.00 out of 1.00

Little Endian byte order puts the byte having address

- a. Most Significant Position
- b. Least Significant Position
- c. Middle Significant Position

Question 11

Complete

Mark 1.00 out of 1.00

For the load and store operation ---

- a. Effective address is calculated between 3rd and 4th stage of the pipeline
- b. Effective address is calculated at 4th stage of the pipeline
- c. Effective address is calculated between 4th and 5th stage of the pipeline
- d. Effective address is calculated at 3rd stage of the pipeline

Question 12

Complete

Mark 0.00 out of 1.00

The instruction $Z=X+Y$; needs to be run on accumulator-based architecture. Choose the current option.

- a. One operand is available in DMA
- b. Both operands are available in the register bank
- c. One operand is available in the accumulator and other need to be fetched from memory
- d. Both operands are available in the accumulator

Question 13

Complete

Mark 1.00 out of 1.00

A four-stage pipeline has stage delays of 150, 120, 160, and 140 ns respectively. Registers are used between the stages and have a delay of 10 ns each. What is the cycle time?

- a. 140 ns
- b. 170 ns
- c. 155 ns
- d. 165 ns

Question 14

Complete

Mark 1.00 out of 1.00

A pipelined processor has seven stages, namely, IF1, IF2, ID, EX, MEM1, MEM2, WB. Assuming all the stages require the same amount of time and the time period of the non-pipelined processors is 14 ns, find out the clock frequency and speedup of the pipelined processor. Assume the delay of the latches is 1 ns.

- a. 1 KHz and 3
- b. None of the mentioned
- c. 1Khz and 50
- d. 1.2 KHz and 30

Question 15

Complete

Mark 1.00 out of 1.00

ARM processors are available in the form of ----- pipelining?

- a. Both 3 and 5 stages
- b. 3 stage
- c. 5 stage
- d. None of them

Question 16

Complete

Mark 0.00 out of 1.00

Parallelism can be achieved by-----technique.

- a. Hardware
- b. Compiler
- c. Software
- d. All of the above

Question 17

Complete

Mark 1.00 out of 1.00

The stages of 3 stage pipelining are----?

- a. Address generation, Fetch, Execute.
- b. Decode, Fetch, Execute
- c. Execute, Fetch, Decode
- d. Fetch, Decode, Execute

Question 18

Complete

Mark 1.00 out of 1.00

Branch predictors, that use the behavior of other branches to make a prediction is called?

- a. one-level predictor
- b. Branch predictors that use the behavior of other branches to make a predicting predictors
- c. non-correlation predictors
- d. multi-level predictors

Question 19

Complete

Mark 1.00 out of 1.00

Forwarding can be implemented in 5-stage and 6-stage MIPS pipeline --

- a. Using three multiplexers
- b. Using one multiplexer
- c. Using two multiplexers with extra latch
- d. Using two multiplexers

Question 20

Complete

Mark 1.00 out of 1.00

In which one of the following addressing modes, the content of the program counter is added to the address part of the instruction in order to obtain the effective address.

- a. Indexed addressing mode
- b. Absolute addressing mode
- c. Register addressing mode
- d. Register indirect addressing mode

Question 21

Complete

Mark 1.00 out of 1.00

The zero flag register of the MIPS pipeline architecture--

- a. Calculate the effective address by using the instruction register content
- b. Calculate the effective address by adding the register content of the ALU
- c. Calculate the effective address by subtracting the register content of the ALU
- d. Calculate the effective address by using the program counter register content

Question 22

Complete

Mark 1.00 out of 1.00

When the data operands are not available then it is called---?

- a. Pop
- b. Data hazard
- c. Deadlock
- d. Push

Question 23

Complete

Mark 1.00 out of 1.00

Using booth's algorithms multiply 7 with 3 and assume register AC is 4 bit. The value of AC after 3rd and 4th cycles are

- a. 1 0 1 0 and 1 0 1 0
- b. 0 0 1 0 and 1 0 1 0
- c. 0 1 1 1 0 and 1 0 1 0 0
- d. 0 0 1 1 and 1 0 1 1

Question 24

Complete

Mark 1.00 out of 1.00

The features of the RISC processor --

- a. Small number of addressing modes
- b. Instruction execute in one or two clock cycle
- c. All of the mentioned
- d. Small number of the instructions

Question 25

Complete

Mark 1.00 out of 1.00

Consider a three address RISC processor ISA. Which one of the following correctly characterizes an effect of doubling the number of registers in the processor?

- a. Instruction size would be increase by 3-bit
- b. Instruction size would be increase by 1-bit
- c. Instruction size would be unaffected
- d. Instruction size would be increase by 2-bit

Question 26

Complete

Mark 0.00 out of 1.00

Throughput is calculated as

- a. Speed of the processor/ Number of instructions
- b. The number of instructions/ Total time to complete the instructions
- c. Total time to complete the instructions/number of instructions
- d. The number of instructions/speed of the processor

Question 27

Complete

Mark 1.00 out of 1.00

In pipelined processor, the WB stage in instruction execution isstage?

- a. Fifth
- b. Seventh
- c. First
- d. Third

Question 28

Complete

Mark 1.00 out of 1.00

An instruction cycle refers to which one of the following?

- a. Executing an instruction
- b. Fetching an instruction
- c. All of the mentioned
- d. Decoding the instruction and calculation of effective address

Question 29

Complete

Mark 1.00 out of 1.00

For calculating the effective address, the upper 6 bits and concatenation done between---

- a. Program counter and constant value which was not the part of the instruction
- b. Address register and constant value which was not the part of the instruction
- c. Program counter and constant value which was the part of the instruction
- d. Address register and constant value which was the part of the instruction

Question 30

Complete

Mark 1.00 out of 1.00

DIV.D F0,F2,F4

ADD.D F6,F0,F8

S.D F6,0(R1)

SUB.D F8,F10,F14

MUL.D F6,F10,F8

Which types of hazards are available in the above-given code?

- a. WAR and RAR
- b. WAR and RAW
- c. WAW and WAR
- d. RAW and WAR

Question 31

Complete

Mark 1.00 out of 1.00

In a pipelined processor, the processing units for integers and floating point is-----?

- a. Same unit.
- b. Separate unit.
- c. No unit.
- d. Within each other.

Question 32

Complete

Mark 1.00 out of 1.00

Addressing modes are used to calculate the effective address by using the --

- a. Control Unit
- b. ALU + control unit
- c. DMA
- d. ALU unit only

Question 33

Complete

Mark 1.00 out of 1.00

What is the arithmetic shift right operation after the 1st cycle for the following binary stream 1 0 0 1 0 0 1 1 0 ?

- a. 1 1 1 0 0 1 0 0 1
- b. 0 1 1 0 0 1 0 0 1
- c. 1 1 0 0 1 0 0 1 1
- d. 1 0 0 1 0 0 1 1 0

Question 34

Complete

Mark 0.00 out of 1.00

Pipelining is a -----technique?

- a. Superscalar operation
- b. Parallel operation
- c. Serial operation
- d. Scalar operation

Question 35

Complete

Mark 1.00 out of 1.00

Out-of-order execution introduces the possibility of ____ hazards.

- a. WAR and WAW
- b. RAR and WAR
- c. WAR and RAW
- d. RAW and RAR

Question 36

Complete

Mark 1.00 out of 1.00

A booth's multiplier circuit needs to inspect at most how many LSB bits to determine whether to add the multiplier, subtract the multiplier or leave the partial result unchanged during any step in the sequence of multiplication steps?

- a. One bit
- b. All bits of the multiplier
- c. All bits of the multiplicand
- d. Two bits

Question 37

Complete

Mark 1.00 out of 1.00

Which of the following instruction is not used for changing state....?

- a. no
- b. nop
- c. nope
- d. no-op

Question 38

Complete

Mark 1.00 out of 1.00

In the MIPS architecture, data transfer takes place between --

- a. Register to register
- b. All of the mentioned
- c. Register to memory
- d. Memory to register

Question 39

Complete

Mark 1.00 out of 1.00

Von Neumann computers helping to which one of the following classes of computers?

- a. MIMD
- b. MISD
- c. SISD
- d. SIMD

Question 40

Complete

Mark 1.00 out of 1.00

Which of the addressing mode refer the memory two times in accessing the data?

- a. indirect addressing mode
- b. Direct addressing mode
- c. Immediate addressing mode
- d. Relative addressing mode

Question 41

Complete

Mark 1.00 out of 1.00

In the MIPS instruction fields, the shamt field is of

- a. 4 bits
- b. 6 bits
- c. 7 bits
- d. 5 bits

Question 42

Complete

Mark 1.00 out of 1.00

The following assembly program is run over the MIPS pipeline architecture. Choose the wrong option.

Assembly code:

- i1. pp1: L.D F0,0(R1);
- i2. ADD.D F4,F0,F2;
- i3. S.D F4,0(R1);
- i4. DADDUI R1,R1,#-8;
- i5. BNE R1,R2,pp1

- a. i1 is used for array element
- b. i4 is used as an increment pointer
- c. i3 is used to store the results
- d. i2 is used for adding scalar value

Question 43

Complete

Mark 1.00 out of 1.00

Which one of the following most profoundly describes the functionality of the control unit in CPU?

- a. To store program instruction
- b. To perform logic operations based on decoded program instructions
- c. To generate the control signals based on decoded program instructions
- d. To perform the arithmetic operations based on decoded program instruction

Question 44

Complete

Mark 1.00 out of 1.00

By using pipelining, the latency of the instructions---?

- a. Increases
- b. Decreases
- c. Remains the same
- d. It is unity

Question 45

Complete

Mark 1.00 out of 1.00

The following lines of code IR <= Memory[PC]; PC <= PC + 4; explains the

- a. None of them
- b. Instruction Decode Step
- c. Instruction Fetch Step
- d. Instruction Execute Step

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