COMPARE INSTRUCTIONS

Oper	Op Code	Adr met	Instruction Format 1. Byte	2. Byte	3. Byte	4. Byte	Status Reg. T	S	N	Y	E	A	Explanation
CMP	Ki,V	V	00011100	0000 Ki	Data		↕	↕	↕	↕	↕	2	Ki - V
	Ki,Kj	L	01011100	00 Ki Kj			↕	↕	↕	↕	↕	2	Ki - Kj
	Ki,<adr>	D	00011100	0010 Ki	Adr (H)	Adr (L)	↕	↕	↕	↕	↕	3	Ki - <Adr>
	Ki,<CD>	K	00011100	0100 Ki			↕	↕	↕	↕	↕	3	Ki - <<CD>>
	Ki,<SK+S>	S	00011100	0110 Ki	S		↕	↕	↕	↕	↕	4	Ki - <SK+S>
	Ki,<SK+S>+R	R	00011100	1000 Ki	S	R	↕	↕	↕	↕	↕	5	Ki - <SK+S>+R
	Ki,<SK+S>-R	Z	00011100	1010 Ki	S	R	↕	↕	↕	↕	↕	5	Ki - <SK+S> - R
	Ki,<SK+CD+S>	U	00011100	1100 Ki	S		↕	↕	↕	↕	↕	6	Ki - <SK+CD+S>
	Ki,<YG+S>	Y	00011100	1110 Ki	S		↕	↕	↕	↕	↕	5	Ki - <YG+S>
CMP	Kii,VV	V	00111100	0000 Kii	Data (H)	Data (L)	↕	↕	↕	–	↕	4	Kii - VV
	Kii,Kjj	L	01111100	00 Kii Kjj			↕	↕	↕	–	↕	4	Kii - Kjj
	Kii,<adr>	D	00111100	0010 Kii	Adr (H)	Adr (L)	↕	↕	↕	–	↕	5	Kii - (<Adr>+<Adr+1>)
	Kii,<CD>	K	00111100	0100 Kii			↕	↕	↕	–	↕	5	Kii - (<<CD>>+<<CD+1>>)
	Kii,<SK+S>	S	00111100	0110 Kii	S		↕	↕	↕	–	↕	6	Kii - (<SK+S>+<SK+S+1>)
	Kii,<SK+S>+R	R	00111100	1000 Kii	S	R	↕	↕	↕	–	↕	7	Kii - (<SK+S>+<SK+S>) +R
	Kii,<SK+S>-R	Z	00111100	1010 Kii	S	R	↕	↕	↕	–	↕	7	Kii - (<SK+S>+>SK+S+1>) - R
	Kii,<SK+CD+S>	U	00111100	1100 Kii	S		↕	↕	↕	–	↕	8	Kii - (<SK+CD+S>+<SK+CD+S+1>
	Kii,<YG+S>	Y	00111100	1110 Kii	S		↕	↕	↕	–	↕	7	Kii - (<YG+S>+<YG+S>)
BIT	Ki,V	V	00011101	0000 Ki	Data		–	↕	↕	–	–	2	Ki • V
	Ki,Kj	L	01011101	00 Ki Kj			–	↕	↕	–	–	2	Ki • Ki
	Ki,<adr>	D	00011101	0010 Ki	Adr (H)	Adr (L)	–	↕	↕	–	–	3	Ki •<Adr>
	Ki,<CD>	K	00011101	0100 Ki			–	↕	↕	–	–	3	Ki •<<CD>>
	Ki,<SK+S>	S	00011101	0110 Ki	S		–	↕	↕	–	–	4	Ki •<SK+S>
	Ki,<SK+S>+R	R	00011101	1000 Ki	S	R	–	↕	↕	–	–	5	Ki •<SK+S> +R
	Ki,<SK+S>-R	Z	00011101	1010 Ki	S	R	–	↕	↕	–	–	5	Ki •<SK+S> - R
	Ki,<SK+CD+S>	U	00011101	1100 Ki	S		–	↕	↕	–	–	6	Ki •<SK+CD+S>
	Ki,<YG+S>	Y	00011101	1110 Ki	S		–	↕	↕	–	–	5	Ki •<YG+S>

JUMP & BRANCH INSTRUCTIONS

Op Code	Adr met	Instruction Format 1. Byte	2. Byte	3. Byte	4. Byte	A	Explanation
BRA V	B	10000000	Step count			2	Branch Always (V step)
JMP Adr	D	00011110	0010	Adr (H)	Adr (L)	2	Jump Always (To address)
JMC S,Adr	D	00011111	00111011	Adr (H)	Adr (L)	3	S=1 => jump to address
JMC N,Adr	D	00011111	00111010	Adr (H)	Adr (L)	3	N=1 => jump to address
JMC E,Adr	D	00011111	00111000	Adr (H)	Adr (L)	3	E=1 => jump to address
JMC T,Adr	D	00011111	00111100	Adr (H)	Adr (L)	3	T=1 => jump to address
BEQ	B	10000001	Step count			2	Branch if equal (V step)
BNE	B	10000010	Step count			2	Branch if not equal (V step)
BGT V	B	10000011	Step count			2	Branch if greater (V step)
BGE V	B	10000100	Step count			2	Branch if greater or equal
BLS V	B	10000101	Step count			2	Branch if less than
BHI V	B	10000110	Step count			2	Branch if higher
BHE V	B	10000111	Step count			2	Branch if higher or equal
BLO V	B	10001000	Step count			2	Branch if lower
BIO V	B	10001001	Step count			2	T=1 => jump V step
BNO V	B	10001010	Step count			2	T=0 => jump V step
BIC V	B	10001011	Step count			2	E=1 => jump V step
BNC V	B	10001100	Step count			2	E=0 => jump V step
BIH V	B	10001101	Step count			2	Y=1 => jump V step
BNH V	B	10001110	Step count			2	Y=0 => jump V step
BSR V	B	10001111	Step count			2	Branch to subprogram (V step)
JSR Adr	D	00010100	0010	Adr (H)	Adr (L)	5	Branch to subprogram (Address)
BSC S,V	B	10010011	Step count			6	S=1 => jump to subprogram (V step)
BSC N,V	B	10010010	Step count			6	N=1 => jump to subprogram (V step)
BSC E,V	B	10010000	Step count			6	E=1 => jump to subprogram (V step)
BSC T,V	B	10010100	Step count			6	T=1 => jump to subprogram (V step)
BSC S,Adr	D	00010101	00111011	Adr (H)	Adr (L)	6	S=1 => jump to subprogram (Address)
BSC N,Adr	D	00010101	00111010	Adr (H)	Adr (L)	6	N=1 => jump to subprogram (Address)
BSC E,Adr	D	00010101	00111000	Adr (H)	Adr (L)	6	E=1 => jump to subprogram (Address)
BSC T,Adr	D	00010101	00111100	Adr (H)	Adr (L)	6	T=1 => jump to subprogram (Address)
DBNZ Ki,V	B	11000110	01 Ki	Step count		8	Decrease Ki, branch if not zero (V step)
DBNZ <Adr>,V	B	11000111	Step count	Adr (H)	Adr (L)	9	Decrease M[adr], branch if not zero (V step)