	OPERATION INSTRUCTIONS										
Oper	Op Code	Adr	Instruction Format			Status Reg.				А	Explanation
		met	1. Byte	2. Byte	T	S	N	Υ	Е		
	E	L	01001100	10000	_	_	_	_	0	1	E ← 0
CLR	Υ	L	01001100	10001	_	_	_	0	_	1	Y ← 0
	N	L	01001100	10 010	_	-	0	_	-	1	N ← 0
	S	L	01001100	10 011	_	0	_	_	_	1	\$ ← 0
	T	L	0 1 0 0 1 1 0 0	100	0	_	_	_	_	1	1 ← 1
	E	L	0 1 0 0 1 1 1 0	10 000	_	_	-	_	1	1	E ← 1
	Υ	L	01001110	10 001	_	_	_	1	_	1	Y ← 1
SET	N	L	01001110	100000	_	_	1	_	-	1	N ← 1
	S	L	0 1 0 0 1 1 1 0	10 011	_	1	_	_	_	1	S ← 1
	T	L	0 1 0 0 1 1 1 0	100	-	_	_	_	_	1	1 ← 1
INC	Kii	L	0 1 1 1 0 0 0 0	0 1 Kii	\$	\$	\$	_	\$	2	Kii ← Kii + 1
DEC	Kii	L	0 1 1 1 0 0 0 1	0 1 Kii	‡	\$	\$	_	\$	2	Kii ← Kii - 1
DAA	Ai	L	01010100	0 1 Ai	_	_	_	0	0	2	Binary to Decimal
PSH	Ai	L	0 1 0 1 0 1 0 1	0 1 Ai	_	_	=	_	_	2	Push Ai to Stack
PUL	Ai	L	0 1 0 1 0 1 1 0	0 1 Ai	_	\$	\$	_	_	2	Pull Stock to Ai
EIN		L	11000000		_	_	_	_		1	Enable Interrupt
DIN		L	1 1 0 0 0 0 0 1		_	_	_	_	_	1	Disable Interrupt
NOP		L	1 1 0 0 0 0 1 0		-	_	_	_	_	1	No Operation
RTS		L	1 1 0 0 0 1 0 0		-	_	_	_		5	Return fron subroutine
RTI		L	1 1 0 0 0 1 0 1		-	-	_	_		15	Return from interrupt
INT		L	1 1 0 0 0 0 1 1		_	_	-	_	-	15	Software Interrupt

				SHIFT	&ROTATE	INSTRUC	TIC	N	S				
		Adr	Instruction Format						Status Reg.			Α	E adams to a
Oper	Op Code	met	1. Byte	2. Byte	3. Byte	4. Byte	Т	S	Ν	Υ	Е	А	Explanation
LSL	Ki	L	01010111	0 1 Ki			-	\$	\$	-	\$	1	
	<adr></adr>	D	00010111	00101	Adr (H)	Adr (L)	_	\$	\$	-	\$	2	
	<cd></cd>	К	00010111	01001			_	\$	\$	_	\$	3	
	<\$K+\$>	S	00010111	01101	S		_	\$	\$	-	\$	4	E V7 V6 V3 V4 V3 V2 VI V0
	<\$K+\$>+R	R	00010111	10001	S	R	_	\$	\$	_	\$	5	
	<sk+s>-R</sk+s>	Z	00010111	10101	S	R	_	\$	♦	-	\$	5	
	<sk+cd+s></sk+cd+s>	U	00010111	11001	S		_	\$	\$	\rightarrow	\$	6	
	<yg+\$></yg+\$>	Υ	00010111	11101	S		-	\$	\$	-	\$	4	
	Ki	L	01011000	0 1 Ki			-	\$	♦	-	*	1	
	<adr></adr>	D		00101	Adr (H)	Adr (L)	-	-	\$	$\overline{}$	\$	2	
LSR	<cd></cd>	K	00011000				-	_	\$	\rightarrow	\$	3	
	<\$K+\$>	S	00011000		S		-	-	\$	\rightarrow	\$	4	V7 V6 V5 V4 V3 V2 V1 V0 E
	<\$K+\$>+R	R			S	R	-	-	\$	\rightarrow	\$	5	
	<sk+s>-R</sk+s>	-	00011000		S	R	_	_	\$	$\overline{}$	\$	5	∥ °
	<\$K+CD+\$>	U	00011000	11001	Ś		-	-	\$	\rightarrow	\$	6	
	<yg+\$></yg+\$>	Υ		- 1/2////	S		_	\$	\$	\rightarrow	\$	4	
	Ki	L	01011001	0 1 Ki			-	\$	♦	-	\$	1	
	<adr></adr>	D	00011001	00101	Adr (H)	Adr (L)	-		\$	\rightarrow	\$	2	
ASR	<cd></cd>	K	00011001	01001			_	\$	\$	-	\$	3	
, tort	<sk+s></sk+s>	S	00011001	01101	S		-	-	\$	\rightarrow	*	4	V7 V6 V5 V4 V3 V2 V1 V0 E
	<\$K+\$>+R	R	00011001	10001	S	R	-		\$	\rightarrow	*	5	
	<sk+s>-R</sk+s>	Z	00011001	10101	S	R	-	\$	\$	\rightarrow	\$	5	
	<sk+cd+s></sk+cd+s>	U	00011001	1 1 0 0 1	Ś		_	\$	\$	-	\$	6	
	<yg+\$></yg+\$>	Υ	00011001	1 1 1 0 1	S S		-	\$	*	-	*	4	
	Ki	L	01011010	0 1 Ki			-	_	\$	-	-	1	
	<adr></adr>	D	00011010	00101	Adr (H)	Adr (L)	-	•	\$	-	_	2	
	<cd></cd>	K		01001			_	\$	\$	-	-	3	
ROL	<\$K+\$>	S		01101	S		-	_	\$	-	-	4	
	<\$K+\$>+R	R		10001	S	R	_	-	\$	-	-	5	E V7 V6 V5 V4 V3 V2 V1 V0
	<sk+s>-R</sk+s>	+-	00011010		S	R	-	-	*	\dashv	-	5	1
	<sk+cd+s></sk+cd+s>	U		11001	S		-		\$	-	-	6	
	<yg+\$></yg+\$>	Υ	00011010		S		-	\$	\$	-	-	4	
	Ki	L	01011011	0 1 Ki			_		\$	-	-	1	
	<adr></adr>	D	00011011	00101	Adr (H)	Adr (L)	-	-	\$	-	-	2	
	<cd></cd>	K		01001			-		\$	-	-	3	
ROR	<sk+s></sk+s>	S		01101	S		-	_	•	-	-	4	
	<\$K+\$>+R	R	00011011	10001	S	R	_	_	\$	-	-	5	V7 V6 V5 V4 V3 V2 V1 V0 E
	<sk+s>-R</sk+s>	Z	00011011		S	R	-	_	\$	-	-	5	V/ V0 V3 V4 V3 V2 V1 V0 E
	<sk+cd+s></sk+cd+s>	-	00011011		Š		-	$\overline{}$	\$	-	-	6	
	<yg+\$></yg+\$>	Υ	00011011	111101	S S		_	\$	\$	-	-	4	