INTERNAL STRUCTURES OF ELECTRONIC DIGITAL CIRCUTS

Until now we have seen abstract logic gates such as AND, OR, NAND, NOT , so on.

There are many different ways to implement a logic gate as an electronic circuit.

In this course we will discuss how different types of transistors are used to design an electronic logic circuit.

In digital circuits transistors act as a current-controlled switch (ON or OFF).

First we introduce the bipolar junction transistor.

Then we will introduce the MOSFET (metal-oxide semiconductor field effect transistor) or simply MOS transistor, which is used almost by all new integrated circuits.

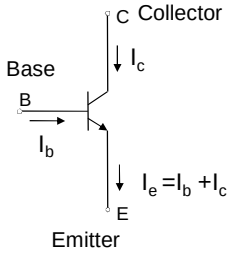
Bipolar Junction Transistor:

Base is the control terminal.

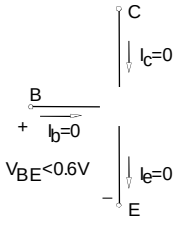
If no current is flowing into the base then no current can flow from the collector to the emitter (OFF).

However, if current is flowing from the base to the emitter, then current is also enabled to flow from the collector to the emitter (ON).

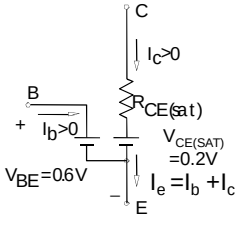
npn Bipolar Transistor



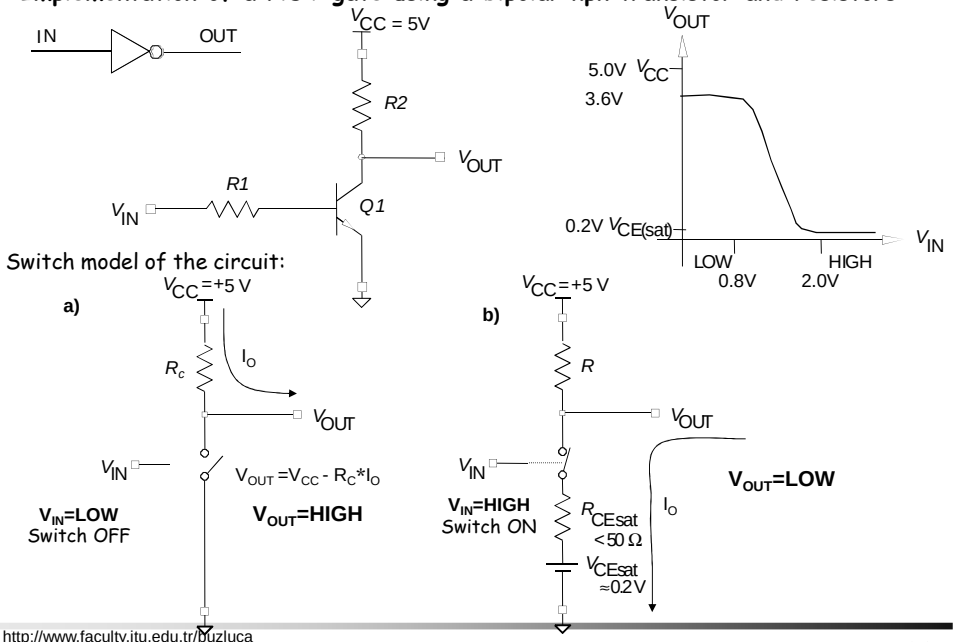
Transistor is cut off (OFF)
$V_{BE} < 0.6V$



Transistor is saturated (ON)
$V_{BE} \geq 0.6V$



Implementation of a NOT gate using a bipolar npn transistor and resistors



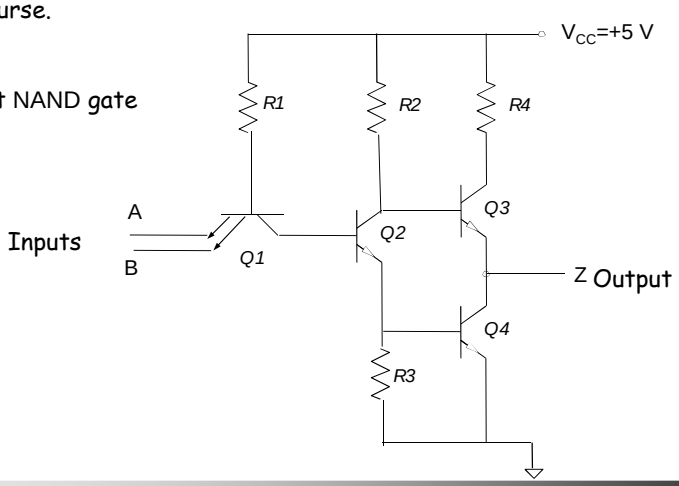
TTL (Transistor- Transistor) Logic Family

Bipolar transistors and resistors are used.

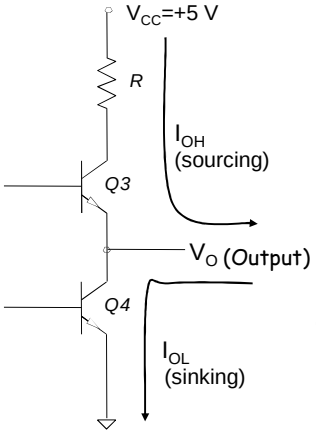
Although TTL was largely replaced by CMOS (we will discuss later), you may encounter TTL components in your labs; therefore, basic TTL concept are covered in this course.

Example:

Two-input NAND gate



Operation of the Output Stage of a TTL Gate



Output is "0" (*LOW*): Q_4 is ON, Q_3 is OFF.

In this case the current I_{OL} flows from the output into the circuit (*sinking current*).

$$V_{OL} = V_{CE(Q4)} + I_{OL} * R_{Q4}$$

Output is "1" (*HIGH*): Q_3 is ON, Q_4 is OFF.

In this case the current I_{OH} flows from the output to the outside of the circuit (*sourcing current*).

$$V_{OH} = V_{CC} - (V_{CE(Q3)} + I_{OH} * (R+R_{Q3}))$$

If both Q_3 and Q_4 are OFF output is in **high-impedance (Hi-Z)** state.

It is also called **third state** (High, Low, Hi-Z).

In this state the output behaves as it isn't even connected to the circuit.

The output is isolated from the line it was connected.

For TTL components $V_{OL(MAX)} = 0.4V$ $V_{OH(MIN)} = 2.4V$

In the TTL family there different types of elements (such as LS,ALS,L, F). They have different current and voltage values which can be found in data catalogs.

TTL Logic Levels

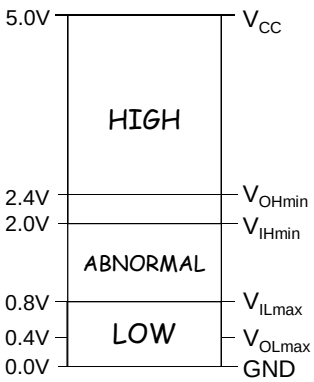
Abstract logic elements process binary digits, 0 and 1.

However, real logic circuits process electrical signals such as voltage levels.

In any logic circuit family, there is a range of voltages that is interpreted as logic 0 and another, nonoverlapping range that is interpreted as logic 1.

TTL circuits are connected to 5-volt power supply (Vcc=5V).

Logic levels of a standard TTL unit:



V_{OHmin}: The minimum output voltage produced in the HIGH state.

V_{IHmin}: The minimum input voltage guaranteed to be recognized as a HIGH.

V_{ILmax}: The maximum input voltage guaranteed to be recognized as a LOW.

V_{OLmax}: The maximum output voltage produced in the LOW state.

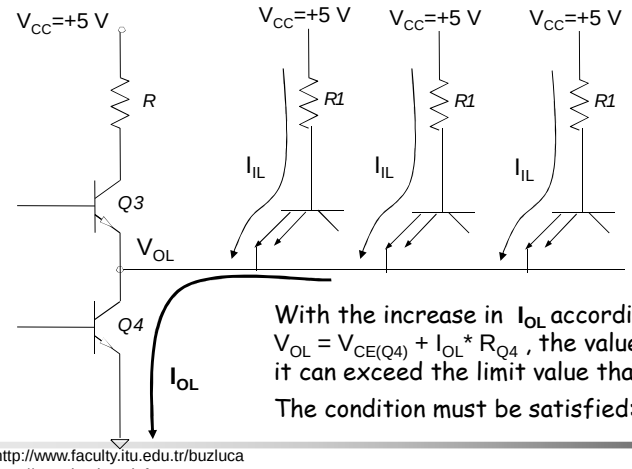
TTL Fanout

Remember, the output of a logic gate is connected to inputs of other gates.

The **fanout** of a logic gate is the number of inputs that the gate can drive without exceeding its worst-case loading specifications.

Because of current issues this number is limited.

When Output is LOW:



From the inputs(LOW) of the components flows the current I_{IL} into the output of the gate.

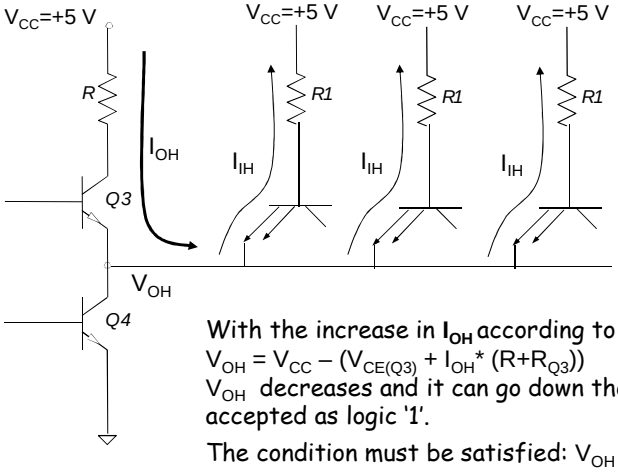
The sum of these currents is sunken by the gate.

$$I_{OL} < \Sigma I_{IL}$$

With the increase in I_{OL} according to the equation $V_{OL} = V_{CE(Q4)} + I_{OL} * R_{Q4}$, the value V_{OL} also increases and it can exceed the limit value that can be accepted as '0'.

The condition must be satisfied: $V_{OL} < V_{ILmax}$

When Output is HIGH:



Into the inputs in HIGH state flows the leakage current I_{IH}.

The sum of these currents is sourced by the output of the gate.

$$I_{OH} < \Sigma I_{IH}$$

With the increase in I_{OH} according to the equation $V_{OH} = V_{CC} - (V_{CE(Q3)} + I_{OH} * (R+R_{Q3}))$ V_{OH} decreases and it can go down the limit value that can be accepted as logic '1'.

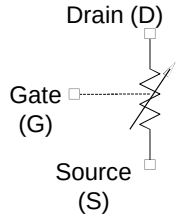
The condition must be satisfied: $V_{OH} > V_{IHmin}$

The fanout of a unit is the minimum of the numbers calculated for LOW and HIGH states.

CMOS (*Complementary MOS*) Logic Family

MOS FET (*Metal-Oxide Semiconductor Field-Effect Transistor*) is used.

A MOS transistor can be modeled as a 3-terminal device that acts like voltage controlled resistance.



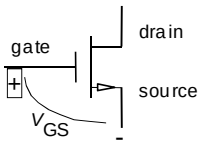
According to the voltage from Gate to Source (V_{GS}) the resistance from Drain to Source (R_{DS}) changes.

If transistor is OFF $R_{DS} \geq 1M\Omega$ ($10^6\Omega$)

If transistor is ON $R_{DS} \leq 10\Omega$

There are two types of MOS transistors.

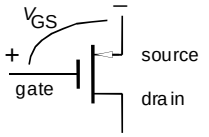
a) n channel MOS: NMOS.



Increase $V_{GS} \rightarrow$ decrease R_{DS}

Normally: $V_{GS} \geq 0V$

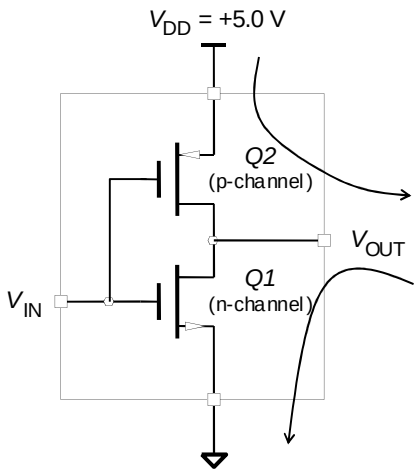
b) p channel MOS: PMOS.

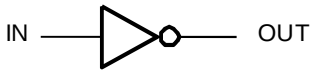


Decrease $V_{GS} \rightarrow$ decrease R_{DS}

Normally: $V_{GS} \leq 0V$

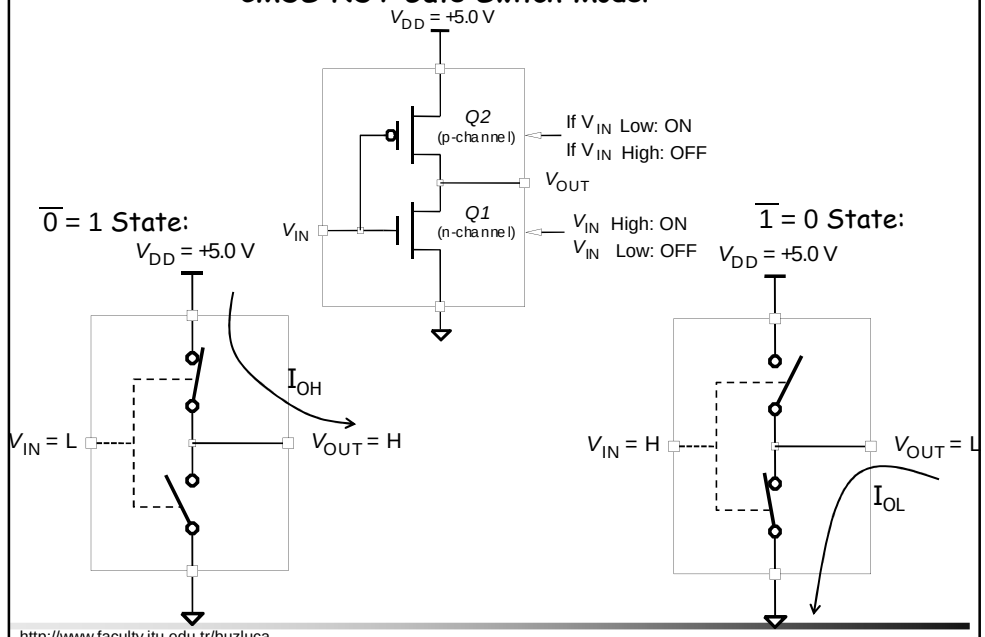
CMOS NOT Gate



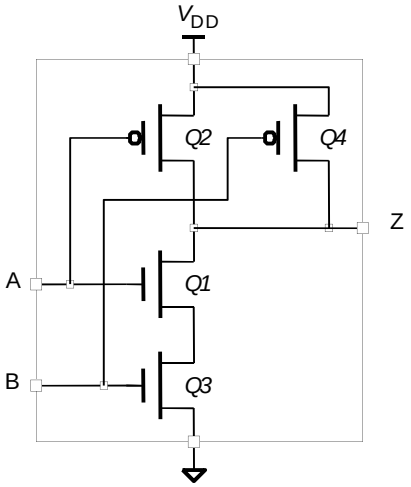


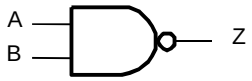
V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

CMOS NOT Gate Switch Model



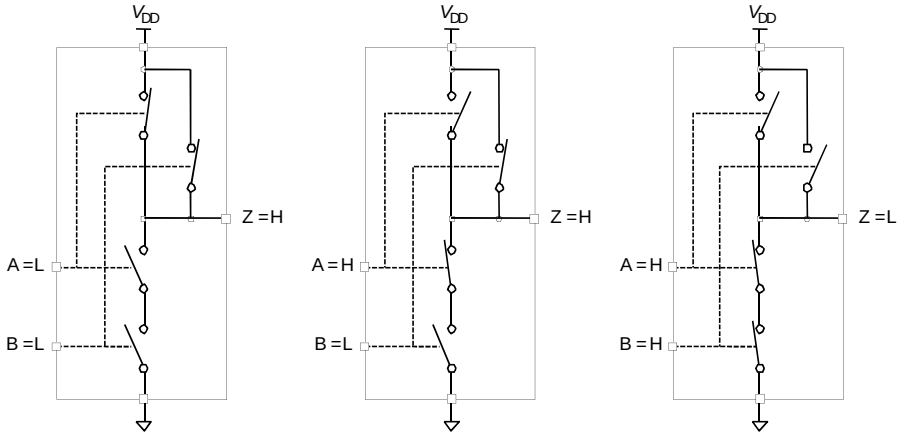
CMOS NAND Gate





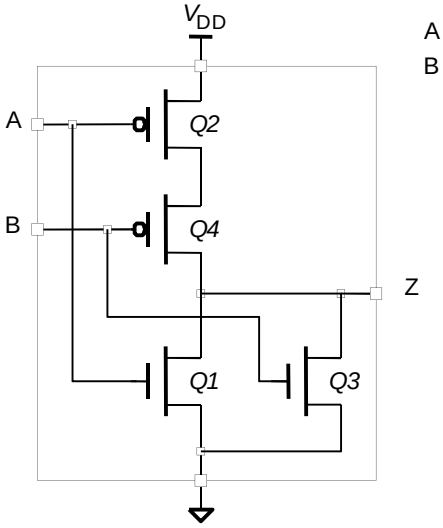
A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

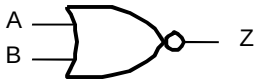
CMOS NAND Gate Switch Model



0 TVE 0 = 1 | 0 TVE 1 = 1 | 1 TVE 1 = 0

CMOS NOR Gate

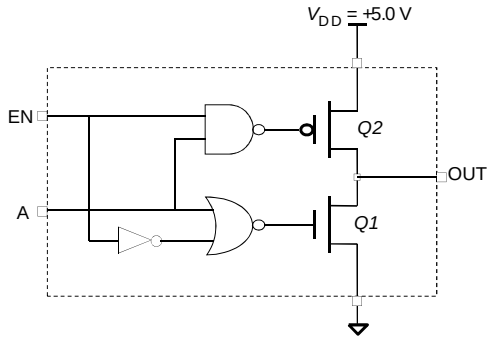


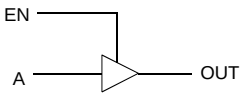


A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

CMOS Three-state Buffer

Remember, if an output is in **high-impedance (Hi-Z)** state (also called **third state**) the output behaves as it isn't even connected to the circuit.





IF EN=HIGH THEN OUT=A
IF EN=LOW THEN OUT= Hi-Z

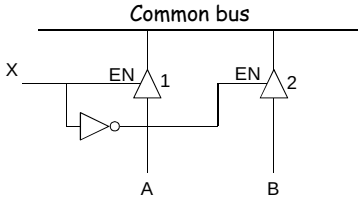
EN	A	Q1	Q2	OUT
L	L	off	off	Hi-Z
L	H	off	off	Hi-Z
H	L	on	on	L
H	H	off	on	H

To simplify the diagram, the internal NAND, NOR and NOT functions are shown as functional abstract gates rather than in transistor form.
They actually consist of 10 transistors.

Three-state Common Bus

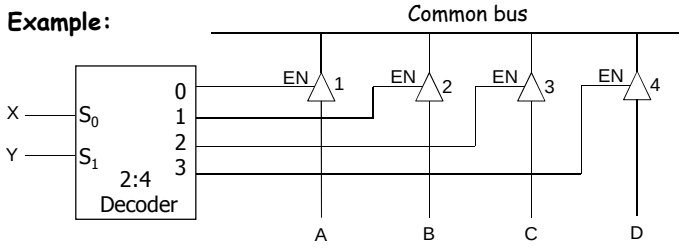
Several three-state outputs can be wired together to form a three-state common bus.
Only one, unit which is enabled can drive the bus.

Example:



If X=0 buffer #2 drives the bus. B is on bus.
If X=1 buffer #1 drives the bus. A is on bus.

Example:

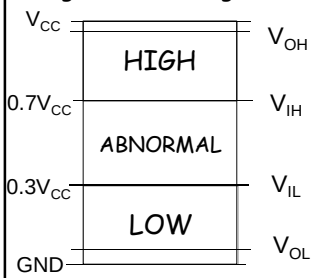


Y	X	Bus
0	0	A
0	1	B
1	0	C
1	1	D

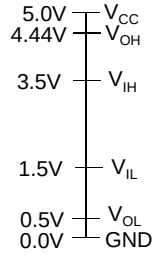
CMOS Logic Levels

CMOS circuits can use power supplies withe voltage less than 5 Volts.

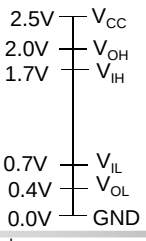
Logic levels change according to the voltage of the power supply.



5-V CMOS families:



2.5-V CMOS families:



1.5-V CMOS families: