MICROPROCESSOR SYSTEMS 11th / April / 2002

1- Calculate the value of A (Accumulator) by using hexadecimal number system at the end of logical operations.

a)
```
MOV   A,#239D          ;  A=(240)10
MOV   R0,#11001100B    ;  R0=(11001100)2
INC   A
XRL   A,R0             ;  ⇒ A= (???)16
```

b)
```
      MOV   A,#204D          ;  A=(204)10
      MOV   R0,#4
LOOP: RL    A
      DJNZ  R0,LOOP
                             ;  ⇒ A= (???)16
```

c) Assume that R0 and R1 are two independent variables defined in RAM locations inside an 8 bit microcontroller. Write the subroutine that returns A=f(R0,R1)=10*LON(R1)+LON(R0) where A is the accumulator and LON assigns low order nibble (4bits).

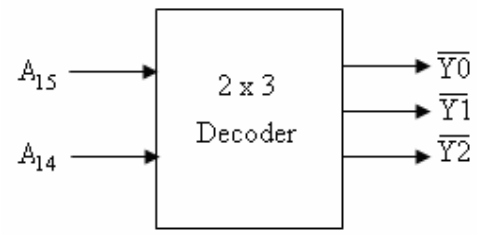
2- Most significant 2bits of the address line in a 64Kbyte memory system is connected through a 2x3 decoder.

a) Define the logical functions of the outputs $\overline{Y0}$, $\overline{Y1}$, $\overline{Y2}$ for the memory component activation table shown below.

0000H-3FFFH Device connected at $\overline{Y0}$ will be active (Active low)
4000H-BFFFH Device connected at $\overline{Y1}$ will be active (Active low)
C000H-FFFFH Device connected at $\overline{Y2}$ will be active (Active low)

b) Find the minimized logical expression of the decoder outputs in terms of address inputs

c) Draw the circuit schema only by using logical TTL gates, given in limited datasheets



3- An 8 bit CPU having 64Kbytes addressing capability will be connected to a memory block containing 1 piece of 27C256 EPROM, 1 piece of 62C128 static RAM, 1 piece of 28C64 EEPROM and an address decoder unit. EPROM will contain the program memory and the initial address after the reset indicates first address of this device (0000H)

Draw the circuit schema of the memory block and the related memory-addressing map of the described system using 74LS138 as decoder.