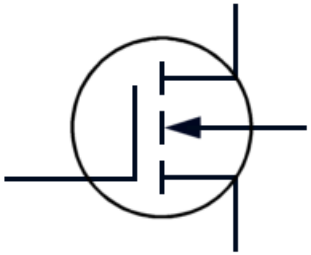
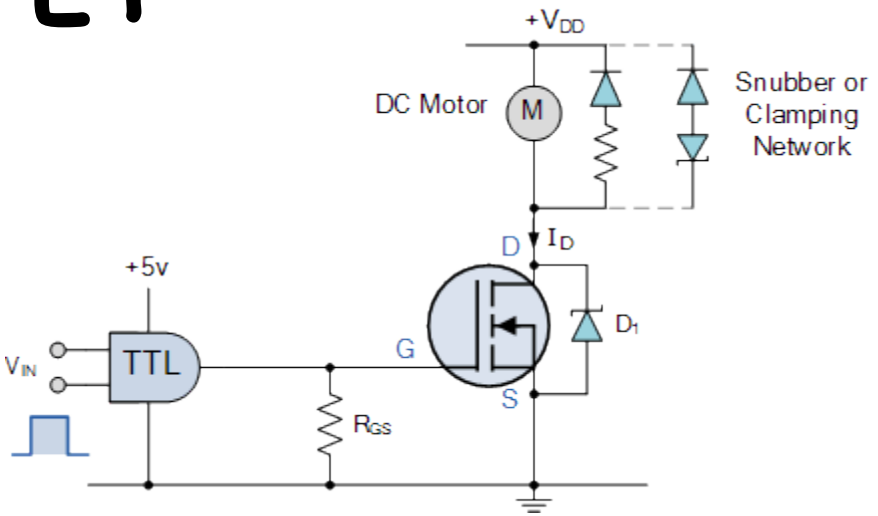
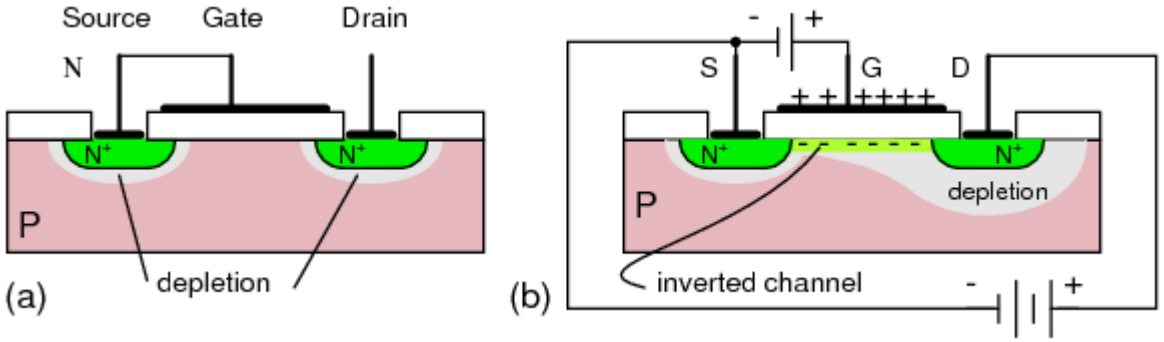
MOSFET




+VDD
DC Motor
M
Snubber or
Clamping
Network
D
ID
+5v
TTL
VIN
G
D1
S
RGS

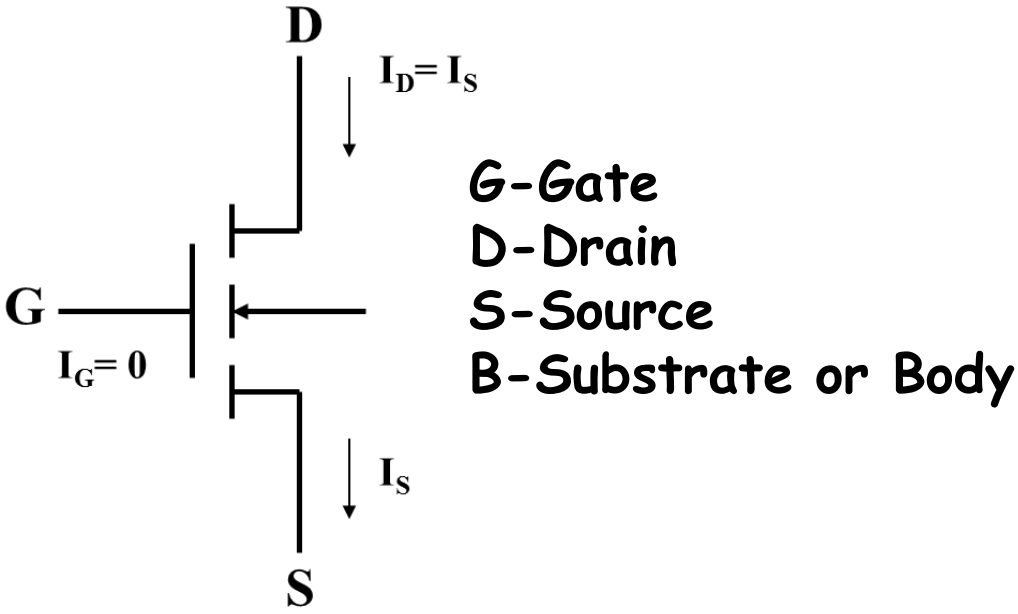

Source
Gate
Drain
N
N+
N+
P
depletion
(a)
-
+
S
G
D
N+
N+
depletion
P
inverted channel
(b)
-
+

MOSFET

MOSFET stands for **metal-oxide semiconductor field-effect transistor**.

Unlike BJT which is 'current controlled', the MOSFET is a voltage controlled device.

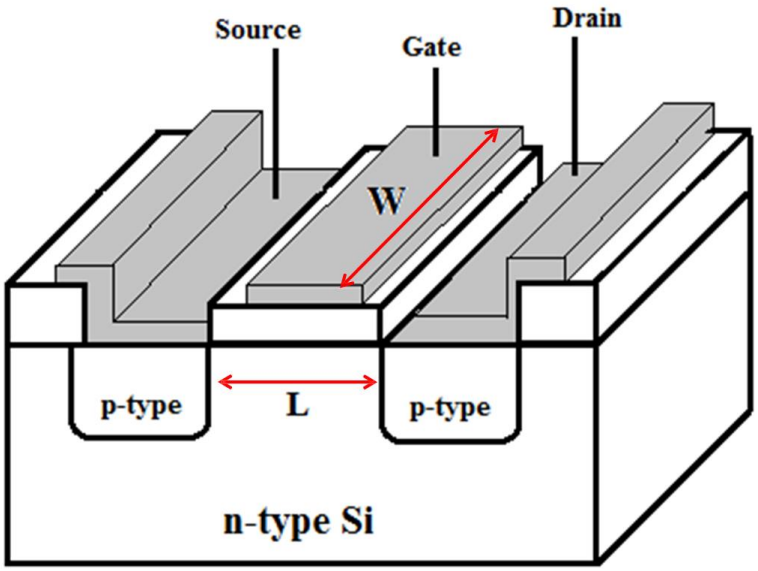
The MOSFET has "**gate**", "**Drain**", "**Source**" and "**Body**" terminals.



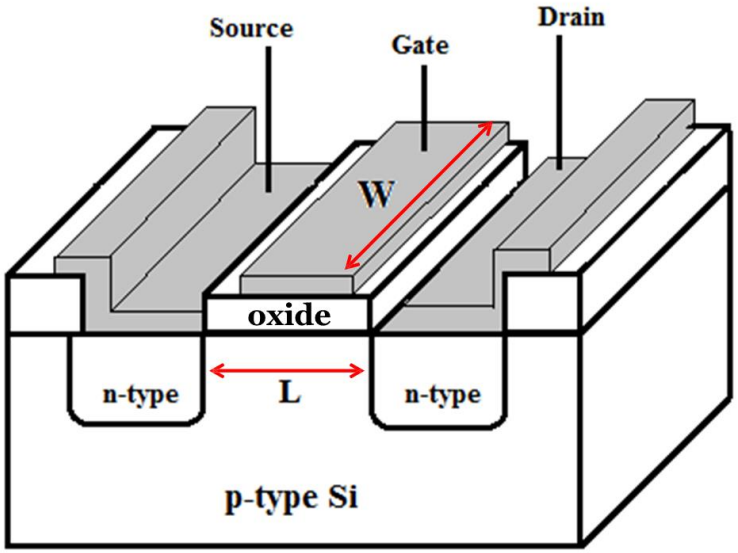
Types of MOSFETS

n-channel **Enhancement Mode** (nMOSFET)	p-channel **Enhancement Mode** (pMOSFET)
n-channel **Depletion Mode** (nMOSFET)	p-channel **Depletion Mode** (pMOSFET)

Cross-Sectional View of p channel Enhancement Mode Transistor



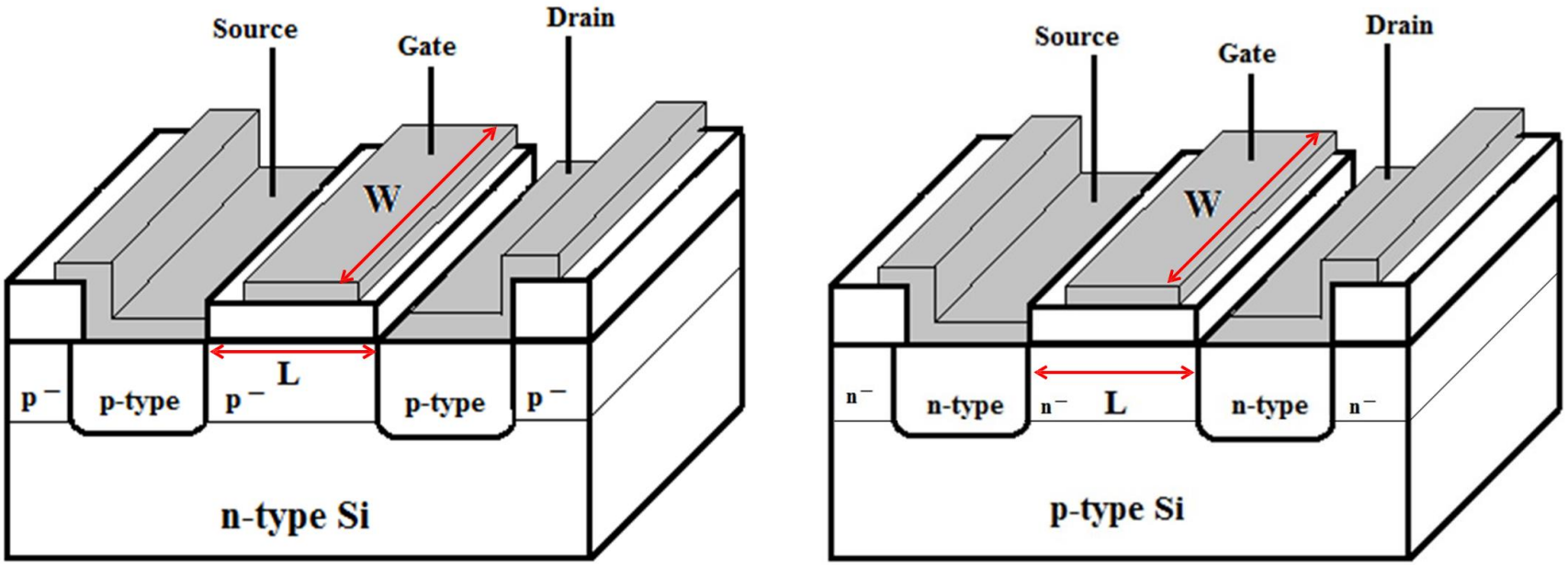
Cross-Sectional View of n channel Enhancement Mode Transistor



Enhancement mode

- **Also known as Normally Off transistors.**
  - A voltage must be applied to the gate of the transistor, at least equal to the threshold voltage, ***to create a conduction path between*** the source and the drain of the transistor before current can flow between the source and drain.

p channel **Depletion** Mode Transistor n channel **Depletion** Mode Transistor



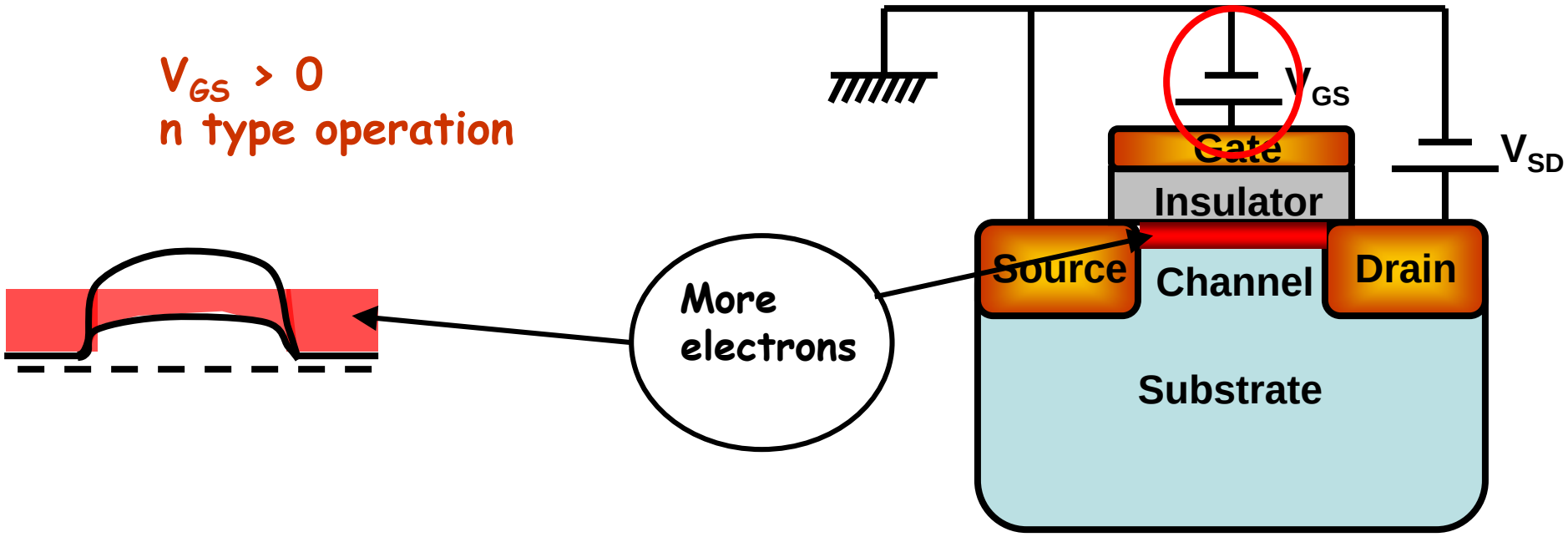
Depletion mode

- **Also known as Normally On transistors.**
  - A voltage must be applied to the gate of the transistor, at least equal to the threshold voltage, to ***destroy a conduction path between*** the source and the drain of the transistor to prevent current from flowing between the source and drain.

Operation of a Enhancement mode transistor

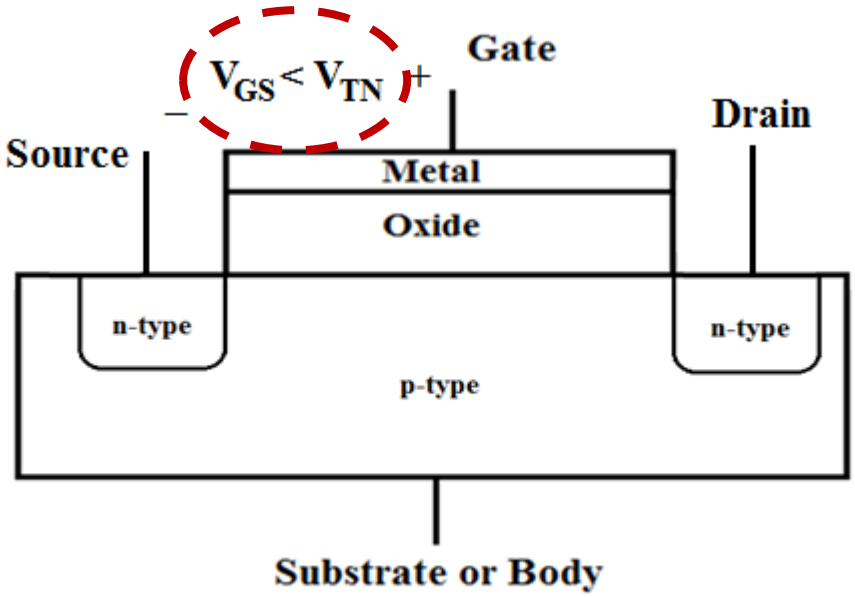
A voltage must be applied to the gate of the transistor, at least equal to the threshold voltage, ***to create a conduction path between*** the source and the drain

$V_{GS} > 0$
n type operation

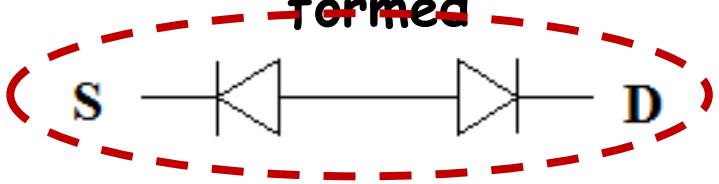


Positive gate bias attracts electrons into channel.
Channel now becomes more conductive

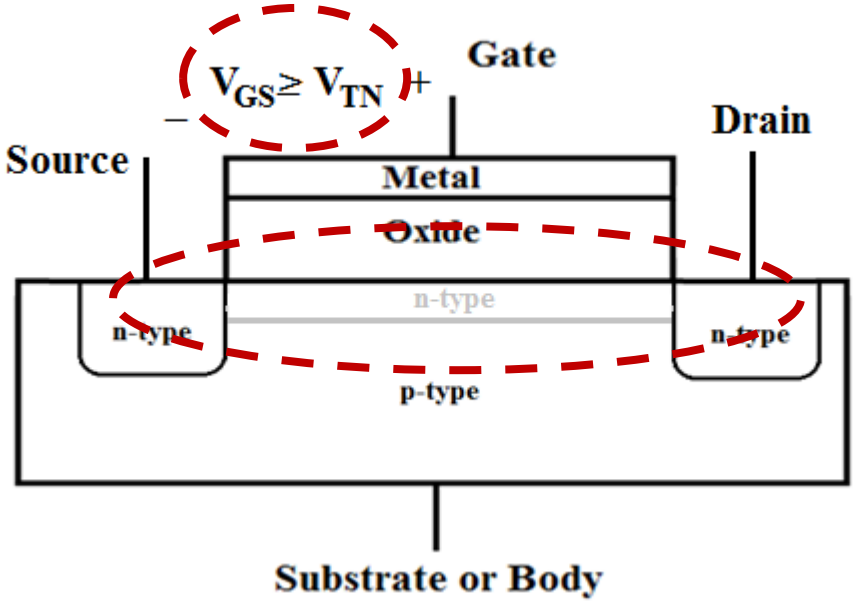
(Enhancement mode)

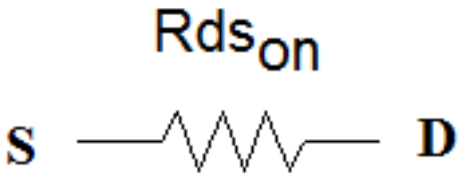


Before electron inversion layer is formed



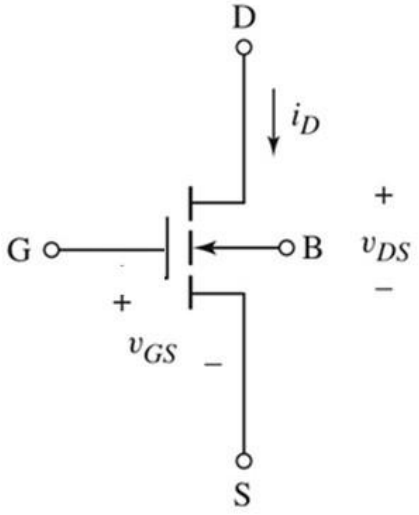
With no bias voltage applied to the gate terminal, there exists two back-to-back pn junctions between the drain and the source. No current flows from drain to source (the resistance will be on the order of 10^{12} Ω).





After electron inversion layer is formed

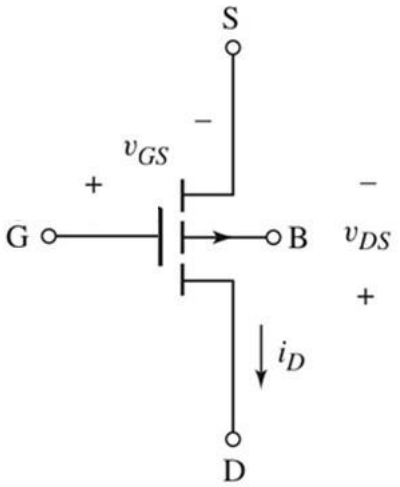
Symbols for n channel Enhancement Mode MOSFET



$V_{GS} \geq 0V$, $V_{DS} \geq 0V$

V_{TN} is positive

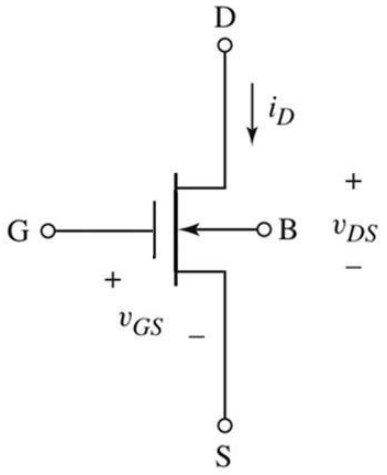
Symbols for p channel Enhancement Mode MOSFET



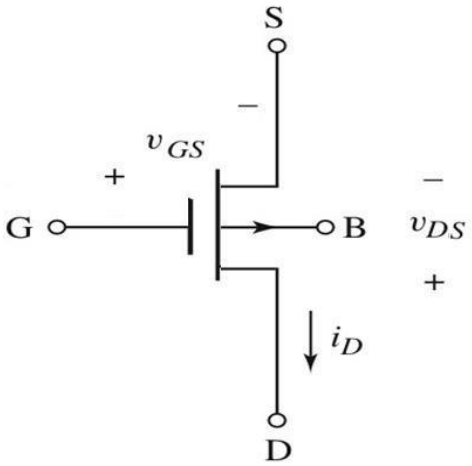
$V_{GS} \leq 0V$, $V_{DS} \leq 0V$

V_{TP} is negative

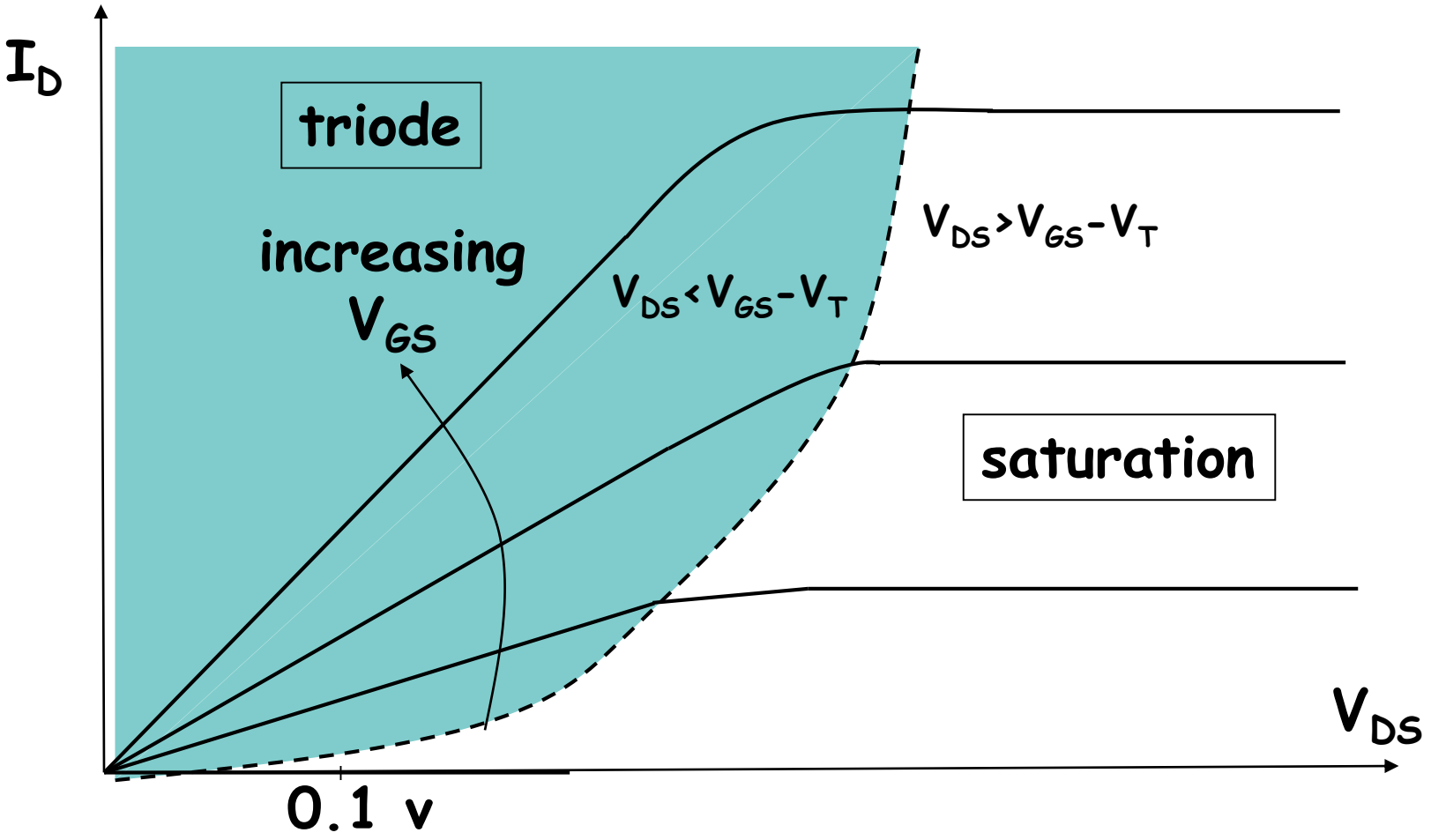
Symbols for n channel Depletion Mode MOSFET



Symbols for p channel Depletion Mode MOSFET

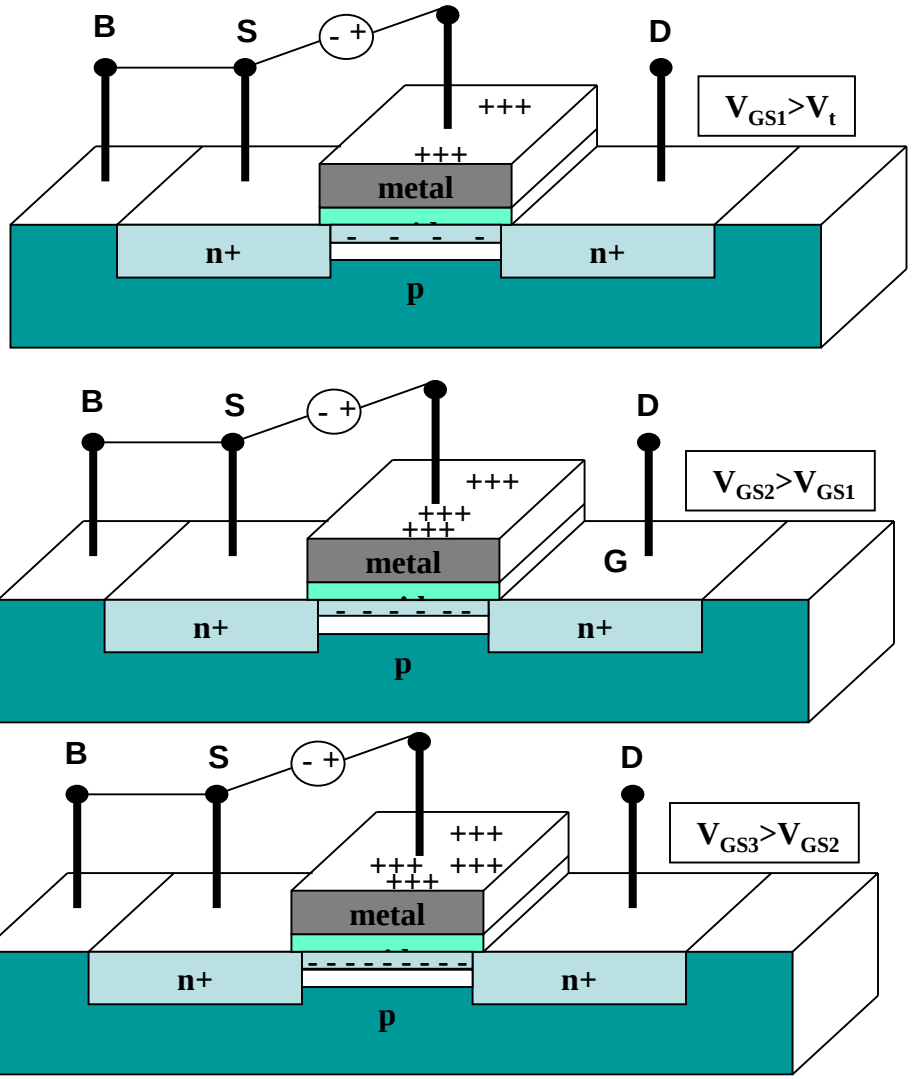


Working Modes *(Enhancement mode)*

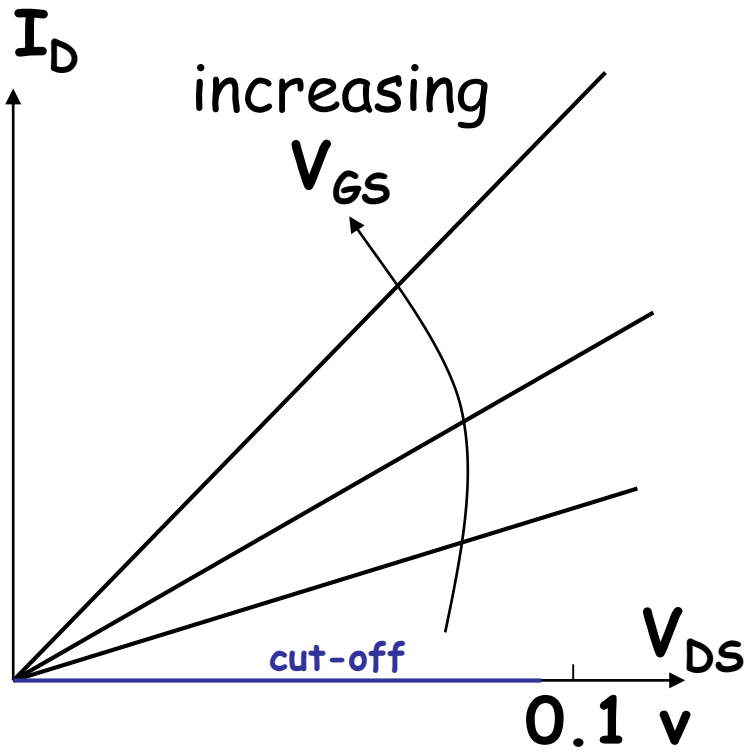


Triode Region *(Enhancement mode)*

A voltage-controlled resistor @small V_{DS}



Positive gate bias attracts electrons into channel.

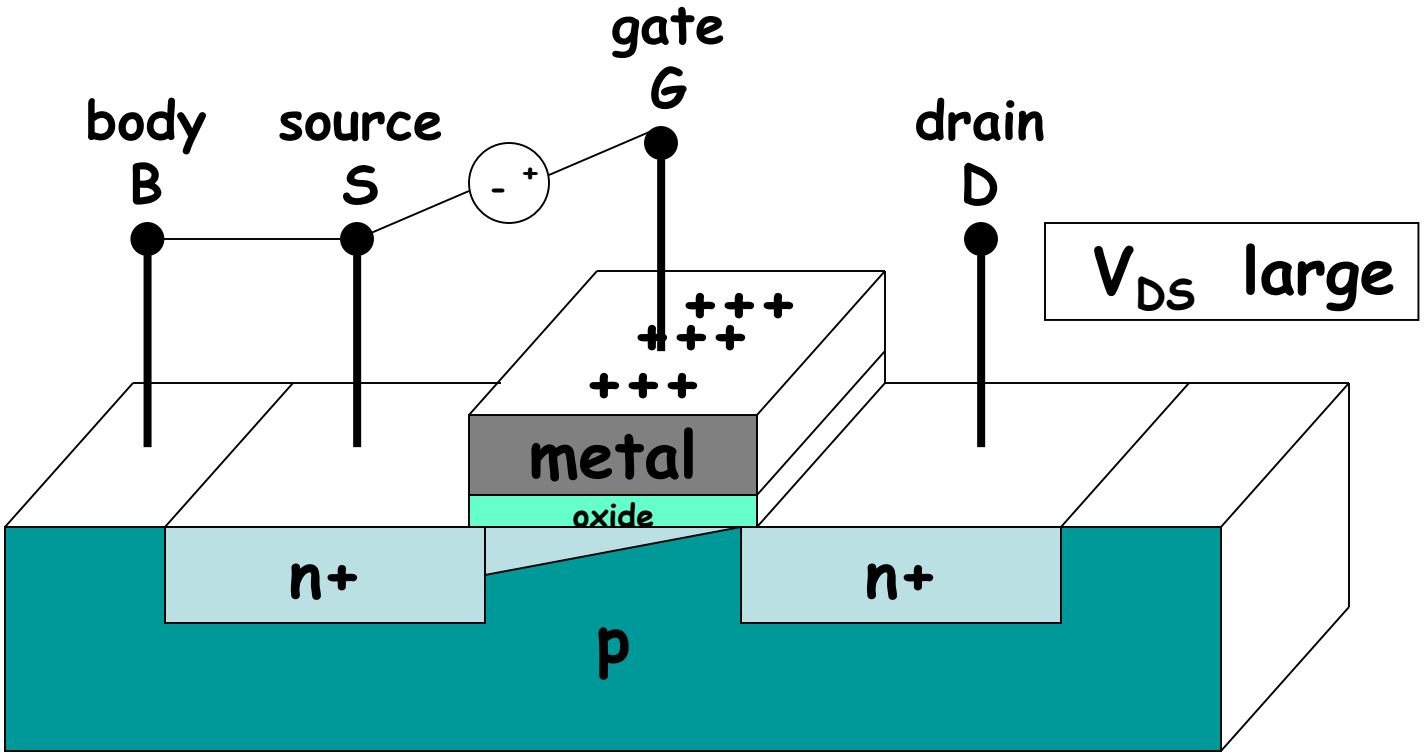


Increasing V_{GS} puts more charge in the channel, allowing more drain current to flow

Saturation Region *(Enhancement mode)*

occurs at large V_{DS}

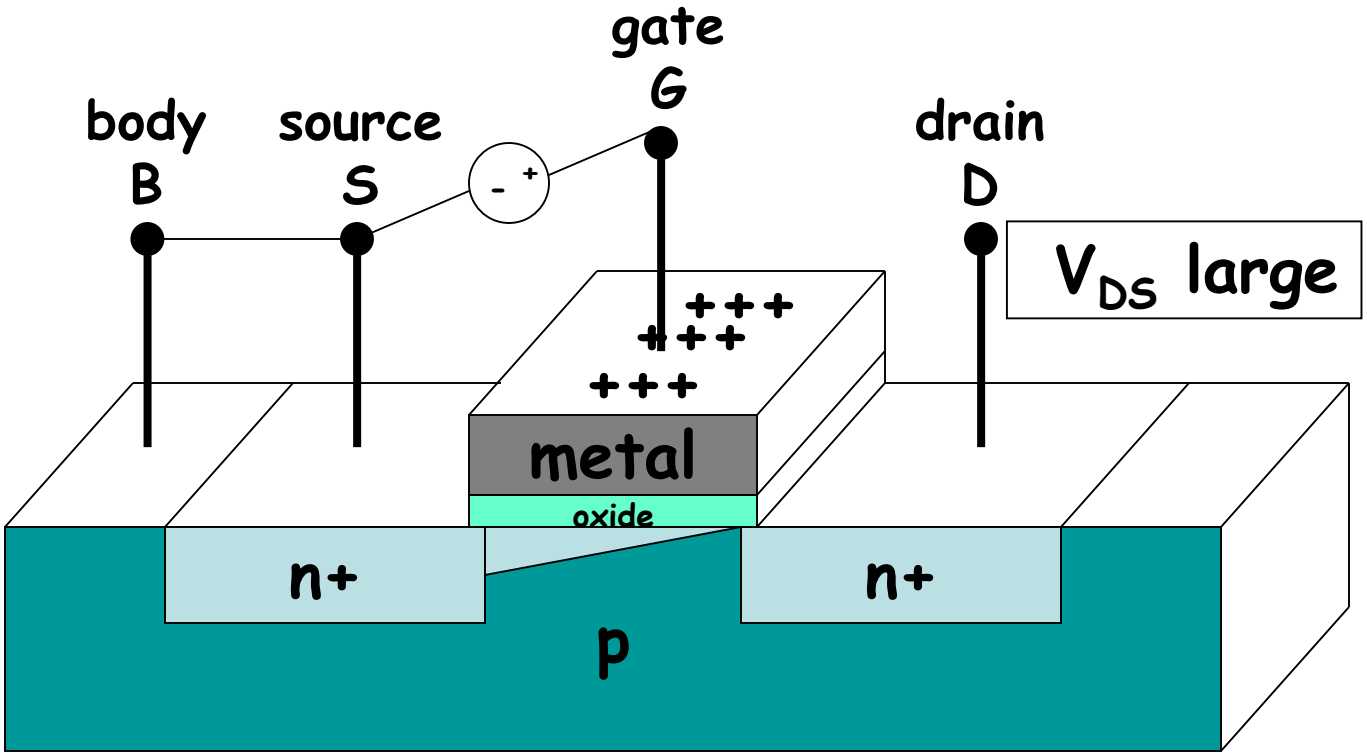
As the drain voltage increases, the *difference* in voltage between the drain and the gate becomes *smaller*. At some point, the difference is too small to maintain the channel near the drain → *pinch-off*



Saturation Region *(Enhancement mode)*

occurs at large V_{DS}

The *saturation region* is when the MOSFET experiences pinch-off. Pinch-off occurs when V_G - V_D is less than V_T.

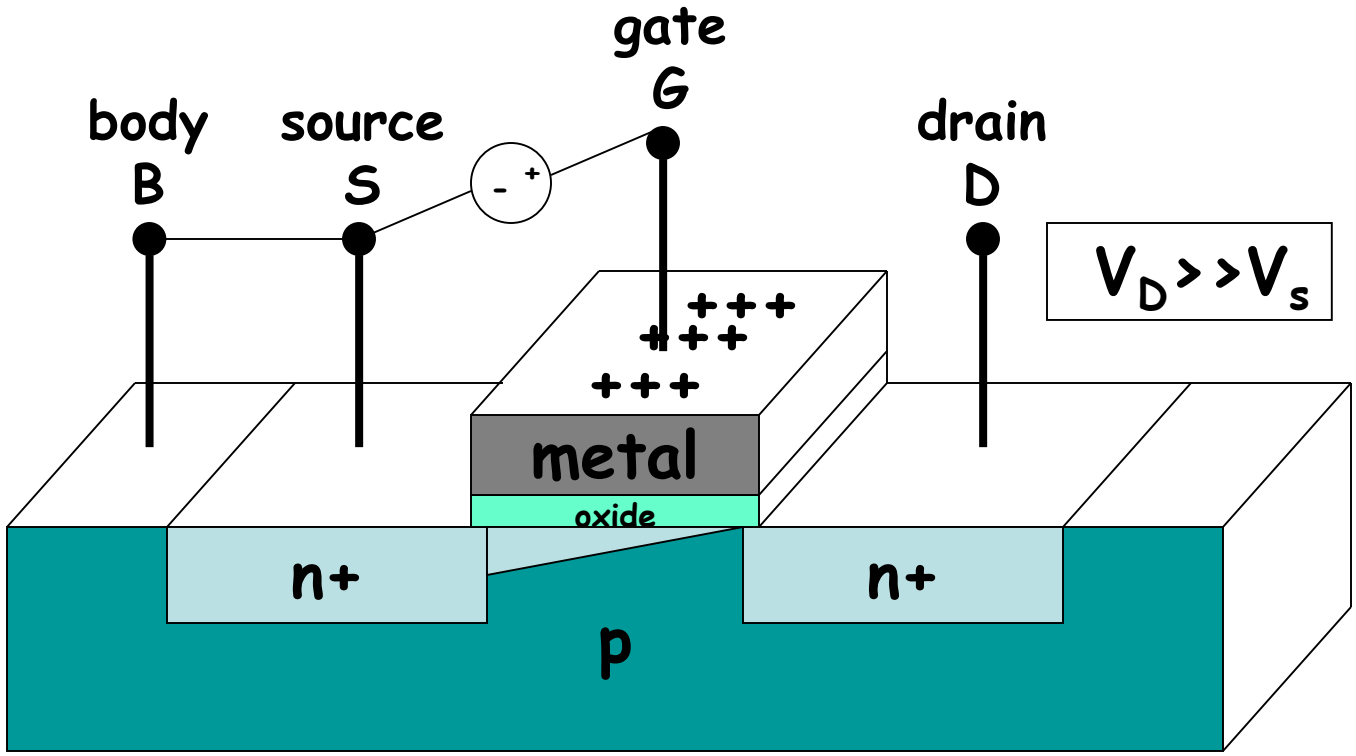


Saturation Region *(Enhancement mode)*

occurs at large V_{DS}

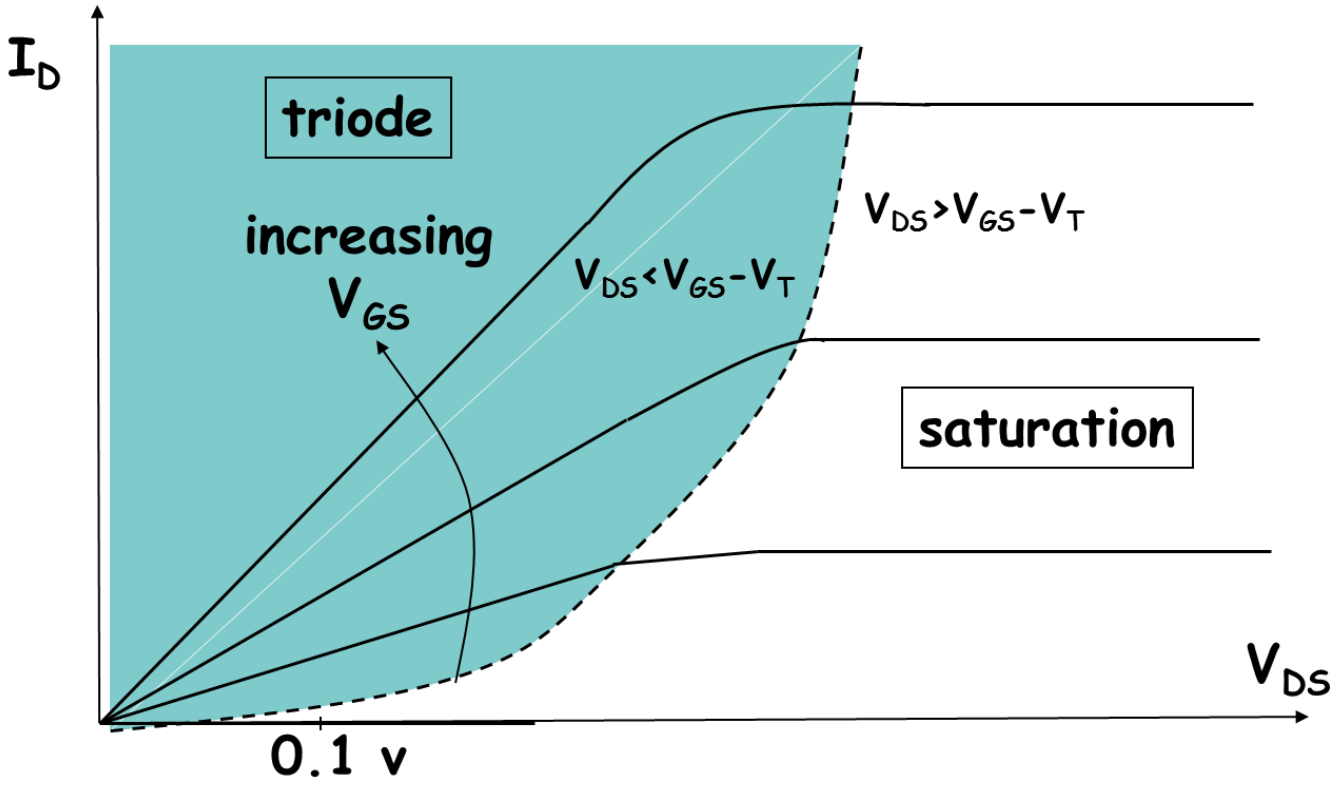
$V_{GS} - V_{DS} < V_T$ or $V_{GD} < V_T$

Or $V_{DS} > V_{GS} - V_T$



Saturation Region *(Enhancement mode)*

once pinch-off occurs, there is no further increase in drain current



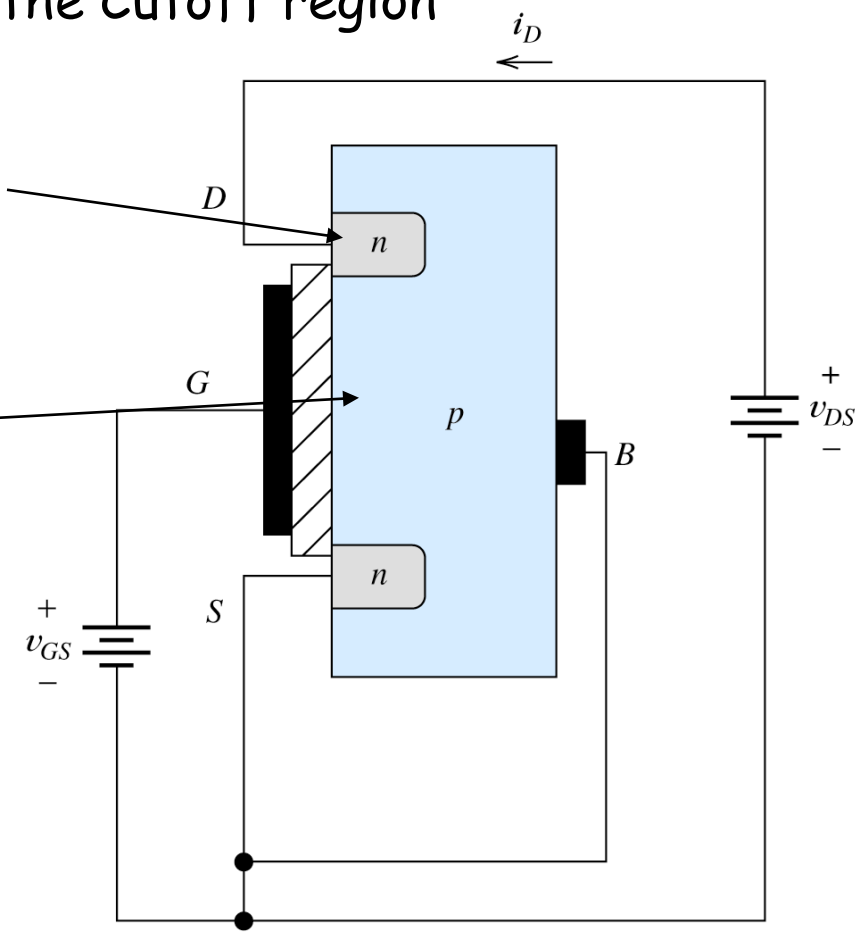
n-channel MOSFET Basic Operation *(Enhancement mode)*

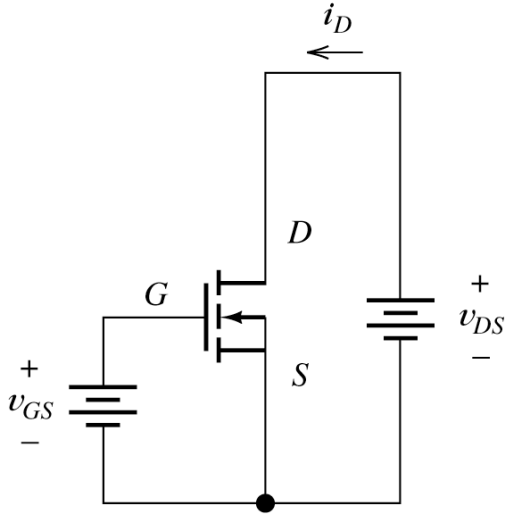
Operation in the Cutoff region

pn junction: reverse bias

i_D=0

for v_{GS}<V_{t0}

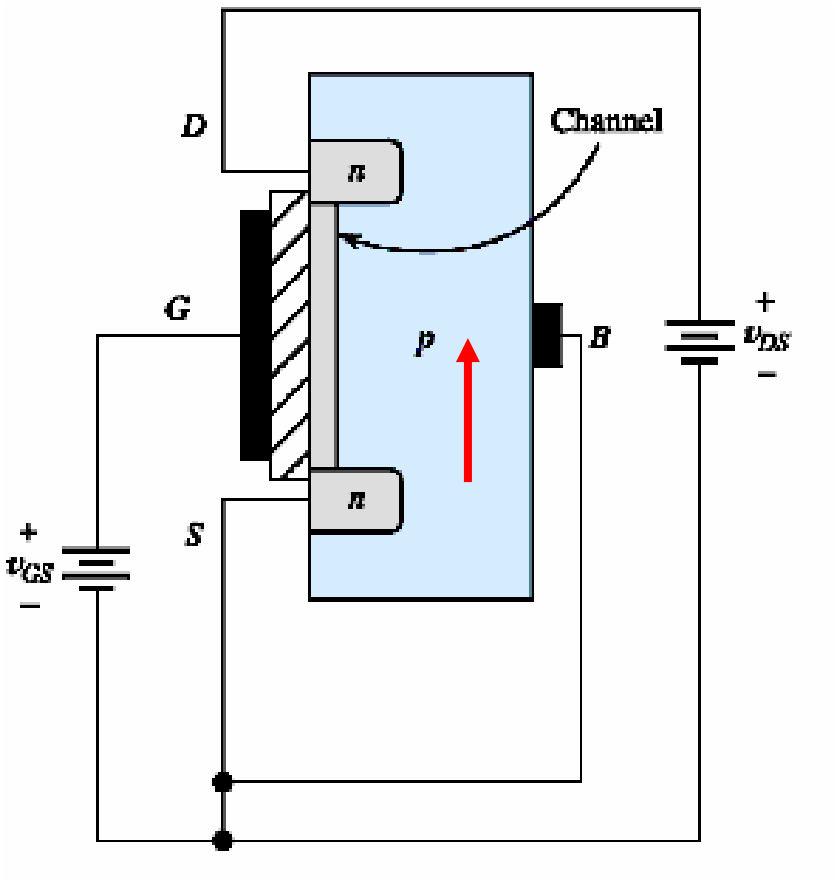




For $v_{GS} < V_{to}$, the pn junction between drain and body is reverse biased and $i_D = 0$.

When v_{GS}=0 then i_D=0 until v_{GS}>V_{t0} (V_{t0} -threshold voltage)

n-channel MOSFET Basic Operation



Operation in the Triode Region

$$i_D = K\left[2(v_{GS} - V_{t0})v_{DS} - v_{DS}^2\right]$$

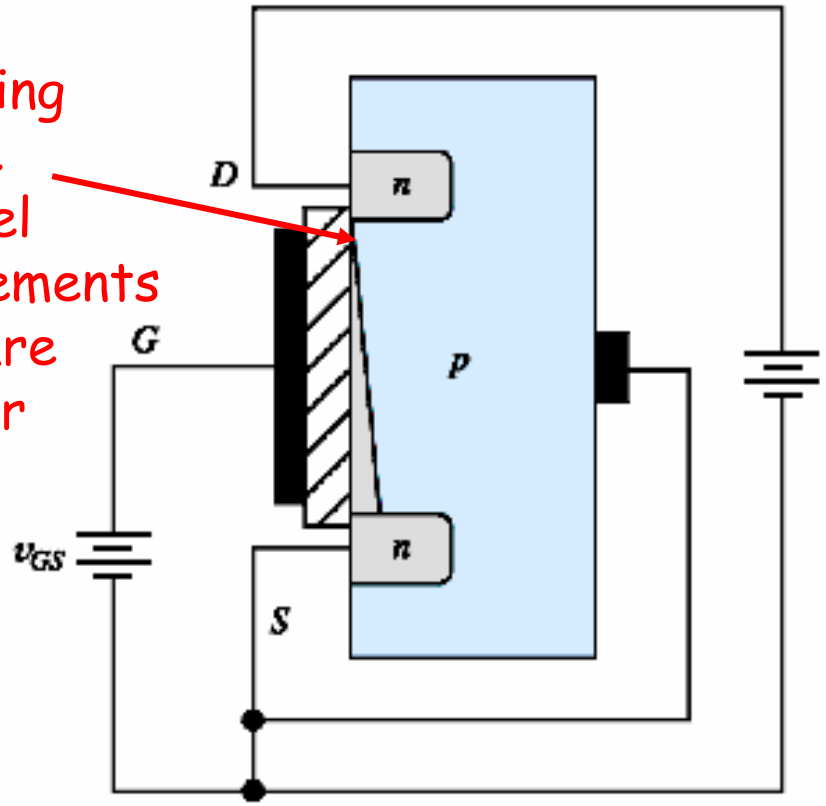
(K is defined by the electrical and physical parameters of the MOSFET)

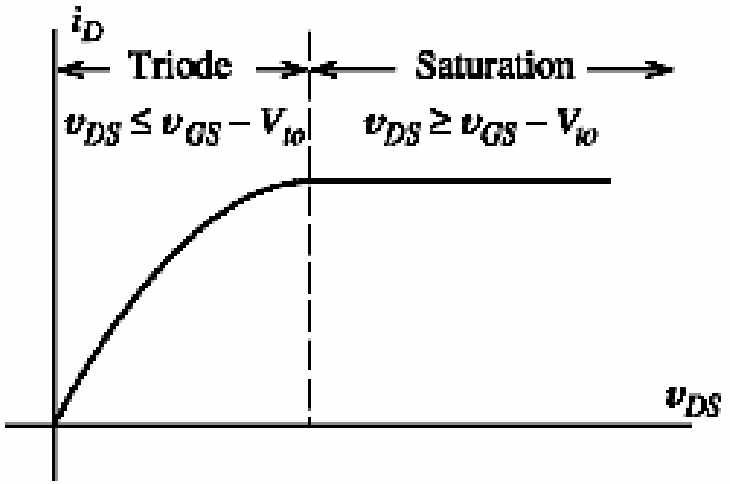
n-channel MOSFET Basic Operation

Operation in the Saturation Region (v_{DS} is increased)

$$i_D = K\left(v_{GS} - V_{t0}\right)^2$$

Tapering of the channel - increments of i_D are smaller when v_{DS} is larger

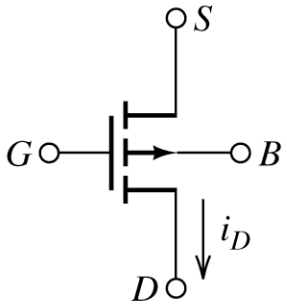




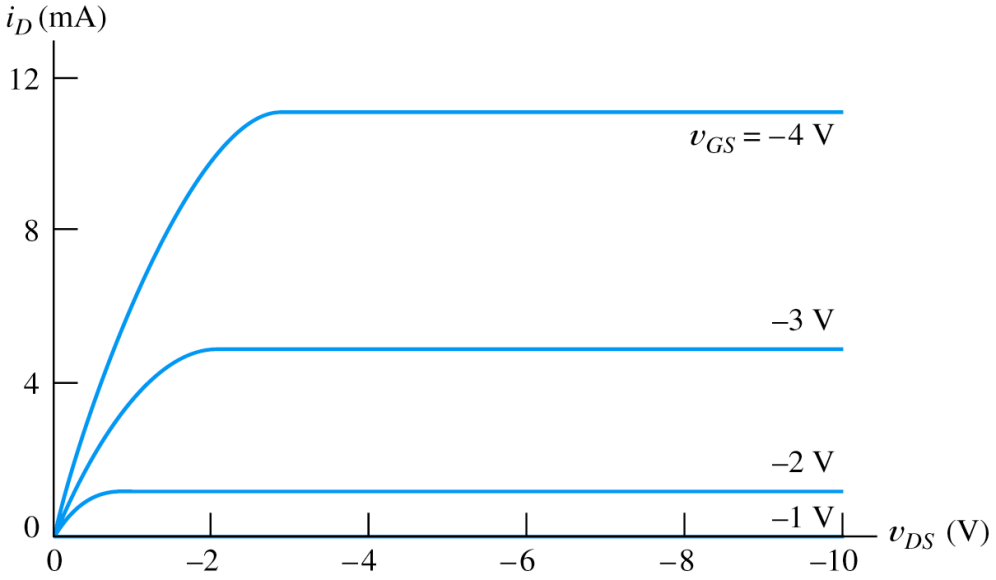
p-channel MOSFET Basic Operation

It is constructed by interchanging the *n* and *p* regions of n-channel MOSFET.

Symbol

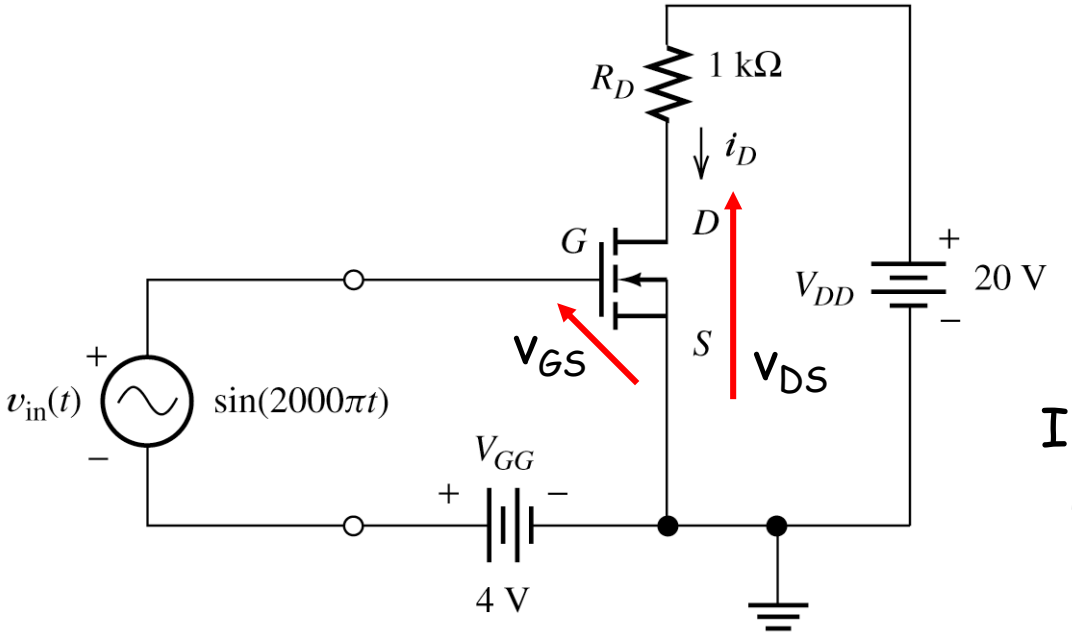


Circuit symbol for PMOS transistor.



Load-Line Analysis of NMOS Amplifier

It is a graphical analysis similar to load-line analysis of pn diode.



Simple NMOS amplifier circuit.

We look for the operating point

Circuit Analysis:

Input loop

$$v_{GS}(t) = v_{in}(t) + V_{GG}$$

$$v_{GS}(t) = \sin(200\pi t) + 4$$

Output loop

$$V_{DD} = R_D i_D(t) + v_{DS}(t)$$

$$v_{DS} = vD - vS$$

$$v_{GS} = vG - vS$$

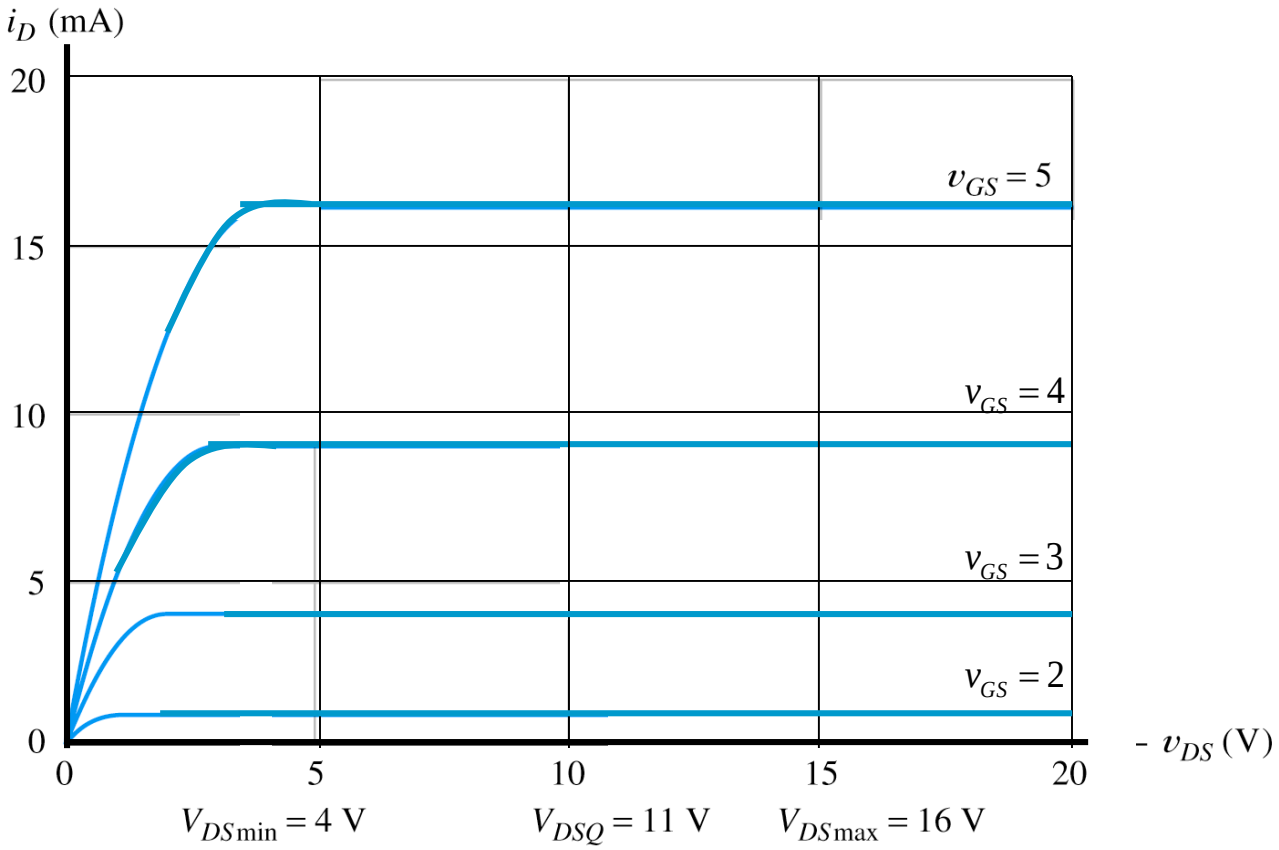
Load line

$$20 - R_D i_D(t) = v_{DS}(t)$$

Load-Line Analysis of NMOS Amplifier

Exercise:

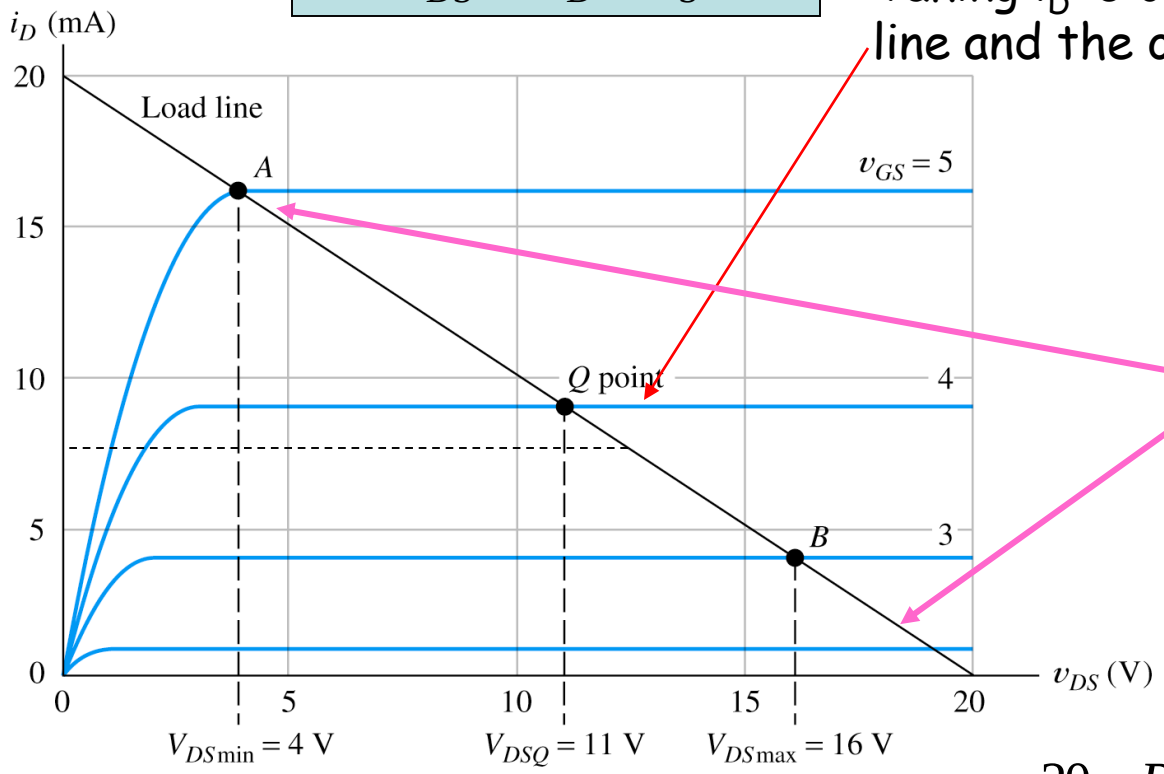
Draw the Load line $20 - R_D i_D(t) = v_{DS}(t)$ R_D= 1 kΩ



Load-Line Analysis of NMOS Amplifier

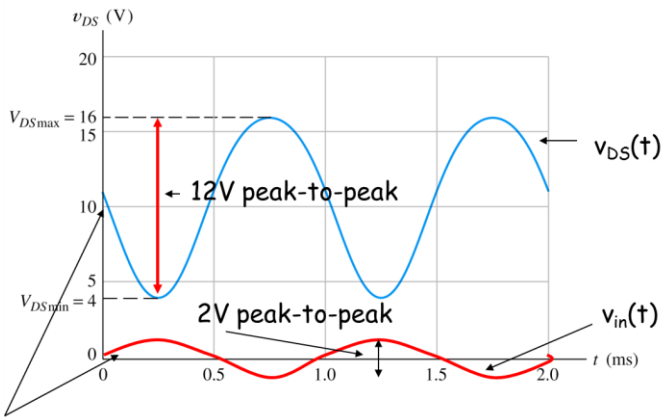
Load line $v_{DS} = v_D - v_S$

Taking i_D=0 or v_{DS}=0 we find out the load line and the operating point Q for V_{GS}=4V

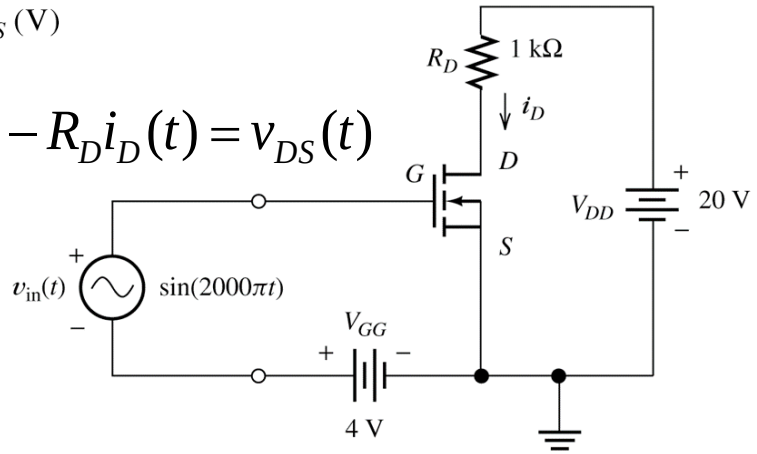


$$v_{GS}(t) = v_{in}(t) + V_{GG}$$

Points A & B intersection of curve and the load-line for the maximum and the minimum gate voltage



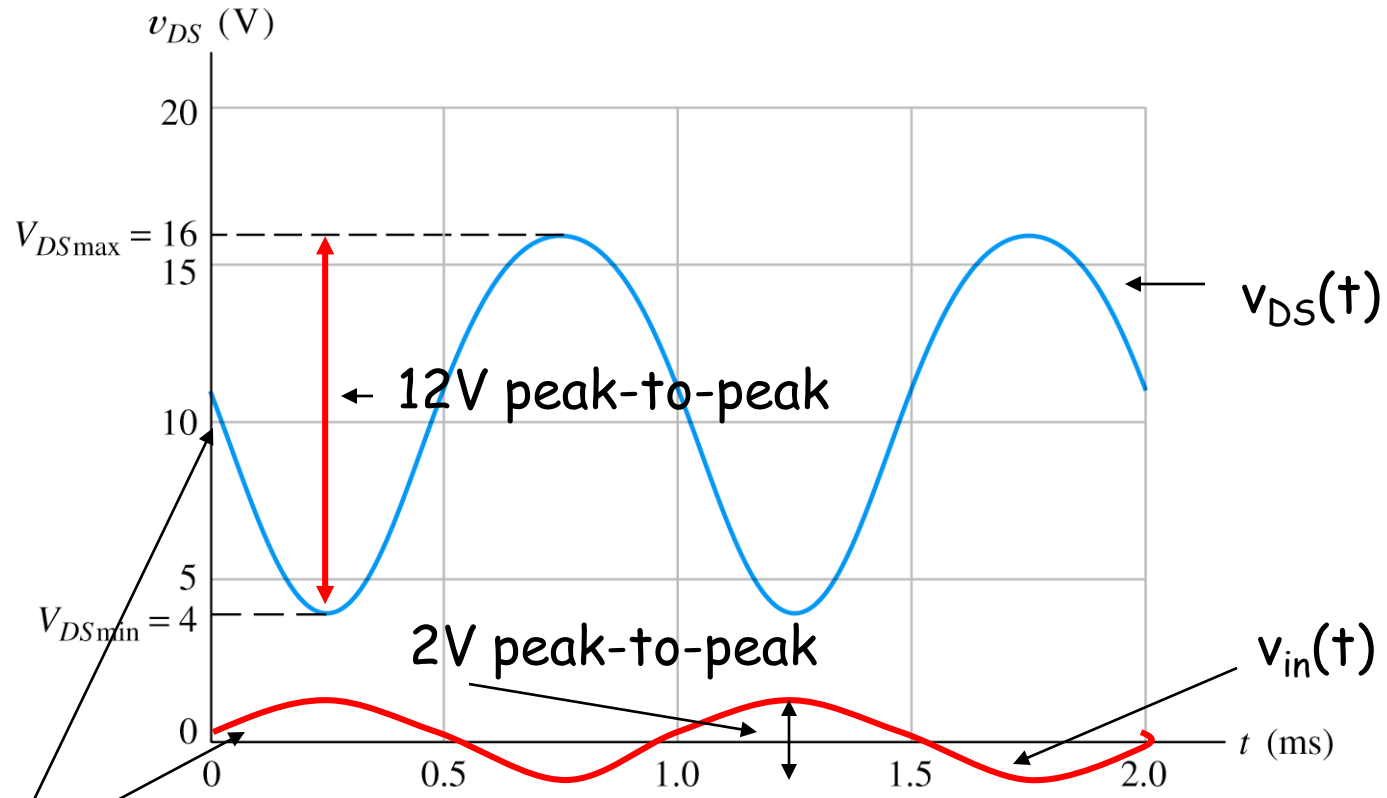
$$20 - R_D i_D(t) = v_{DS}(t)$$



Simple NMOS amplifier circuit.

Load-Line Analysis of NMOS Amplifier

Input signal $v_{in}(t) = 1\sin(200\pi t)$ (peak-to-peak amplitude is 2V)



The positive peak of the input occurs at the same time as the min. value of v_{DS}. The output is not a symmetrical sinusoid! (nonlinear distortion)

Self Bias Circuits

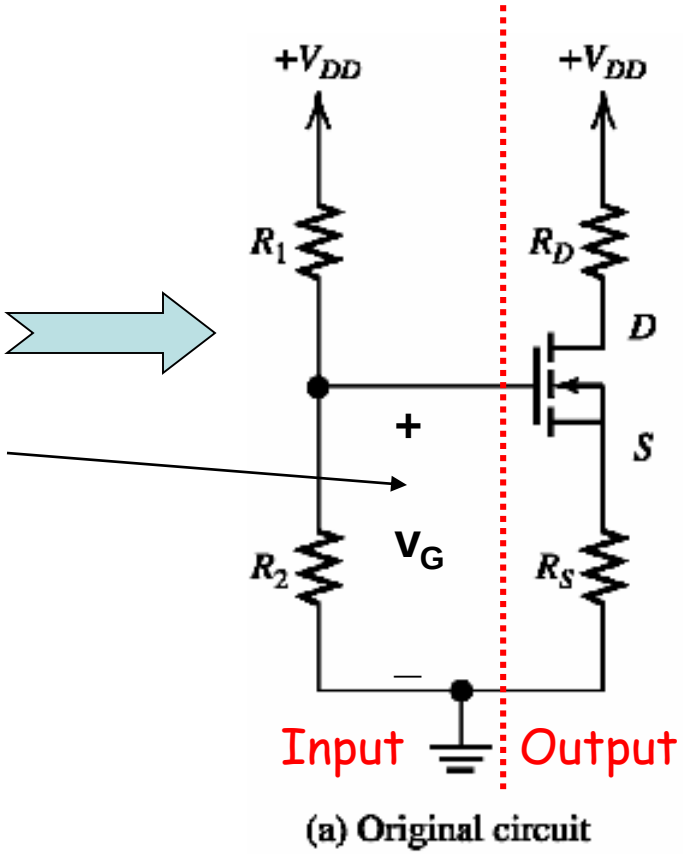
Analysis of amplifier circuits is often undertaken in two steps:

(1) The DC circuit analysis to determine the Q point. It involves the nonlinear equation solution or the load-line method. This is called bias analysis

The fixed-plus self-bias circuit

Exercise:

Find V_G voltage as a function of V_{DD}, R_1 and R_2



(a) Original circuit

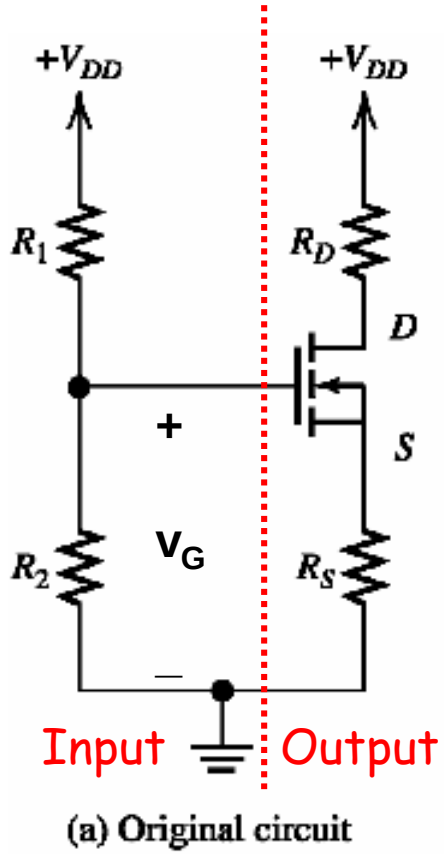
Self Bias Circuits

Analysis of amplifier circuits is often undertaken in two steps:

(1) The DC circuit analysis to determine the Q point. It involves the nonlinear equation solution or the load-line method. This is called bias analysis

The fixed-plus self-bias circuit

$$V_G = V_{DD}\frac{R_2}{R_1 + R_2}$$



(a) Original circuit

Self Bias Circuits

Analysis of amplifier circuits is often undertaken in two steps:

(1) The DC circuit analysis to determine the Q point. It involves the nonlinear equation or the load-line method. This is called bias analysis

(2) Use a linear small-signal equivalent circuit to determine circuit parameters

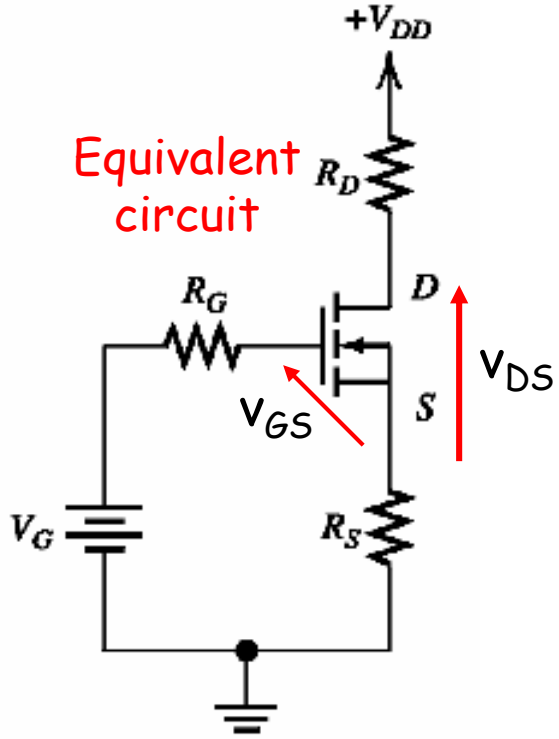
Analysis…

For saturation region

$$V_G = v_{GS} + R_S i_D$$

$$i_D = K\left(v_{GS} - V_{t0}\right)^2$$

find v_{GS}



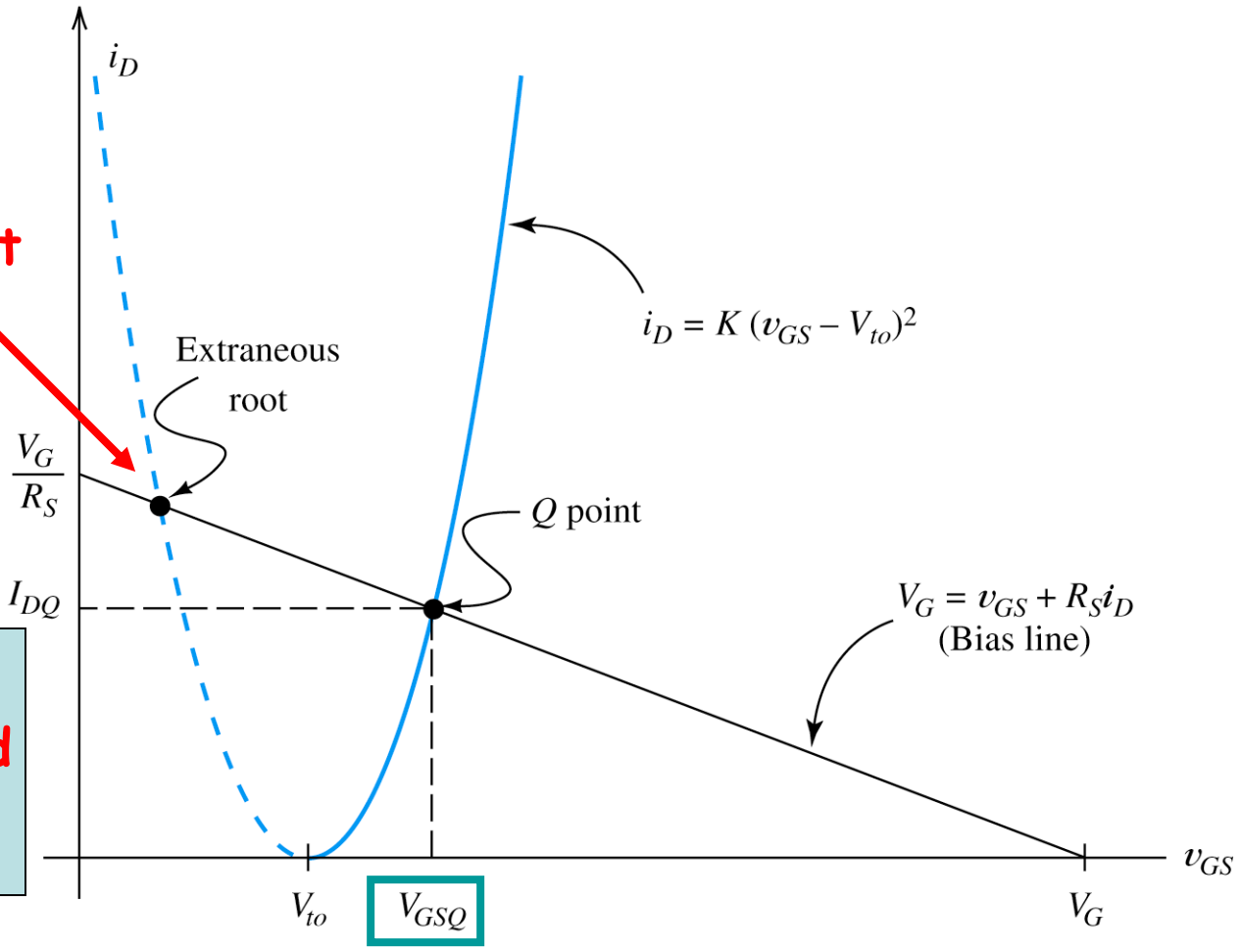
(b) Gate bias circuit replaced by its Thévenin equivalent

Self Bias Circuits

For saturation region

Plot of $V_G = v_{GS} + R_S i_D$ and $i_D = K(v_{GS} - V_{t0})^2$

Disregarded root for $v_{GS} < V_{t0}$



Use only larger root for v_{GS} and smaller for i_D

Self Bias Circuits

Analysis of amplifier circuits is often undertaken in two steps:

(1) The dc circuit analysis to determine the Q point. It involves the nonlinear equation or the load-line method. This is called bias analysis

(2) Use a linear small-signal equivalent circuit to determine circuit parameters

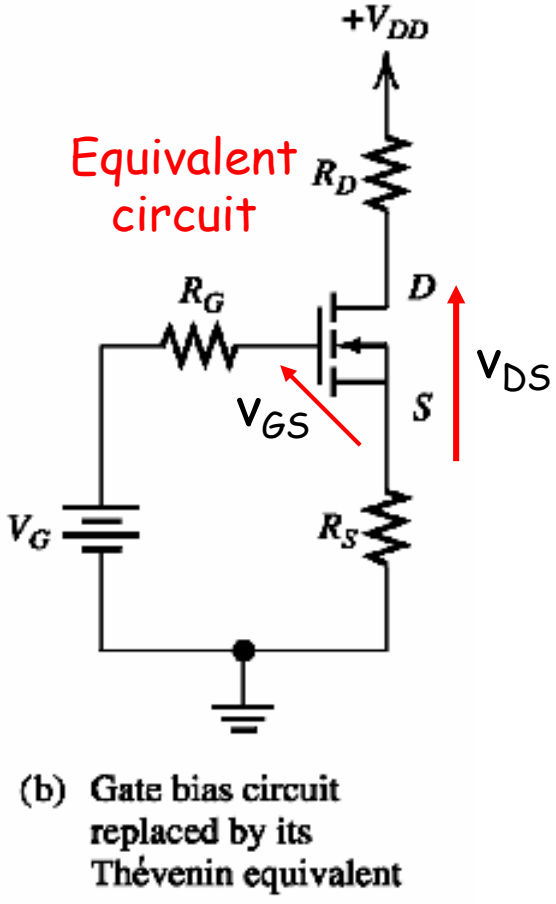
Analysis…

find i_D

For saturation region

$$i_D = K\left(v_{GS} - V_{t0}\right)^2$$

$$v_{DS} = V_{DD} - \left(R_D + R_S\right) i_D$$



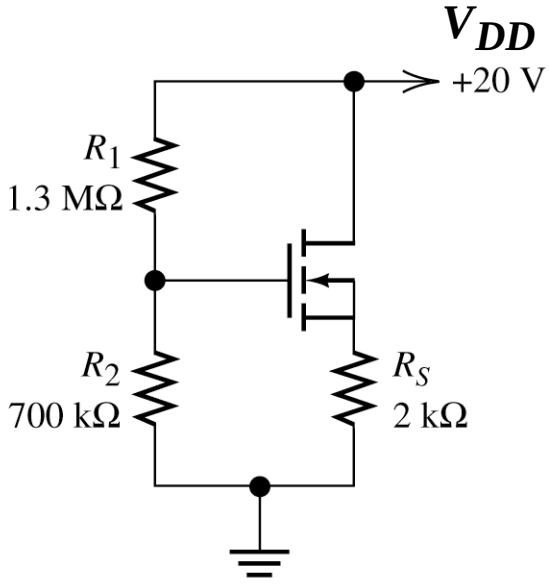
(b) Gate bias circuit replaced by its Thévenin equivalent

Self Bias Circuits (For saturation region)

Analyze the self-bias circuit shown. The transistor has K=1mA/V^2, V_{to}=2V.

$$V_G = V_{DD}\frac{R_2}{R_1 + R_2}$$

$$\left.\begin{aligned} V_G &= v_{GS} + R_S i_D \\ i_D &= K\left(v_{GS} - V_{t0}\right)^2 \end{aligned}\right\} \text{ find } v_{GS}$$



find i_D $\quad i_D = K\left(v_{GS} - V_{t0}\right)^2$

find v_{DS} $\quad v_{DS} = V_{DD} - (R_S)i_D$

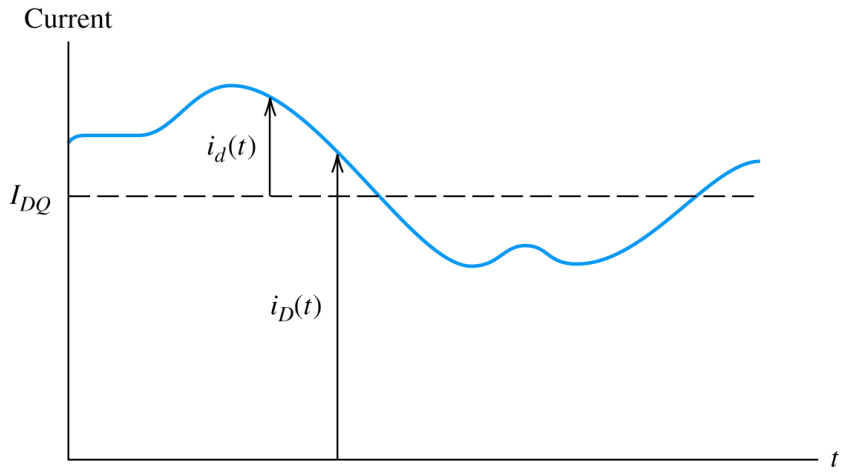
Small-Signal Equivalent Circuit for FETs

Output signal from an amplifier using MOSFET can be effectively modulated by small changes of input signal current. In this way it is possible to make small changes from the Q point.

Symbols:
The total quantities: $i_D(t)$, $v_{GS}(t)$
The DC point values: I_{DQ}, V_{GSQ}
The signal $i_d(t)$, $v_{gs}(t)$

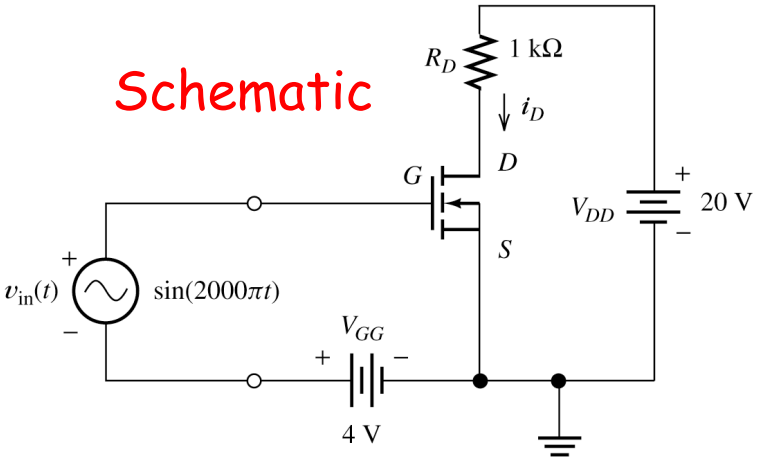
$$v_{GS}(t) = V_{GSQ} + v_{gs}(t)$$

$$i_D(t) = I_{DQ} + i_d(t)$$



Small-Signal Equivalent Circuit -Transconductance

Schematic

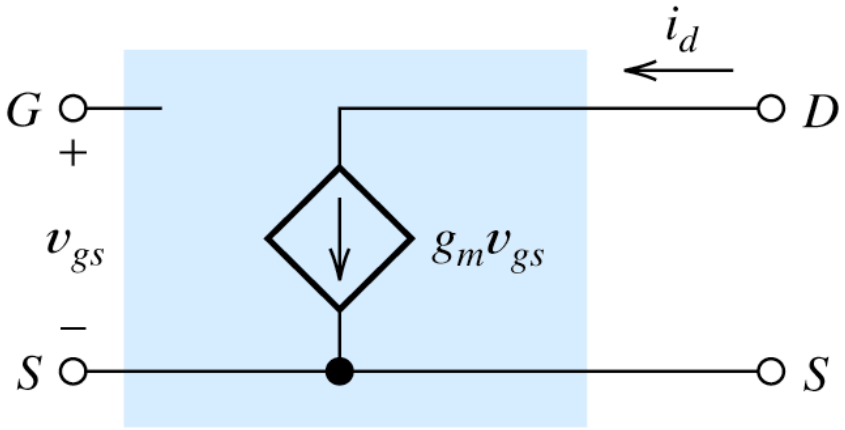


Simple NMOS amplifier circuit.

We define the transconductance as

$$g_m = \frac{i_d(t)}{v_{gs}(t)}$$

$$i_d(t) = g_m v_{gs}(t)$$



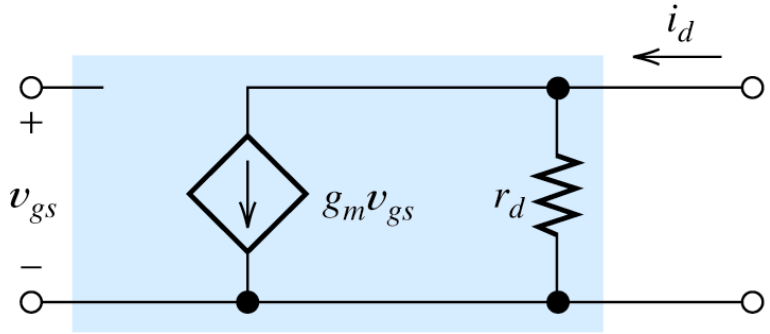
$$g_m = 2\sqrt{KI_{DQ}}$$

Small-signal equivalent circuit for FETs.

More Complex Equivalent Circuits

For more accurate analyses of FET transistor we have to add more components to an equivalent circuit.

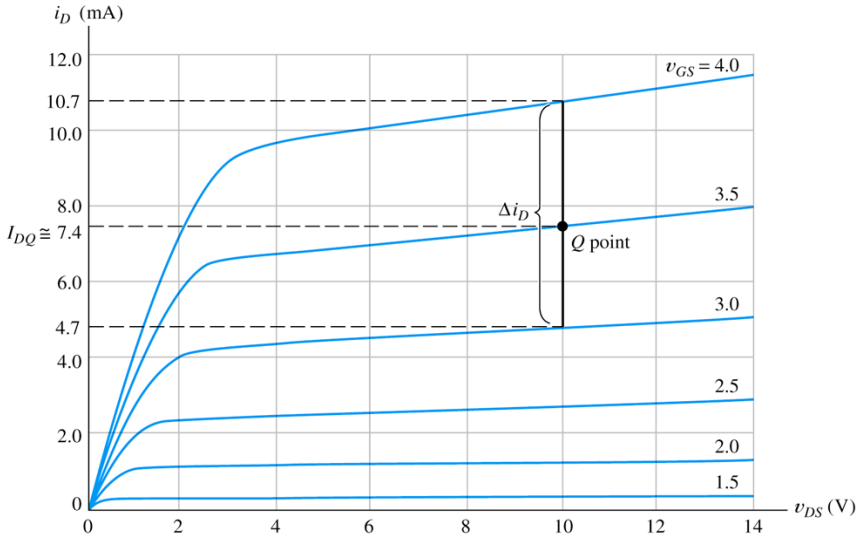
Drain resistor: account for the effect of v_{DS} on the drain current



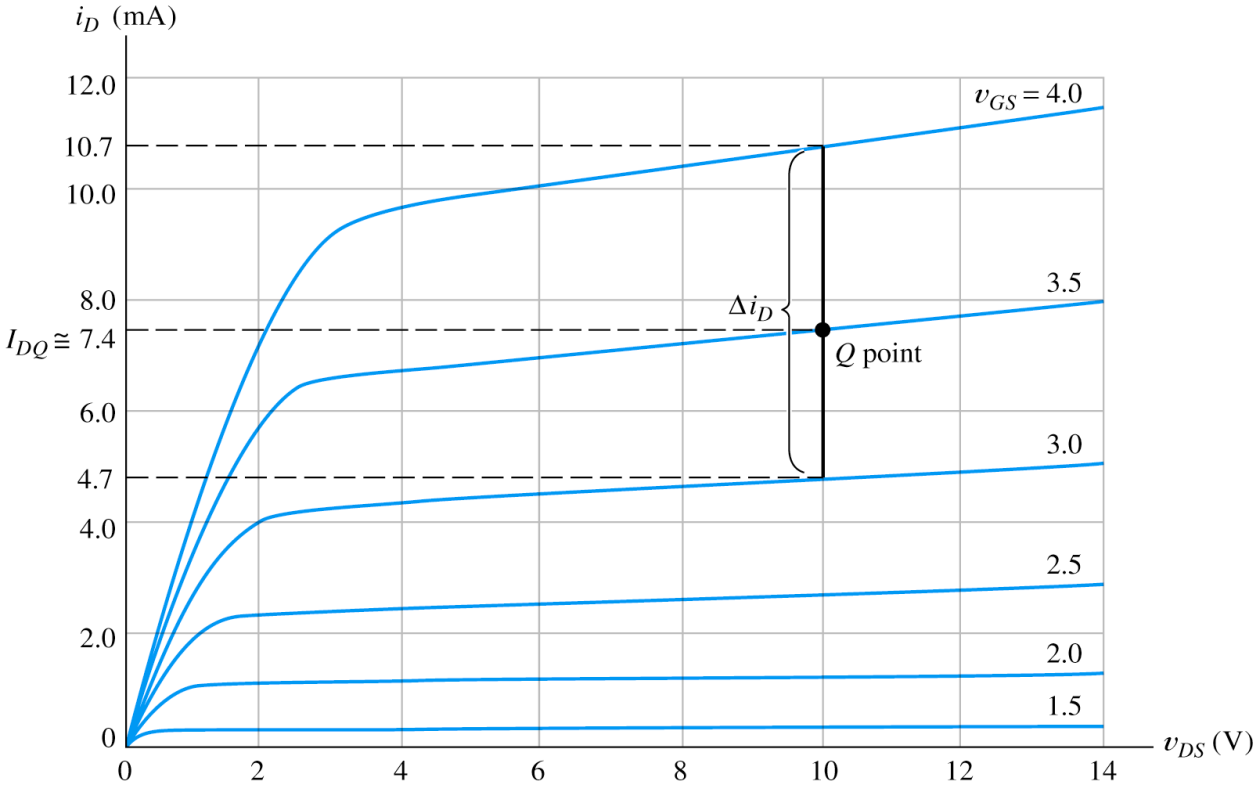
Correction for i_d

$$i_d(t) = g_m v_{gs}(t) + v_{ds}/r_d$$

FET small-signal equivalent circuit that accounts for the dependence of i_D on v_{DS}.



Drain Resistance Calculation

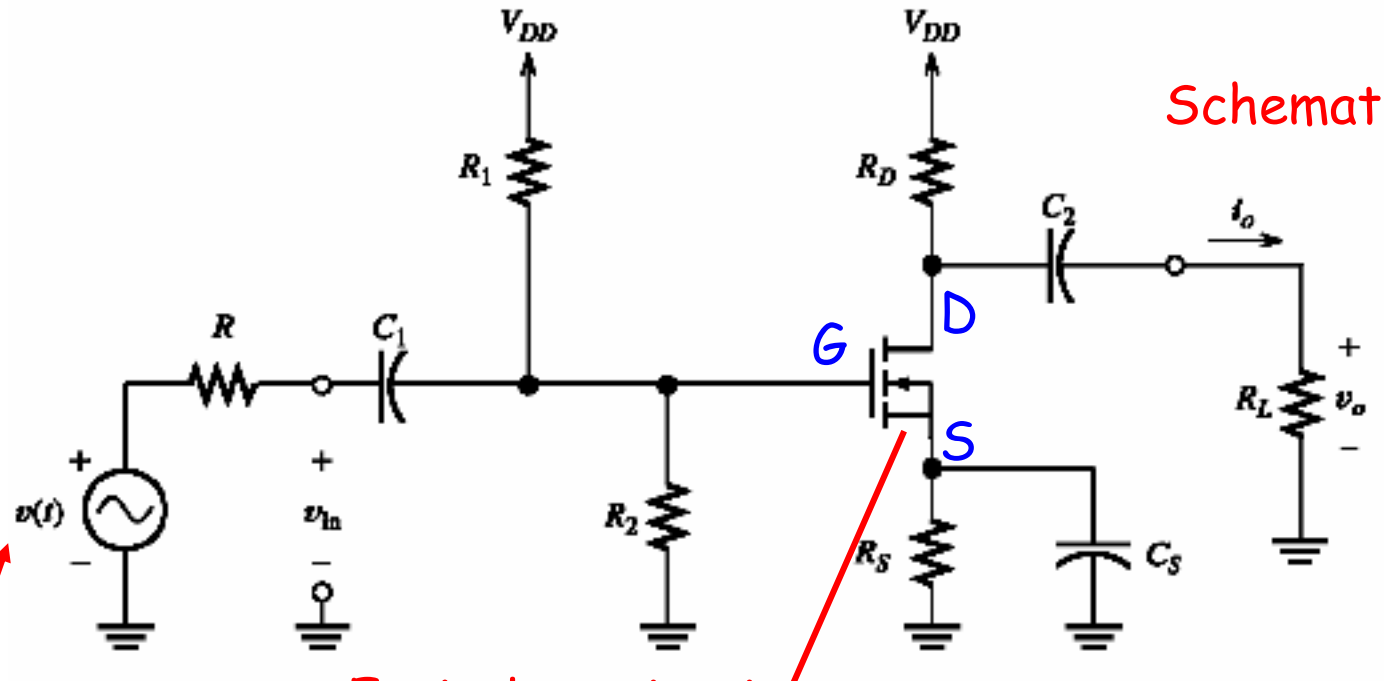


$$\frac{1}{r_d} = \frac{\Delta i_D}{\Delta v_{DS}}$$

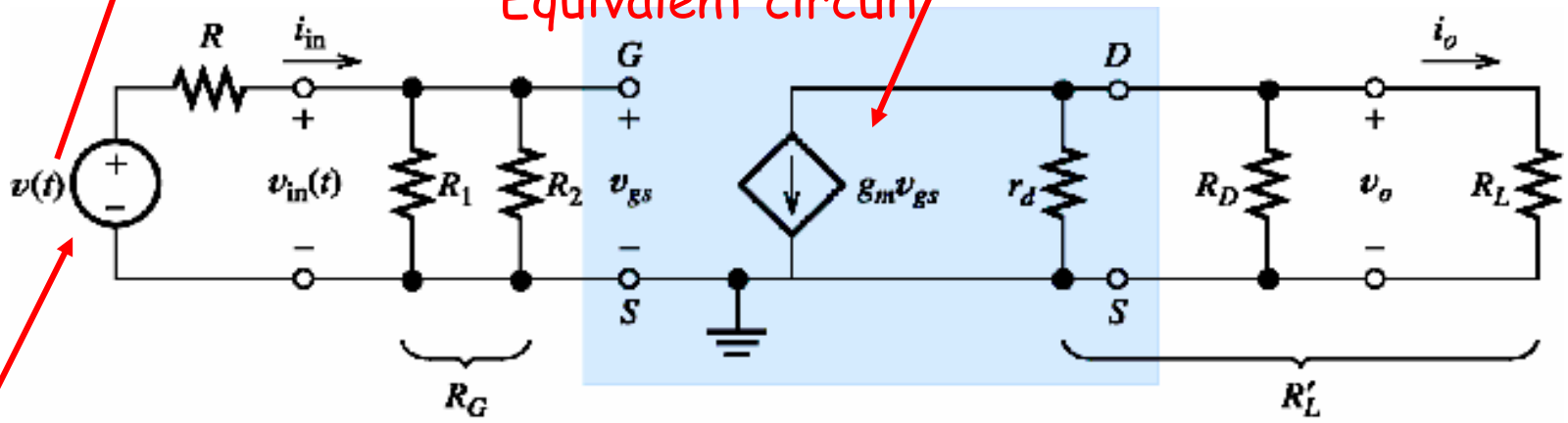
so at v_{GS}=4V

$$\frac{1}{r_d} = \frac{\Delta i_D}{\Delta v_{DS}} = \frac{(10.7-10)mA}{(10-6)V} = \frac{0.7}{4} mS = 0.175\,mS \qquad r_d = 5.7k\Omega$$

Common-Source Amplifier



Equivalent circuit



The dc supply voltage acts as a short circuit for the ac current.

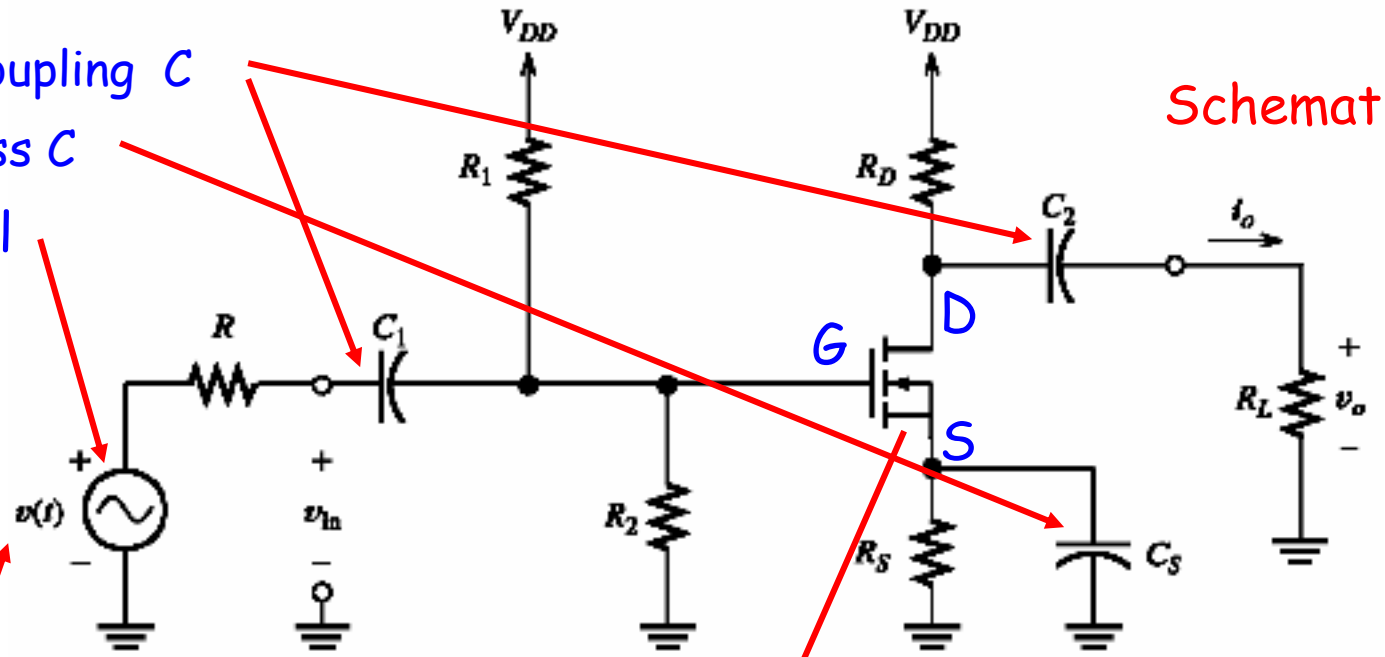
Common-Source Amplifier

C_1, C_2 -coupling C

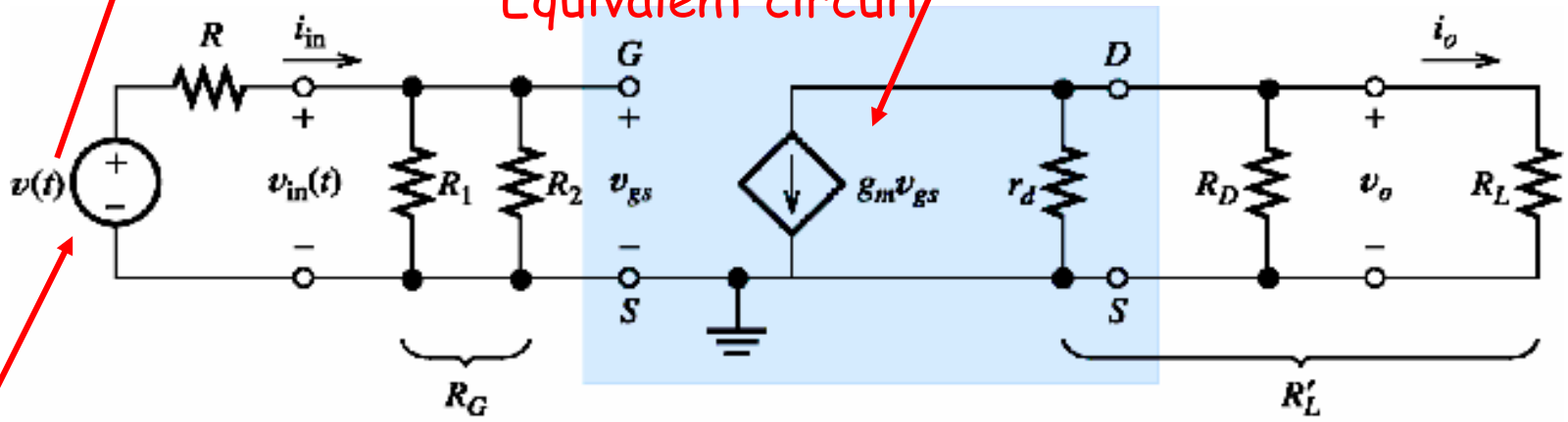
C_s -bypass C

ac signal

Schematic



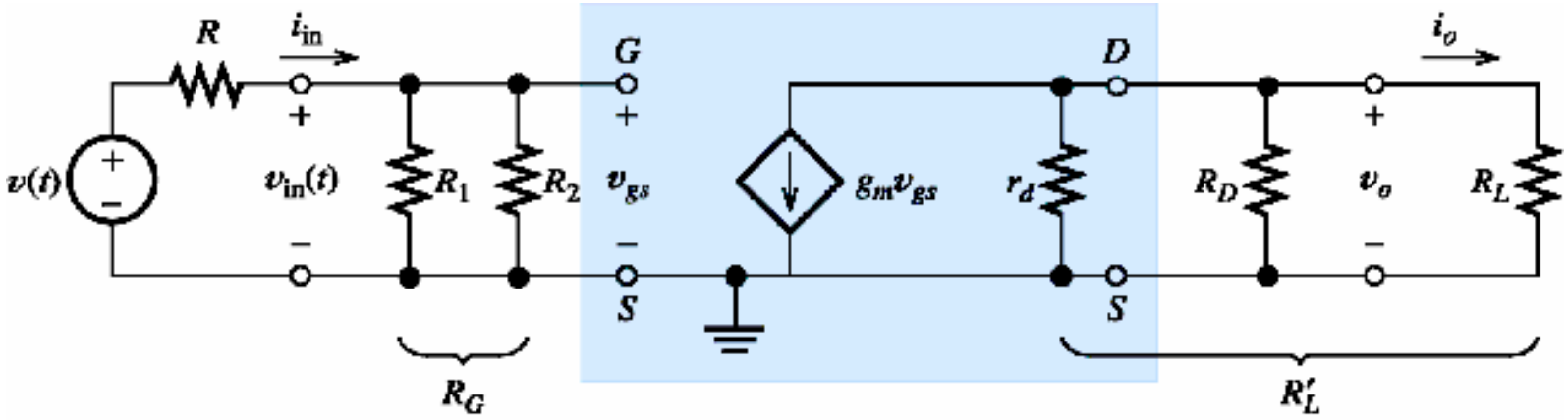
Equivalent circuit



The dc supply voltage acts as a short circuit for the ac current.

Common-Source Amplifier: Gain, R_{in} and R_{out}

Equivalent circuit (once more)



$$R_L' = \frac{1}{1/r_d + 1/R_D + 1/R_L}$$

Voltage gain

$$v_0 = -(g_m v_{gs}) R_L' \qquad v_{in} = v_{gs}$$

$$A_v = \frac{v_0}{v_{in}} = -g_m R_L'$$

Input resistance

$$R_{in} = \frac{v_{in}}{i_{in}} = R_G = R_1 \,||\, R_2$$

From bias point analysis