MICROPROCESSOR SYSTEMS 8th / April / 2004
Visa Exam

1- Calculate the value of A (Accumulator) by using hexadecimal number system at the end of following series of logical operations. (Please, write the results in a box)

a)
```
MOV   A,#75H          ;  A=(75)16
ANL   A,#00001111B
XRL   A,#0FH          ;  ⇒ A= (???)16
```

b)
```
      MOV   A,#1H     ;  A=(1)16
      MOV   R1,#10D
LOOP2: MOV  R0,#3D
LOOP1: ADD  A,R0
      DJNZ  R0,LOOP1
      DJNZ  R1,LOOP2
                      ;  ⇒ A= (???)16
```

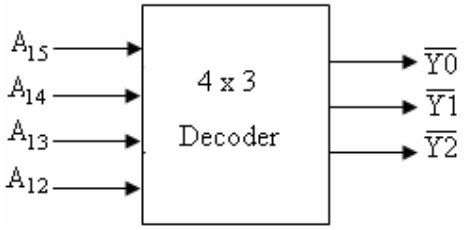
2- In a 64Kbyte memory system, most significant 4bits of the address lines are connected to the activation inputs ($\overline{CE}$) of the memory components through a 4x3 decoder.

a) Draw the component activation table (Logical truth table of the decoder) with respect to memory component activation addresses listed below

0000H-1FFFH Device connected at $\overline{Y0}$ will be active (Active low)
2000H-9FFFH Device connected at $\overline{Y1}$ will be active (Active low)
A000H-AFFFH Device connected at $\overline{Y2}$ will be active (Active low)

b) Find the minimized logical expressions of the outputs $\overline{Y0}$, $\overline{Y1}$ and $\overline{Y2}$

c) Draw the related logical circuit schema using the TTL gates given in the datasheet



3- An 8 bit CPU having 64Kbytes addressing capability will be connected to a memory block containing 1 piece of 27C64 EPROM, 1 piece of 62C128 static RAM, 1 piece of 28C64 EEPROM and an address decoder unit. EPROM will contain the program memory and the initial address after the reset indicates first address of this device (0000H)

a) Give the outline of the memory organization map
b) Draw the circuit schema of the memory block and the related memory-addressing map of the described system using 74HC138 as decoder.

Total time : 95minutes
Suggested timing : 1-a)5m b)10m 2-a)10m b)20m c)15m 3-a)10m b)25minutes
1- a)10P b)15P 2- a) 10P b) 20 c)10 P 3-a)10 b) 25 Points