S1:

PC → Mem address ADD

Mem data → IR

PC → ALU_A

+1 (16 bits) → ALU_B

ALU_C → PC, T3

S2:

‘111’ → A3

PC → D3

S3:

IR 11-9 → A1

IR 8-6 → A2

D1 → T1

D2 → T2

S4:

T1 → ALU_A ADD

T2 → ALU_B

ALU_C → T3

S5:

IR 5-3 → A3

T3 → D3

S6:

IR 8-6 → A2

D2 → T2

IR 5-0 → SE 10 → T1

S7:

T1 → ALU_A SUB

T2 → ALU_B

ALU_C → T3

S8:

T3 → Mem address

Mem data → T3

S9:

IR 11-9 → A3

T3 → D3

S10:

T1 → ALU_A ADD

T2 → ALU_B

ALU_C → T3

IR 11-9 → A1

D1 → T1

S11:

T3 → Mem address

T1 → Mem data

S12:

IR 11-9 → A1

D1 → T1

Counter = 0

S13:

T1 → ALU_A ADD

+1 → ALU_B

ALU_C → T1

Counter +1

S14:

T1 → Mem address

Mem data → T3

Counter binary → A3

S15:

T3 → ALU_A SUB

1 → ALU_B

ALU_C → T3

IR 5-0 → SE 10 → T2

S16:

T3 → ALU_A

T2 → ALU_B

ALU_C → PC

S17:

IR 11-9 → A3

T3 → D3

IR 8-0 → SE 7 → T2

S18:

IR 11-9 → A3

T3 → D3

IR 8-6 → A2

D2 → PC

S19:

IR 11-9 → A3

IR 8-0 → SE 7 → 7S → D3

S20:

Counter binary → A2

D2 → Mem data

T1 → Mem address

S21:

IR 11-9 → A1

D1 → T1

IR 5-0 → SE 10 → T2

S22:

T3 → ALU_A SUB

1 → ALU_B

ALU_C → T3

S23:

T1 → ALU_A NAND

T2 → ALU_B

ALU_C → T3