**Filter Design Requirements:**

DataRate = 20 MHz

SampleRate = 700 MHz

A picture containing text, line, plot, screenshot

Description automatically generatedIf we want to generate an ideal FIR filter with 0.01 dB peak to peak ripple, 80 dB stopband attenuation and 4MHz transition width, the filter needs to be minimum 726th order filter having 727 coefficients. This is huge to build in circuit level / FPGA level in terms of resources.

Figure 1: Minimum order FIR filter Magnitude Response

The code is attached with this report as “FIR\_Filter\_Design.m” and coefficients are attached as “ coefficient\_values\_minorder.mat”

**9th Order FIR Filter**:

So, we have decided to go for lower Filter order. So, considering 9th order filter, we got the coefficients as

6 0 13 67 127 127 67 13 0 6

A picture containing text, plot, line, diagram

Description automatically generated

Figure 2: 9th order FIR Filter Magnitude Response

Though the frequency domain response is not as good as ideal filter, we tried to implement it on Verilog and simulate it using test bench. In test bench, we actually mixed a 10 MHz sinusoidal signal with another 100 MHz sinusoidal signal and got the response which have the frequency of 10 MHz. This verifies that our filter is working in Verilog.

Here is the response that we got simulating our test bench with filter in Verilog,

Figure 3: Time domain response of 9th order FIR Filter in Verilog

A screen shot of a computer screen

Description automatically generated with low confidence

Hrudaya got another set of 9th order FIR Filter coefficient using her method. The coefficients are,

116 121 124 126 127 127 126 124 121 116

A screenshot of a computer screen

Description automatically generated with low confidenceWe applied the same input signal for these coefficients and got this response which also shows the same 10MHz frequency. The response is shown below,

Figure 4: Time domain response of FIR Filter in Verilog with Hrudaya's Coefficients

**16th Order FIR Filter:**

So, we decided to compare our result with a higher order filter and considered a 16th order filter. The coefficient of this filter is,

A picture containing text, plot, line, diagram

Description automatically generated7 5 1 0 9 36 76 112 127 112 76 36 9 0 1 5 7

Figure 5: 16th order FIR Filter Magnitude Response

A screen shot of a computer

Description automatically generated with low confidenceThe frequency domain response is better than the 9th order filter. We checked the filter in Verilog for the same input as previous ones and got the time domain response which has periodicity of 10 MHz. The response is also better than the 9th order filter response in terms of shape.

Figure 6: Time domain response of 16th order FIR Filter in Verilog

**Analysis:**

If the minimum order for filter cannot be met due to resource constraints, increasing the filter order as possible may improve the performance of the implemented filter. Another observation is that quantizing the lower order coefficient values gives better response than quantizing the non-zero values of higher order filter coefficients.

Resource Utilization:

|  |  |  |
| --- | --- | --- |
| **Parameters** | **9th Order FIR Filter** | **16th Order FIR Filter** |
| FF | 72 | 128 |
| DSP | 19 | 33 |
| IO | 138 | 194 |
| BUFG | 1 | 1 |
| Worst Negative Slack (WNS) | 1.477 ns | 1.957 ns |
| Power | 0.23 W | 0.266 W |