



8086 16-BIT HMOS MICROPROCESSOR 8086/8086-2/8086-1

- Direct Addressing Capability 1 MByte of Memory
- Architecture Designed for Powerful Assembly Language and Efficient High Level Languages
- 14 Word, by 16-Bit Register Set with Symmetrical Operations
- 24 Operand Addressing Modes
- Bit, Byte, Word, and Block Operations
- 8 and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide
- Range of Clock Rates:
5 MHz for 8086,
8 MHz for 8086-2,
10 MHz for 8086-1
- MULTIBUS System Compatible Interface
- Available in EXPRESS
— Standard Temperature Range
— Extended Temperature Range
- Available in 40-Lead Cerdip and Plastic Package
(See Packaging Spec. Order #231369)

The Intel 8086 high performance 16-bit CPU is available in three clock rates: 5, 8 and 10 MHz. The CPU is implemented in N-Channel, depletion load, silicon gate technology (HMOS-III), and packaged in a 40-pin CERDIP or plastic package. The 8086 operates in both single processor and multiple processor configurations to achieve high performance levels.

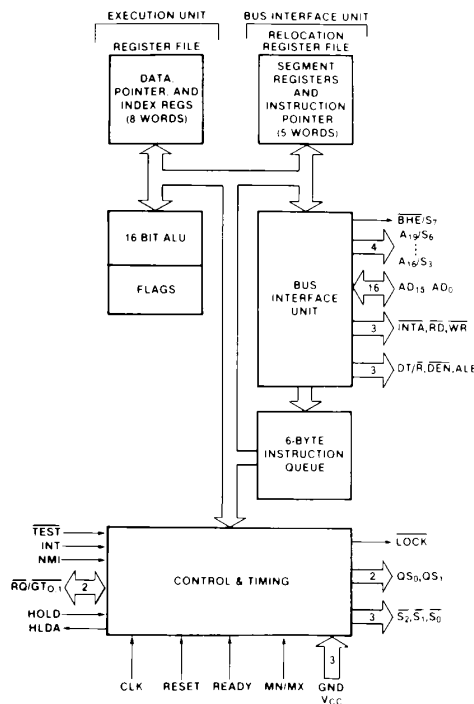
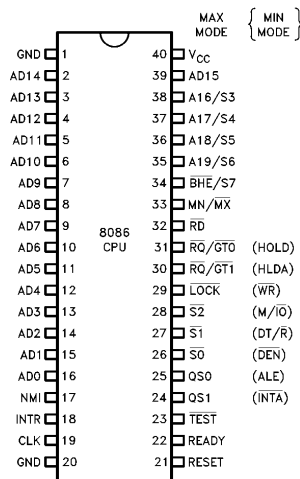


Figure 1. 8086 CPU Block Diagram

231455-1



40 Lead
Figure 2. 8086 Pin
Configuration

231455-2

Table 1. Pin Description

The following pin function descriptions are for 8086 systems in either minimum or maximum mode. The “Local Bus” in these descriptions is the direct multiplexed bus interface connection to the 8086 (without regard to additional bus buffers).

Symbol	Pin No.	Type	Name and Function		
AD ₁₅ –AD ₀	2–16, 39	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/I/O address (T ₁), and data (T ₂ , T ₃ , T _W , T ₄) bus. A ₀ is analogous to BHE for the lower byte of the data bus, pins D ₇ –D ₀ . It is LOW during T ₁ when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A ₀ to condition chip select functions. (See BHE.) These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus “hold acknowledge”.		
A ₁₉ /S ₆ , A ₁₈ /S ₅ , A ₁₇ /S ₄ , A ₁₆ /S ₃	35–38	O	ADDRESS/STATUS: During T ₁ these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T ₂ , T ₃ , T _W , T ₄ . The status of the interrupt enable FLAG bit (S ₅) is updated at the beginning of each CLK cycle. A ₁₇ /S ₄ and A ₁₆ /S ₃ are encoded as shown. This information indicates which relocation register is presently being used for data accessing. These lines float to 3-state OFF during local bus “hold acknowledge.”		
			A ₁₇ /S ₄	A ₁₆ /S ₃	Characteristics
			0 (LOW) 0 1 (HIGH) 1 S ₆ is 0 (LOW)	0 1 0 1	Alternate Data Stack Code or None Data
BHE/S ₇	34	O	BUS HIGH ENABLE/STATUS: During T ₁ the bus high enable signal (BHE) should be used to enable data onto the most significant half of the data bus, pins D ₁₅ –D ₈ . Eight-bit oriented devices tied to the upper half of the bus would normally use BHE to condition chip select functions. BHE is LOW during T ₁ for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S ₇ status information is available during T ₂ , T ₃ , and T ₄ . The signal is active LOW, and floats to 3-state OFF in “hold”. It is LOW during T ₁ for the first interrupt acknowledge cycle.		
			BHE	A ₀	Characteristics
			0 0 1 1	0 1 0 1	Whole word Upper byte from/to odd address Lower byte from/to even address None
RD	32	O	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the S ₂ pin. This signal is used to read devices which reside on the 8086 local bus. RD is active LOW during T ₂ , T ₃ and T _W of any read cycle, and is guaranteed to remain HIGH in T ₂ until the 8086 local bus has floated. This signal floats to 3-state OFF in “hold acknowledge”.		

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
READY	22	I	READY: is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The READY signal from memory/I/O is synchronized by the 8284A Clock Generator to form READY. This signal is active HIGH. The 8086 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.
INTR	18	I	INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{\text{TEST}}$	23	I	$\overline{\text{TEST}}$: input is examined by the “Wait” instruction. If the $\overline{\text{TEST}}$ input is LOW execution continues, otherwise the processor waits in an “Idle” state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V _{CC}	40		V_{CC}: +5V power supply pin.
GND	1, 20		GROUND
MN/ $\overline{\text{MX}}$	33	I	MINIMUM/MAXIMUM: indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the 8086/8288 system in maximum mode (i.e., $\text{MN}/\overline{\text{MX}} = V_{\text{SS}}$). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

$\overline{\text{S}}_2, \overline{\text{S}}_1, \overline{\text{S}}_0$	26–28	O	STATUS: active during T_4 , T_1 , and T_2 and is returned to the passive state (1, 1, 1) during T_3 or during T_W when READY is HIGH. This status is used by the 8288 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{\text{S}}_2$, $\overline{\text{S}}_1$, or $\overline{\text{S}}_0$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle.
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Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function			
$\overline{S_2}, \overline{S_1}, \overline{S_0}$ (Continued)	26–28	O	These signals float to 3-state OFF in “hold acknowledge”. These status lines are encoded as shown.			
			$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Characteristics
			0 (LOW)	0	0	Interrupt Acknowledge
			0	0	1	Read I/O Port
			0	1	0	Write I/O Port
			0	1	1	Halt
			1 (HIGH)	0	0	Code Access
			1	0	1	Read Memory
			1	1	0	Write Memory
			1	1	1	Passive
$\overline{RQ}/\overline{GT_0},$ $\overline{RQ}/\overline{GT_1}$	30, 31	I/O	<p>REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT_0}$ having higher priority than $\overline{RQ}/\overline{GT_1}$. $\overline{RQ}/\overline{GT}$ pins have internal pull-up resistors and may be left unconnected. The request/grant sequence is as follows (see Page 2-24):</p> <ol style="list-style-type: none">1. A pulse of 1 CLK wide from another local bus master indicates a local bus request (“hold”) to the 8086 (pulse 1).2. During a T_4 or T_1 clock cycle, a pulse 1 CLK wide from the 8086 to the requesting master (pulse 2), indicates that the 8086 has allowed the local bus to float and that it will enter the “hold acknowledge” state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during “hold acknowledge”.3. A pulse 1 CLK wide from the requesting master indicates to the 8086 (pulse 3) that the “hold” request is about to end and that the 8086 can reclaim the local bus at the next CLK. <p>Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.</p> <p>If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met:</p> <ol style="list-style-type: none">1. Request occurs on or before T_2.2. Current cycle is not the low byte of a word (on an odd address).3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.4. A locked instruction is not currently executing. <p>If the local bus is idle when the request is made the two possible events will follow:</p> <ol style="list-style-type: none">1. Local bus will be released during the next clock.2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.			
LOCK	29	O	<p>LOCK: output indicates that other system bus masters are not to gain control of the system bus while LOCK is active LOW. The LOCK signal is activated by the “LOCK” prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in “hold acknowledge”.</p>			

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function		
QS ₁ , QS ₀	24, 25	O	QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed. QS ₁ and QS ₀ provide status to allow external tracking of the internal 8086 instruction queue.		
			QS ₁	QS ₀	Characteristics
			0 (LOW)	0	No Operation
			0	1	First Byte of Op Code from Queue
			1 (HIGH)	0	Empty the Queue
			1	1	Subsequent Byte from Queue

The following pin function descriptions are for the 8086 in minimum mode (i.e., $MN/\overline{MX} = V_{CC}$). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

M/\overline{IO}	28	O	STATUS LINE: logically equivalent to S ₂ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/\overline{IO} becomes valid in the T ₄ preceding a bus cycle and remains valid until the final T ₄ of the cycle (M = HIGH, IO = LOW). M/\overline{IO} floats to 3-state OFF in local bus "hold acknowledge".
\overline{WR}	29	O	WRITE: indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/\overline{IO} signal. \overline{WR} is active for T ₂ , T ₃ and T _W of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge".
\overline{INTA}	24	O	\overline{INTA}: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T ₂ , T ₃ and T _W of each interrupt acknowledge cycle.
ALE	25	O	ADDRESS LATCH ENABLE: provided by the processor to latch the address into the 8282/8283 address latch. It is a HIGH pulse active during T ₁ of any bus cycle. Note that ALE is never floated.
DT/ \overline{R}	27	O	DATA TRANSMIT/RECEIVE: needed in minimum system that desires to use an 8286/8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/ \overline{R} is equivalent to $\overline{S_1}$ in the maximum mode, and its timing is the same as for M/\overline{IO} . (T = HIGH, R = LOW.) This signal floats to 3-state OFF in local bus "hold acknowledge".
\overline{DEN}	26	O	DATA ENABLE: provided as an output enable for the 8286/8287 in a minimum system which uses the transceiver. \overline{DEN} is active LOW during each memory and I/O access and for \overline{INTA} cycles. For a read or \overline{INTA} cycle it is active from the middle of T ₂ until the middle of T ₄ , while for a write cycle it is active from the beginning of T ₂ until the middle of T ₄ . \overline{DEN} floats to 3-state OFF in local bus "hold acknowledge".
HOLD, HLDA	31, 30	I/O	HOLD: indicates that another master is requesting a local bus "hold." To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of a T ₄ or T ₁ clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWer the HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold acknowledge (HLDA) and HOLD have internal pull-up resistors. The same rules as for $\overline{RQ}/\overline{GT}$ apply regarding when the local bus will be released. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.



82C55A CHMOS PROGRAMMABLE PERIPHERAL INTERFACE

- Compatible with all Intel and Most Other Microprocessors
- High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188
- 24 Programmable I/O Pins
- Low Power CHMOS
- Completely TTL Compatible
- Control Word Read-Back Capability
- Direct Bit Set/Reset Capability
- 2.5 mA DC Drive Capability on all I/O Port Outputs
- Available in 40-Pin DIP and 44-Pin PLCC
- Available in EXPRESS
 - Standard Temperature Range
 - Extended Temperature Range

The Intel 82C55A is a high-performance, CHMOS version of the industry standard 8255A general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The 82C55A is pin compatible with the NMOS 8255A and 8255A-5.

In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

The 82C55A is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The 82C55A is available in 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC) packages.

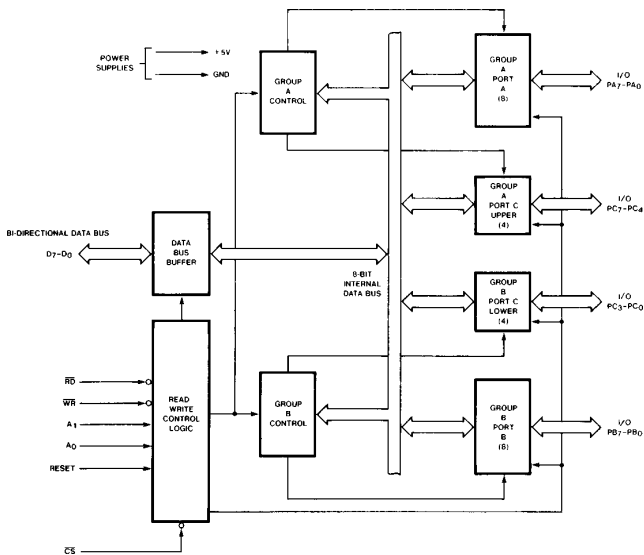
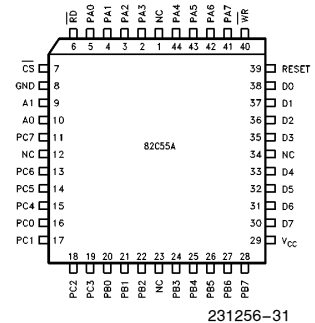
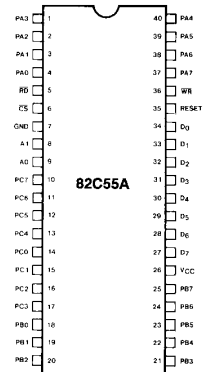


Figure 1. 82C55A Block Diagram

231256-1



231256-31



231256-82

Figure 2. 82C55A Pinout

Diagrams are for pin reference only. Package sizes are not to scale.

Table 1. Pin Description

Symbol	Pin Number Dip PLCC		Type	Name and Function					
PA ₃₋₀	1-4	2-5	I/O	PORT A, PINS 0-3: Lower nibble of an 8-bit data output latch/ buffer and an 8-bit data input latch.					
\overline{RD}	5	6	I	READ CONTROL: This input is low during CPU read operations.					
\overline{CS}	6	7	I	CHIP SELECT: A low on this input enables the 82C55A to respond to \overline{RD} and \overline{WR} signals. \overline{RD} and \overline{WR} are ignored otherwise.					
GND	7	8		System Ground					
A ₁₋₀	8-9	9-10	I	ADDRESS: These input signals, in conjunction \overline{RD} and \overline{WR} , control the selection of one of the three ports or the control word registers.					
				A ₁	A ₀	\overline{RD}	\overline{WR}	\overline{CS}	Input Operation (Read)
				0	0	0	1	0	Port A - Data Bus
				0	1	0	1	0	Port B - Data Bus
				1	0	0	1	0	Port C - Data Bus
				1	1	0	1	0	Control Word - Data Bus
				Output Operation (Write)					
				0	0	1	0	0	Data Bus - Port A
				0	1	1	0	0	Data Bus - Port B
				1	0	1	0	0	Data Bus - Port C
				1	1	1	0	0	Data Bus - Control
				Disable Function					
				X	X	X	X	1	Data Bus - 3 - State
				X	X	1	1	0	Data Bus - 3 - State
PC ₇₋₄	10-13	11,13-15	I/O	PORT C, PINS 4-7: Upper nibble of an 8-bit data output latch/ buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.					
PC ₀₋₃	14-17	16-19	I/O	PORT C, PINS 0-3: Lower nibble of Port C.					
PB ₀₋₇	18-25	20-22, 24-28	I/O	PORT B, PINS 0-7: An 8-bit data output latch/buffer and an 8-bit data input buffer.					
V _{CC}	26	29		SYSTEM POWER: + 5V Power Supply.					
D ₇₋₀	27-34	30-33, 35-38	I/O	DATA BUS: Bi-directional, tri-state data bus lines, connected to system data bus.					
RESET	35	39	I	RESET: A high on this input clears the control register and all ports are set to the input mode.					
\overline{WR}	36	40	I	WRITE CONTROL: This input is low during CPU write operations.					
PA ₇₋₄	37-40	41-44	I/O	PORT A, PINS 4-7: Upper nibble of an 8-bit data output latch/ buffer and an 8-bit data input latch.					
NC		1, 12, 23, 34		No Connect					



8254 PROGRAMMABLE INTERVAL TIMER

- Compatible with All Intel and Most Other Microprocessors
- Handles Inputs from DC to 10 MHz
 - 8 MHz 8254
 - 10 MHz 8254-2
- Status Read-Back Command
- Six Programmable Counter Modes
- Three Independent 16-Bit Counters
- Binary or BCD Counting
- Single +5V Supply
- Available in EXPRESS
 - Standard Temperature Range

The Intel 8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 8254 is a superset of the 8253.

The 8254 uses HMOS technology and comes in a 24-pin plastic or Cerdip package.

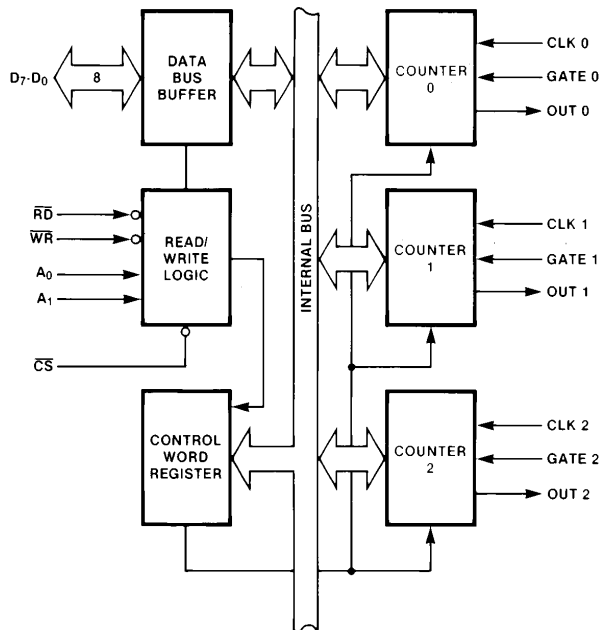


Figure 1. 8254 Block Diagram

231164-1

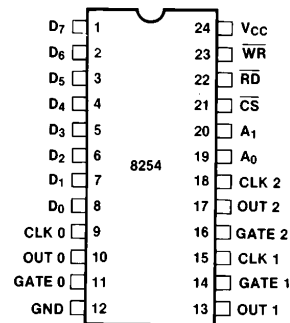


Figure 2. Pin Configuration

231164-2

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function		
D ₇ –D ₀	1–8	I/O	DATA: Bi-directional three state data bus lines, connected to system data bus.		
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.		
OUT 0	10	O	OUTPUT 0: Output of Counter 0.		
GATE 0	11	I	GATE 0: Gate input of Counter 0.		
GND	12		GROUND: Power supply connection.		
V _{CC}	24		POWER: + 5V power supply connection.		
WR	23	I	WRITE CONTROL: This input is low during CPU write operations.		
RD	22	I	READ CONTROL: This input is low during CPU read operations.		
CS	21	I	CHIP SELECT: A low on this input enables the 8254 to respond to RD and WR signals. RD and WR are ignored otherwise.		
A ₁ , A ₀	20–19	I	ADDRESS: Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.		
			A ₁	A ₀	Selects
			0	0	Counter 0
			0	1	Counter 1
			1	0	Counter 2
1	1	Control Word Register			
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.		
OUT 2	17	O	OUT 2: Output of Counter 2.		
GATE 2	16	I	GATE 2: Gate input of Counter 2.		
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.		
GATE 1	14	I	GATE 1: Gate input of Counter 1.		
OUT 1	13	O	OUT 1: Output of Counter 1.		

FUNCTIONAL DESCRIPTION

General

The 8254 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8254 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 8254 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 8254 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other counter/timer functions common to microcomputers which can be implemented with the 8254 are:

- Real time clock
- Event-counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Block Diagram

DATA BUS BUFFER

This 3-state, bi-directional, 8-bit buffer is used to interface the 8254 to the system bus (see Figure 3).

8284A, 8284A-1

Clock Generator and Driver for 8086/8088 Processors

The 8284A is a single chip clock generator/driver for the 8086/8088 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, complete MULTIBUS 'Ready' synchronization and reset logic.

The oscillator circuit of the 8284A is designed primarily for use with a fundamental mode, series resonant crystal from which the operating frequency is derived.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

8284A/8284A-1

Clock Generator and Driver for 8086, 8088 Processors

8284A/8284A-1

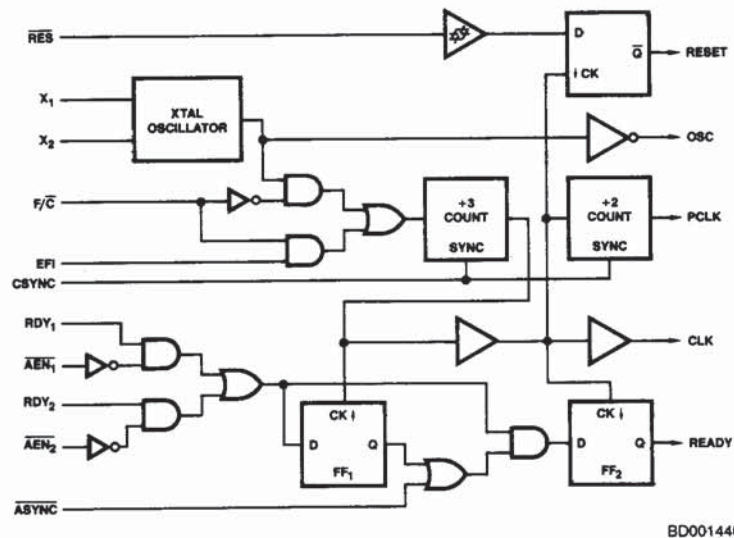
DISTINCTIVE CHARACTERISTICS

- Generates the System Clock for the 8086, 8088 Processors: 5MHz, 8MHz with 8284A; 10MHz with 8284A-1
- Uses a crystal or a TTL signal for frequency source
- Provides local READY and Multibus* READY synchronization
- Generates system reset output from Schmitt trigger input
- Capable of clock synchronization with other 8284As

GENERAL DESCRIPTION

The 8284A is a single chip clock generator/driver for the 8086, 8088 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, complete MULTIBUS* "Ready" synchronization and reset logic.

BLOCK DIAGRAM



3

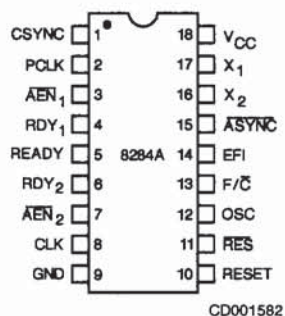
RELATED AMD PRODUCTS

Part No.	Description
Am8086	16-Bit Microprocessor
8288	Bus Controller

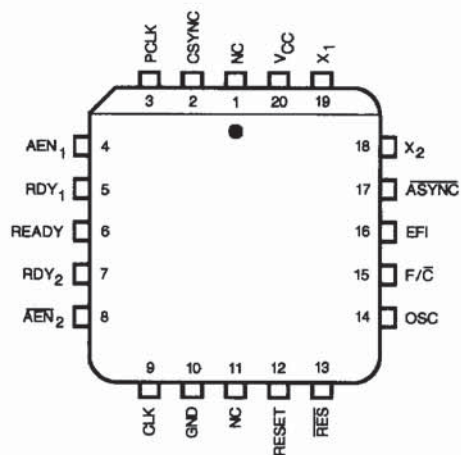
*MULTIBUS is a registered trademark of Intel Corp.

CONNECTION DIAGRAMS Top View

DIPs



PLCC



Note: Pin 1 is marked for orientation.

PIN DESCRIPTION

Pin No.	Name	I/O	Description
3, 7	AEN ₁ , AEN ₂	I	Address Enable. The AEN signal is used to qualify the Bus Ready signal (RDY ₁ or RDY ₂). AEN ₁ validates RDY ₁ while AEN ₂ validates RDY ₂ . It is possible for the processor to access two Multi-Master System Busses if you use both signals. Both signals are tied LOW in non Multi-Master Systems.
4, 6	RDY ₁ , RDY ₂	I	Bus Ready. These signals are indications from a device located on the system bus that it is available or data has been received. RDY ₁ and RDY ₂ are qualified by AEN ₁ and AEN ₂ respectively.
15	ASYNC	I	Ready Synchronous Select. The ASYNC signal defines the synchronization mode of the READY logic. When ASYNC is open (internal pull-up resistor is provided) or pulled HIGH, there is one stage of READY Synchronization. When ASYNC is LOW, there are two stages of READY Synchronization.
5	READY	O	Ready. READY is the synchronized RDY signal input. After the guaranteed hold time to the processor has been met, the READY signal is cleared.
7, 16	X ₁ , X ₂	I	Crystal In. These are the input pins for the attached crystal. The crystal frequency is 3 times the desired process clock frequency.
13	F/ \bar{C}	I	Frequency/Crystal Select. When F/ \bar{C} is strapped HIGH, CLK is generated from the EFI input. When strapped LOW, the F/ \bar{C} allows the processor clock to be generated by the crystal.
14	EFI	I	External Frequency. Used in conjunction with a HIGH signal on F/ \bar{C} , CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
8	CLK	O	Processor Clock. CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (including bipolar support chips and other MOS devices). An output HIGH of 4.5V (V _{CC} = 5V) is provided on this pin to drive MOS devices. The output frequency of CLK is 1/3 of the crystal on EFI input frequency and a 1/3 duty cycle.
2	PCLK	O	Peripheral Clock. This signal is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
12	OSC	O	Oscillator Output. This signal is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
11	RES	I	Reset In. This signal is used to generate a RESET. The 8284A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
10	RESET	O	Reset. This signal is used to reset the 8086 family processors.
1	CSYNC	I	Clock Synchronization. This signal is designed to allow multiple 8284As to be synchronized to provide clocks that are in phase. CSYNC HIGH will reset the internal counters, when CSYNC goes LOW the counters will resume counting. CSYNC needs to be externally synchronized to EFI. When used with the internal oscillator, CSYNC should be hard wired to ground.

DETAILED DESCRIPTION

OSCILLATOR

The oscillator circuit of the 8284A is designed primarily for use with a fundamental mode, series resonant crystal from which the operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X₁ and X₂ are the two crystal input crystal connections. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Two 510 Ω series resistors are optional for systems which have a V_{CC} ramp time greater than (or equal to) 1V/ms and/or inherent board capacitance between X₁ or X₂ exceeding 10pF. This capacitance value should not include the 8284A's pin capacitance. By limiting the stray capacitance to less than 10pF on X₁ or X₂, the deviation from the desired fundamental frequency is minimized.

CLOCK GENERATOR

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input, (CSYNC), allows the output clock to be synchronized with an external event (such as another 8284A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 8284A (see Figure 1). This is accomplished with two Schottky flip-flops. The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/ \bar{C} input is a strapping pin that selects either the EFI input or the crystal oscillator as the clock for the $\div 3$ counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

CLOCK OUTPUTS

The CLK output is a 33% duty cycle MOS clock driver designed to drive the 8086 or 8088 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

RESET LOGIC

Reset logic for the 8284A is provided by a Schmitt trigger input (RES) and a synchronizing flip-flop to generate the reset timing.

The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 8284A.

READY SYNCHRONIZATION

Two READY inputs (RDY₁, RDY₂) are provided to accommodate two Multi-Master system busses. Each input has a qualifier (AEN₁ and AEN₂, respectively). The AEN signals validate their respective RDY signals. If a Multi-Master system is not being used the AEN pin should be tied LOW.

To assure RDY setup and hold times are met, synchronization is required for all asynchronous active going edges of either RDY input. Inactive-going edges of RDY (in normally ready systems) do not require synchronization, but must satisfy RDY setup and hold as a matter of proper system design.

The two modes of RDY synchronization operation are defined by the ASYNC input.

When ASYNC is LOW, two stages of synchronization are provided for active RDY input signals. Positive-going asynchronous RDY inputs will first be synchronized to flip-flop one at the rising edge of CLK and then synchronized to flip-flop two at the next falling edge of CLK; after which time the READY output will go active (HIGH). Negative-going asynchro-



8259A PROGRAMMABLE INTERRUPT CONTROLLER (8259A/8259A-2)

- 8086, 8088 Compatible
- MCS-80, MCS-85 Compatible
- Eight-Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- Available in 28-Pin DIP and 28-Lead PLCC Package
(See Packaging Spec., Order #231369)
- Available in EXPRESS
 - Standard Temperature Range
 - Extended Temperature Range

The Intel 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The 8259A is fully upward compatible with the Intel 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).

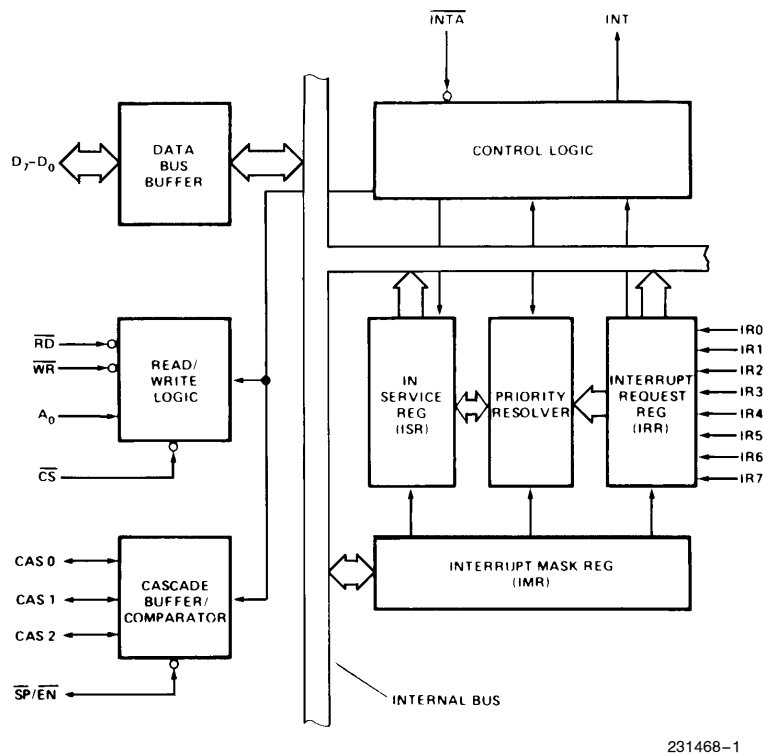


Figure 1. Block Diagram

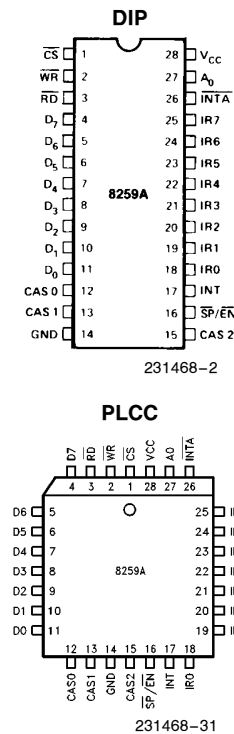


Figure 2. Pin Configurations

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
V _{CC}	28	I	SUPPLY: +5V Supply.
GND	14	I	GROUND
\overline{CS}	1	I	CHIP SELECT: A low on this pin enables \overline{RD} and \overline{WR} communication between the CPU and the 8259A. INTA functions are independent of CS.
\overline{WR}	2	I	WRITE: A low on this pin when CS is low enables the 8259A to accept command words from the CPU.
\overline{RD}	3	I	READ: A low on this pin when CS is low enables the 8259A to release status onto the data bus for the CPU.
D ₇ –D ₀	4–11	I/O	BIDIRECTIONAL DATA BUS: Control, status and interrupt-vector information is transferred via this bus.
CAS ₀ –CAS ₂	12, 13, 15	I/O	CASCADE LINES: The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A.
$\overline{SP}/\overline{EN}$	16	I/O	SLAVE PROGRAM/ENABLE BUFFER: This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR ₀ –IR ₇	18–25	I	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
\overline{INTA}	26	I	INTERRUPT ACKNOWLEDGE: This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A ₀	27	I	AO ADDRESS LINE: This pin acts in conjunction with the \overline{CS} , \overline{WR} , and \overline{RD} pins. It is used by the 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for 8086, 8088).

MM2716E 16,384-Bit (2048 × 8) UV Erasable PROM Extended Temperature Range

General Description

The MM2716E is a high speed 16k UV erasable and electrically reprogrammable EPROM ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

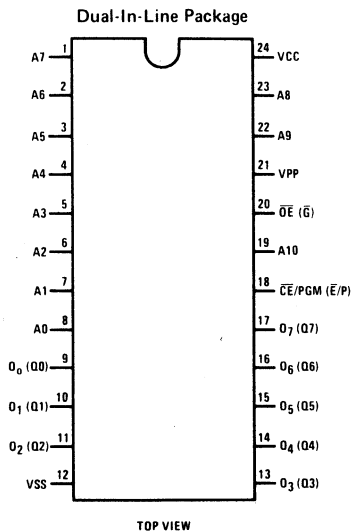
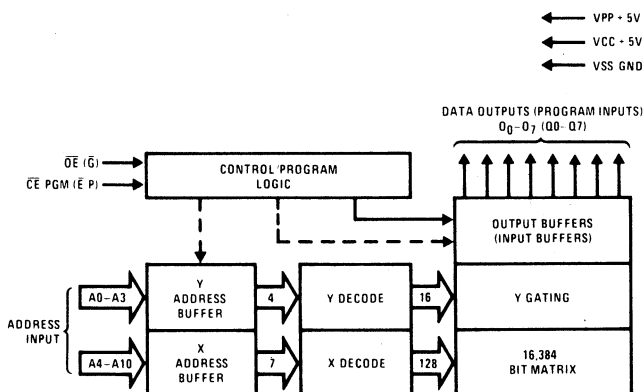
The MM2716E is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

Features

- -40°C to $+85^{\circ}\text{C}$
- 2048 × 8 organization
- 550 mW max active power, 137.5 mW max standby power
- Low power during programming
- Access time — 450 ns
- Single 5V $\pm 10\%$ power supply
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE[®] output

Block and Connection Diagrams*



Pin Connection During Read or Program

MODE	PIN NAME/NUMBER				
	$\overline{\text{CE}}/\text{PGM} (\bar{E}/P)$ 18	$\overline{\text{OE}} (\bar{G})$ 20	VPP 21	VCC 24	OUTPUTS 9-11, 13-17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

Order Number MM2716QE
See NS Package J24CQ

Pin Names

A0-A10	Address Inputs
$Q_0-Q_7 (Q_0-Q_7)$	Data Outputs
$\overline{\text{CE}}/\text{PGM} (\bar{E}/P)$	Chip Enable/Program
$\overline{\text{OE}} (\bar{G})$	Output Enable
VPP	Read 5V, Program 25V
VCC	Power (5V)
VSS	Ground

*Symbols in parentheses are proposed industry standard



CMOS Static RAM 16K (2K x 8-Bit)

**IDT6116SA
IDT6116LA**

Features

- ♦ High-speed access and chip select times
 - Military: 20/25/35/45/55/70/90/120/150ns (max.)
 - Industrial: 20/25/35/45ns (max.)
 - Commercial: 15/20/25/35/45ns (max.)
- ♦ Low-power consumption
- ♦ Battery backup operation
 - 2V data retention voltage (LA version only)
- ♦ Produced with advanced CMOS high-performance technology
- ♦ CMOS process virtually eliminates alpha particle soft-error rates
- ♦ Input and output directly TTL-compatible
- ♦ Static operation: no clocks or refresh required
- ♦ Available in ceramic and plastic 24-pin DIP, 24-pin Thin Dip, 24-pin SOIC and 24-pin SOJ
- ♦ Military product compliant to MIL-STD-883, Class B

Description

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

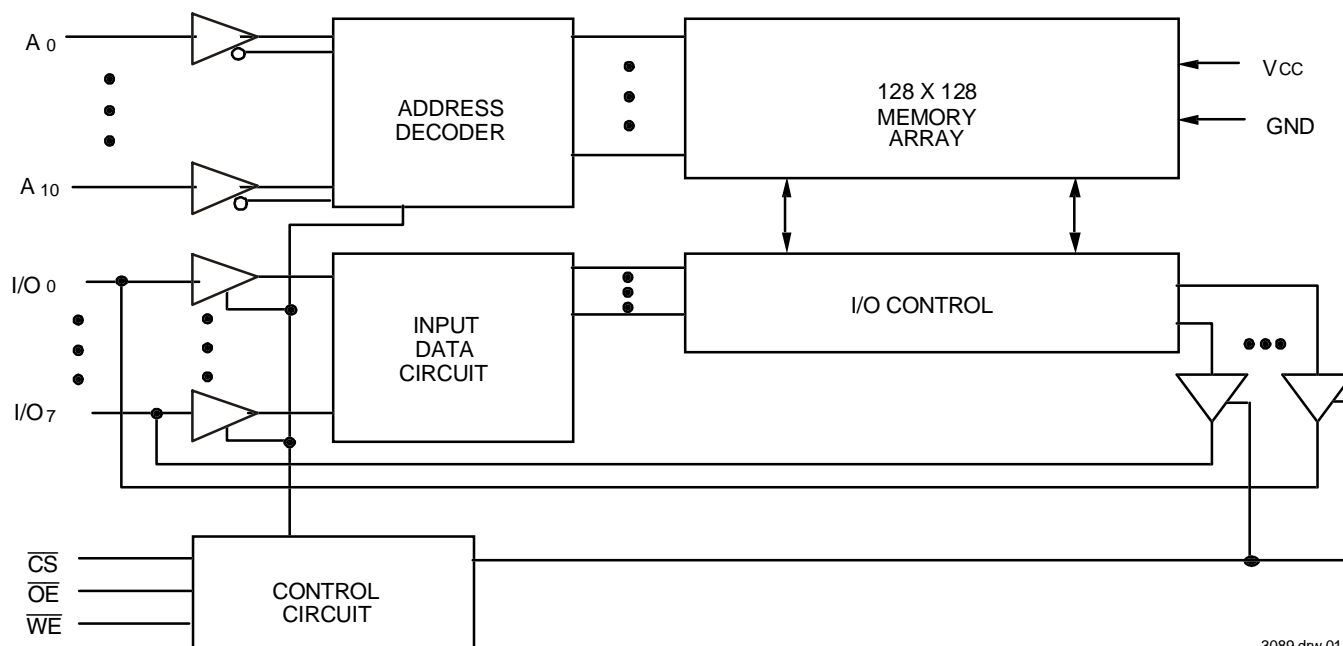
Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When \overline{CS} goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as \overline{CS} remains HIGH. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW to 4µW operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 24-lead gull-wing SOIC, and 24-lead J-bend SOJ providing high board-level packing densities.

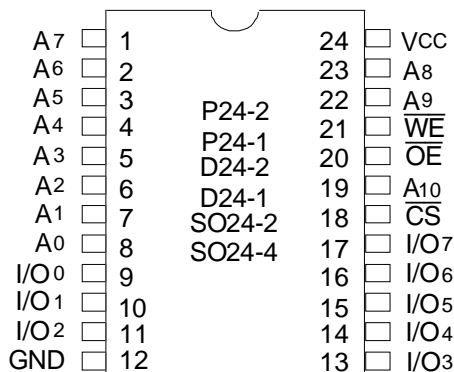
Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Functional Block Diagram



FEBRUARY 2001

Pin Configurations



3089 drw 02

DIP/SOIC/SOJ Top View

Pin Description

Name	Description
A0 - A10	Address Inputs
I/O0 - I/O7	Data Input/Output
\overline{CS}	Chip Select
\overline{WE}	Write Enable
\overline{OE}	Output Enable
VCC	Power
GND	Ground

3089 tbl 01

Truth Table⁽¹⁾

Mode	\overline{CS}	\overline{OE}	\overline{WE}	I/O
Standby	H	X	X	High-Z
Read	L	L	H	DATA _{OUT}
Read	L	H	H	High-Z
Write	L	X	L	DATA _{IN}

3089 tbl 02

NOTE:

1. H = V_{IH}, L = V_{IL}, X = Don't Care.

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{VO}	I/O Capacitance	V _{OUT} = 0V	8	pF

3089 tbl 03

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

3089 tbl 04

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. V_{TERM} must not exceed V_{CC} +0.5V.

SN54LS373, SN54LS374, SN54S373, SN54S374, SN74LS373, SN74LS374, SN74S373, SN74S374

OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

SDLS165B – OCTOBER 1975 – REVISED AUGUST 2002

- Choice of Eight Latches or Eight D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Clock-Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce DC Loading on Data Lines ('S373 and 'S374)

description

These 8-bit registers feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The high-impedance 3-state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pullup components. These devices are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

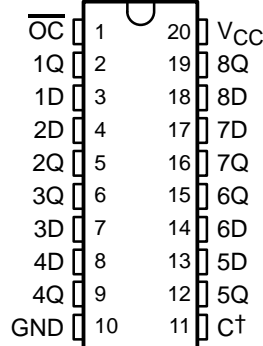
The eight latches of the 'LS373 and 'S373 are transparent D-type latches, meaning that while the enable (C or CLK) input is high, the Q outputs follow the data (D) inputs. When C or CLK is taken low, the output is latched at the level of the data that was set up.

The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output-control (\overline{OC}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly.

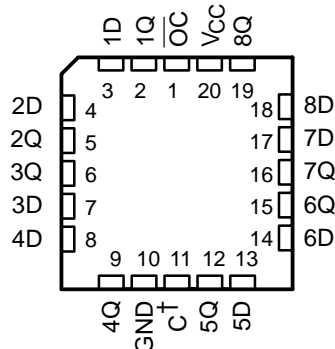
\overline{OC} does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered, even while the outputs are off.

SN54LS373, SN54LS374, SN54S373,
SN54S374 ... J OR W PACKAGE
SN74LS373, SN74S374 ... DW, N, OR NS PACKAGE
SN74LS374 ... DB, DW, N, OR NS PACKAGE
SN74S373 ... DW OR N PACKAGE
(TOP VIEW)



† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.

SN54LS373, SN54LS374, SN54S373,
SN54S374 ... FK PACKAGE
(TOP VIEW)



† C for 'LS373 and 'S373; CLK for 'LS374 and 'S374.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

74LS244

Octal 3-STATE Buffer/Line Driver/Line Receiver

General Description

These buffers/line drivers are designed to improve both the performance and PC board density of 3-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

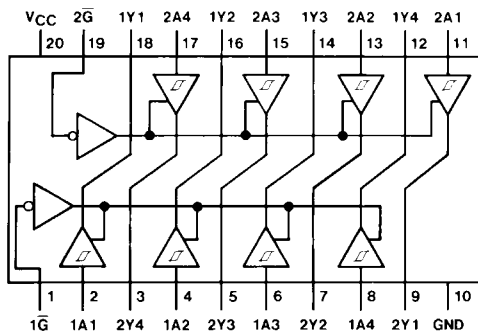
- 3-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at data inputs improves noise margins
- Typical I_{OL} (sink current) 24 mA
- Typical I_{OH} (source current) -15 mA
- Typical propagation delay times
 - Inverting 10.5 ns
 - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
 - Inverting 130 mW
 - Noninverting 135 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74LS244WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS244SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS244N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs		Output
\bar{G}	A	Y
L	L	L
L	H	H
H	X	Z

L = LOW Logic Level
H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
Z = High Impedance

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
V _{IH}	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-15	mA
I _{OL}	LOW Level Output Current			24	mA
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

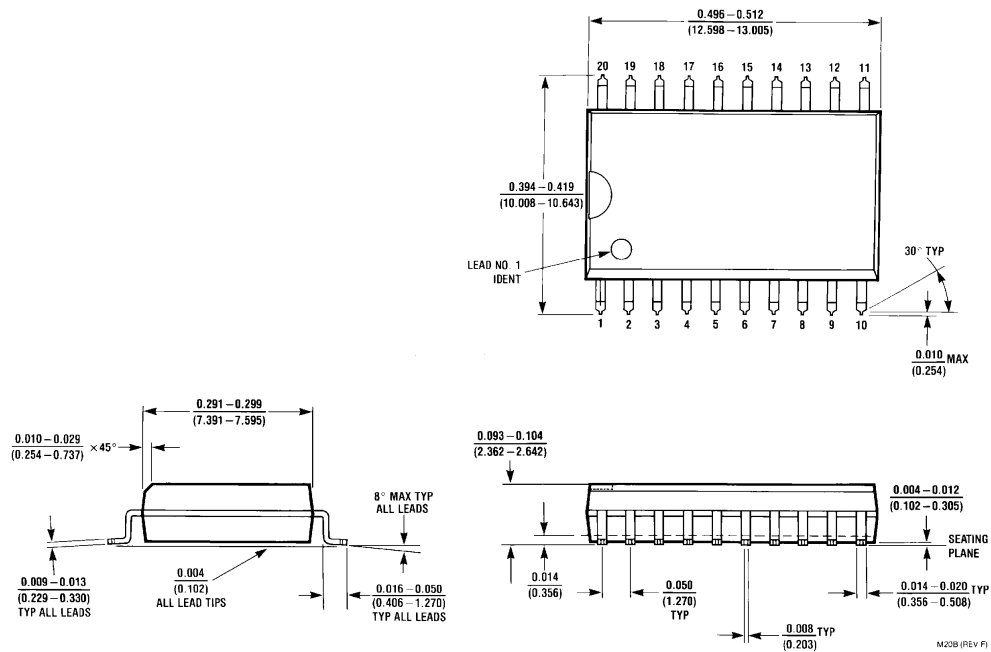
Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = -18 mA			-1.5	V
HYS	Hysteresis (V _{T+} - V _{T-}) Data Inputs Only	V _{CC} = Min	0.2	0.4		V
V _{OH}	HIGH Level Output Voltage	V _{CC} = Min, V _{IH} = Min V _{IL} = Max, I _{OH} = -1 mA	2.7			V
		V _{CC} = Min, V _{IH} = Min V _{IL} = Max, I _{OH} = -3 mA	2.4	3.4		
		V _{CC} = Min, V _{IH} = Min V _{IL} = 0.5V, I _{OH} = Max	2			
V _{OL}	LOW Level Output Voltage	V _{CC} = Min I _{OL} = 12 mA			0.4	V
		V _{IL} = Max I _{OL} = Max			0.5	
		V _{IH} = Min				
I _{OZH}	Off-State Output Current, HIGH Level Voltage Applied	V _{CC} = Max V _{IL} = Max	V _O = 2.7V		20	μA
I _{OZL}	Off-State Output Current, LOW Level Voltage Applied	V _{IH} = Min	V _O = 0.4V		-20	μA
I _I	Input Current at Maximum Input Voltage	V _{CC} = Max	V _I = 7V		0.1	mA
I _{IH}	HIGH Level Input Current	V _{CC} = Max	V _I = 2.7V		20	μA
I _{IL}	LOW Level Input Current	V _{CC} = Max	V _I = 0.4V	-0.5	-200	μA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 3)	-40		-225	mA
I _{CC}	Supply Current	V _{CC} = Max, Outputs Open	Outputs HIGH		13	mA
			Outputs LOW		27	
			Outputs Disabled		32	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

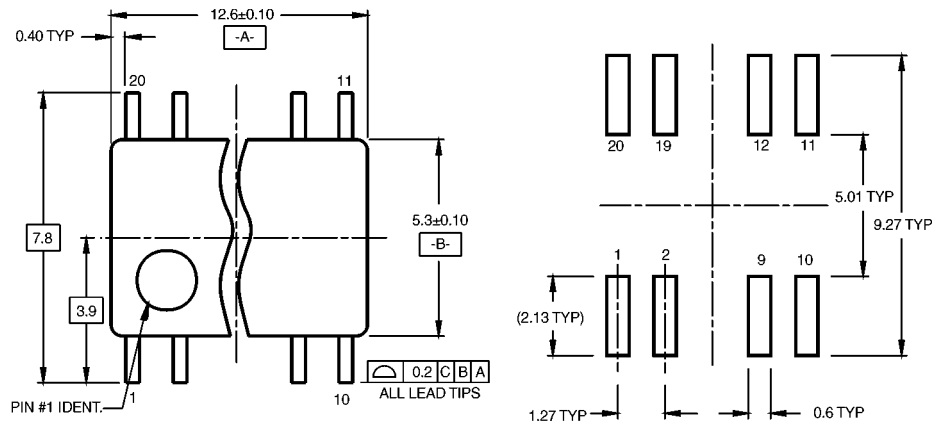
Switching Characteristics				
at $V_{CC} = 5V$, $T_A = 25^{\circ}C$				
Symbol	Parameter	Conditions	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$C_L = 45\text{ pF}$ $R_L = 667\Omega$	18	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	$C_L = 45\text{ pF}$ $R_L = 667\Omega$	18	ns
t_{PZL}	Output Enable Time to LOW Level	$C_L = 45\text{ pF}$ $R_L = 667\Omega$	30	ns
t_{PZH}	Output Enable Time to HIGH Level	$C_L = 45\text{ pF}$ $R_L = 667\Omega$	23	ns
t_{PLZ}	Output Disable Time from LOW Level	$C_L = 5\text{ pF}$ $R_L = 667\Omega$	25	ns
t_{PHZ}	Output Disable Time from HIGH Level	$C_L = 5\text{ pF}$ $R_L = 667\Omega$	18	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$C_L = 150\text{ pF}$ $R_L = 667\Omega$	21	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	$C_L = 150\text{ pF}$ $R_L = 667\Omega$	22	ns
t_{PZL}	Output Enable Time to LOW Level	$C_L = 150\text{ pF}$ $R_L = 667\Omega$	33	ns
t_{PZH}	Output Enable Time to HIGH Level	$C_L = 150\text{ pF}$ $R_L = 667\Omega$	26	ns

Physical Dimensions inches (millimeters) unless otherwise noted

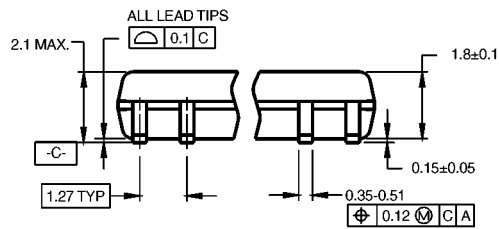


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**

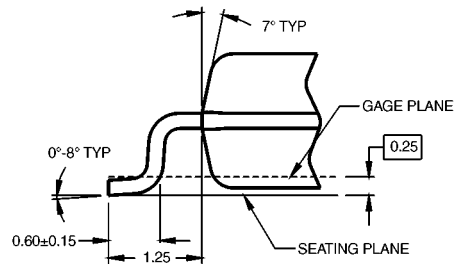
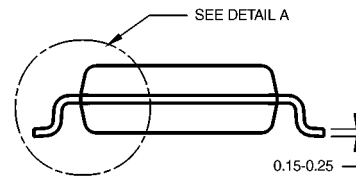
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

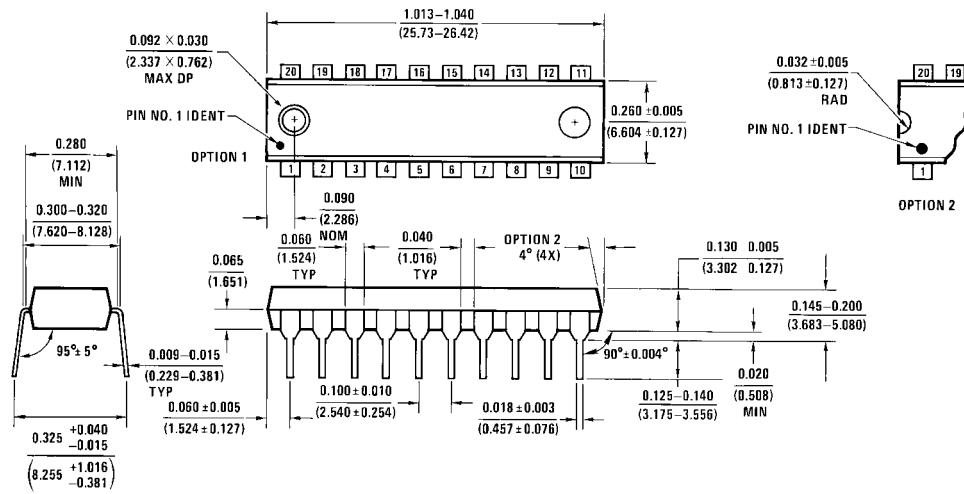
NOTES:

- CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A**

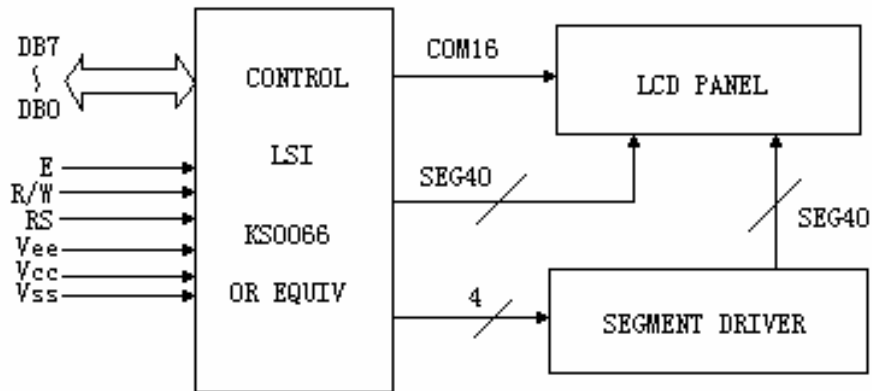
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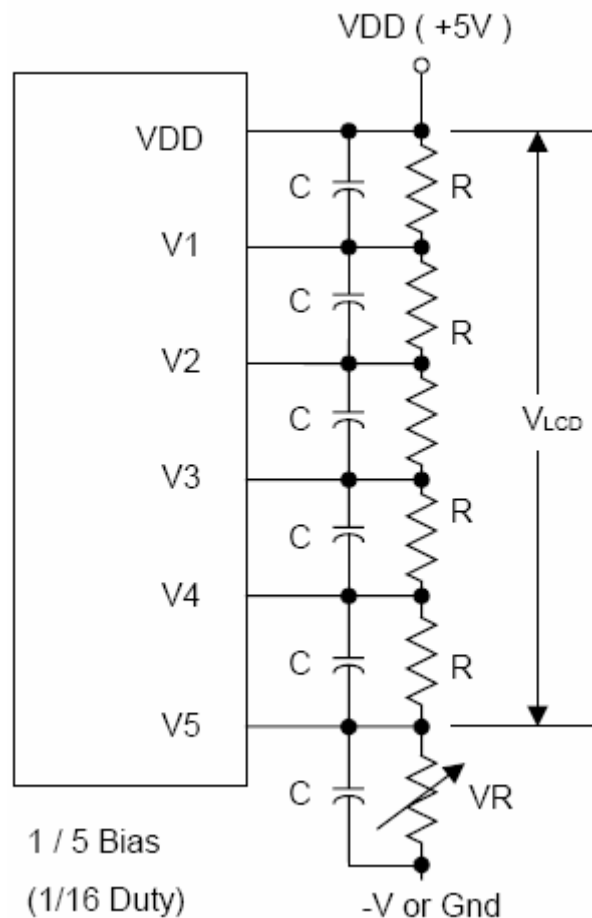
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8. BLOCK DIAGRAM



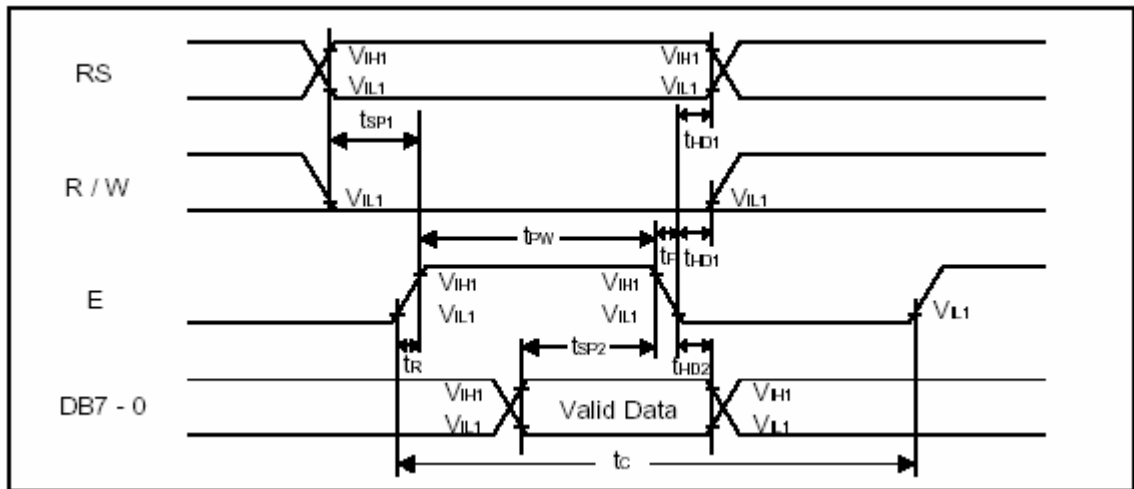
9. POWER SUPPLY



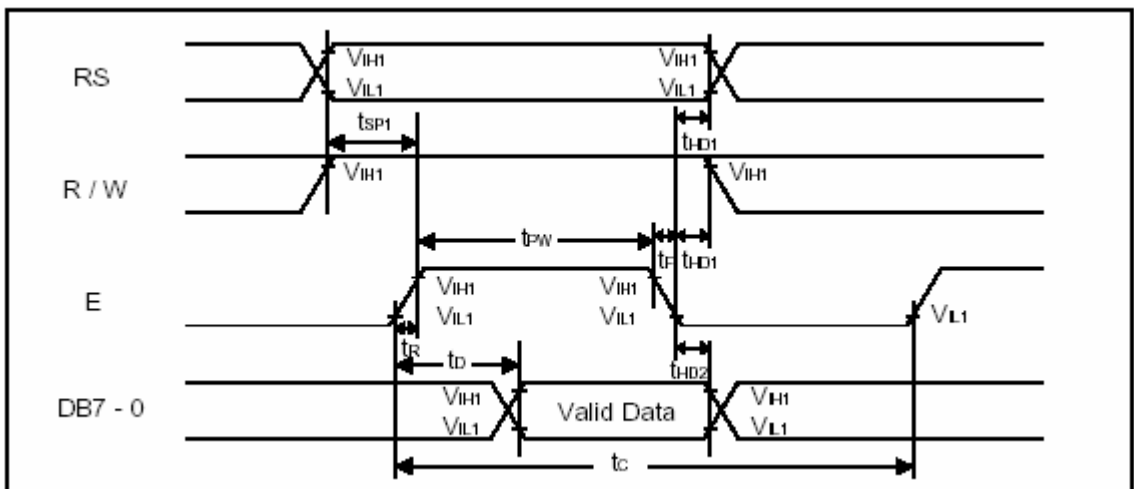
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10. TIMING DIAGRAM

• WRITE OPERATION



• READ OPERATION



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11. AC CHARACTERISTICS

• WRITE MODE

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t _c	1000	-	-	ns	Pin E
E Pulse Width	t _{pw}	450	-	-	ns	Pin E
E Rise/Fall Time	t _r , t _f	-	-	25	ns	Pin E
Address Setup Time	t _{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t _{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t _{SP2}	195	-	-	ns	Pins: DB7 - 0
Data Hold Time	t _{HD2}	10	-	-	ns	Pins: DB7 - 0

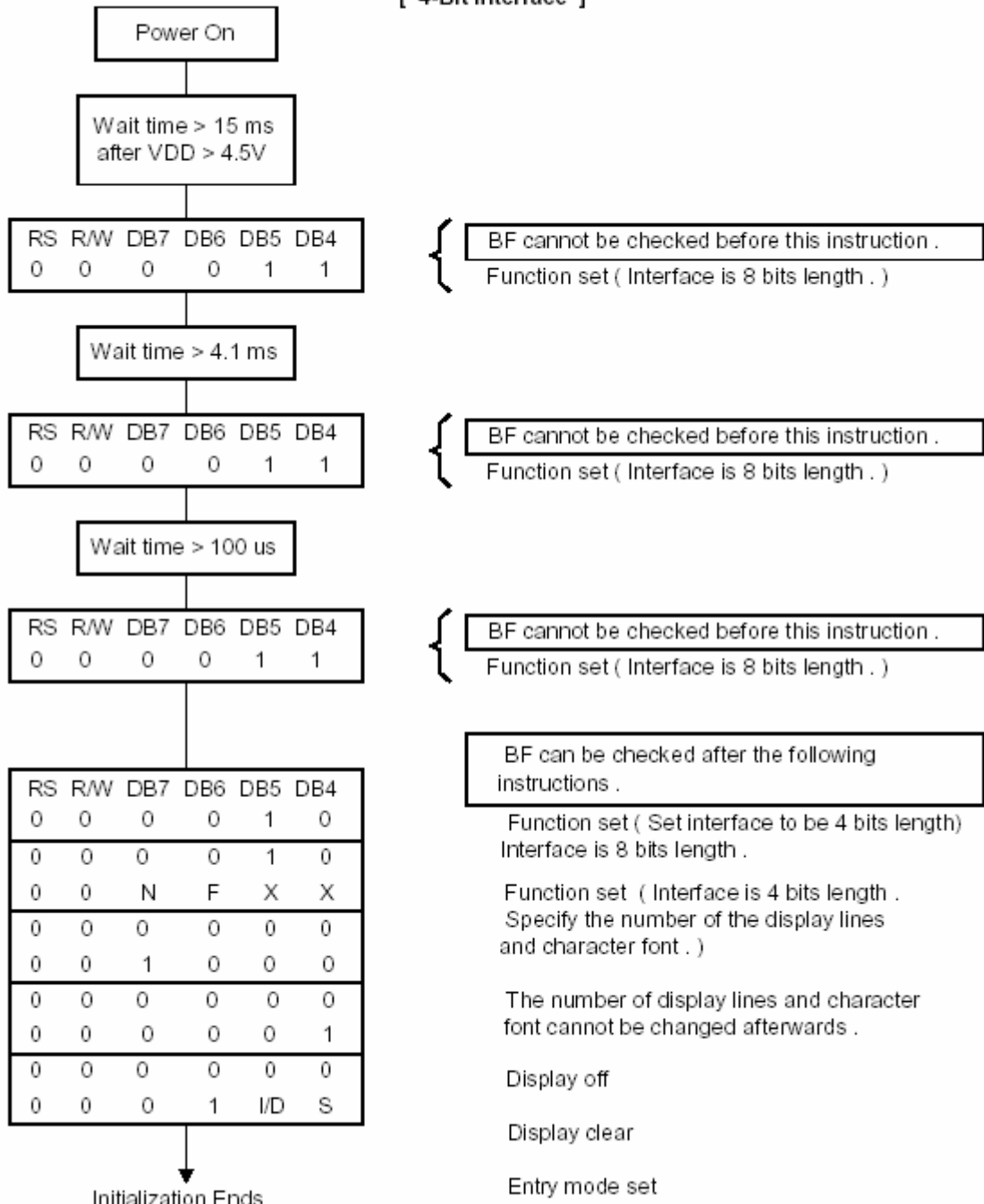
• READ MODE

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t _c	1000	-	-	ns	Pin E
E Pulse Width	t _w	450	-	-	ns	Pin E
E Rise/Fall Time	t _r , t _f	-	-	25	ns	Pin E
Address Setup Time	t _{SP1}	60	-	-	ns	Pins: RS, R/W,E
Address Hold Time	t _{HD1}	20	-	-	ns	Pins: RS, R/W,E
Data Output Delay Time	t _o	-	-	360	ns	Pins: DB7 - 0
Data hold time	t _{HD2}	5.0	-	-	ns	Pin DB7 - 0

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12. INITIALIZATION SEQUENCE

[4-Bit Interface]



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13. INSTRUCTION SET

COMMAND	COMMAND CODE										COMMAND CODE	E-CYCLE f _{osc} =250KHz	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
SCREEN CLEAR	0	0	0	0	0	0	0	0	0	1	Screen Clear, Set AC to 0 Cursor Reposition	1.64ms	
CURSOR RETURN	0	0	0	0	0	0	0	0	0	1	*	DDRAM AD=0, Return, Content Changeless	1.64ms
INPUT SET	0	0	0	0	0	0	0	0	1	I/D	S	Set moving direction of cursor, Appoint if move	40us
DISPLAY SWITCH	0	0	0	0	0	0	0	1	D	C	B	Set display on/off,cursor on/off, blink on/off	40us
SHIFT	0	0	0	0	0	0	1	S/C	R/L	*	*	Remove cursor and whole display,DDRAM changeless	40us
FUNCTION SET	0	0	0	0	0	1	DL	N	F	*	*	Set DL,display line,font	40us
CGRAM AD SET	0	0	0	0	1	ACG					Set CGRAM AD, send receive data	40us	
DDRAM AD SET	0	0	0	1	ADD					Set DDRAM AD, send receive data	40us		
BUSY/AD READ CT	0	0	1	BF	AC					Executing internal function, reading AD of CT	40us		
CGRAM/ DDRAM DATA WRITE	1	0	DATA WRITE					Write data from CGRAM or DDRAM				40us	
CGRAM/ DDRAM DATA READ	1	1	DATA READ					Read data from CGRAM or DDRAM				40us	
	I/D=1: Increment Mode; I/D=0: Decrement Mode S=1: Shift S/C=1: Display Shift; S/C=0: Cursor Shift R/L=1: Right Shift; R/L=0: Left Shift DL=1: 8D DL=0: 4D N=1: 2R N=0: 1R F=1: 5x10 Style; F=0: 5x7 Style BF=1: Execute Internal Function; BF=0: Command Received										DDRAM: Display data RAM CGRAM: Character Generator RAM ACG: CGRAM AD ADD: DDRAM AD & Cursor AD AC: Address counter for DDRAM & CGRAM	E-cycle changing with main frequency. Example: If f _{cp} or f _{osc} =270KHz 40us x 250/270 =37us	

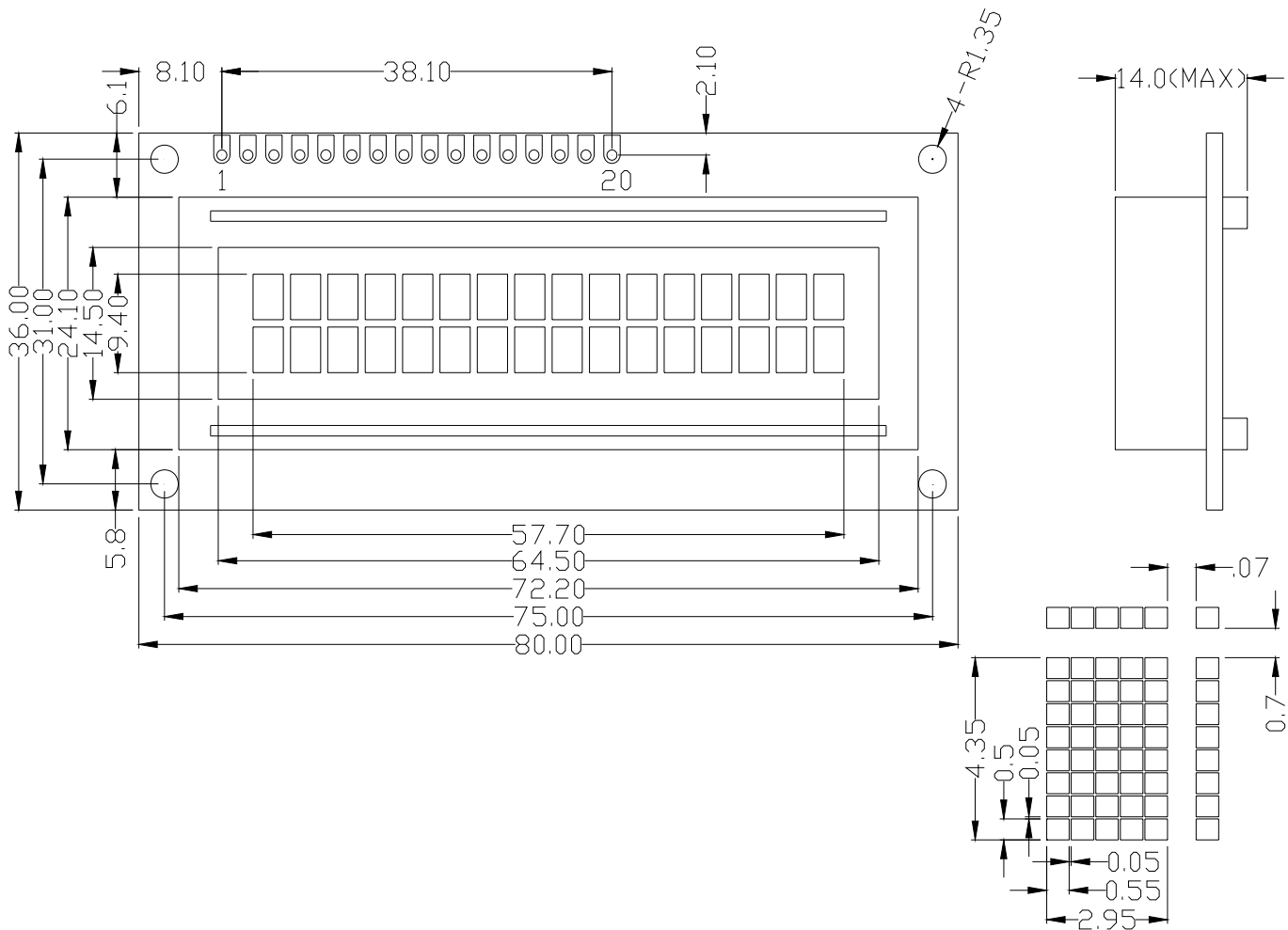
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14. FONT TABLE

b7- b3 b4 -b0		0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)		0	a	P	`	P		—	9	E		α	p
0001	(2)	!	1	A	Q	a	q	a	7	+	4		ä	q
0010	(3)	"	2	B	R	b	r	r	イ	ウ	×		ß	θ
0011	(4)	#	3	C	S	c	s	」	ウ	テ	E		ε	∞
0100	(5)	\$	4	D	T	d	t	、	工	ト	ト		μ	Ω
0101	(6)	%	5	E	U	e	u	・	オ	ナ	1		ε	0
0110	(7)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ		ρ	Σ
0111	CG RAM (8)	'	7	G	W	g	w	7	+	ヌ	ウ		g	π
1000	CG RAM (1)	(8	H	X	h	x	イ	ウ	ホ	リ		γ	×
1001	(2))	9	I	Y	i	y	ウ	ク	リ	ル		ˆ	y
1010	(3)	*	:	J	Z	j	z	エ	コ	ン	レ		j	≠
1011	(4)	+	:	K	[k	[オ	サ	ヒ	ロ		*	π
1100	(5)	,	<	L	¥	l	l	ホ	シ	フ	ワ		φ	π
1101	(6)	—	=	M	I	m	}	ユ	ズ	へ	ン		±	÷
1110	(7)	.	>	N	^	n	→	ヨ	セ	ホ	・		ñ	
1111	CG RAM (8)	/	?	O	_	o	+	ッ	リ	マ	"		ö	■

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16. EXTERNAL DIMENSION



1	2	3	4	5	6	7	8
VSS	VCC	VEE	RS	R/W	E	DB0	DB1
9	10	11	12	13	14	15	16
DB2	DB3	DB4	DB5	DB6	DB7	LED+	LED-

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17. INTERFACE

PIN NO.	SYMBOL	DESCRIPTION	FUNCTION
1	VSS	GROUND	0V (GND)
2	VCC	POWER SUPPLY FOR LOGIC CIRCUIT	+5V
3	VEE	LCD CONTRAST ADJUSTMENT	
4	RS	INSTRUCTION/DATA REGISTER SELECTION	RS = 0 : INSTRUCTION REGISTER RS = 1 : DATA REGISTER
5	R/W	READ/WRITE SELECTION	R/W = 0 : REGISTER WRITE R/W = 1 : REGISTER READ
6	E	ENABLE SIGNAL	
7	DB0	DATA INPUT/OUTPUT LINES	8 BIT: DB0-DB7
8	DB1		
9	DB2		
10	DB3		
11	DB4		
12	DB5		
13	DB6		
14	DB7		
15	LED+	SUPPLY VOLTAGE FOR LED+	+5V
16	LED-	SUPPLY VOLTAGE FOR LED-	0V

74LS138 / 74LS138-SMD / 74LS139

Decoder/Demultiplexer

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The DM74LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The DM74LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
 - Memory decoders
 - Data transmission systems
- DM74LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- DM74LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)

DM74LS138	21 ns
DM74LS139	21 ns
- Typical power dissipation

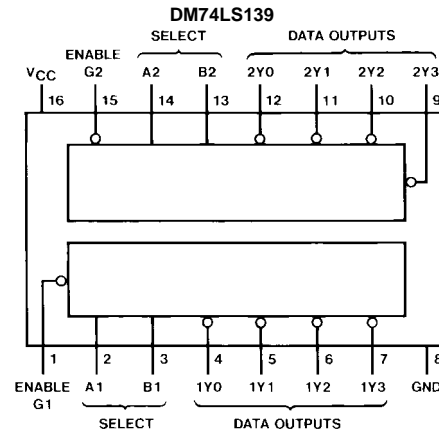
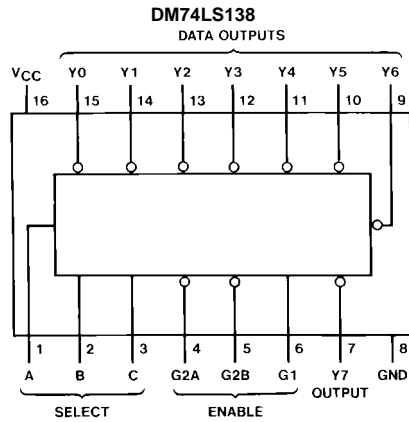
DM74LS138	32 mW
DM74LS139	34 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74LS138M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS138N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74LS139M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS139SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS139N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams



Function Tables

DM74LS138

Inputs			Outputs							
Enable		Select								
G1	G2 (Note 1)	C B A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X X X	H	H	H	H	H	H	H	H
L	X	X X X	H	H	H	H	H	H	H	H
H	L	L L L	H	H	H	H	H	H	H	H
H	L	L L H	H	H	H	H	H	H	H	H
H	L	L H L	H	H	H	H	H	H	H	H
H	L	L H H	H	H	H	H	H	H	H	H
H	L	H L L	H	H	H	H	H	H	H	H
H	L	H L H	H	H	H	H	H	H	H	H
H	L	H H L	H	H	H	H	H	H	H	H
H	L	H H H	H	H	H	H	H	H	H	L
H	L	H H H	H	H	H	H	H	H	L	L

DM74LS139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Level
L = LOW Level
X = Don't Care

Note 1: G2 = G2A + G2B

Logic Diagrams

