**Acceptance Filter Requirement（Prefix：AF）**

**Reset Condition:**

1. ‘o\_rx\_w\_en’ and ‘o\_acfbsy’ shall be set to 0 when ‘i\_reset’ is 1.
2. ‘o\_rx\_fifo\_w\_data[127:0]’ shall be set to all 0s when ‘i\_reset’ is 1.

**Acceptance Filter Register (Prefix: AF\_AFR)**

1. ‘i\_can\_ready’ and ‘i\_rx\_message[127:0]’ shall be synchronized with the ‘i\_sys\_clk’.
2. If ‘i\_uaf1’ is set to 1 and input data ‘i\_rx\_message[127:96]’ is passed checking by AFR1, internal signal ‘in\_pass1’ shall be set to 1.
3. If ‘i\_uaf1’ is set to 0 or input data ‘i\_rx\_message[127:96]’ isn’t passed checking by AFR1, internal signal ‘in\_pass1’ shall be set to 0.
4. If ‘i\_uaf2’ is set to 1 and input data ‘i\_rx\_message[127:96]’ is passed checking by AFR2, internal signal ‘in\_pass2’ shall be set to 1.
5. If ‘i\_uaf2’ is set to 0 or input data ‘i\_rx\_message[127:96]’ isn’t passed checking by AFR2, internal signal ‘in\_pass2’ shall be set to 0.
6. If ‘i\_uaf3’ is set to 1 and input data ‘i\_rx\_message[127:96]’ is passed checking by AFR3, internal signal ‘in\_pass3’ shall be set to 1.
7. If ‘i\_uaf3’ is set to 0 or input data ‘i\_rx\_message[127:96]’ isn’t passed checking by AFR3, internal signal ‘in\_pass3’ shall be set to 0.
8. If ‘i\_uaf4’ is set to 1 and input data ‘i\_rx\_message[127:96]’ is passed checking by AFR4, internal signal ‘in\_pass4’ shall be set to 1.
9. If ‘i\_uaf4’ is set to 0 or input data ‘i\_rx\_message[127:96]’ isn’t passed checking by AFR4, internal signal ‘in\_pass4’ shall be set to 0.
10. Internal signal ‘next\_state’ shall enter ‘compare’ state from ‘idle’ state when ‘i\_can\_ready’ is 1 and ‘i\_rx\_full’ is set to 0;
11. Module shall set ‘o\_rx\_w\_en’ to 1 for one clock cycle on the rising edge of ‘i\_sys\_clk’, if internal signal ‘current\_state’ is in ‘pass’ state.
12. Internal signal ‘current\_state’ shall stay in ‘idle’ state, when ‘i\_rx\_full’ is set to 1.
13. ‘o\_rx\_fifo\_w\_data[127:0]’ shall be set to the corresponding bits from ‘i\_rx\_message[127:0]’ on the rising edge of ‘i\_sys\_clk’, if internal signal ‘current\_state’ is in ‘pass’ state.
14. ‘o\_rx\_fifo\_w\_data[127:0]’ shall retain its previous value, if internal signal ‘current\_state’ is in ‘idle’ state.
15. . If all exist ‘i\_uaf’ bits or number of acceptance filters are set to 0, ‘o\_rx\_w\_en’ shall be set to 1 for one clock cycle on the rising edge of ‘i\_sys\_clk’ when ‘i\_can\_ready’ is set to 1 and ‘i\_rx\_full’ is set to 0.
16. If all exist ‘i\_uaf’ bits or number of acceptance filters are set to 0, ‘o\_rx\_fifo\_w\_data[127:0]’ shall be set to the corresponding bits from ‘i\_rx\_message[127:0]’ on the rising edge of ‘i\_sys\_clk’
17. If all exist ‘i\_uaf’ bits or number of acceptance filters are set to 0,’o\_acfbsy’ shall be set to 0.
18. If any exist ‘i\_uaf’ bit is set to 0, ‘o\_acfbsy’ shall be set to 1 on the rising edge of ‘i\_sys\_clk’.

**Acceptance Filter ID Register (Prefix: AF\_AFIR)**

1. If ‘i\_uaf1’ is set to 0, internal ID register ’AFIR1[31:0]’ shall be set to the corresponding bits from ‘i\_afir1[31:0]’ on the rising edge of ‘i\_sys\_clk’
2. If ‘i\_uaf2’ is set to 0, internal ID register ’AFIR2[31:0]’ shall be set to the corresponding bits from ‘i\_afir2[31:0]’ on the rising edge of ‘i\_sys\_clk’
3. If ‘i\_uaf3’ is set to 0, internal ID register ’AFIR3[31:0]’ shall be set to the corresponding bits from ‘i\_afir3[31:0]’ on the rising edge of ‘i\_sys\_clk’
4. If ‘i\_uaf4’ is set to 0, internal ID register ’AFIR4[31:0]’ shall be set to the corresponding bits from ‘i\_afir4[31:0]’ on the rising edge of ‘i\_sys\_clk’

**Acceptance Filter Master Register (Prefix: AF\_AFMR)**

1. If ‘i\_uaf1’ is set to 0, internal mask register ’AFMR1[31:0]’ shall be set to the corresponding bits from ‘i\_afmr1[31:0]’ on the rising edge of ‘i\_sys\_clk’
2. If ‘i\_uaf2’ is set to 0, internal mask register ’AFMR2[31:0]’ shall be set to the corresponding bits from ‘i\_afmr2[31:0]’ on the rising edge of ‘i\_sys\_clk’
3. If ‘i\_uaf3’ is set to 0, internal mask register ’AFMR3[31:0]’ shall be set to the corresponding bits from ‘i\_afmr3[31:0]’ on the rising edge of ‘i\_sys\_clk’
4. If ‘i\_uaf4’ is set to 0, internal mask register ’AFMR4[31:0]’ shall be set to the corresponding bits from ‘i\_afmr4[31:0]’ on the rising edge of ‘i\_sys\_clk’