**TX Priority Logic (TXPL):**

1. All output signals shall be set to zeros when ‘i\_reset’ is set to 1.
2. Output data to the stream processor shall be synchronized to the CAN clock.
3. ‘o\_send\_en’ shall be synchronized to the CAN clock.
4. ‘i\_busy\_can’ shall be synchronized to the system clock.
5. The module shall implement a state machine running on the system clock.
6. The state machine shall have at least the following states: idle, prepare, send\_hpb and send\_fifo.
7. The state machine shall be initialized at idle state.
8. The state machine shall transition to and stay in idle state when ‘i\_reset’ is set to 1.
9. ‘o\_send\_en’ shall be set to 0 when the state is in idle.
10. The state shall transition from idle to prepare when ‘i\_busy\_can’ is set to 0 and ‘i\_cen’ is set to 1.
11. The state shall transition from prepare to send\_hpb when ‘i\_busy\_can’ is set to 0, ‘i\_cen’ is set to 1 and ‘i\_hpbfull’ is set to 1.
12. ‘o\_hpb\_r\_en’ shall be pulsed for one system clock cycle when the state transitions from prepare to send\_hpb.
13. ‘i\_hpb\_data’ shall be latched internally when the state transitions from prepare to send\_hpb.
14. The state shall transition from prepare to send\_fifo when ‘i\_busy\_can’ is set to 0, ‘i\_cen’ is set to 1, ‘i\_hpbfull’ is set to 0 and ‘i\_tx\_empty’ is set to 0.
15. ‘o\_fifo\_r\_en’ shall be pulsed for one system clock cycle when the state transitions from prepare to send\_fifo.
16. ‘i\_fifo\_data’ shall be latched internally when the state transitions from prepare to send\_fifo.
17. ‘o\_send\_en’ shall be set to 1 when the state is in send\_hpb or send\_fifo.
18. ‘o\_send\_data’ shall be set to the latched data when the state is in send\_hpb or send\_fifo.
19. The state shall transition from send\_hpb to idle when ‘i\_busy\_can’ is set to 1 and ‘i\_cen’ is set to 1.
20. The state shall transition from send\_fifo to idle when ‘i\_busy\_can’ is set to 1 and ‘i\_cen’ is set to 1.