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Requirements: FIFO

* FIFO\_00: The FIFO module shall have a parameterizable memory depth variable, labeled ‘DEPTH’, that can have a value of either 2, 4, 8, 16, 32, or 64.
* FIFO\_01: ‘o\_full’, ‘o\_overflow’, and ‘o\_underflow’ shall be set to 0 when ‘i\_reset’ is 1.
* FIFO\_02: ‘o\_empty’ shall be set to 1 when ‘i\_reset’ is 1.
* FIFO\_03: ‘o\_underflow’ shall be 1 for one clock cycle only when ‘i\_sys\_clk’ transitions from 0 to 1 when both ‘i\_r\_en’ and ‘o\_empty’ are 1.
* FIFO\_04: ‘o\_overflow’ shall be 1 for one clock cycle only when ‘i\_sys\_clk’ transitions from 0 to 1 when both ‘i\_w\_en’ and ‘o\_full’ are 1.
* FIFO\_05: ‘o\_empty’ shall be 1 only when the internal read and write pointers are equal.
* FIFO\_06: ‘o\_full’ shall be 1 only when the internal read and write pointers’ most significant bit are not equal and while the least significant bits are equal.
* FIFO\_07: The internal write pointer shall be incremented by a value of 1 when ‘i\_sys\_clk’ is set from 0 to 1 while ‘i\_w\_en’ is 1, unless ‘o\_full’ is 1.
* FIFO\_08: The memory location the internal write pointer is pointing to shall store the input of ‘i\_fifo\_w\_data’ when i\_sys\_clk transitions from 0 to 1 when i\_w\_en is 1, unless o\_full is 1.
* FIFO\_09: The internal read pointer shall be incremented by a value of 1 when ‘i\_sys\_clk’ is set from 0 to 1 while ‘i\_r\_en’ is 1, unless ‘o\_empty’ is 1.
* FIFO\_10: ‘o\_fifo\_r\_data’ shall output the value at the register the read pointer is currently pointing to.
* FIFO\_11: The memory locations within the FIFO module shall be set to 0 when i\_reset is 1.