**Purpose:**

Create a stop-watch module in Verilog that runs on the Nexys A7 development board.

**Scope:**

A stop-watch that runs from 0:00:00 to 9:59:99 formatted as M:ss:mm (M: minute, s: second, m: milli-second) , with one button to reset and one button to stop/start count.

**General Requirements:**

**Trigger Detection Circuit**

**1 Second Timer**

**12 Bit Up Counter**

**7-Segment Display**

**Traceability:**