Indian Institute of Technology Kharagpur

AUTUMN Semester, 2021
COMPUTER SCIENCE AND ENGINEERING

Computer Organization Laboratory

Laboratory Test–2 (Version–1 [for odd roll numbers])

Full Marks: 20

Time allowed: 2 hours

INSTRUCTIONS: Every student should make one submission in the form of a single zipped folder containing his/her Verilog source code files(s) and Verilog testbench. Name your submitted zipped folder as `CT_2_Ver_1_<Roll_no>.zip`. Inside each submitted source and testbench files, there should be a clear header describing the name and roll number of the submitting student. Liberally comment your code to improve its comprehensibility.

1. [**Unsigned Binary Sequential Multiplier Using Right Shifts**] Consider the iterative multiplication of two n-bit unsigned integers, $X = \sum_{j=0}^{n-1} x_j 2^j$ and $Y = \sum_{j=0}^{n-1} y_j 2^j$, to form the $2n$-bit product $P = X \cdot Y$. Multiplication proceeds by calculating the partial products $P_{i+1} = P_i + x_j 2^i Y$ for each bit x_j of the multiplier, with $P_0 = 0$ and $P_n = P$. However, for hardware implementation, an alternative scheme is preferable. In the i-th iteration, the following calculation is performed:

$$P_i = P_i + x_j Y \quad \text{and} \quad P_{i+1} = 2^{-1} P_i \tag{1}$$

Design (using Verilog) and simulate an **6-bit unsigned binary sequential multiplier** following the scheme of Eqn. (1). Include a proper Verilog testbench to simulate it. The interface of your top-level design should be:

```
module sign_mag_seq_mult (input clk, input start, input [5:0] a, input [5:0] b, output
done, output [11:0] product);
```

It is suggested that you modularize your design, to clearly differentiate between the data path and the control path. (20 marks)