Indian Institute of Technology Kharagpur

COA-22 Verilog Assignment-2

Designing Counters and Displaying the output on the LEDs of the FPGA Board

Hardik Pravin Soni 20CS30023

Abhay Kumar Keshari 20CS10001

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1 Problem Definition

Binary Counter: is a sequential circuit. An up-counter will count up, say from 0. Consider a 4-bit binary counter, which when reset is initialized to 0000, and then at the positive edge of the clock starts counting in the sequence: $(0000)_2, (0001)_2, (0010)_2, (0011)_2, ..., (1111)_2, (0000)_2$. Let us consider two ways of designing the above counter.

1.1 Behavioral Design

Write a verilog code to design the up-counter. You can use verilog constructs to define the logic of the counter. The counter should have an asynchronous reset, so that the counter can be reset at any time to zero. The result of the counter should be displayed on the LED's in your board.

1.2 Structural Design

Design the architecture of the up-counter using a 4-bit adder. Note that you can design an add by one adder by optimizing the design of the RCA/CLA you have done in the last assignment. Work out the details of the optimized add-by-one block, and write the verilog codes. Also you need to design a D-FlipFlop as mentioned in the lab. Draw the architecture for the up-counter, with the above blocks as sub-modules.

2 Abstract

2.1 Behavioral Design

The 4-bit counter starts incrementing from 4'b0000 to 4'h1111 and come back to 4'b0000. It will keep counting as long as it is provided with a running clock, and reset is held high.

The rollover happens when the most significant bit of the final addition gets discarded. When the counter is at a maximum value of 4'h1111 and gets one more count request, the counter tries to reach 5'b10000, but since it can support only 4-bits, the MSB will be discarded, resulting in 0.

2.2 Structural Design

When it comes to optimise the design of a 4-bit asynchronous counter with the help of a CLA, we make use of CLA with inputs (a = counter[3:0], b = $(0000)_2$, $c_{in} = 1$). We solve the equations for Block Propagate Signal and the Generate Signal to obtain the following Boolean expressions for the CLA:-

$$out_0 = \neg a_0$$

$$out_1 = a_1 \oplus a_0$$

$$out_2 = a_2 \oplus (a_1 \& a_0)$$

$$out_3 = a_3 \oplus (a_2 \& a_1 \& a_0)$$

3 Implementation

3.1 Behavioral Design

In digital logic and computing, a Counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. Counters are used in digital electronics for counting purpose, they can count specific event happening in the circuit. For example, in UP counter a counter increases count for every rising edge of clock. Not only counting, a counter can follow the certain sequence based on our design like any random sequence 0,1,3,2... .They can also be designed with the help of flip flops.flip-flops. It is a group of flip-flops with a clock signal applied.

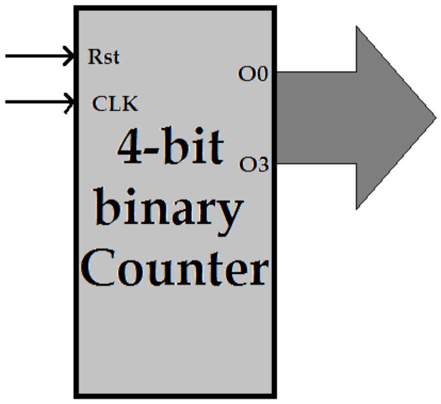

Figure 1: Schematic Diagram of the 4-bit Counter

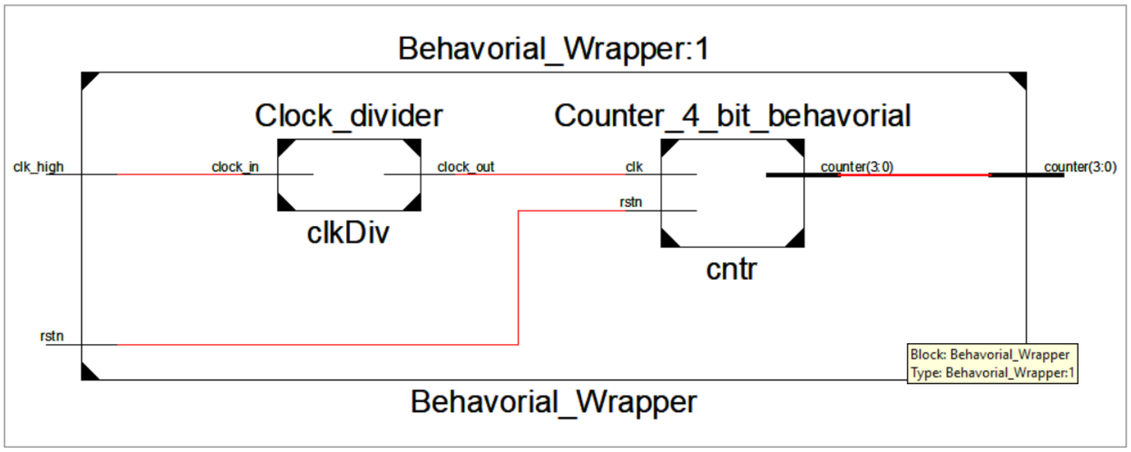

Figure 2: Circuit Diagram of Behavioral Design

Asynchronous or Ripple Counters In asynchronous counter we don't use universal clock, only first flip flop is driven by main clock and the clock input of rest of the following counters is driven by output of previous flip flops. We can understand it by following diagram.

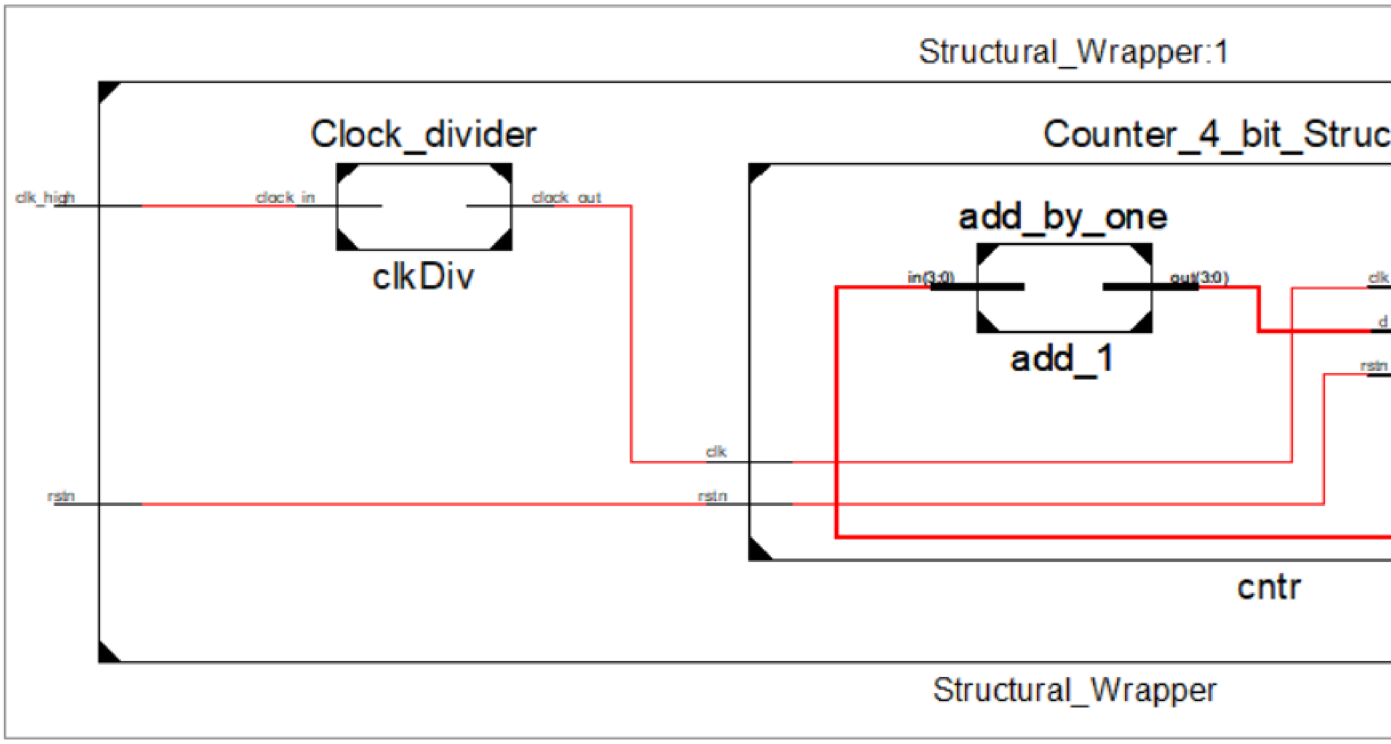

Figure 3: Circuit Diagram of

Figure 4: Circuit Diagram of

3.2 Structural Design

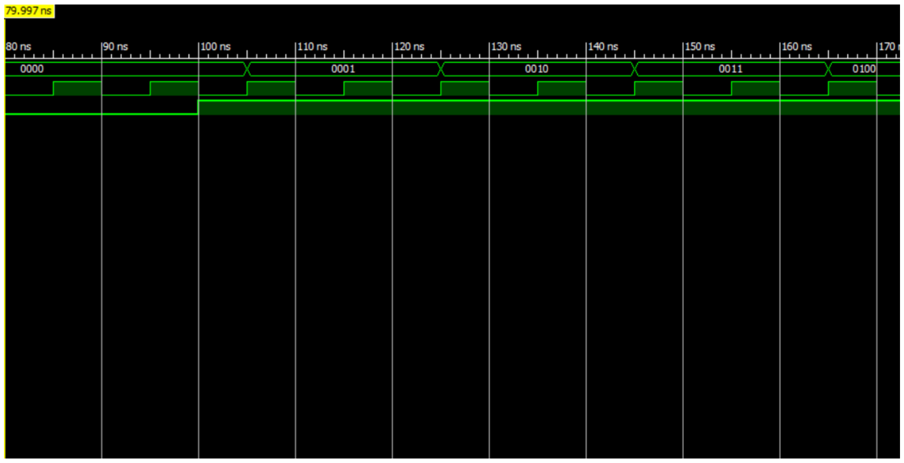

Figure 5: Wave Signal with Clock Divider

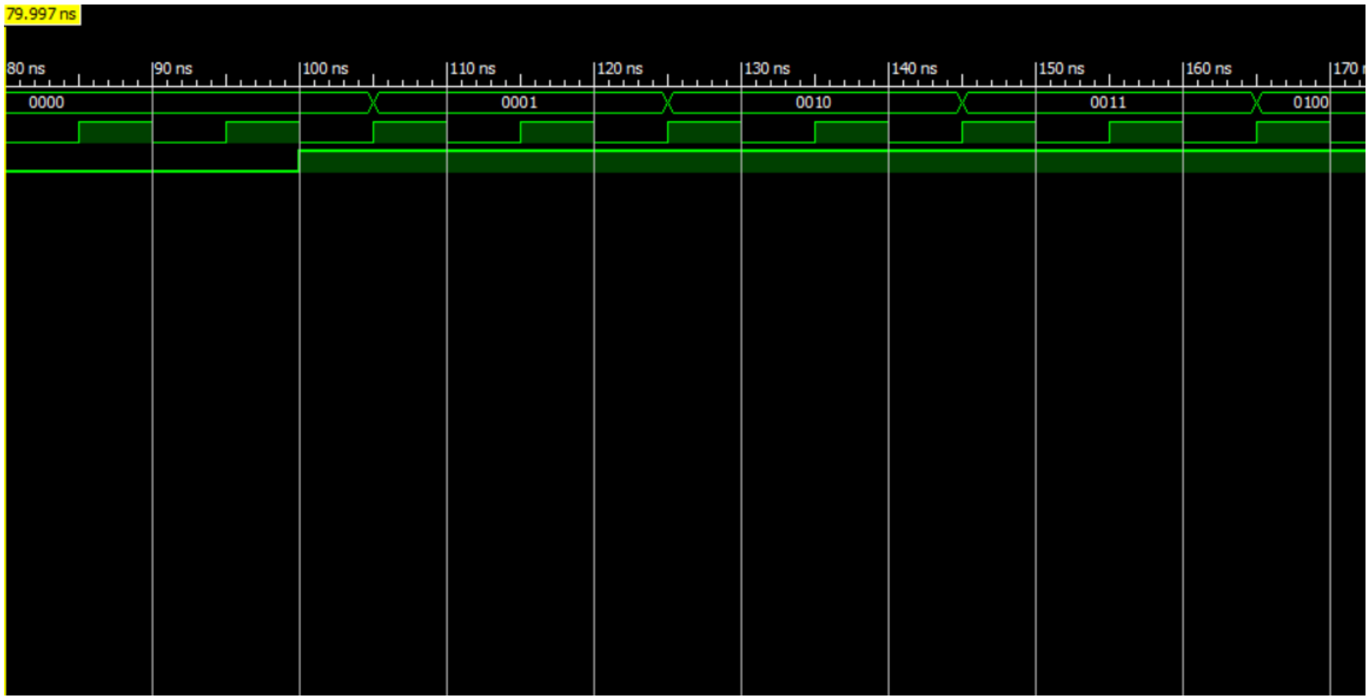

Figure 6: Wave Signal without Clock Divider

4 Conclusion

With the Optimised **add-by-one** module employing the 4-bit CLA as well as using D-Flip Flops in order to retrieve the value during positive edge of the clock cycle in the structural design of the 4-bit binary counter has increased it's efficiency and reduced it's gate delay.