CS 31007 Autumn 2021 COMPUTER ORGANIZATION AND ARCHITECTURE

Instructors

Rajat Subhra Chakraborty (RSC)

Bhargab B. Bhattacharya (BBB)

Lecture #3: Tutorial

12 August 2021

Indian Institute of Technology Kharagpur Computer Science and Engineering

1. Consider the following Boolean function F of three variables A, B, C:

$$F(A, B, C) = \overline{(AB + BC + CA)} \oplus AB \oplus BC \oplus CA$$

where \oplus denotes Exclusive-OR (XOR) operation and "bar" denotes complementation. F is equivalent to (choose one):

(i) ABC, (ii) ABC,

(iii) 0,

(iv) 1, (v) none of these

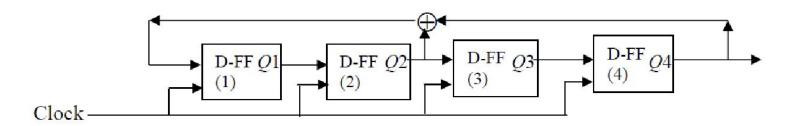
Show your work.

Answer: (iv) 1

$$G(A,B,C) = AB + BC + CA$$

$$= AB + BC + CA$$

2. In the following circuit, four D flip-flops (D-FF) are connected serially to form a 4-bit register as shown. All the flip-flops are leading-edge clock triggered. The present state of the register (Q1 Q2 Q3 Q4) is 0 1 0 1. The symbol ⊕ denotes exclusive-OR operation.

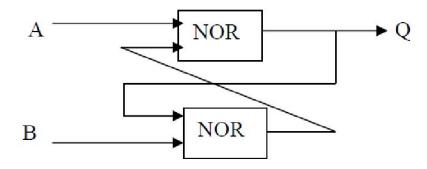


Just after the arrival of the two clock pulses, the state (Q1 Q2 Q3 Q4) of the register will be (choose one):

(i) 1 0 1 0 (ii) 0 1 0 1 (iii) 0 0 1 1 (iv) 0 0 0 1 (vi) none of these

Answer: (iv) 0001

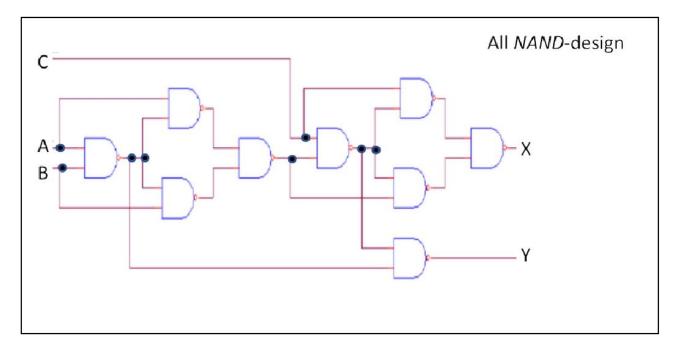
3. Two NOR gates are cross-connected to form a latch as shown. We set A = B = 1, and the circuit is allowed to become stable. Next, we set A = B = 0. The logic value at the output Q (choose one):



- (i) 0, (ii) 1, (iii) is stable, but cannot be predicted, (iv) depends on previous inputs,
- (v) oscillates between 0 and 1, (vi) none of these.

Answer: (iii)

4. In the logic circuit shown below, express X and Y in terms of Boolen inputs A, B, C. What operations are performed by this circuit?



Answer: X is the Sum function of a binary full-adder (parity function), i.e., $X = A \oplus B \oplus C$; Y is the Carry function (majority function), i.e.,

$$Y = AB + BC + CA$$
;

- 5. You are given a hypothetical computer M where all words comprise only 8 bits each. M is capable of performing signed integer addition in 2's complement arithmetic. The result of adding two signed binary numbers A = 01100011 and B = 00101010, i.e., A + B will be (choose one):
- (i) 01001001, (ii) 10001101, (iii) 11101101, (iv) invalid result, (v) none of these.

Answer: (iv) invalid result;

Solution: Apparently the answer is (ii) 10001101; however, both A and B are positive numbers, and the result becomes negative in 2's complement arithmetic. Hence, it is case of overflow. Thus, the correct answer is (iv) invalid result.

6. Convert the following sign-magnitude number into 8-bit 2's complement binary: 10001010

Solution: The number is -10 in decimal; Hence, in 2's complement binary, it is 11110110.

7. Synthesize an XOR-gate using a 2 \rightarrow 1 MUX. Use minimum additional logic.