# Sukhyun Han (한석현)

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## Research Interests

Domain Specific Accelerator Architecture
- Deep Learning Accelerator Architecture
- Memory Subsystem for Domain Specific Accelerators
- Hardware-Software Co-Design Methodology

Artificial Intelligence
- Software Optimization for DL Accelerators
- Static Compilation of DNN Models

## Education

**Ph.D Course**
Sungkyunkwan university, Suwon, South Korea (Aug. 2025 ~ Present)
Department of Electrical and Computer Engineering

**Master's Degree**
Sungkyunkwan university, Suwon, South Korea (Mar. 2024~ Aug. 2025)
Department of Electrical and Computer Engineering

**Bachelor's Degree**
Sungkyunkwan university, Suwon, South Korea (Mar. 2019 ~ Mar. 2024)
Department of Electronic and Electrical Engineering

## Skills and Techniques

Programming Languages
- Digital system design with Verilog HDL
- Software programming with C, C++, Python
- Deep Learning Frameworks (PyTorch, ONNX, …)

EDA Tool
- Synopsys Design Compiler
- Vivado FPGA Suite

## Major Publications

**Avalanche: Optimizing Cache Utilization via Matrix Reordering for Sparse Matrix Multiplication Accelerator**
- 2025 International Symposium on Computer Architecture (ISCA 2025)
- Gwangeun Byeon, **Seongwook Kim**, Hyungjin Kim, Sukhyun Han, Jinkwon Kim, Prashant Nair, Taewook Kang, Seokin Hong

- This paper addresses cache contention in sparse matrix multiplication accelerators with outer product dataflow. My major contribution on this paperwork is to implement the Avalanche architecture into the RTL model and measure hardware overhead of this architecture by using Synopsys Design Compiler.

**Zebra: Leveraging Diagonal Attention Pattern for Vision Transformer Accelerator**

- 2025 Design, Automation & Test in Europe Conference & Exhibition (DATE 2025)
- Sukhyun Han, **Seongwook Kim**, Gwangeun Byeon, Jihun Yoon, Seokin Hong
- This paper proposes a novel accelerator for ViT. This paper reveals that the self-attention map of ViT models usually show the diagonal pattern, and it is possible to apply pruning with respect to the pattern. My major contribution on this paperwork is to give some advice about some details of the hardware architecture.

## Publications

## Projects and Research Experiences