CSE 321b: Computer Organization (II)
Third Year, Computer & Systems Engineering

Assignment #1

Due date: **Wednesday, March 8th, 2017**

1. A 2M×8 read-only memory is to be implemented using 512K×4 ROM chips (with no chip-select (CS) lines) and 2×1 (single-bit) multiplexers.
   (a) How many ROM chips and multiplexers are required to implement this memory?
   (b) Draw a block diagram of the memory to show how the ROM chips should be connected together with the multiplexers and how the input address lines and the output data lines are routed. Make sure in your design to map successive memory locations to different chips.
   (c) Calculate the overall access time of the memory given that the access time of each ROM chip is 9ns and the propagation delay of each multiplexer is 3ns.

2. A DDR3-SDRAM module contains four memory chips. All the chips receive the same address and command. The module can store 1 GB of data that can be transferred in 64-bit words over the bus at a maximum rate of 12800 MB/s.
   (a) Represent the size of each memory chip in the form "$m \times n$".
   (b) What is the bus speed (in MHz)?
   (c) What is memory speed (in MHz)?

3. A memory chip is equipped with a **SEC** mechanism that uses 18-bit long codewords.
   (a) How many check bits are contained in each codeword?
   (b) Suppose the following codeword is read at some point from memory: "101111101110111000":
      i. Show that this codeword is illegal.
      ii. Describe the error in this codeword.
      iii. Identify the closest legal codeword to this codeword.

4. An error correcting code contains four 10-bit codewords. Two of which are "0101101001" and "1010001111". Suppose the code can correct double-bit errors and detect triple-bit errors.
   (a) What must be the minimum Hamming distance of this code? Justify your answer.
   (b) Suggest a suitable value for each the other two codewords.