

CSE 321a: Computer Organization (I)
Third Year, Computer & Systems Engineering

Solution to Assignment #2

Two otherwise identical memory systems, MS₁ and MS₂, have slightly different cache ...

1. Show the address format for each of the two memory systems MS₁ and MS₂.

$$s + w = \log_2 16K = 14$$

For MS₁:

$$w = \log_2 (128/8) = 4$$

$$r = \log_2 8 = 3$$

Format:

Tag ($s - r$) [7 bits]	Line (r) [3 bits]	Word (w) [4 bits]
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For MS₂:

$$w = \log_2 (64/8) = 3$$

$$d = \log_2 (8/2) = 2$$

Format:

Tag ($s - d$) [9 bits]	Set (d) [2 bits]	Word (w) [3 bits]
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2. Fill up the following table according to the read and write operations ...

	Iteration	1 st						2 nd							
	Instruction	1 st	2 nd	3 rd		4 th		5 th	1 st	2 nd	3 rd		4 th		5 th
	<u>F</u> etch/ <u>E</u> xecute (F/E)	F	F	F	E	F	E	F	F	F	F	E	F	E	F
	<u>R</u> ead/ <u>W</u> rite (R/W)	R	R	R	W	R	R	R	R	R	R	W	R	R	R
	Address (Hexadecimal)	2DB0	2DB8	2DC0	3FB0	2DC8	3FC0	2DD0	2DB0	2DB8	2DC0	3FB0	2DC8	3FC0	2DD0
MS ₁	Line (Hexadecimal)	3	3	4	3	4	4	5	3	3	4	3	4	4	5
	Tag (Hexadecimal)	5B	5B	5B	7F	5B	7F	5B	5B	5B	5B	7F	5B	7F	5B
	<u>H</u> it/ <u>M</u> iss (H/M)	M	H	M	M	H	M	M	H	H	M	M	H	M	H
	Allocate line? (Y/N)	Y	N	Y	N	N	Y	Y	N	N	Y	N	N	Y	N
MS ₂	Set (Hexadecimal)	2	3	0	2	1	0	2	2	3	0	2	1	0	2
	Tag (Hexadecimal)	16D	16D	16E	1FD	16E	1FE	16E	16D	16D	16E	1FD	16E	1FE	16E
	<u>H</u> it/ <u>M</u> iss (H/M)	M	M	M	M	M	M	M	M	H	H	M	H	H	M
	Write back? (Y/N)	N	N	N	N	N	N	N	Y	N	N	N	N	N	N

3. Which of the two memory systems would definitely have smaller average access time?

MS₁ and MS₂ have the same hit ratio in steady state ==> $H_1 = H_2 \approx 4/7$

MS₁ cache has smaller associativity ==> MS₁ hit time (T_{c1}) may be **less** than MS₂ hit time (T_{c2})

MS₂ cache has smaller size ==> MS₁ hit time (T_{c1}) may be **greater** than MS₂ hit time (T_{c2})

Therefore, based on the given information, it will not be possible to decide which of the two memory systems MS₁ and MS₂ would definitely have a smaller hit time!

Since the average access time of MS₁ (T_{av1}) = $T_{c1} + (1-H_1) T_M$ and the average access time of MS₂ (T_{av2}) = $T_{c2} + (1-H_2) T_M$. Then it will not be possible to say for sure which of the two memory systems MS₁ and MS₂ has a smaller average access time!!

4. Calculate the access time of the cache used in MS₁ ...

Average access time of MS₁ (T_{av1}) = 72 ns

Memory access time (T_m) = 140 ns

Cache access time (T_{c1}) is unknown

Hit ratio (H_1) = number of hits / number of accesses $\approx 4/7$

$$T_{av1} = T_{c1} + (1 - H_1) * T_m$$

$$\Rightarrow 72 = T_{c1} + (1 - 4/7) * 140$$

$$\Rightarrow T_{c1} = 12 \text{ ns}$$

5. Would it possible to use an L2 cache ... to reduce the average access time of MS₁ ...

L2 cache access time (T_{c2}) = 56 ns

Hit ratio of L2 cache (H_2) is unknown

New average access time of MS₁ (T_{av1}') = $0.5 * T_{av1} = 0.5 * 72 \text{ ns} = 36 \text{ ns}$

$$T_{av1}' = T_{c1} + (1 - H_1) * (T_{c2} + (1 - H_2) * T_m)$$

$$\Rightarrow 36 = 12 + (1 - 4/7) * (56 + (1 - H_2) * 140)$$

$$\Rightarrow H_2 = 1$$

\Rightarrow To achieve the target reduction: L2 cache must have a perfect hit ratio!!

\Rightarrow This is **theoretically possible** but **practically impossible!!!!**