CSE 321a: Computer Organization (I)
Third Year, Computer & Systems Engineering

Assignment #2

Due date: **Thursday, November 10th, 2016**

Consider two single-level cached memory systems: **MS_1** and **MS_2**. Each of which has a 1M-byte main memory that is byte-addressable. However, MS_1 has a **unified cache** (one 64K-byte cache, 16-byte lines, 2-way set-associative, LFU, write-allocate, write-back), while MS_2 has a **split cache** (two 16K-byte caches C1 and C2, 16-byte lines, direct-mapped, write-allocate, write-through).

1. Show the address format for each of the two memory systems MS_1 and MS_2.

2. Suppose the two memory systems MS_1 and MS_2 are evaluated using a simple benchmark program that contains **five 16-bit machine instructions** forming a loop that gets executed **millions of times**. The first instruction in the loop is stored in the main memory starting at location 2F6BA (hexadecimal). The third instruction is an unconditional branch to the fourth instruction which is located in memory starting at 776AE (hexadecimal). Only two of the five loop instructions make reference to data in main memory: the second instruction reads from location 4BEE4 (hexadecimal), while the fourth instruction writes to location 0F6B8 (hexadecimal). Fill up the following table according to the read and write operations that instructions make during the first **two iterations** of the loop. Assume, in both memory systems, the caches are initially empty.

	Iteration	**1st**							**2nd**	
	Instruction	**1st**	**2nd**		**3rd**	**4th**		**5th**	**1st**	**...**
	Fetch/Execute (F/E)	F	F	E	F	F	E	F	F	...
	Read/Write (R/W)	R	R	R	...	...	...	...	R	…
	Address (Hexadecimal)	2F6BA	2F6BC	...	...	...	...	...	2F6BA	...
MS_1	**Set (Hexadecimal)**	...	...	...	...	...	...	...	...	...
	Tag (Hexadecimal)	...	...	...	...	...	...	...	...	...
	Hit/Miss (H/M)	...	...	...	...	...	...	...	...	...
	Write back? (Y/N)	...	...	...	...	...	...	...	...	...
MS_2	**Line (Hexadecimal)**	...	...	...	...	...	...	...	...	...
	Tag (Hexadecimal)	...	...	...	...	...	...	...	...	...
	C1/C2 (1/2)	...	...	...	...	...	...	...	...	...
	Hit/Miss (H/M)	...	...	...	...	...	...	...	...	...

3. Estimate the **overall hit ratio** that each of the two memory systems MS1 and MS2 achieves in this benchmarking experiment? *Hint: Ignore the first iteration of the loop in your calculations.*

4. Suppose the main memories used in MS1 and MS2 have the same performance. Show that the two memory systems will almost have the same **average access time** (according to this benchmarking

experiment) if:

- The cache in MS1 is **seven** times faster than the main memory.
- The instruction cache in MS2 is **ten** times faster than main memory.
- The data cache in MS2 is **four** times faster than main memory.

5. Specify which of the two memory systems would benefit from a **change in its write policy**. Justify your answer quantitatively based on this benchmarking experiment.