CSE 321a: Computer Organization (I)
Third Year, Computer & Systems Engineering

Solution to Assignment #2

Consider two single-level cached memory systems: MS_1 and MS_2. Each of which …

1. **Show the address format for each of the two memory systems MS_1 and MS_2.**

$s + w = log_2$ 1M = 20
$w = log_2$ 16 = 4
For MS_1:
$d = log_2$ (64K/(16*2)) = 11

Format:

Tag ($s - d$) [5 bits]	Set (d) [11 bits]	Word (w) [4 bits]

For MS_2:
$r = log_2$ (16K/16) = 10

Format:

Tag ($s - r$) [6 bits]	Line (r) [10 bits]	Word (w) [4 bits]

2. **Fill up the following table according to the read and write operations that instructions make during the first two iterations of the loop.**

	Iteration	**1st**							**2nd**						
	Instruction	**1st**	**2nd**		**3rd**	**4th**		**5th**	**1st**	**2nd**		**3rd**	**4th**		**5th**
	Fetch/Execute (F/E)	F	F	E	F	F	E	F	F	F	E	F	F	E	F
	Read/Write (R/W)	R	R	R	R	R	W	R	R	R	R	R	R	W	R
	Address (Hexadecimal)	2F6BA	2F6BC	4BEE4	2F6BE	776AE	0F6B8	776B0	2F6BA	2F6BC	4BEE4	2F6BE	776AE	0F6B8	776B0
MS_1	**Set (Hexadecimal)**	76B	76B	3EE	76B	76A	76B	76B	76B	76B	3EE	76B	76A	76B	76B
	Tag (Hexadecimal)	5	5	9	5	E	1	E	5	5	9	5	E	1	E
	Hit/Miss (H/M)	M	H	M	H	M	M	M	H	H	H	H	H	M	M
	Write back? (Y/N)	N	N	N	N	N	N	Y	N	N	N	N	N	N	Y
MS_2	**Line (Hexadecimal)**	36B	36B	3EE	36B	36A	36B	36B	36B	36B	3EE	36B	36A	36B	36B
	Tag (Hexadecimal)	B	B	12	B	1D	3	1D	B	B	12	B	1D	3	1D
	C1/C2 (1/2)	1	1	2	1	1	2	1	1	1	2	1	1	2	1
	Hit/Miss (H/M)	M	H	M	H	M	M	M	M	H	H	H	H	H	M

3. Estimate the **overall hit ratio** that each of the two memory systems MS1 and MS2 achieves in this benchmarking experiment? *Hint: Ignore the first iteration of the loop in your calculations.*

- For MS_1:
  - The cache access pattern stabilizes from the second iteration on.
  - Overall hit ratio (H_1) ≈ hit ratio during second iteration = 5/7
- For MS_2:
  - The cache access pattern stabilizes from the second iteration on.
  - Overall hit ratio (H_2) ≈ hit ratio during second iteration = 5/7

4. Suppose the main memories used in MS1 and MS2 have the same performance. Show that the two memory systems will almost have the same **average access time** (according to this benchmarking experiment) if:
   - The cache in MS1 is **seven** times faster than the main memory.
   - The instruction cache in MS2 is **ten** times faster than main memory.
   - The data cache in MS2 is **four** times faster than main memory.

   Suppose TM = 140*x*
   - For MS_1:
     - $T_C = T_M/7 = 20x$
     - Average access time (T_{av1}) = $T_C + (1 - H_1) * T_M = 20x + (1 - 5/7) * 140x = 60x$
   - For MS_2:
     - $T_{C1} = T_M/10 = 14x$ and $T_{C2} = T_M/4 = 35x$
     - Here we can't use the formula for average access time because the cache is split!!
     - The cache access pattern stabilizes from the second iteration on.
     - Average access time (T_{av1}) ≈ average access time during second iteration
       $= (3*T_{C1} + 2*T_{C2} + 2*(T_{C1}+T_M)) / 7 = (42x + 70x + 308x) / 7 = 60x$

   Conclusion: average access time of MS_1 (T_{av1}) ≈ average access time of MS_2 (T_{av2})

5. Specify which of the two memory systems would benefit from a **change in its write policy**. Justify your answer quantitatively based on this benchmarking experiment.

   - For MS_1:
     - Switching to no-write-allocate ==> hit ratio changes from ~5/7 to ~6/7 (since from second loop iteration on, the "read from 776B0" will become a cache hit!) ==> **BETTER!!**
     - Switching to write-through ==> hit ratio does not change, and total number of writes to main memory does not change as well ==> **SAME!!**
   - For MS_2:
     - Switching to no-write-allocate ==> hit ratio changes from ~5/7 to ~4/7 (since the "write to 776B0" will be always a cache miss!). ==> **WORSE!!**
     - Switching to write-back ==> hit ratio does not change but total number of memory writes will be reduced to just one (just the final write)! ==> **BETTER!!**

   Conclusion: **MS_1** will benefit by switching its write-miss policy to **no-write-allocate**, and **MS_2** will benefit by switching its write-hit policy to **write-back**.