Zagazig University	CSE 321a	Midterm Examination
Faculty of Engineering	**Computer Organization (I)**	November 19th, 2017
Computer & Systems Engineering	**(Single-Sided)**	12:30pm - 1:45pm
3rd Year - 1st Term - 2017/2018	**(Duration: 75 minutes)**	4 pages, 25 questions, 25 points

Use the attached bubble sheet to answer the following questions. Fill in the bubble of the choice that best answers the corresponding question. No more than one bubble should be filled in per question.

1. What could happen when a new feature is added to the architecture of a processor family?
    (a) New processors cannot execute old machine programs
    (b) Old processors cannot execute new machine programs
    (c) New processors execute old machine programs faster
    (d) Old processors execute new machine programs faster
    (e) None of the above

2. Which functional facilities must be involved in almost every task that the computer performs?
    (a) Data movement
    (b) Data processing
    (c) Control mechanism
    (d) Data storage
    (e) None of the above

3. Which of the following combinations of terms best describes a bus that serves a subset of system devices, and uses separate lines to transfer data, address, control and clock signals?
    (a) Synchronous, physically-dedicated, functionally-dedicated
    (b) Synchronous, physically-dedicated, multiplexed
    (c) Synchronous, functionally-dedicated, multiplexed
    (d) Asynchronous, physically-dedicated, functionally-dedicated
    (e) None of the above

4. In a high performance hierarchical bus architecture, which bus is likely the fastest?
    (a) Expansion bus
    (b) System bus
    (c) High-speed bus
    (d) Local bus
    (e) None of the above

5. Which of the following statements about the addressable unit in internal memory is true?
    (a) It is defined to be the smallest location that can be uniquely addressed
    (b) Its size must be big enough to hold a complete instruction
    (c) Its size must be small enough for its contents to be transferred on the bus at once
    (d) All the above
    (e) None of the above

6. Which access method is used in floppy-disk drives?
    (a) Sequential   (b) Direct   (c) Random   (d) Associative   (e) None of the above

7. Which of the following performance metrics must be greater than or equal to the recovery time?
    (a) Access time   (b) Cycle time   (c) Transfer time   (d) All the above   (e) None of the above

8. Which of the following statements about physical and virtual caches is true?
    (a) Physical cache sets between CPU and MMU

(b) Virtual cache sets between MMU and main memory
(c) Physical cache must be flushed on every context switch
(d) Virtual cache access is slower than physical cache access
(e) None of the above

Questions 9 – 11 are based on the following information:

A loop in a program performs three tasks: (1) processes some data collected in real-time, (2) sends the processed data to a printer and initiates a printing job, and (3) adds a record to a log file after printing is complete. Suppose the three tasks take x, y, and z seconds, respectively. Suppose further that the printer takes on average w seconds to finish a job, and no new data can be transferred to the printer buffers before finishing the current job. Consider the following three loop implementation options:

◆ **Option #1**: Tasks are performed in order using function calls from the loop (i.e., no interrupts).
◆ **Option #2**: Third task is implemented as an interrupt service routine that gets triggered by the printer once the current job is complete, and is completely executed before starting the next job.
◆ **Option #3**: Third task is implemented as an interrupt service routine that gets triggered by the printer once the current job is complete, and can be executed while printing the next job.

9. How long does each loop iteration take on average in **option #1**?
    (a) $x+y+z$
    (b) $max(x+y+z,w)$
    (c) $w+x+z$
    (d) $w+x+y$
    (e) None of the above

10. How long does each loop iteration take on average in **option #2**?
    (a) $max(x+y+z,w)$
    (b) $x+max(y+z,w)$
    (c) $y+z+max(x,w)$
    (d) $y+max(x+z,w)$
    (e) None of the above

11. How long does each loop iteration take on average in **option #3**?
    (a) $max(x+y+z,w)$
    (b) $x+max(y+z,w)$
    (c) $y+z+max(x,w)$
    (d) $y+max(x+z,w)$
    (e) None of the above

Questions 12 – 15 are based on the following information:

A processor supports two classes of instructions: class-A and class-B. Any program can be completely written using instructions that belong to class-A alone, class-B alone, or both. All instructions in class-A have the same CPI value which is 5, while all instructions in class-B have the same CPI value which is 4. The processor adapts its clock speed according to the class of instructions that it executes. If the program only contains class-A instructions, the processor runs on a minimum clock speed of 100 MHz. The clock speed increases (linearly) by increasing the percentage of class-B instructions in the program. The processor runs on a maximum clock speed of 176 MHz if the program only contains class-B instructions. Suppose a certain program contains 1000 instructions; all of which are class-A. Consider an optimized version of that program in which x class-A instructions are replaced with $2x$ class-B instructions.

12. How many instructions does the optimized program contain?
    (a) $1000+x/2$ (b) $1000-x$ (c) $1000+x$ (d) $1000+2x$ (e) None of the above

13. What is the total number of cycles needed to execute the optimized program?

(a) $5000+11x$ (b) $5000+3x$ (c) $2000+2x$ (d) $4000+x$ (e) None of the above

14. How fast (in MHz) does the processor run when it executes the optimized program?
    (a) $100+76x$
    (b) $100+152x/(1000+x)$
    (c) $100+76x/(1000-x)$
    (d) $100+76(1000-x)/(1000+x)$
    (e) None of the above

15. What will be the speedup when the optimized program no longer contain any class-A instructions?
    (a) 1.1   (b) 1.25   (c) 1.76   (d) 2   (e) None of the above

Questions 16 – 20 are based on the following information:

Consider a small computer in which memory locations, general-purpose registers, and machine instructions are all 20-bit long. The processor has only four general-purpose registers (numbered 0, 1, 2, and 3). The six most-significant bits of each machine instruction ($X_{19\text{-}14}$) represent an opcode. The remaining bits ($X_{13\text{-}0}$) specify three operands:
 ◆ First operand (specified by $X_{13\text{-}5}$): if X_{13} is 1, the operand value is $X_{12\text{-}5}$, otherwise, the operand value is in the memory location whose address is $X_{12\text{-}5}$.
 ◆ Second operand (specified by $X_{4\text{-}3}$): the operand value is in register $X_{4\text{-}3}$.
 ◆ Third operand (specified by $X_{2\text{-}0}$): if X_2 is 1, the operand value is in register $X_{1\text{-}0}$, otherwise, the operand value is in the memory location whose address is in register $X_{1\text{-}0}$.
Operand values are interpreted as signed integers according to the 2's complement representation. The following table contains some of the supported opcodes:

Mnemonic	Binary	Meaning
SWITCH	000111	Exchange the values of the four registers with the values of the four successive memory locations whose starting address is the value of the first operand.
NEG	001101	Negate the values of the three operands.
ADD	011011	Add the (signed) value of the first operand to the (signed) value of the second operand and save the result to the third operand.
BRGT	101100	If the (signed) value of the second operand is greater than the (signed) value of the third operand, branch to the instruction whose address is obtained by adding the (signed) value of the first operand to the PC, else continue normally.

Suppose the values of the registers and memory locations in the **initial state** are:

PC	MDR	Register 1	Register 2	Location 0006B	Location 0006C
C0FFE	0BEEF	FFFF7	FFFF1	81E7D	FFFF2

16. What is the maximum range of signed values that can be taken by the first operand?
    (a) $-2^{19} \rightarrow 2^{19}\text{-}1$
    (b) $-2^{19}+1 \rightarrow 2^{19}$
    (c) $-2^{20} \rightarrow 2^{20}\text{-}1$
    (d) $-2^{20}+1 \rightarrow 2^{20}\text{-}1$
    (e) None of the above

17. How many memory accesses are needed to fetch and execute instruction 1DD9F?
    (a) 3   (b) 8   (c) 9   (d) 10   (e) None of the above

18. What will be the value of MDR after executing instruction 34D6E from initial state?
    (a) 34D6E   (b) 81E7D   (c) 7E183   (d) C0FFF   (e) None of the above

19. What will be the value of register 2 after executing instruction 6E12E from initial state?
    (a) FFFFB   (b) FFFFF   (c) FFFEE   (d) 00000   (e) None of the above

20. Which of the following instructions will load PC with C0FF0 after being executed from initial state?
    (a) B0D95   (b) B4D8E   (c) B0D96   (d) B0D8E   (e) None of the above

Questions 21 – 25 are based on the following information:

Two single-level cached memory systems, MS_1 and MS_2, have 64 KB main memories that are byte-addressable. MS_1 has a k-way set-associative cache, while MS_2 has a direct-mapped cache. The following table reveals some partial information about the first eight memory references (*i.e.*, read/write operations) made during the execution of a program (assuming the caches were initially empty) in each of the two memory systems:

	Address (decimal)	43439							
	Read/**W**rite? (R/W)	W	R	W	W	R	R	R	R
	Word	x							
MS_1	Set	y	$y+6$	$y+6$	$y+6$	$y+6$	y	$y+6$	$y+6$
	Tag	z	$z+2$	$z+1$	$z+2$	$z+5$	z	$z+1$	$z+5$
	Hit/**M**iss? (H/M)	M	M	M	H	M	M	M	M
	Write to MM? (Y/N)	Y	N	Y	Y	N	N	N	N
MS_2	Word	x-4							
	Line	$2y+1$							
	Tag	$4z$							

21. What is the format of the memory address used in MS_1?
    (a) Tag → 6 bits, Set → 7 bits, Word → 3 bits
    (b) Tag → 7 bits, Set → 7 bits, Word → 2 bits
    (c) Tag → 5 bits, Set → 8 bits, Word → 3 bits
    (d) Tag → 5 bits, Set → 7 bits, Word → 4 bits
    (e) None of the above

22. Which write policy is used in MS_1 cache?
    (a) No-write-allocate, write-through
    (b) Write-allocate, write-through
    (c) No-write-allocate, write-back
    (d) Write-allocate, write-back
    (e) None of the above

23. Which replacement algorithm is used in MS_1 cache?
    (a) LRU   (b) FIFO   (c) LFU   (d) All the above   (e) None of the above

24. What is the value of k (for MS_1 cache)?
    (a) 1   (b) 2   (c) 3   (d) 4   (e) None of the above

25. What is the size of MS_1 cache?
    (a) 2 KB   (b) 4 KB   (c) 6 KB   (d) 16 KB   (e) None of the above

** End of Exam **