CSE 321a: Computer Organization (I)
Third Year, Computer & Systems Engineering

Solution to Assignment #2

Two otherwise identical memory systems, MS_1 and MS_2, have slightly different cache …

1. **Show the address format for each of the two memory systems MS_1 and MS_2.**

$s + w = log_2 16K = 14$
For **MS_1**:
$w = log_2 (128/8) = 4$
$r = log_2 8 = 3$

Format:

Tag ($s - r$) [7 bits]	Line (r) [3 bits]	Word (w) [4 bits]

For **MS_2**:
$w = log_2 (64/8) = 3$
$d = log_2 (8/2) = 2$

Format:

Tag ($s - d$) [9 bits]	Set (d) [2 bits]	Word (w) [3 bits]

2. **Fill up the following table according to the read and write operations ...**

	Iteration	**1st**							**2nd**						
	Instruction	**1st**	**2nd**	**3rd**		**4th**		**5th**	**1st**	**2nd**	**3rd**		**4th**		**5th**
	Fetch/Execute (F/E)	F	F	F	E	F	E	F	F	F	F	E	F	E	F
	Read/Write (R/W)	R	R	R	W	R	R	R	R	R	R	W	R	R	R
	Address (Hexadecimal)	2DB0	2DB8	2DC0	3FB0	2DC8	3FC0	2DD0	2DB0	2DB8	2DC0	3FB0	2DC8	3FC0	2DD0
MS_1	**Line (Hexadecimal)**	3	3	4	3	4	4	5	3	3	4	3	4	4	5
	Tag (Hexadecimal)	5B	5B	5B	7F	5B	7F	5B	5B	5B	5B	7F	5B	7F	5B
	Hit/Miss (H/M)	M	H	M	M	H	M	M	H	H	M	M	H	M	H
	Allocate line? (Y/N)	Y	N	Y	N	N	Y	Y	N	N	Y	N	N	Y	N
MS_2	**Set (Hexadecimal)**	2	3	0	2	1	0	2	2	3	0	2	1	0	2
	Tag (Hexadecimal)	16D	16D	16E	1FD	16E	1FE	16E	16D	16D	16E	1FD	16E	1FE	16E
	Hit/Miss (H/M)	M	M	M	M	M	M	M	M	H	H	M	H	H	M
	Write back? (Y/N)	N	N	N	N	N	N	N	Y	N	N	N	N	N	N

3. **Which of the two memory systems would definitely have smaller average access time?**

MS_1 and MS_2 have the same hit ratio in steady state ==> $H_1 = H_2 \approx 4/7$
MS_1 cache has smaller associativity ==> MS_1 hit time (T_{c1}) may be **less** than MS_2 hit time (T_{c2})
MS_2 cache has smaller size ==> MS_1 hit time (T_{c1}) may be **greater** than MS_2 hit time (T_{c2})
Therefore, based on the given information, it will not be possible to decide which of the two memory systems MS_1 and MS_2 would definitely have a smaller hit time!
Since the average access time of MS_1 (T_{av1}) = $T_{c1} + (1-H_1)\, T_M$ and the average access time of MS_2 (T_{av2}) = $T_{c2} + (1-H_2)\, T_M$. Then it will not be possible to say for sure which of the two memory systems MS_1 and MS_2 has a smaller average access time!!

4. Calculate the access time of the cache used in MS_1 …

Average access time of MS_1 (T_{av1}) = 72 ns
Memory access time (T_m) = 140 ns
Cache access time (T_{c1}) is unknown
Hit ratio (H_1) = number of hits / number of accesses ≈ 4/7
$T_{av1} = T_{c1} + (1 – H_1) * T_m$
⇨ $72 = T_{c1} + (1 – 4/7) * 140$
⇨ $T_{c1} = 12$ ns

5. Would it possible to use an L2 cache … to reduce the average access time of MS_1 …

L2 cache access time (T_{c2}) = 56 ns
Hit ratio of L2 cache (H_2) is unknown
New average access time of MS_1 (T_{av1}') = 0.5 * T_{av1} = 0.5 * 72 ns = 36 ns
$T_{av1}' = T_{c1} + (1 – H_1) * (T_{c2} + (1 – H_2) * T_m)$
⇨ $36 = 12 + (1 – 4/7) * (56 + (1 – H_2) * 140)$
⇨ $H_2 = 1$
⇨ To achieve the target reduction: L2 cache must have a perfect hit ratio!!
⇨ This is **theoretically possible** but **practically impossible**!!!!