Tutorial #2

CSE 321a: Computer Organization (I)

Third Year, Computer and Systems Engineering

External Problem

A hypothetical computer has the following characteristics. The processor contains a sing-le general-purpose register, called an accumulator (AC), a Program Counter (PC), a Memory Address Register (MAR), and a Memory Buffer Register (MBR). Both instructions and data are 16 bits long. Hence, memory words are 16 bits long. The instruction format provides 4 bits for the opcode and 12 bits for the memory address. The left table below contains a partial list of the opcodes and their corresponding operations. Assume the memory contains the contents shown in the right table below, where values are in hexadecimal.

Opcode (binary)	Operation
0000	Load AC from memory
0001	Store AC into memory
0010	Add to AC from memory, result in AC
0011	Subtract memory from AC, result in AC
0100	Multiply AC times memory, result in AC
0101	Divide AC by memory, result in AC
0110	Logical AND memory and AC, result in AC
0111	Logical OR memory and AC, result in AC

Address	Contents
ABD	0E2E
ABE	3E2F
ABF	4E30
AC0	2E31
AC1	1E31

1. What is the maximum memory address space this processor can access?

2. In the following table, fill in the contents of every register and memory location after the fetch cycle and after the execute cycle of every instruction. Values are in hexadecimal.

Instruction	Cycle	PC	MAR	MBR	AC	Location: E2E	Location: E2F	Location: E30	Location: E31
Initially	---	0ABD	ABCD	F43A	50C8	0009	0007	0005	0003
0E2E	Fetch								
	Execute								
3E2F	Fetch								
	Execute								
4E30	Fetch								
	Execute								
2E31	Fetch								
	Execute								
1E31	Fetch								
	Execute								

3. Assume an interrupt occurs during the execution of the instruction at location ABF. Describe the sequence of events that would take place to handle this interrupt.

4. How many memory accesses (references) are needed to run the given 5-instruction program?

(Answers don't contains the steps of work in solution)

Solution

1. **Maximum accessible address space = 2^{12} = 4 k locations**

2.

Instruction	Cycle	PC	MAR	MBR	AC	Location: E2E	Location: E2F	Location: E30	Location: E31
Initially	---	0ABD	ABCD	F43A	50C8	0009	0007	0005	0003
0E2E	Fetch	**0ABE**	**0ABD**	**0E2E**	**50C8**	**0009**	**0007**	**0005**	**0003**
	Execute	**0ABE**	**0E2E**	**0009**	**0009**	**0009**	**0007**	**0005**	**0003**
3E2F	Fetch	**0ABF**	**0ABE**	**3E2F**	**0009**	**0009**	**0007**	**0005**	**0003**
	Execute	**0ABF**	**0E2F**	**0007**	**0002**	**0009**	**0007**	**0005**	**0003**
4E30	Fetch	**0AC0**	**0ABF**	**4E30**	**0002**	**0009**	**0007**	**0005**	**0003**
	Execute	**0AC0**	**0E30**	**0005**	**000A**	**0009**	**0007**	**0005**	**0003**
2E31	Fetch	**0AC1**	**0AC0**	**2E31**	**000A**	**0009**	**0007**	**0005**	**0003**
	Execute	**0AC1**	**0E31**	**0003**	**000D**	**0009**	**0007**	**0005**	**0003**
1E31	Fetch	**0AC2**	**0AC1**	**1E31**	**000D**	**0009**	**0007**	**0005**	**0003**
	Execute	**0AC2**	**0E31**	**000D**	**000D**	**0009**	**0007**	**0005**	**000D**

3. Sequence will be:

1. **After the instruction at location ABF finishes execution, CPU checks interrupts.**
2. **CPU saves current contents of PC, which are AC0, and other relevant data.**
3. **CPU loads PC with the address of the first instruction of the interrupt service routine (ISR).**
4. **ISR executes.**
5. **CPU restores PC (AC0) and relevant data.**

4. **Every instruction needs one memory access to fetch and one memory access to fetch or store the operand ➔ Total number of memory accesses = 2 + 2 + 2 + 2 + 2 = 10 memory access.**

CSE 321a – Midterm Exam– Fall 2014

Consider a small hypothetical computer with four 16-bit general-purpose registers numbered from 0 to 3. Each machine contains 16 bits (X15-0). The six most-significant bits of the instruction (X15-10) represent an op-code. The following two bits (X9-8) represent a register number. The remaining bits (X7-0) may represent the value or the address of an operand. The following table contains some of the supported op-codes:

Mnemonic	Binary Meaning
LOAD 011100	Load register X9-8 from memory location X7-0.
STORE 011101	Store value of register X9-8 to memory location X7-0.
ADDLD 110001	Add value of memory location X7-0 to register X9-8.
ADDST 110011	Add value of register X9-8 to memory location X7-0.
DECBRNZ 111010	Decrement value of register X9-8 by 1, and if new value of register X9-8 is not 0, branch to instruction whose address is X7-0, else continue normally.

22. How many memory accesses are needed to fetch and execute instruction EA9B?
(a) 0
(b) 1
(c) 2
(d) 3
(e) None of the above

23. Suppose the values of register 2 and location 3A are: 2D15 and 11B5 respectively. What would be their values after executing instruction 763A?
(a) 2D15 and 11B5
(b) 2D15 and 2D15
(c) 11B5 and 11B5
(d) 11B5 and 2D15
(e) None of the above

24. Suppose the values of register 1 and location 75 are: 623E and 2935 respectively. What would be their values after executing instruction C575?
(a) 623E and 9174
(b) 623E and 2935
(c) 9174 and 2935
(d) 8B74 and 623E
(e) None of the above

25. Suppose the values of register 3 and program counter (PC) are: 0001 and 005B respectively. Which of the following instructions will load the PC with 008F after being executed?
(a) EB8F
(b) 738F
(c) EAF8
(d) C78F
(e) None of the above