Tutorial #3

CSE 321a: Computer Organization (I)
Third Year, Computer and Systems Engineering

External Problem

A hypothetical computer has the following characteristics. The processor contains a sing-le general-purpose register, called an accumulator (AC), a Program Counter (PC), a Memory Address Register (MAR), and a Memory Buffer Register (MBR). Both instructions and data are 16 bits long. Hence, memory words are 16 bits long. The instruction format provides 4 bits for the opcode and 12 bits for the memory address. The left table below contains a partial list of the opcodes and their corresponding operations. Assume the memory contains the contents shown in the right table below, where values are in hexadecimal.

Opcode (binary)	Operation
0000	Load AC from memory
0001	Store AC into memory
0010	Add to AC from memory, result in AC
0011	Subtract memory from AC, result in AC
0100	Multiply AC times memory, result in AC
0101	Divide AC by memory, result in AC
0110	Logical AND memory and AC, result in AC
0111	Logical OR memory and AC, result in AC

Address	Contents
ABD	0E2E
ABE	3E2F
ABF	4E30
AC0	2E31
AC1	1E31

1. What is the maximum memory address space this processor can access?

2. In the following table, fill in the contents of every register and memory location after the fetch cycle and after the execute cycle of every instruction. Values are in hexadecimal.

Instruction	Cycle	PC	MAR	MBR	AC	Location: E2E	Location: E2F	Location: E30	Location: E31
Initially	---	0ABD	ABCD	F43A	50C8	0009	0007	0005	0003
0E2E	Fetch								
	Execute								
3E2F	Fetch								
	Execute								
4E30	Fetch								
	Execute								
2E31	Fetch								
	Execute								
1E31	Fetch								
	Execute								

3. Assume an interrupt occurs during the execution of the instruction at location ABF. Describe the sequence of events that would take place to handle this interrupt.

4. How many memory accesses (references) are needed to run the given 5-instruction program?

(Answers don't contains the steps of work in solution)

Solution

1. **Maximum accessible address space = 2^{12} = 4 k locations**

2.

Instruction	Cycle	PC	MAR	MBR	AC	Location: E2E	Location: E2F	Location: E30	Location: E31
Initially	---	0ABD	ABCD	F43A	50C8	0009	0007	0005	0003
0E2E	Fetch	**0ABE**	**0ABD**	**0E2E**	**50C8**	**0009**	**0007**	**0005**	**0003**
	Execute	**0ABE**	**0E2E**	**0009**	**0009**	**0009**	**0007**	**0005**	**0003**
3E2F	Fetch	**0ABF**	**0ABE**	**3E2F**	**0009**	**0009**	**0007**	**0005**	**0003**
	Execute	**0ABF**	**0E2F**	**0007**	**0002**	**0009**	**0007**	**0005**	**0003**
4E30	Fetch	**0AC0**	**0ABF**	**4E30**	**0002**	**0009**	**0007**	**0005**	**0003**
	Execute	**0AC0**	**0E30**	**0005**	**000A**	**0009**	**0007**	**0005**	**0003**
2E31	Fetch	**0AC1**	**0AC0**	**2E31**	**000A**	**0009**	**0007**	**0005**	**0003**
	Execute	**0AC1**	**0E31**	**0003**	**000D**	**0009**	**0007**	**0005**	**0003**
1E31	Fetch	**0AC2**	**0AC1**	**1E31**	**000D**	**0009**	**0007**	**0005**	**0003**
	Execute	**0AC2**	**0E31**	**000D**	**000D**	**0009**	**0007**	**0005**	**000D**

3. Sequence will be:

1. **After the instruction at location ABF finishes execution, CPU checks interrupts.**
2. **CPU saves current contents of PC, which are AC0, and other relevant data.**
3. **CPU loads PC with the address of the first instruction of the interrupt service routine (ISR).**
4. **ISR executes.**
5. **CPU restores PC (AC0) and relevant data.**

4. **Every instruction needs one memory access to fetch and one memory access to fetch or store the operand ➔ Total number of memory accesses = 2 + 2 + 2 + 2 + 2 = 10 memory access.**

Problem 3.14

A microprocessor has an increment memory direct instruction, which adds 1 to the value in a memory location. The instruction has five stages: fetch opcode (four bus clock cycles), fetch operand address (three cycles), fetch operand (three cycles), add 1 to operand (three cycles), and store operand (three cycles).
a. By what amount (in percent) will the duration of the instruction increase if we have to insert two bus wait states in each memory read and memory write operation?
b. Repeat assuming that the increment operation takes 13 cycles instead of 3 cycles.

a. Without the wait states, the instruction takes 16 bus clock cycles. The instruction requires four memory accesses, resulting in 8 wait states. The instruction, with wait states, takes 24 clock cycles, for an increase of 50%.
b. In this case, the instruction takes 26 bus cycles without wait states and 34 bus cycles with wait states, for an increase of 33%.

Problem 3.18 (Extension of problem 3.14)

The microprocessor of Problem 3.14 initiates the fetch operand stage of the increment memory direct instruction at the same time that a keyboard actives an interrupt request line. After how long does the processor enter the interrupt processing cycle? Assume a bus clocking rate of 10 MHz.

The processor needs another nine clock cycles to complete the instruction. Thus, the Interrupt Acknowledge will start after 900 ns.