Tutorial #5

CSE 321a: Computer Organization (I)
Third Year, Computer and Systems Engineering

Questions (16 – 20) Midterm 2015:

A computer has a 16 MB main memory (that is byte-addressable) and a 4-way set-associative cache. The following table describes the first nine memory references (*i.e.*, read/write operations) made during the execution of a program (assuming the cache was initially empty):

Address (decimal)	738117								
Read/**W**rite (R/W)	R	R	W	W	R	R	R	R	R
Set (decimal)	52	52	63	52	52	52	63	52	52
Tag (decimal)	90	40	90	40	70	20	90	10	...
Hit/**M**iss (H/M)	M	M	M	H	M	M	M	M	H
Write-back? (Y/N)	N	N	N	N	N	N	N	Y	

16. What is the format of the memory address?
(a) Tag → 7 bits, Set → 13 bits, Word → 4 bits
(b) Tag → 14 bits, Set → 6 bits, Word → 4 bits
(c) Tag → 7 bits, Set → 6 bits, Word → 3 bits
(d) Tag → 11 bits, Set → 9 bits, Word → 4 bits
(e) None of the above

17. What is the size of the cache?
(a) 2 KB
(b) 32 KB
(c) 8 KB
(d) 512 B
(e) None of the above

18. Which replacement algorithm is used?
(a) LRU
(b) LFU
(c) FIFO
(d) Random
(e) None of the above

19. Which write-miss policy is used?
(a) No-write-allocate
(b) Write-allocate
(c) Write-through
(d) Write-back
(e) None of the above

20. Which of the following **cannot** be the tag associated with the last read operation in the table?
(a) 90
(b) 70
(c) 20
(d) 10
(e) None of the above

External problem

Consider a computer with a 1-kB byte-addressable main memory and a 32-byte write-back initially-empty cache memory with 4-byte blocks. Assume that the following sequence of memory references to the given addresses (in decimal) has occurred in order:

40 (write), 20 (read), 43 (read), and 8 (read).

1. If direct mapping is used, how many bits are needed for the tag, line, and word fields, respectively?

# of word field bits = lg(4) = 2 bits

# of lines in cache = Cache size/ line size = 32 / 4 = 8

# of line field bits = lg(8) = 3 bits

# of address bits = lg(1024) = 10 bits

# of Tag field bits = 10 – (2+3) = 5 bits

2. Assume that the main memory access time is 10τ seconds, the cache memory access time is τ seconds, and direct mapping is used. What is the total time (in seconds) needed to perform the given sequence of read/write operations?

Address	**40**	**20**	**43**	**8**	**26**
R/W	**W**	**R**	**R**	**R**	**R**
Line	2	5	2	2	6
Tag	1	0	1	0	0
Hit/Miss	M	M	H	M	M
Write back?	No	No	No	Yes	No

Cache hit time = τ , Cache miss time = (10τ + τ) , Write back time = 10τ

Total time = (10τ + τ) + (10τ + τ) + τ + (10τ + 10τ + τ) = 44τ sec

3. Assume direct mapping, and that the byte at location 26 (decimal) is read right after the given sequence of read/write operations. Will a cache hit occur? Will a write back be needed?

   As showing in table above there is no cache hit occur and also, it isn't needed to write back.

4. If 4-way set-associative mapping is used, how many bits are needed for the tag, set, and word fields, respectively?

   # of word field = 2 bits

   # of sets = # of lines in cache/ 4 = 8 /4 = 2 sets

   # of sets bits = lg(2) = 1 bits

   # of tag bits = 10 – (2+1) = 7 bits

Address	**40**	**20**	**43**	**8**	**26**
R/W	**W**	**R**	**R**	**R**	**R**
Set	0	1	0	0	0
Tag	5	2	5	1	3
Hit/Miss	M	M	H	M	M
Write back?	No	No	No	No	No

5. Assume 4-way set-associative mapping, with FIFO replacement, and that the byte at location 26 (decimal) is read right after the given sequence of read/write operations. Will a cache hit occur? Will a write back be needed?

   From the table above, answer is no hit and no write back.