Tutorial #2

Questions:

5.9 What is a parity bit?

A bit appended to an array of binary digits to make the sum of all the binary digits, including the parity bit, always odd (odd parity) or always even (even parity).

Problems:

5.13 How many check bits are needed if the Hamming error correction code is used to detect single bit errors in a 1024-bit data word?

Need K check bits such that $2K - 1 \geq 1024 + K$.

The minimum value of K that satisfies this condition is 11.

External problem

Suppose an 8-bit data word stored in memory is 11011100.

i. Determine no. of check bits

ii. Using the Hamming algorithm, determine what check bits would be stored in memory with the data word. Show how you got your answer.

iii. Suppose error occur in data bit D3 where data word read from memory is 11011000. Show how hamming algorithm can be used to detect and correct error.

i. Need K check bits such that $2K - 1 \geq 1024 + K$.

Using try and error the minimum value of K that satisfies this condition is 4.

ii. Code word will organized as shown

Position	12	11	10	9	8	7	6	5	4	3	2	1
Bits	D8	D7	D6	D5	**C8**	D4	D3	D2	**C4**	D1	**C2**	**C1**
Data	1	1	0	1		1	1	0		0		

C1 = 0 $\oplus$ 1 $\oplus$ 1 $\oplus$ 1 $\oplus$ 0 = 1

C2 = 1 $\oplus$ 0 $\oplus$ 1 $\oplus$ 1 $\oplus$ 0 = 1

C4 = 1 $\oplus$ 1 $\oplus$ 1 $\oplus$ 0 = 1

C8 = 1 $\oplus$ 1 $\oplus$ 0 $\oplus$ 1 = 1

So, hamming word will be: 110111101011

iii. When data word read from memory is 11011000, new check bits will be calculated to be

Position	12	11	10	9	8	7	6	5	4	3	2	1
Bits	D8	D7	D6	D5	**C8**	D4	D3	D2	**C4**	D1	**C2**	**C1**
Hamming word	1	1	0	1	**1**	1	0	0	**0**	0	**0**	**1**

Doing an XOR of 1001 and 1111 yields 0110 ➔ error in bit position 6 (six) of the Hamming word. Thus, the correct data word was 11011100

Q2-2 Final W2014

An SDRAM module (DIMM) is made out of eight 64M x 8 SDRAM chips that receive the same address and command. Each chip contributes 8 bits to the overall data word handled by the module. Suppose the module is connected to a bus clocked at 100MHz.

(a) Represent the size of the module in the form "*m* x *n*".
(b) What is the maximum data transfer rate of the module (measured in MB/s)?
(c) Suppose a burst read command is issued while the burst length is set to 8 and the latency is set to 2. How much time is consumed between issuing the command and finishing the data transfer?
(d) If the same command in part (c) was issued to a DDR-SDRAM module with the same cell speed and bus frequency, how long does it take to finish the transfer in this case?

a) Size of the module is 64M x 64 bits
b) Max rate is achieved by producing 64 bits every cycle at 100 MHz speed so, Max rate = 64 b/cycle * 100 M cycle/s = 6400 Mb/s = 800 MB/s
c) # of cycle taken = 2+8 = 10 cycles
So, Time taken = 10 cycles * 1/100 M cycles/s = 100 ns
d) # of cycle taken = 2+8/2 = 6 cycles
So, Time taken = 6 cycles * 1/100 M cycles/s = 60 ns