# **Tutorial #4**

#### CSE 321a: Computer Organization (I)

Third Year, Computer and Systems Engineering

# Prob. (4.2):

A two-way set-associative cache has lines of 16 bytes and a total size of 8 Kbytes. The 64-Mbyte main memory is byte addressable. Show the format of main memory addresses.

```
Word size = 1 byte (byte addressable)

Word field (W) = \lg(\# \text{ of words in block}) = \lg(16) = 4 \text{ bits}

Set field (S) = \lg(\# \text{ of sets in cache}) = \lg(\text{cache size} / \text{ set size}) = \lg(8 \text{ K/}16 * 2) = 8 \text{ bits}

Tag field (T) = address field – (s+w) = \lg(64 \text{ M}) - (4+8) = 14 \text{ bits}
```

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# Prob. (4.11):

Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size.

- a. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.
- **b.** Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.
- **c.** Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag.

```
Address size= 32 bits

Word size = 1byte (bit level)

Line size = block size = 64 bytes. \rightarrow L=6, W=6

T=A-(L+W) = 20
```

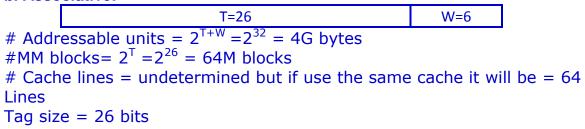
# a. Direct Mapped:

	T=2	20	L=6	W=6
 		- V - 3.3		

# Addressable units =  $2^A = 2^{32} = 4G$  bytes

```
#MM blocks= MM size / Block size = 4G/64 = 64M blocks
# Cache lines = 2^L = 2^6 = 64 Lines
Tag size = 20 bits
```

#### b. Associative:



### c. 4 way set associative:

	T=9	S=17	W=6			
K=4						
	essable units = 4G bytes					
#MM b	#MM blocks= $2^{T+S}=2^{26}=64M$ blocks					
# Lines per set = $k = 4$ lines						
# Cache sets = cache size/set size =4k/4*64 =128K sets						
# Cache lines = # cache sets * # lines per set						
= 128k * 4 = 512 K lines						
Tag size = 9 bits						

#### **External problem**

Consider a computer with a 1-kB byte-addressable main memory and a 32-byte write-back initially-empty cache memory with 4-byte blocks. Assume that the following sequence of memory references to the given addresses (in decimal) has occurred in order:

```
40 (write), 20 (read), 43 (read), and 8 (read).
```

1. If direct mapping is used, how many bits are needed for the tag, line, and word fields, respectively?

```
# of word field bits = Ig(4) = 2 bits
# of lines in cache = Cache size/ line size = 32 / 4 = 8
# of line field bits = Ig(8) = 3 bits
```

```
# of address bits = lg(1024) = 10 bits
# of Tag field bits = 10 - (2+3) = 5 bits
```

2. Assume that the main memory access time is  $10\tau$  seconds, the cache memory access time is  $\tau$  seconds, and direct mapping is used. What is the total time (in seconds) needed to perform the given sequence of read/write operations?

Address	40	20	43	8	26
R/W	W	R	R	R	R
Line	2	5	2	2	6
Tag	1	0	1	0	0
Hit/Miss	М	М	Н	M	М
Write back?	No	No	No	Yes	No

Cache hit time = 
$$\tau$$
 , Cache miss time =  $(10\tau + \tau)$  , Write back time =  $10\tau$   
Total time =  $(10\tau + \tau) + (10\tau + \tau) + \tau + (10\tau + 10\tau + \tau) = 44\tau$  sec

3. Assume direct mapping, and that the byte at location 26 (decimal) is read right after the given sequence of read/write operations. Will a cache hit occur? Will a write back be needed?

As showing in table above there is no cache hit occur and also, it isn't needed to write back.

4. If 4-way set-associative mapping is used, how many bits are needed for the tag, set, and word fields, respectively?

```
# of word field = 2 bits

# of sets = # of lines in cache/ 4 = 8 / 4 = 2 sets

# of sets bits = lg(2) = 1 bits

# of tag bits = 10 - (2+1) = 7 bits
```

Address	40	20	43	8	26
R/W	W	R	R	R	R
Set	0	1	0	0	0
Tag	5	2	5	1	3
Hit/Miss	М	М	Н	M	М
Write back?	No	No	No	No	No

5. Assume 4-way set-associative mapping, with FIFO replacement, and that the byte at location 26 (decimal) is read right after the given sequence of read/write operations. Will a cache hit occur? Will a write back be needed?

From the table above, answer is no hit and no write back.