Tutorial #9

CSE 321a: Computer Organization (I)
Third Year, Computer and Systems Engineering

Question (3) – Final exam F2014

Write in your answer sheet the sequence of micro-operations (and show the steps) required for a CPU (with a single internal bus, 2 general purpose registers R0 and R1, and a stack pointer SP) to perform the following:

(a) Fetch cycle
t1: MAR ← [PC], Z ← [PC] + 1
t2: MBR ← Memory, PC ← [Z]
t3: IR ← [MBR]

(b) ADD R0,(100)(R1)
t1: MAR ← [IR-address]
t2: MBR ← Memory, Y ← [R1]
t3: Z ← [Y] + [MBR]
t4: MAR ← [Z]
t5: MBR ← Memory, Y ← [R0]
t6: Z ← [Y] + [MBR]
t7: R0 ← [Z]

(c) NOT (100(R1))
t1: Y ← [IR-address]
t2: Z ← [Y] + [R1]
t3: MAR ← [Z]
t4: MBR ← Memory
t5: MAR ← [MBR]
t6: MBR ← Memory
t7: Z ← NOT [MBR]
t8: MBR ← [Z]
t9: Memory ← [MBR]

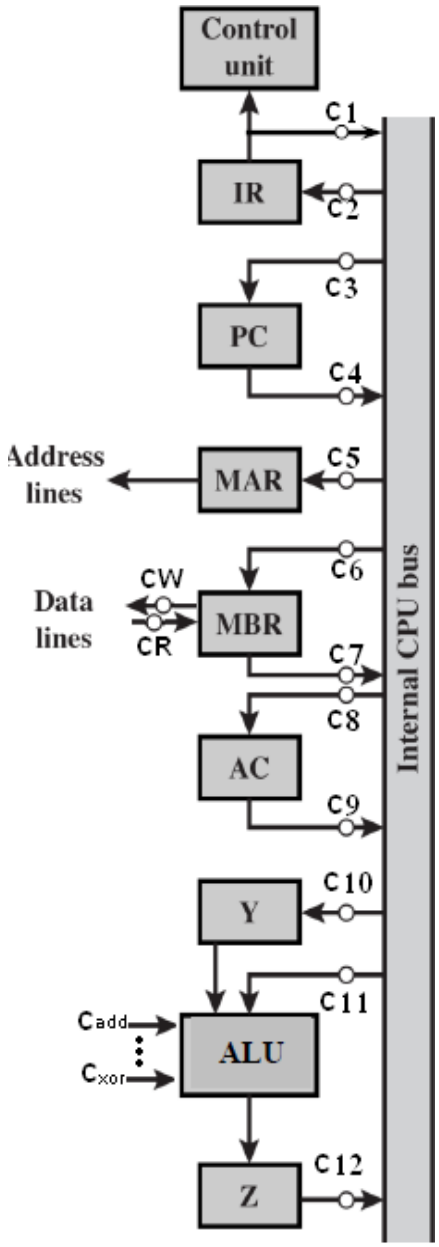
External problem:

If there is a processor with a single CPU internal bus as shown below:

Write the micro-operation & active control signal

In steps for:

1. Fetch cycle
2. Indirect cycle
3. Execute of: ADD @(5)
4. Interrupt cycle



1. Fetch cycle:

T1:	MAR ← [PC]	C4, C5
T2:	MBR ← Mem, Z ← [PC] + 1	CR, C4,C_{add}, C11
T3:	PC ← [Z]	C3, C12
T4:	IR ← [MBR]	C7, C2

2. Indirect cycle:

T1:	MAR ← [IR-Add]	C1, C5
T2:	MBR ← Mem	CR
T3:	[IR-Add] ← [MBR]	C7,C2

3. Execute of: ADD @(5)

T1:	Y ← [IR-Add]	C1, C10
T2:	Z ← [PC] + [Y]	C4,C_{add}, C11
T3:	MAR ← [Z]	C5, C12
T4:	MBR ← Mem, Y ← [AC]	CR, C9, C10
T5:	Z ← [MBR] + [Y]	C7, C11, C_{add}
T6:	AC ← [Z]	C12, C8

4. Interrupt

T1:	MBR ← [PC]	C4, C6
T2:	MAR ← SAVE ADDRESS	C5
T3:	Mem ← [MBR], PC ← [IR-Add]	CW, C3, C1

Question (5) – Final exam F2013

Write in your answer sheet the sequence of micro-operations (and show the steps) required for a CPU (with a single internal bus, 2 general purpose registers R0 and R1, and a stack pointer SP) to perform the following:

(a) Indirect cycle
t1: MAR ← [IR-Address]
t2: MBR ← Memory
t3: IR-Address ← [MBR]

(b) Add (R1), #5
t1: MAR ← [R1]
t2: MBR ← Memory, Y ← [IR-Address]
t3: Z ← [Y] + [MBR]
t4: MBR ← [Z]
t5: Memory ← [MBR]

(c) Call @(300)
t1: Z ← [SP] – 1
t2: SP ← [Z]
t3: MAR ← [SP]
t4: MBR ← [PC]
t5: Memory ← [MBR], Y ← [IR-Address]
t6: Z ← [PC] + [Y]
t7: [PC] ← [Z]