Tutorial #01

[6 points] A 512K×8 bit memory is to be implemented using SRAM chips of size 64K×8 bit, binary decoders of size 2×4, and inverters. Suppose each SRAM chip has a chip select line (CS) and each binary decoder has an enable line (E).

(a) How many SRAM chips, decoders, and inverters are required to implement this memory?

(b) Draw a block diagram of the memory to show the array configuration of the chips and the way they are connected to the decoders and the address lines. Do not bother showing any data lines.

(c) Calculate the overall access time of the memory given that the access time of an SRAM chip is 12ns and propagation delay through a binary decoder is 2ns. Ignore propagation delay through inverters.

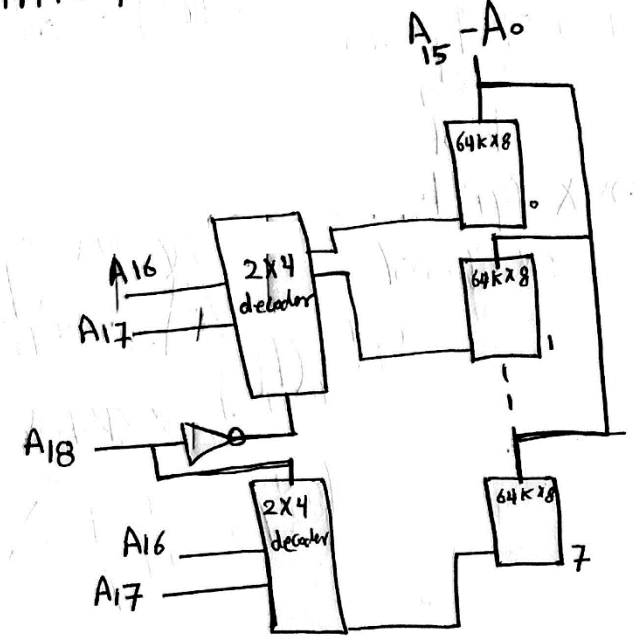
Solution

(a) # sRAM chips $= \frac{512}{64} = 2^3 = 8$ chips

decoders = 2

of inverters = 1

(b)



(c) Access time = 2 nsec + 12 nsec

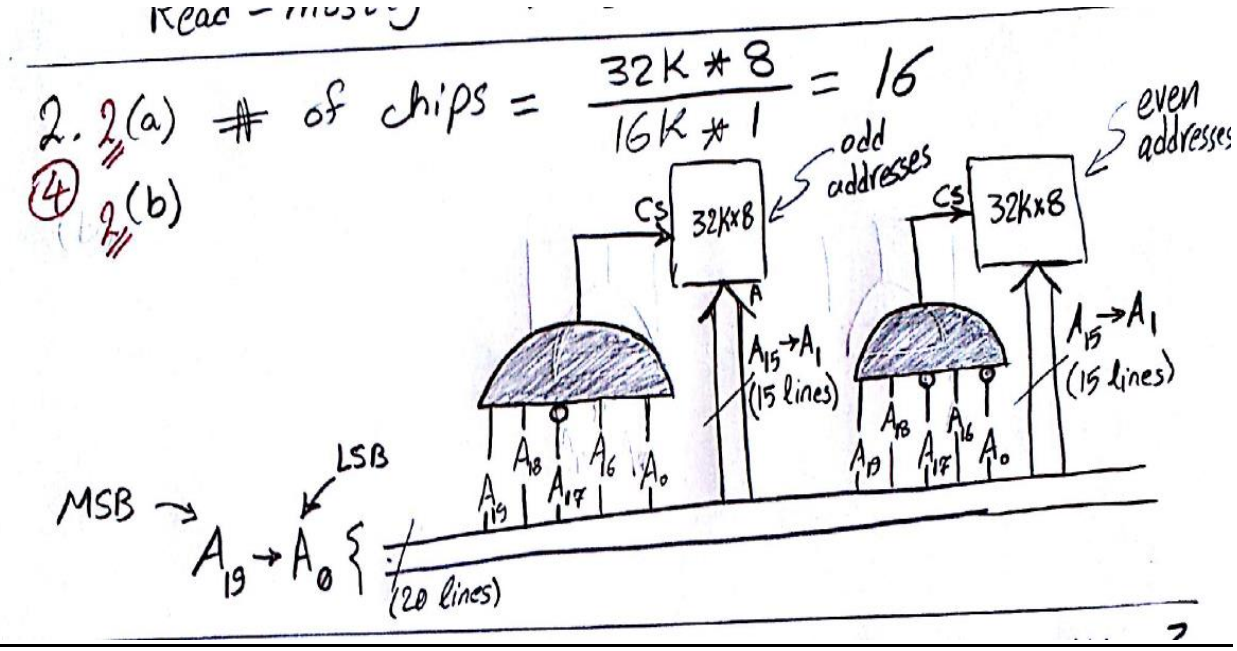
= 14 nsec

[4 points] A 32K×8 bit memory module is to be implemented using memory chips of size 16K×1 bit.

(a) How many chips are required to implement this memory module?

(b) Suppose two 32K×8 memory modules are implemented and equipped with two separate chip select lines (CS). Draw a simple block diagram to illustrate how the two memory modules can be connected to a bus that supports an address space of 1M byte, assuming that the two modules are assigned a range of 64K consecutive addresses starting at D0000 where all even addressees are given to the first module and all odd addresses are given to the second module.

Solution



5.2 Consider a dynamic RAM that must be given a refresh cycle 64 times per ms. Each refresh operation requires 150 ns; a memory cycle requires 250 ns. What percentage of the memory's total operating time must be given to refreshes?

In 1 ms, the time devoted to refresh is 64 × 150 ns = 9600 ns. The fraction of time devoted to memory refresh is $(9.6 \times 10^{-6}\ s)/10^{-3}\ s = 0.0096$, which is approximately 1%.

4. How long is the address in a memory built using k smaller memories of size $m \times n$ each?

(a) $log_2\ m$
(b) $k * log_2\ m$
(c) $log_2\ k + log_2\ m$
(d) Either (a) or (b)
(e) Either (a) or (c)

5. Consider a DRAM that must be refreshed x times every second. Suppose y% of the total operating time of the DRAM is spent in refreshing the cells. Given that the DRAM is organized into z rows, how long does it take to refresh each row?

(a) $(x * y * z) / 100$
(b) $y / (100 * x * z)$
(c) $(100 * x * z) / y$
(d) $(100 * y) / (x * z)$
(e) None of the above

External problem

Design 8M X 32 bits DRAM from 512K X 8 bits DRAM. Show no. of refreshment circuits

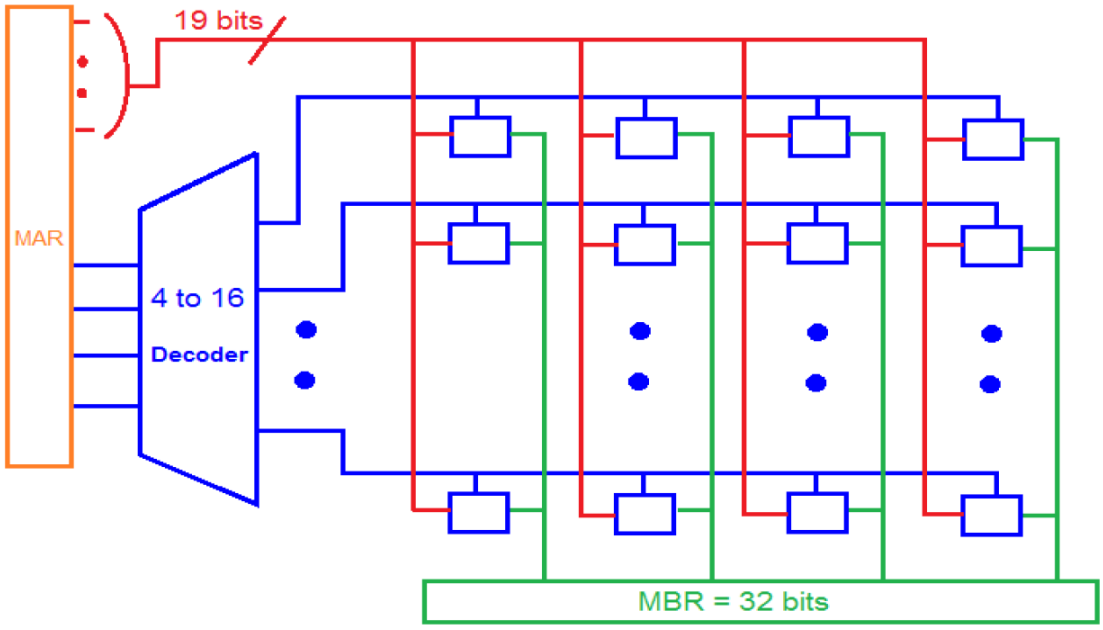
# of Row = 8M/ 512K = 16 Rows = # of refreshment circuits

# of Column = 32/ 8 = 4 Columns

# of Address lines = 23 bits

Address lines are used for:

- 4 bits to select chip (group)
- 19 bits to select byte in chip



Questions

5.3 What is the difference between DRAM and SRAM in terms of application?

SRAM is used for cache memory (both on and off chip), and DRAM is used for main memory.

5.4 What is the difference between DRAM and SRAM in terms of characteristics such as speed, size, and cost?

Characteristics	DRAM	SRAM
Structure	One transistor per cell	Six transistor per cell
Speed	Less speed	Faster
Size	Less size	Larger
Cost	Less expensive	More Expensive

5.6 What are some applications for ROM?

Micro-programmed control memory, library subroutines for frequently wanted functions, system programs, and function tables.