CSE 321a: Computer Organization (I)
Third Year, Computer & Systems Engineering

Assignment #2

Due date: **Thursday, November 2nd, 2017**

Two otherwise identical memory systems, **MS_1** and **MS_2**, have slightly different cache configurations. Both systems have a 16K-byte memory that is byte-addressable, and a unified single-level cache that is divided into 8 lines. However, the cache in the first memory system (**MS_1**) is: direct-mapped, 128-bit lines, no-write-allocate, write-through, while the cache in the second memory system (**MS_2**) is: 2-way set-associative, 64-bit lines, FIFO, write-allocate, write-back.

1. Show the address format for each of the two memory systems MS_1 and MS_2.

2. Suppose the two memory systems **MS_1** and **MS_2** are evaluated using a simple benchmark program that contains **five 64-bit machine instructions** forming a loop that gets executed **millions of times**. The first instruction in the loop is stored in the main memory starting at location 2DB0 (hexadecimal). Only two of the five loop instructions make reference to data in main memory: the third instruction writes to location 3FB0 (hexadecimal), while the fourth instruction reads from location 3FC0 (hexadecimal). Fill up the following table according to the read and write operations that instructions make during the first **two iterations** of the loop. Assume, in both memory systems, the cache is initially empty.

	Iteration	**1st**							**2nd**	
	Instruction	**1st**	**2nd**	**3rd**		**4th**		**5th**	**1st**	**...**
	Fetch/Execute (F/E)	F	F	F	E	F	E	F	F	...
	Read/Write (R/W)	R	R	...	...	...	...	...	R	…
	Address (Hexadecimal)	2DB0	2DB8	...	...	...	...	...	2DB0	...
MS_1	**Line (Hexadecimal)**	...	...	...	...	...	...	...	...	...
	Tag (Hexadecimal)	...	...	...	...	...	...	...	...	...
	Hit/Miss (H/M)	...	...	...	...	...	...	...	...	...
	Allocate line? (Y/N)	...	...	...	...	...	...	...	...	...
MS_2	**Set (Hexadecimal)**	...	...	...	...	...	...	...	...	...
	Tag (Hexadecimal)	...	...	...	...	...	...	...	...	...
	Hit/Miss (H/M)	...	...	...	...	...	...	...	...	...
	Write back? (Y/N)	...	...	...	...	...	...	...	...	...

3. Which of the two memory systems **MS_1** and **MS_2** would definitely have a smaller average access time? Justify your answer based on the hit ratios, hit times, sizes, and associativity of the caches.

4. Suppose in this benchmarking experiment, the average access time of **MS_1** turns out to be 72 ns. Calculate the access time of the cache used in **MS_1** given that the access time of the main memory is known to be 140 ns.

5. Would it possible to use an L2 cache, whose access time is 56 ns, to reduce the average access time of **MS_1** in this benchmarking experiment by 50%? Justify your answer quantitatively.