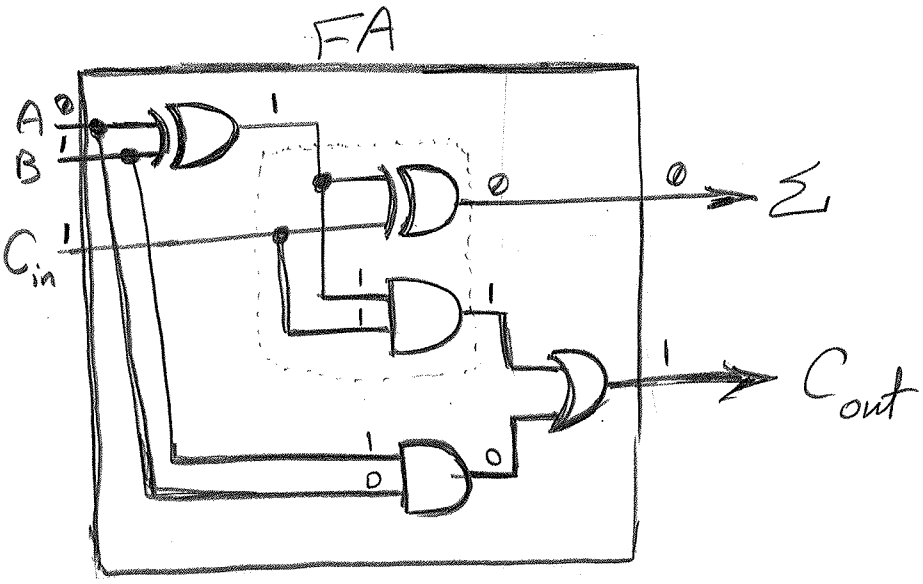
Ch6

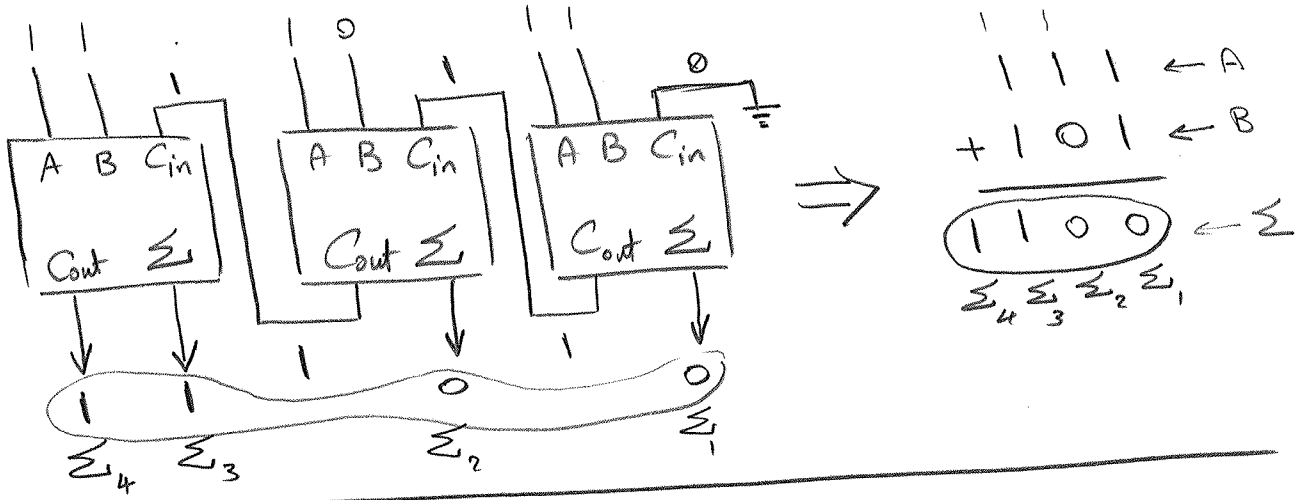
1 (b)

$A = 0, B = 1, C_{in} = 1$

$\Sigma = 0$, $C_{out} = 1$



4



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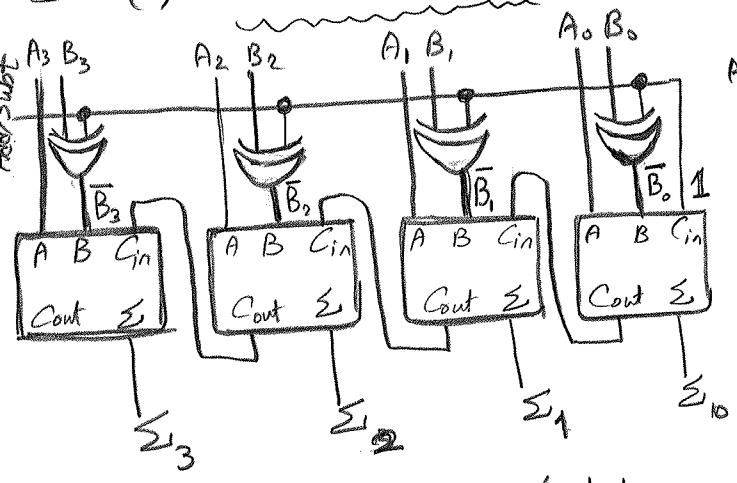
6 (a) $\overline{Add/Subt} = 1$



In this case the circuit behaves like a subtractor (for singned numbers in the 2's comp. form)

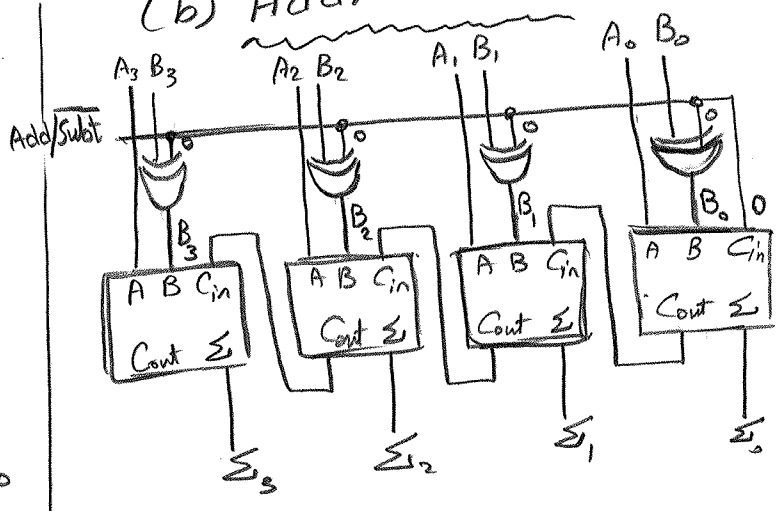
$\Sigma_3\Sigma_2\Sigma_1\Sigma_0 = A_3A_2A_1A_0 + \overline{B}_3\overline{B}_2\overline{B}_1\overline{B}_0 + 1$

$\Sigma = A$ + 1's comp of $B + 1$

$= A$ + 2's comp of B

$\boxed{\Sigma = A - B}$

(b) $\overline{Add/Subt} = 0$

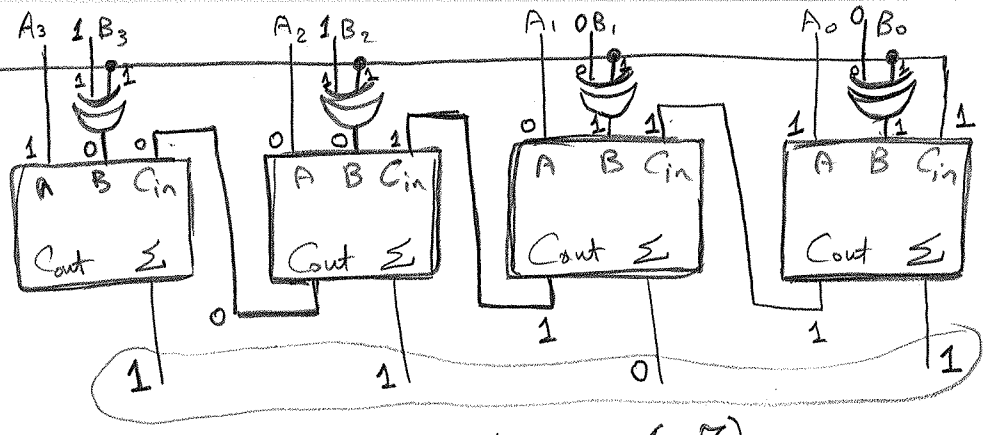


In this case the circuit behaves like the regular 4-bit adder:

$\Sigma_3\Sigma_2\Sigma_1\Sigma_0 = A_3A_2A_1A_0 + B_3B_2B_1B_0$

$\boxed{\Sigma = A + B}$

7 Add/Subt

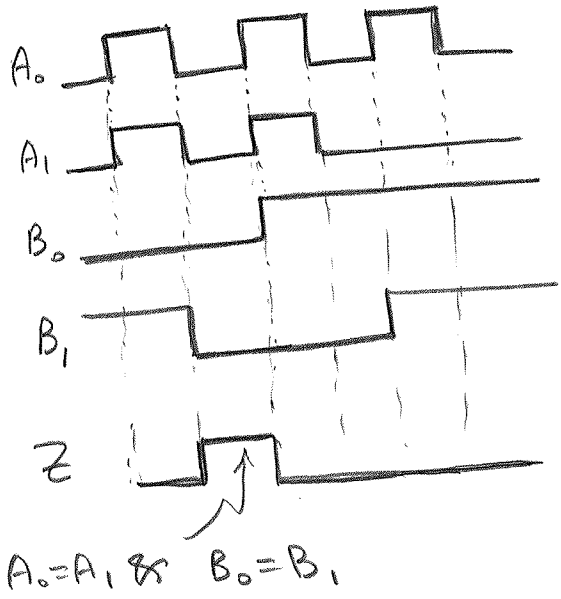


$$1001 \rightarrow (-7)$$
$$-\ 1100 \rightarrow (-4)$$
$$1001$$

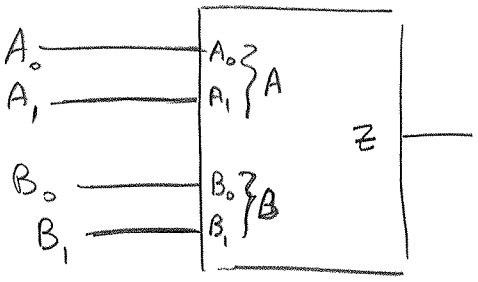
1's comp. of (-4) + 1

$$+\ 0100 \rightarrow \text{2's comp. of } (-4)$$
$$1101 \rightarrow -3$$

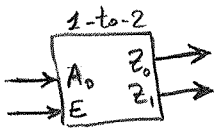
13



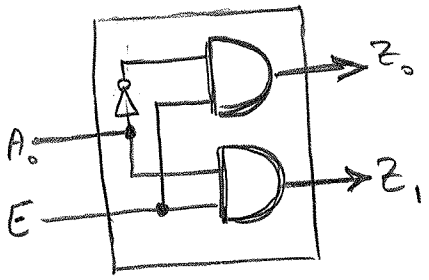
$A_0 = A_1$ & $B_0 = B_1$



***** Design 1-to-2 Decoder with an active-high enable signal (E) using AND-OR Logic.

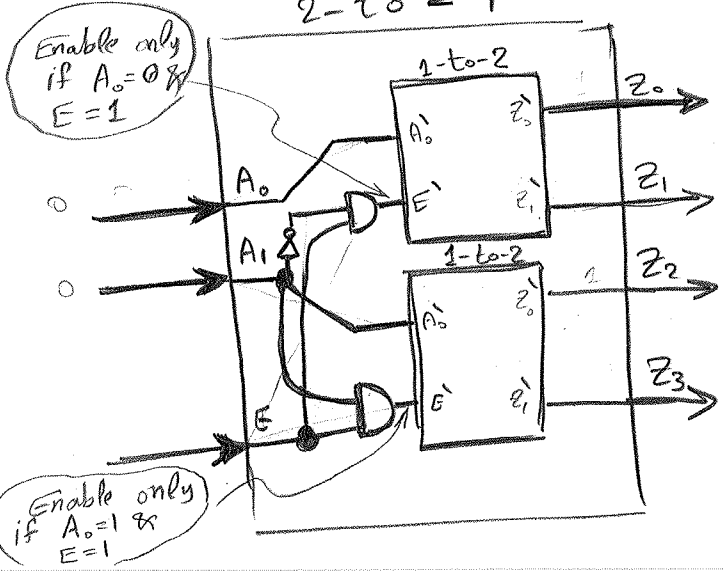


	E	A_0	Z_0	Z_1	
Disable	0	0	0	0	
	0	1	0	0	
Enable	1	0	1	0	$E\bar{A}_0$
	1	1	0	1	EA_0



***** Design a 2-to-4 Decoder with an active-high enable signal (E) using 1-to-2 Decoders.

2-to-4



★ Implement Z using a binary decoder

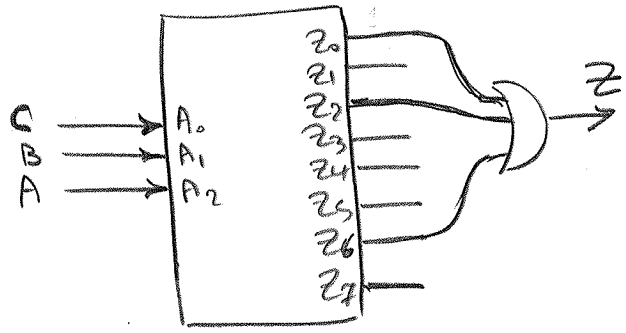
Given:

A	B	C	Z	
0	0	0	1	← Z_0
0	0	1	0	
0	1	0	1	← Z_2
0	1	1	0	
1	0	0	0	
1	0	1	0	
1	1	0	1	← Z_6
1	1	1	0	

Solution:

Since we have 3 inputs

⇒ we need a 3-to-8 decoder



Given $Z = A + \bar{B}$

Solution:

First convert to (standard SOP)

$$Z = A(B+\bar{B}) + (\bar{A}+A)\bar{B}$$

$$= AB + A\bar{B} + \bar{A}\bar{B} + A\bar{B}$$

$$= AB + A\bar{B} + \bar{A}\bar{B}$$

(Z_3: 1 1, Z_2: 1 0, Z_1: 0 0)

Since we have 2 inputs

⇒ we need a 2-to-4 decoder