CSE 401: Computer Engineering (2)
Fourth Year, Electronics & Communication Engineering

Assignment #1

Due date: **Thursday, March 10th, 2016**

1. A 128M×8 DRAM is organized into a cell array that has 4096 rows. The DRAM follows a distributed refreshment approach. Instead of refreshing the whole cell array at once in a single refresh cycle, the array is refreshed incrementally in multiple small refresh cycles where only two rows get to be refreshed each cycle.
   (a) Suppose each memory cell can retain its data for up to 64 ms (without being refreshed). What should be the maximum time elapsed from the beginning of any refresh cycle to the next?
   (b) If it takes 0.25 μs to refresh one row, what percentage of the DRAM time is spent in refreshment?

2. A 256K×4 read-only memory is to be implemented using 128K×1 ROM chips (with no chip-select (CS) lines) and 2×1 multiplexers.
   (a) How many ROM chips and multiplexers are required to implement this memory?
   (b) Draw a block diagram of the memory to show how the ROM chips should be connected together with the multiplexers and how the input address lines and the output data lines are routed.
   (c) Calculate the overall access time of the memory given that the access time of each ROM chip is 10ns and the propagation delay of each multiplexer is 2ns.

3. A memory chip is equipped with a SEC-DED mechanism that generates 13-bit codewords. Every codeword contains 8 bits of data, 4-bit Hamming code, and 1 global parity bit. For each of the following cases: specify whether the codeword is legal or not, and unless the codeword is legal, identify the error and correct it if possible.
   (a) Data bits = “11011011”, Hamming code = “1111”, parity bit = “1”.
   (b) Data bits = “11001011”, Hamming code = “1011”, parity bit = “0”.
   (c) Data bits = “11001011”, Hamming code = “0110”, parity bit = “1”.
   (d) Data bits = “11001011”, Hamming code = “1111”, parity bit = “0”.