Tutorial #2

CSE 321a: Computer Organization (I)
Third Year, Computer and Systems Engineering

CSE 321a – Midterm Exam– Fall 2014

Consider a small hypothetical computer with four 16-bit general-purpose registers numbered from 0 to 3. Each machine contains 16 bits (X15-0). The six most-significant bits of the instruction (X15-10) represent an op-code. The following two bits (X9-8) represent a register number. The remaining bits (X7-0) may represent the value or the address of an operand. The following table contains some of the supported op-codes:

Mnemonic	Binary Meaning
LOAD 011100	Load register X9-8 from memory location X7-0.
STORE 011101	Store value of register X9-8 to memory location X7-0.
ADDLD 110001	Add value of memory location X7-0 to register X9-8.
ADDST 110011	Add value of register X9-8 to memory location X7-0.
DECBRNZ 111010	Decrement value of register X9-8 by 1, and if new value of register X9-8 is not 0, branch to instruction whose address is X7-0, else continue normally.

22. How many memory accesses are needed to fetch and execute instruction EA9B?
(a) 0
(b) 1
(c) 2
(d) 3
(e) None of the above

23. Suppose the values of register 2 and location 3A are: 2D15 and 11B5 respectively. What would be their values after executing instruction 763A?
(a) 2D15 and 11B5
(b) 2D15 and 2D15
(c) 11B5 and 11B5
(d) 11B5 and 2D15
(e) None of the above

24. Suppose the values of register 1 and location 75 are: 623E and 2935 respectively. What would be their values after executing instruction C575?
(a) 623E and 9174
(b) 623E and 2935
(c) 9174 and 2935
(d) 8B74 and 623E
(e) None of the above

25. Suppose the values of register 3 and program counter (PC) are: 0001 and 005B respectively. Which of the following instructions will load the PC with 008F after being executed?
(a) EB8F
(b) 738F
(c) EAF8
(d) C78F
(e) None of the above

CSE 321a – Midterm Exam– Fall 2015

Consider a small computer in which memory locations, general-purpose registers, and machine instructions are all 14-bit long. The processor has only two general-purpose registers (numbered 0 and 1). The three most-significant bits of each machine instruction (X13-11) represent an opcode. The following two bits (X10 and X9) represent two register numbers. The remaining bits (X8-0) may represent the value or the address of an operand. The following table contains some of the supported opcodes:

Mnemonic	Binary	Meaning
LOAD	001	Load registers X9 and X10 from memory locations X8-0 and X8-0+1, respectively.
STORE	011	Store registers X9 and X10 to memory locations X8-0 and X8-0+1, respectively.
ADDCONST	100	Add value X8-0 to value of register X9, and save result to register X10.
ADDLOC	101	Add value of location X8-0 to value of register X9, and save result to register X10.
INCBREQ	111	Increment value of register X9 by 1, and if new value of register X9 is equal to that of register X10, branch to instruction in location X8-0, else continue normally.

Suppose the values of the registers and memory locations in the initial state are:

PC	MDR	Register 0	Register 1	Location 01E2	Location 01E3
01D2	**2B0A**	**03C0**	**03BF**	**30CA**	**1FA3**

21. Which of the following must be 14-bit long in this computer?
(a) MAR
(b) PC
(c) Word
(d) Unit of transfer
(e) None of the above

22. How many memory accesses are needed to fetch and execute instruction 1C76?
(a) 0
(b) 1
(c) 2
(d) 3
(e) None of the above

23. What will be the value of MDR after executing instruction 2BE3 from initial state?
(a) 2B0A
(b) 01E3
(c) 1FA3
(d) 2BE3
(e) None of the above

24. What will be the values of registers 0 and 1 after executing instruction 27F7 from initial state?
(a) 03C0 and 03BF
(b) 03C0 and 05B6
(c) 05B7 and 03BF
(d) 05B6 and 05B7
(e) None of the above

25. Which of the following instructions will load PC with 01A4 after being executed from initial state?
(a) 39A4
(b) 3BA4
(c) 3DA4
(d) 3FA4
(e) None of the above