Tutorial #3

CSE 321a: Computer Organization (I)
Third Year, Computer and Systems Engineering

CSE 321a – Midterm Exam– Fall 2015

Consider a small computer in which memory locations, general-purpose registers, and machine instructions are all 14-bit long. The processor has only two general-purpose registers (numbered 0 and 1). The three most-significant bits of each machine instruction (X13-11) represent an opcode. The following two bits (X10 and X9) represent two register numbers. The remaining bits (X8-0) may represent the value or the address of an operand. The following table contains some of the supported opcodes:

Mnemonic	Binary	Meaning
LOAD	001	Load registers X9 and X10 from memory locations X8-0 and X8-0+1, respectively.
STORE	011	Store registers X9 and X10 to memory locations X8-0 and X8-0+1, respectively.
ADDCONST	100	Add value X8-0 to value of register X9, and save result to register X10.
ADDLOC	101	Add value of location X8-0 to value of register X9, and save result to register X10.
INCBREQ	111	Increment value of register X9 by 1, and if new value of register X9 is equal to that of register X10, branch to instruction in location X8-0, else continue normally.

Suppose the values of the registers and memory locations in the initial state are:

PC	MDR	Register 0	Register 1	Location 01E2	Location 01E3
01D2	**2B0A**	**03C0**	**03BF**	**30CA**	**1FA3**

21. Which of the following must be 14-bit long in this computer?
(a) MAR
(b) PC
(c) Word
(d) Unit of transfer
(e) None of the above

22. How many memory accesses are needed to fetch and execute instruction 1C76?
(a) 0
(b) 1
(c) 2
(d) 3
(e) None of the above

23. What will be the value of MDR after executing instruction 2BE3 from initial state?
(a) 2B0A
(b) 01E3
(c) 1FA3
(d) 2BE3
(e) None of the above

24. What will be the values of registers 0 and 1 after executing instruction 27F7 from initial state?
(a) 03C0 and 03BF
(b) 03C0 and 05B6
(c) 05B7 and 03BF
(d) 05B6 and 05B7
(e) None of the above

25. Which of the following instructions will load PC with 01A4 after being executed from initial state?
(a) 39A4
(b) 3BA4
(c) 3DA4
(d) 3FA4
(e) None of the above

Problem 3.14

A microprocessor has an increment memory direct instruction, which adds 1 to the value in a memory location. The instruction has five stages: fetch opcode (four bus clock cycles), fetch operand address (three cycles), fetch operand (three cycles), add 1 to operand (three cycles), and store operand (three cycles).
a. By what amount (in percent) will the duration of the instruction increase if we have to insert two bus wait states in each memory read and memory write operation?
b. Repeat assuming that the increment operation takes 13 cycles instead of 3 cycles.

a. Without the wait states, the instruction takes 16 bus clock cycles. The instruction requires four memory accesses, resulting in 8 wait states. The instruction, with wait states, takes 24 clock cycles, for an increase of 50%.
b. In this case, the instruction takes 26 bus cycles without wait states and 34 bus cycles with wait states, for an increase of 33%.

Problem 3.18 (Extension of problem 3.14)

The microprocessor of Problem 3.14 initiates the fetch operand stage of the increment memory direct instruction at the same time that a keyboard actives an interrupt request line. After how long does the processor enter the interrupt processing cycle? Assume a bus clocking rate of 10 MHz.

The processor needs another nine clock cycles to complete the instruction. Thus, the Interrupt Acknowledge will start after 900 ns.