CSE 321b: Computer Organization (II)
Third Year, Computer & Systems Engineering

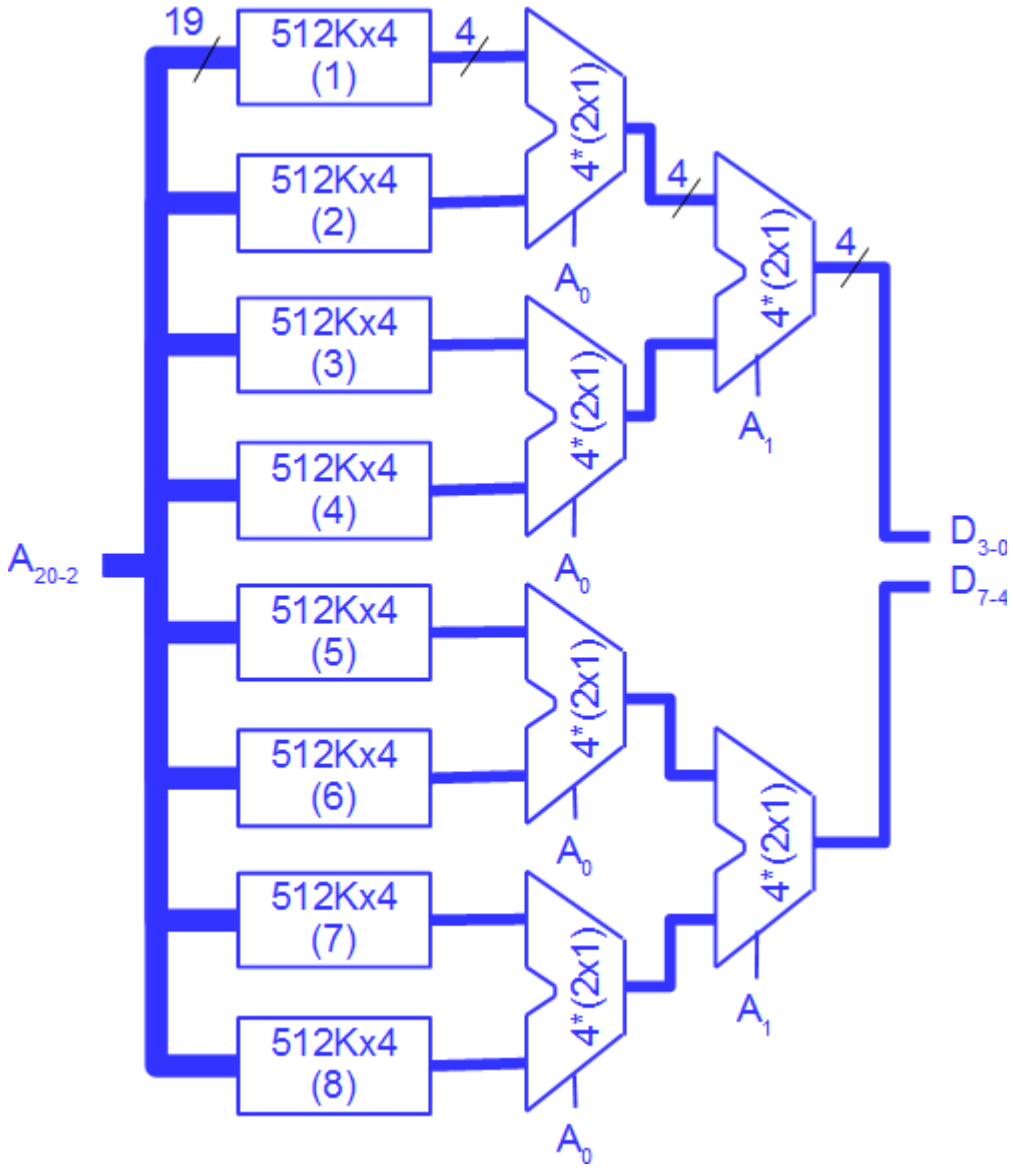
Solution to Assignment #1

1. A 2M×8 read-only memory is to be implemented using 512K×4 ROM chips (with no chip-select (CS) lines) and 2×1 (single-bit) multiplexers.

   (a) How many ROM chips and multiplexers are required to implement this memory?

   Number of ROM chips = (2M * 8) / (512K * 4) = 8
   Number of 2×1 multiplexers = 8 * (2 + 1) = 24 (needed to build eight 4×1 multiplexers!)

   (b) Draw a block diagram of the memory.



   (c) Calculate the overall access time of the memory.

The overall access time = 9ns (ROM) + 2 * 3ns (2-level of multiplexers) = 15 ns

2. A DDR3-SDRAM module contains four memory chips. All the chips receive the same address and command. The module can store 1 GB of data that can be transferred in 64-bit words over the bus at a maximum rate of 12800 MB/s.

(a) Represent the size of each memory chip in the form "*m*×*n*".

The storage capacity of each chip = (1 GB) / 4 = 256 MB
The location size in each chip = (64 b) / 4 = 16 b = 2 B
Number of locations in each chip = (256 MB) / (2 B/location) = 128 M location
The size of each memory chip is: 128M×16

(b) What is the bus speed (in MHz)?

Number of bytes per word = (64 b/word) / (8 b/B) = 8 B/word
Number of words transferred each second = (12800 MB/s) / (8 B/word) = 1600 M word/s
DDRx ==> Number of words transferred each bus cycle = 2 word/cycle
The bus speed = (1600 M word/s) / (2 word/cycle) = 800 MHz

(c) What is memory speed (in MHz)?

DDR3 ==> produce 8 words every memory cycle which take 4 bus cycles to be sent
Every memory cycle corresponds to four bus cycles
The memory speed = (800 MHz) / 4 = 200 MHz

3. A memory chip is equipped with a **SEC** mechanism that uses 18-bit long codewords.

(a) How many check bits are contained in each codeword?

Suppose each codeword contains m data bits and k check bits
Knowing that: $m + k = 18$ and $m + k + 1 \leq 2^k$
Then: $18 + 1 \leq 2^k$ ==> k=5
The number of data bits in each codeword = $m = 18 - k = 13$
The number of check bits in each codeword = $k = 5$

(b) Suppose the following codeword is read at some point from memory: "1011111011101110000":

i. Show that this codeword is illegal.

Given that the codeword:
"$D_{18}D_{17}C_{16}D_{15}D_{14}D_{13}D_{12}D_{11}D_{10}D_9C_8D_7D_6D_5C_4D_3C_2C_1$" = "1011111011101110000"
we can calculate the values of the check bits as follows:
$C_1 = D_3 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{11} \oplus D_{13} \oplus D_{15} \oplus D_{17} = 0$
$C_2 = D_3 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{11} \oplus D_{14} \oplus D_{15} \oplus D_{18} = 1$
$C_4 = D_5 \oplus D_6 \oplus D_7 \oplus D_{12} \oplus D_{13} \oplus D_{14} = 1$
$C_8 = D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} = 0$
$C_{16} = D_{17} \oplus D_{18} = 1$
Calculated values of check bits "10110" ≠ given values of check bits "11100"
Then given codeword is illegal

ii. Describe the error in this codeword.

The position of the error = "10110" ⊕ "11100" = "01010"
This indicates that there is a single-bit error in position #10 ==> D_{10}

iii. Identify the closest legal codeword to this codeword.

The closest legal codeword is "1011111001101110000"

4. An error correcting code contains four 10-bit codewords. Two of which are "0101101001" and "1010001111". Suppose the code can correct double-bit errors and detect triple-bit errors.

(a) What must be the minimum Hamming distance of this code? Justify your answer.

To be able to specify that a triple-bit error happens, the illegal codeword (containing the three bit errors) must be at a distance greater than two from any legal codeword, to prevent wrong correction!!
The minimum Hamming distance of this code = 3 + (2+1) = 6

(b) Suggest a suitable value for each the other two codewords.

There are many possible values for the other two code words. All of them can be generated by following these two patterns: "$x_9x_8x_7x_6x_5$10$x_2x_1$0" and "$y_9y_8y_7y_6y_5$10$y_2y_1$0" and satisfy the following two conditions: (1) three (or four) x_i bits must be different from their corresponding bits in each of the two given codewords, (2) (six or seven) y_i bits must be different from their corresponding x_i bits. For instance, here are two possible values for the missing codewords: "01100**10**000**0**" and "10011**10**110**0**".