Kingdom of Saudi Arabia
Ministry of Education
Shaqra University
CCIT

CSC 211 – Digital Logic Design
First Term – 1439/1440
Solution to Assignment #2

1. Simplify the following expressions using Boolean algebra:

a. $(\boldsymbol{B}+\overline{\boldsymbol{C}})(\overline{\boldsymbol{B}}+\boldsymbol{C})+\overline{\overline{\boldsymbol{A}}+\boldsymbol{B}+\overline{\boldsymbol{C}}}$

$= B\bar{B}+BC+\bar{B}\bar{C}+C\bar{C}+\bar{\bar{A}}+\bar{B}+\bar{\bar{C}}$ [Dist. + DM]

$= 0+BC+\bar{B}\bar{C}+0+A+\bar{B}+C$ [R8, R9]

$= A+\bar{B}+C$ [R1, R10]

b. $\overline{(\overline{\boldsymbol{A}}+\boldsymbol{B}+\overline{\boldsymbol{C}})(\boldsymbol{A}+\boldsymbol{B}+\overline{\boldsymbol{C}})(\overline{\boldsymbol{A}}+\boldsymbol{B}+\boldsymbol{C})(\overline{\boldsymbol{BC}+\overline{\boldsymbol{A}}\overline{\boldsymbol{B}}\overline{\boldsymbol{C}}})}$

$= \left(\overline{\bar{A}+B+\bar{C}}\right)+\left(\overline{A+B+\bar{C}}\right)+\left(\overline{\bar{A}+B+C}\right)+\left(\overline{\overline{BC+\bar{A}\bar{B}\bar{C}}}\right)$ [DM]

$= \bar{\bar{A}}\bar{B}\bar{\bar{C}}+\bar{A}\bar{B}\bar{\bar{C}}+\bar{\bar{A}}\bar{B}\bar{C}+BC+\bar{A}\bar{B}\bar{C}$ [DM, R9]

$= A\bar{B}C+\bar{A}\bar{B}C+A\bar{B}\bar{C}+BC+\bar{A}\bar{B}\bar{C}$ [R9]

$= A\bar{B}C+\bar{A}\bar{B}C+A\bar{B}\bar{C}+BC+\bar{A}\bar{B}\bar{C}$ [R9]

$= A\bar{B}(C+\bar{C})+\bar{A}\bar{B}(C+\bar{C})+BC$ [Dist.]

$= A\bar{B}+\bar{A}\bar{B}+BC$ [R6, R4]

$= \bar{B}(A+\bar{A})+BC$ [Dist.]

$= \bar{B}+BC$ [R6, R4]

$= \bar{B}+C$ [R11]

2. Suppose a Boolean variable *Z* is described by the following Karnaugh map

a. Construct a minimum SOP expression for *Z*.

$AB \backslash CD$	00	01	11	10
00	X	X	X	0
01	0	X	1	1
11	0	1	1	X
10	0	X	X	0

$Z = D + BC$

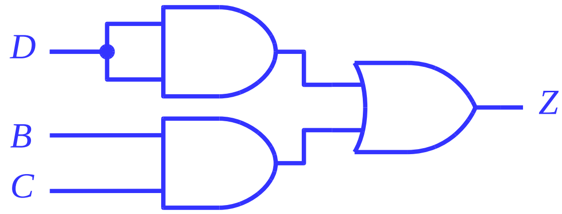
b. Construct a minimum POS expression for *Z*.

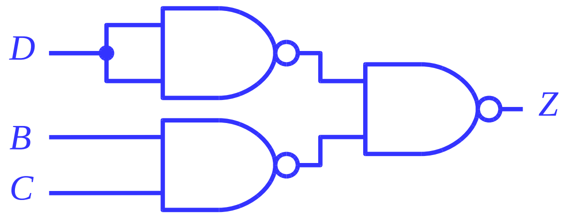
$AB \backslash CD$	00	01	11	10
00	X	X	X	0
01	0	X	1	1
11	0	1	1	X
10	0	X	X	0

$Z = B(\mathrm{C} + \mathrm{D})$

c. Implement *Z* using NAND gates.

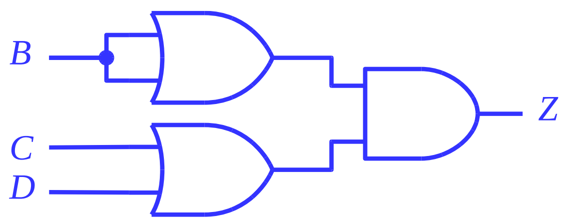
$$Z = D + BC$$

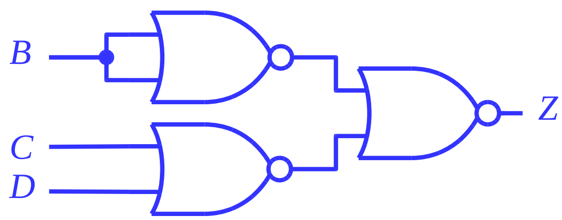




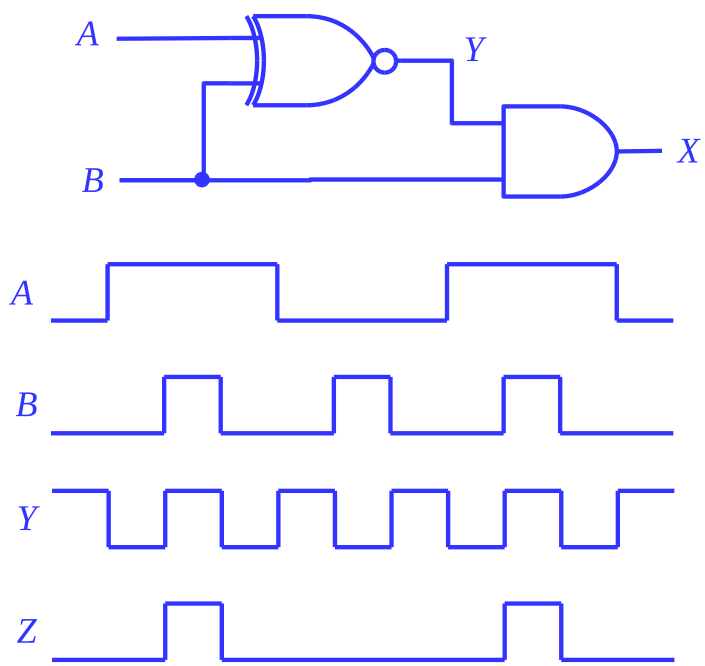
d. Implement *Z* using NOR gates.

$$Z = B(\mathrm{C} + \mathrm{D})$$

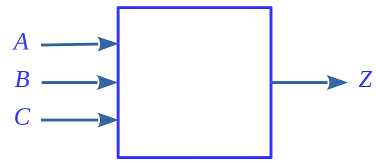




3. For the following logic circuit, draw the output waveform …



4. Design a logic circuit whose output Z is HIGH only when a majority of its inputs A, B, and C are LOW.



Inputs			Output
A	***B***	***C***	***Z***
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

$AB \backslash C$	0	1
00	1	1
01	1	0
11	0	0
10	1	0

$$Z = \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C}$$