CSE 321b: Computer Organization (II)
Third Year, Computer & Systems Engineering

Assignment #2

Due date: **Thursday, April 6th, 2017**

1. A hard disk drive has 10 surfaces, 10240 tracks per surface, and 512 sectors per track. Sector size is 4 KB. The drive head traverses 1280 track/ms and the spindle spins at 5400 r.p.m.
   (a) What is the total capacity of hard disk drive (in GB)?
   (b) What is the physical address of the sector whose logical block address (LBA) is 2312349?
   (c) What is the longest time needed to read any sector anywhere on the disk?

2. Suppose each layer of the DVD can store 3.5 GB of data.
   (a) What is the maximum amount of data that can be stored on the DVD (in GB)?
   (b) Suppose the DVD is used to store a video with 30 frames/s, 720×480 pixels/frame, 24 bit/pixel:
      i. What is the maximum number of minutes that can be stored on the DVD?
      ii. What is the compression ratio required to fit a 133-minute movie in one layer of the DVD?

3. A RAID level 2 array is built using 7 disk drives. Each drive can store 4 TB.
   (a) What is the overall data storage capacity of this array (in TB)?
   (b) Suppose disks #3, #5 and #7 in the array fail at the same time. Show how their data can be restored. *Hint: assume any partial stripe value (e.g., "?1?0?01") and calculate the missing bits.*

4. An I/O device transfers 2500 independent data blocks each second over a system bus, which has a transfer data rate of 100 MB/s. The block size is 4000 B. The processor of the system operates at 200 MHz. With DMA enabled, it takes the processor 1000 clock cycles to initiate a DMA transaction, and 1500 cycles to respond to the device's interrupt when the DMA transfer completes. What fraction of the processor's time is spent handling the data transfer with and without DMA?

5. A given CPU requires 1000 cycles to perform a context switch and start an interrupt handler (and the same number of cycles to switch back to the program that was running when the interrupt occurred), or 500 cycles to poll an I/O device. An I/O device attached to that CPU makes 150 requests per second, each of which takes 10000 cycles to resolve once the handler has been started. By default, the CPU polls every 0.5 ms if it is not using interrupts.
   (a) How many cycles per second does the CPU spend in I/O with the device if interrupts are used?
   (b) How many cycles per second are spent on I/O if polling is used (including all polling attempts)? Assume the CPU only polls during time slices when user programs are not running, so do not include any context-switch time in your calculation.
   (c) How often would CPU have to poll for polling to take as many cycles per second as interrupts?