# **Tutorial #4**

# CSE 321a: Computer Organization (I)

Third Year, Computer and Systems Engineering

## Prob. (4.2):

A two-way set-associative cache has lines of 16 bytes and a total size of 8 Kbytes. The 64-Mbyte main memory is byte addressable. Show the format of main memory addresses.

```
Word size = 1 byte (byte addressable)

Word field (W) = \lg(\# \text{ of words in block}) = \lg(16) = 4 \text{ bits}

Set field (S) = \lg(\# \text{ of sets in cache}) = \lg(\text{cache size} / \text{set size}) = \lg(8 \text{ K/16 * 2}) = 8 \text{ bits}

Tag field (T) = address field – (s+w) = \lg(64 \text{ M}) - (4+8) = 14 \text{ bits}
```

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# Prob. (4.11):

Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size.

- a. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.
- **b.** Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.
- **c.** Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag.

```
Address size= 32 bits

Word size = 1byte (bit level)

Line size = block size = 64 bytes. \rightarrow L=6, W=6

T=A-(L+W) = 20
```

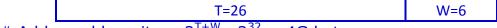
# a. Direct Mapped:

	T=2	20	L=6	W=6
 		- A - 22		

# Addressable units =  $2^A = 2^{32} = 4G$  bytes

```
#MM blocks= MM size / Block size = 4G/64 = 64M blocks
# Cache lines = 2^L = 2^6 = 64 Lines
Tag size = 20 bits
```

### b. Associative:



# Addressable units =  $2^{T+W} = 2^{32} = 4G$  bytes

#MM blocks  $= 2^T = 2^{26} = 64M$  blocks

# Cache lines = undetermined but if use the same cache it will be = 64 Lines

Tag size = 26 bits

## c. 4 way set associative:

T=9 S=17 W=6

#### K=4

# Addressable units = 4G bytes

#MM blocks=  $2^{T+S}=2^{26}=64M$  blocks

# Lines per set = k = 4 lines

# Cache sets = cache size/set size =4k/4\*64 = 128K sets

# Cache lines = # cache sets \* # lines per set

= 128k \* 4 = 512 K lines

Tag size = 9 bits