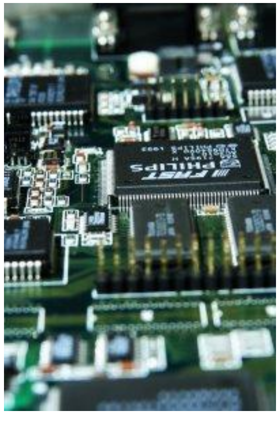
# CSE 401

# Computer Engineering (2)

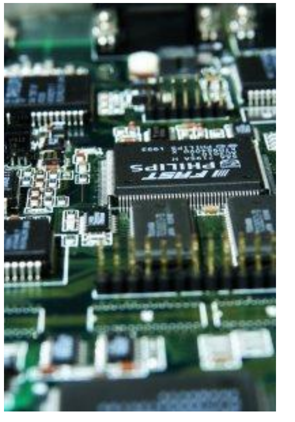
# هندسة الحاسبات (2)



4th year, Comm. Engineering

Winter 2016

**Lecture #1**



Dr. Hazem Ibrahim Shehata

Dept. of Computer & Systems Engineering

Credits to Dr. Ahmed Abdul-Monem Ahmed for the slides

# Teaching Staff

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- Teaching Assistants:
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    - Tutorials: TBA
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    - Email: sanaafekry2003@yahoo.com
    - Labs: TBA

# Course Info

- Course website:
  - http://www.bit.do/hshehata-courses-zu-cse401
  - http://www.googledrive.com/host/0B9ExmUsPoGjSWUpOQ05XT3loYUE
- Textbook:
  - “Computer Organization and Architecture: Designing for Performance”, William Stallings, 9th Edition, 2013, www.williamstallings.com/ComputerOrganization

# Course Info (Cont.)

- Grading:

| Course work | Grade distribution | |
|---|---|---|
| Participation | 3pt | 30 |
| Assignments | 12pt | |
| Midterm Exam | 15pt | |
| Labs | 16pt | 30 |
| Oral Exam | 14pt | |
| Final Exam | 90pt | |
| **Total Points** | **150** | |

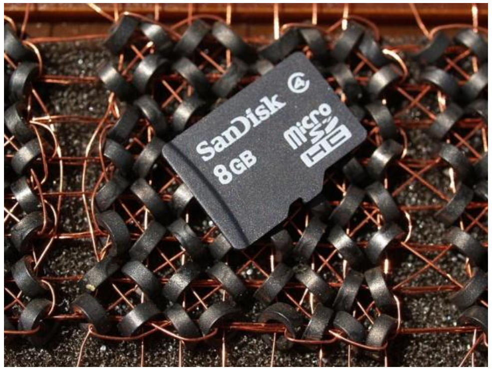
# Course Overview

- Ch. 5: Internal Memory Technology
  - Semiconductor MM, error correction, ..., *etc*.
- Ch. 6: External Memory
  - Magnetic disks, optical disks, magnetic tapes, ... *etc*.
- Ch. 7: Input / Output
  - Programmed i/o, interrupt-driven i/o, DMA, ..., *etc*.
- Ch. 10: Computer Arithmetic
  - Integer representation, Integer arithmetic , FP representation, FP arithmetic, ..., *etc*.
- Ch. 14: Processor Structure and Function
  - Processor organization, register organization, Instruction pipelining, ..., *etc*.

# Ch 5: Internal Memory Technology

# Memory Cell

- Semiconductor memory: electronic memory implemented on a semiconductor-based IC.

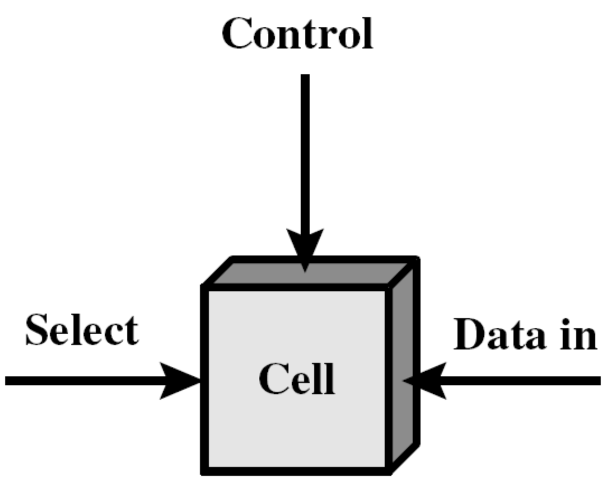



Semiconductor Memory
vs.
Magnetic-core Memory

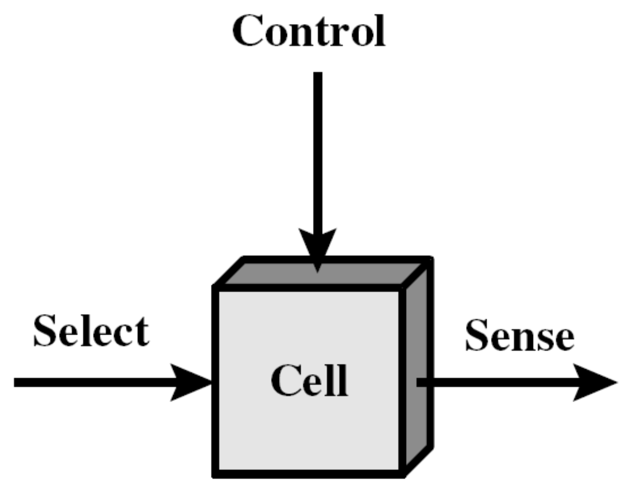
- Memory cell: basic element of a semiconductor memory.
  - Holds **one** bit.
  - Properties
    - **Two** stable states to represent 0 and 1 ➔ bi-stable!
    - Can be **written** into to **set** the state.
    - Can be **read** to **sense** the state.

# Conceptual Operation of a Memory Cell

- Three terminals: select, control, data in/sense.
  - Select: select a memory cell for read/write.
  - Control: indicate required operation: read or write.
  - Data in/sense:
    - Read: Output the state of the cell.
    - Write: electrical signal that sets the state to 0 or 1.




(a) Write




(b) Read

# Semiconductor Memory Types

- Volatile
  - Random Access Memory (RAM)
    - Dynamic RAM (DRAM)
    - Static RAM (SRAM)
- Non-volatile
  - Read-Only Memory (ROM)
  - Programmable ROM (PROM)
  - Erasable Programmable ROM (EPROM)
  - Electrically Erasable Programmable ROM (EEPROM)
  - Flash Memory

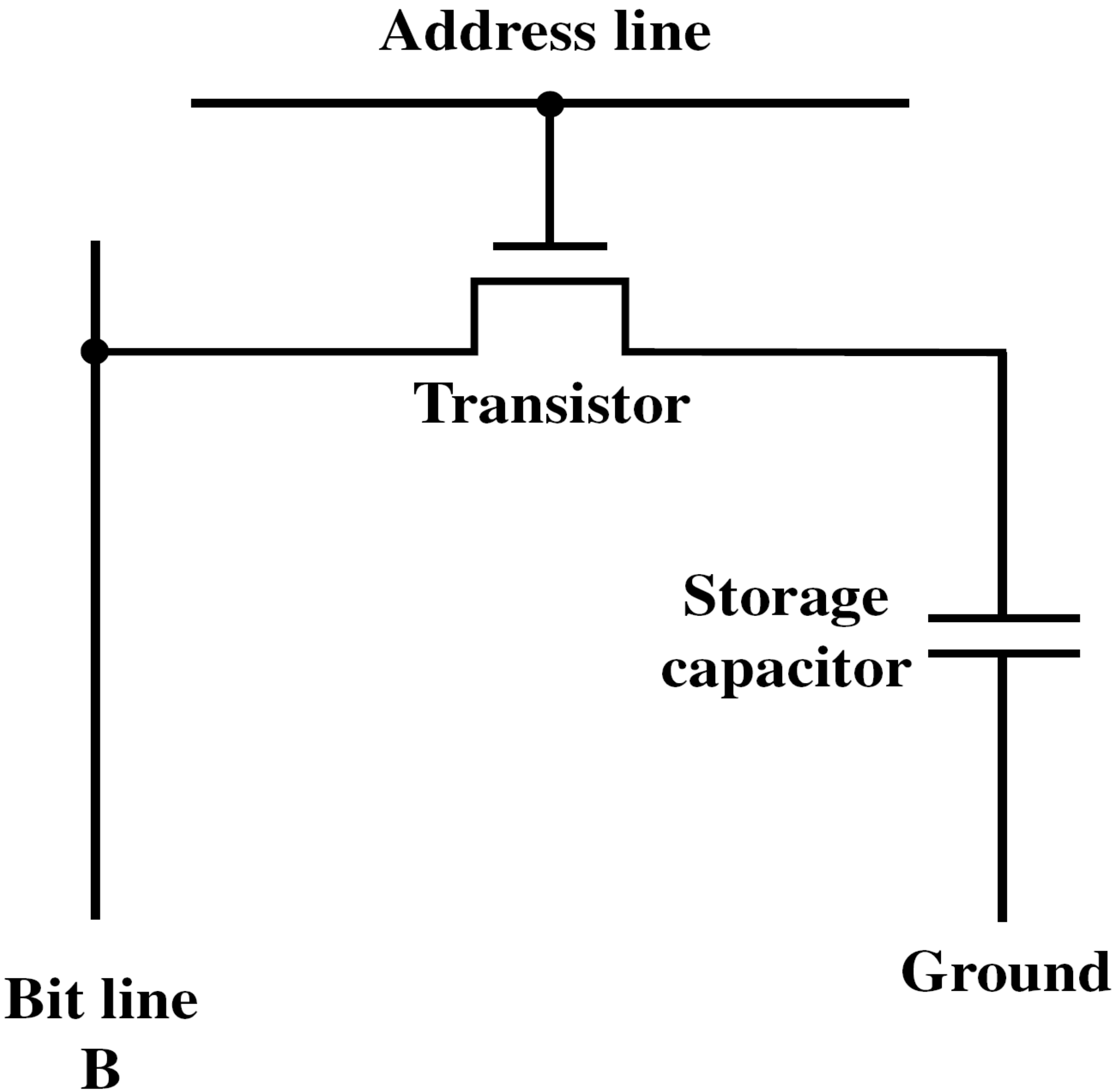
# RAM

- Individual words of memory are directly accessed through wired-in addressing logic.
- Misnamed!! All semiconductor memories are random access!!
- Read/Write: by electrical signals.
- Volatile: must be provided with a constant power supply ➔ temporary storage.
- Dynamic or static.

# Dynamic RAM (DRAM)

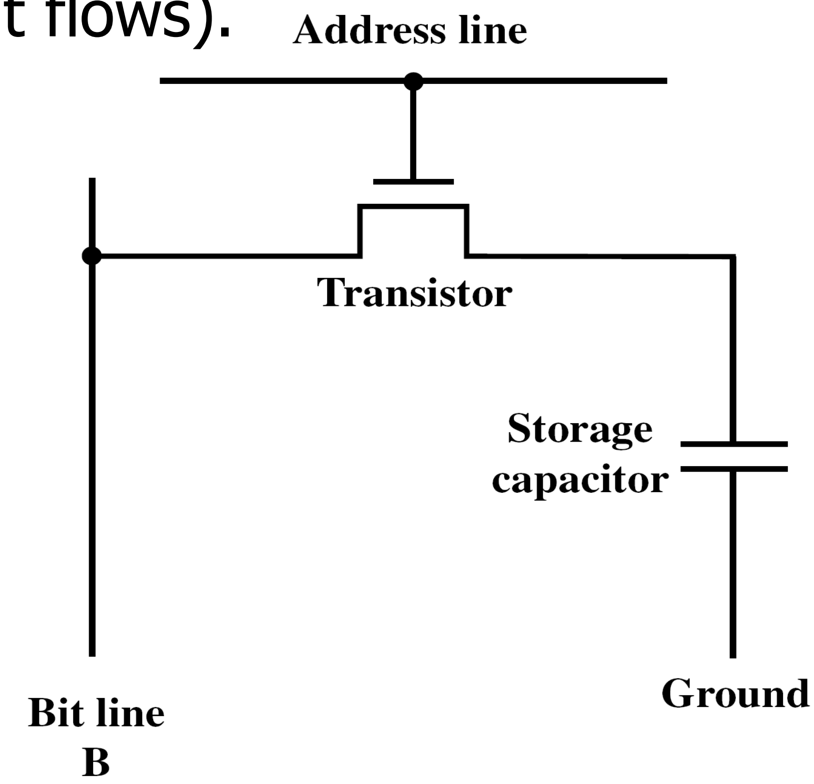
- Bits are stored as charge on capacitors.
  - Charge → 1, no charge → 0.
- Capacitors discharge → DRAM needs periodic charge refreshing even when powered.
- Analog device: capacitor can store any charge value within a range → a threshold value is used.
- Pros
  - Simpler construction.
  - Smaller per bit.
  - Less expensive.
- Cons
  - Need refresh circuits.
  - Slower.
- Most common usage: main memory.

# DRAM Structure



# DRAM Operation

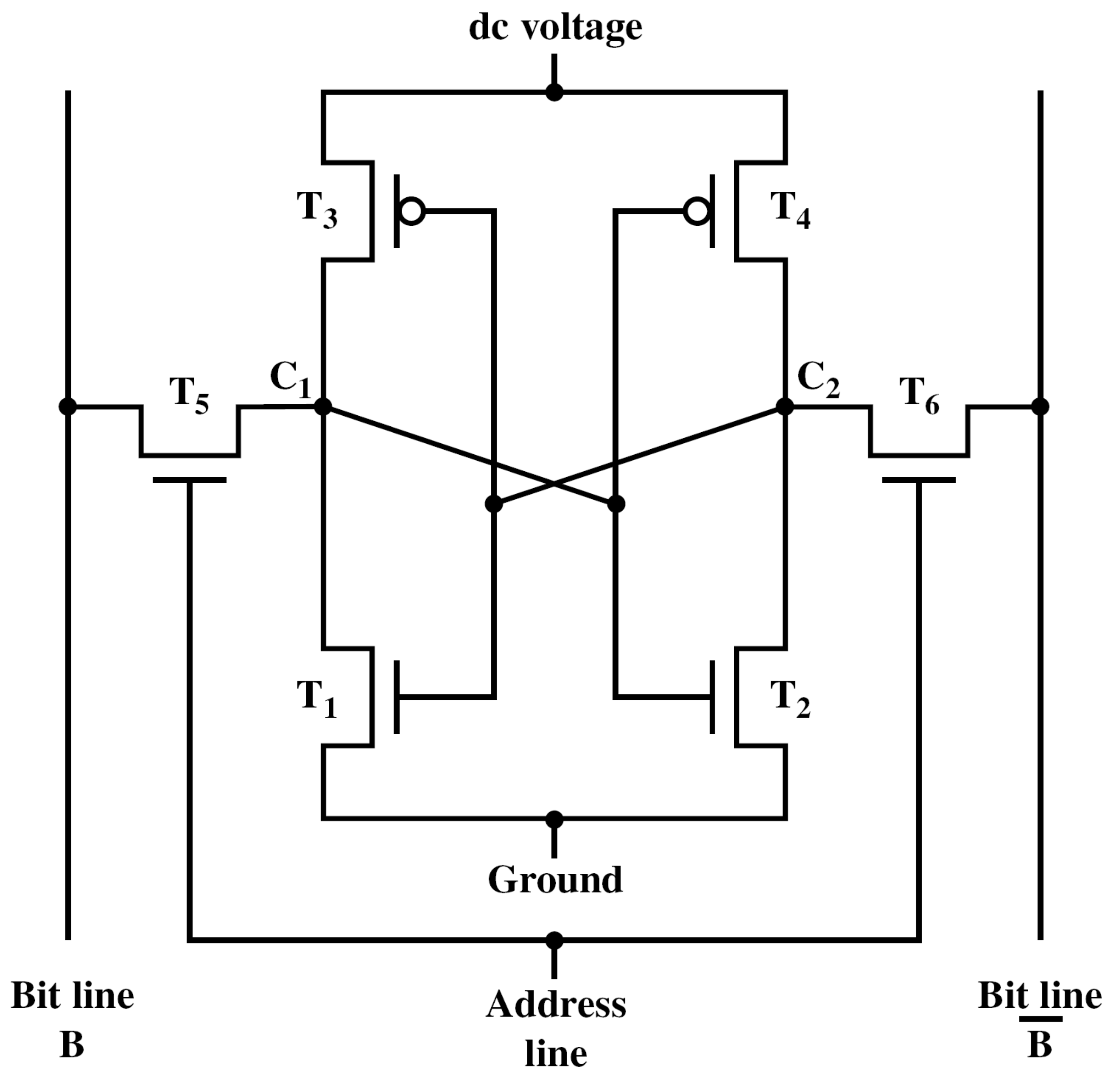
- Address line active when bit read or written.
  - Transistor switch closed (current flows).
- Write
  - Voltage to bit line
    - High for 1 low for 0.
  - Then signal address line
    - Transfers charge to capacitor.
- Read
  - Address line selected
    - transistor turns on.
  - Charge from capacitor fed via bit line to a sense amplifier
    - Compares with threshold/reference value to determine 0 or 1.
  - Readout discharges capacitor ➔ charge must be restored



# Static RAM (SRAM)

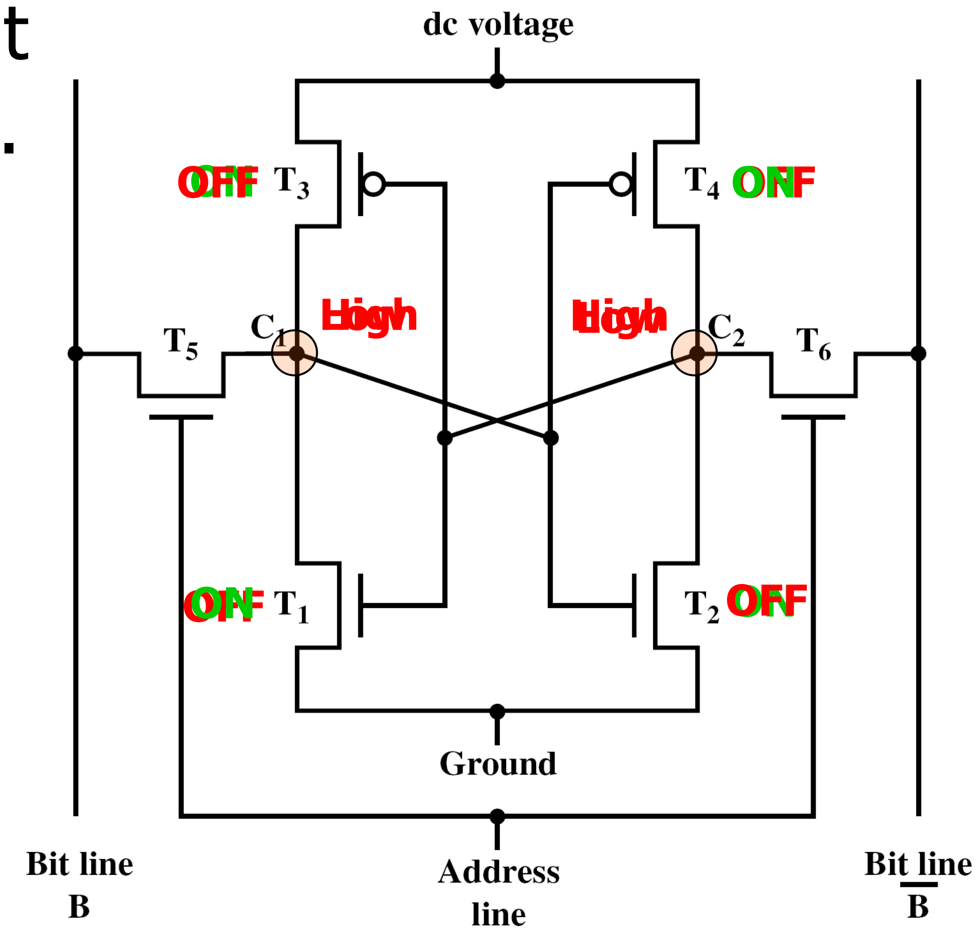
- Bits stored as on/off switches.
- Digital device: uses flip-flops.
- No charges to leak.
- No refreshing needed.
- Pros
  - Does not need refresh circuits.
  - Faster.
- Cons
  - More complex construction.
  - Larger per bit.
  - More expensive.
- Most common usage: cache memory.

# SRAM Structure



# SRAM Operation

- Transistor arrangement gives stable logic state.
- $C_1$ and $C_2$: diff. states
- State 1
  - $C_1$ high, $C_2$ low
  - $T_2$ on, $T_4$ off
  - $T_1$ off, $T_3$ on
- State 0
  - $C_1$ low, $C_2$ high
  - $T_2$ off, $T_4$ on
  - $T_1$ on, $T_3$ off




- Address line transistors $T_5$ $T_6$ are switches.
- Write – apply value to B & compliment to $\overline{B}$.
- Read – value is on line B.

# DRAM vs SRAM

- Both volatile
  - —Power needed to preserve data.
- Dynamic cell
  - —Simpler to build, smaller.
  - —More dense: more cells per unit area.
  - —Less expensive.
  - —Needs refreshment.
  - —Fixed cost of refreshment circuitry ➔ use large memory units to benefit from the small cell cost.
  - —Used in **main memory**.
- Static cell
  - —Faster
  - —Used in **cache memory**.

# Read Only Memory (ROM)

- Permanent storage that cannot be changed.
  - Nonvolatile.
- Can read stored data, cannot write new data.
- Written during fabrication
  - Large fixed cost of data insertion ➔ expensive for small number of copies.
  - No room for error. One bit error ➔ throw the whole batch of ROMs.
- Why useful?
  - Data or program is permanently in main memory and need never be loaded from a secondary storage device.
- Applications
  - Microprogramming.
  - Library subroutines.
  - System programs (BIOS).

# Programmable ROM (PROM)

- Nonvolatile.
- Can be written into only once.
- Writing (or programming):
  - Performed electrically using a special equipment.
    - Writing one ➔ do nothing! (all cells store one by default).
    - Writing zero ➔ blow a fuse (or melt an anti-fuse) in the cell.
  - Performed by supplier or customer (after fabrication).
- Useful when a small number of ROMs with a particular memory content is needed.
- Flexible and convenient.
- ROM is good for high-volume production.

# Erasable Programmable ROM (EPROM)

- Nonvolatile.
- Read-mostly memory: read operations are far more than write operations.
- Read and written electrically.
  - —Before a write operation, all cells must be optically erased to the same initial state.
- Erasure
  - —Done optically by exposure of the packaged chip to ultraviolet radiation.
  - —Takes up to 20 minutes.
  - —Can be done repeatedly.

- One transistor per bit ➔ dense.
- More expensive than PROM, but can do multiple updates.

## Electrically Erasable Programmable ROM (EEPROM)

- Nonvolatile.
- Read-mostly memory.
- Can be written into without erasing prior contents
  - Only the byte/bytes addressed are updated.
- Write operation takes longer than read.
- Flexible: updatable in place using ordinaly bus lines.
- More expensive than EPROM.
- Less dense than EPROM: fewer bits per chip.

# Flash Memory

- Nonvolatile.
- Read-mostly memory.
- First introduced in the mid-1980s.
- Intermediate between EPROM and EEPROM in cost and functionality
  - Like EEPROM, it uses electrical erasing technology.
  - Entire flash memory can be erased in a few seconds ➔ much faster than EPROM.
  - Only a block of memory can be erased.
  - No byte-level erasure.
  - Like EPROM, one transistor per bit ➔ higher density than EEPROM.

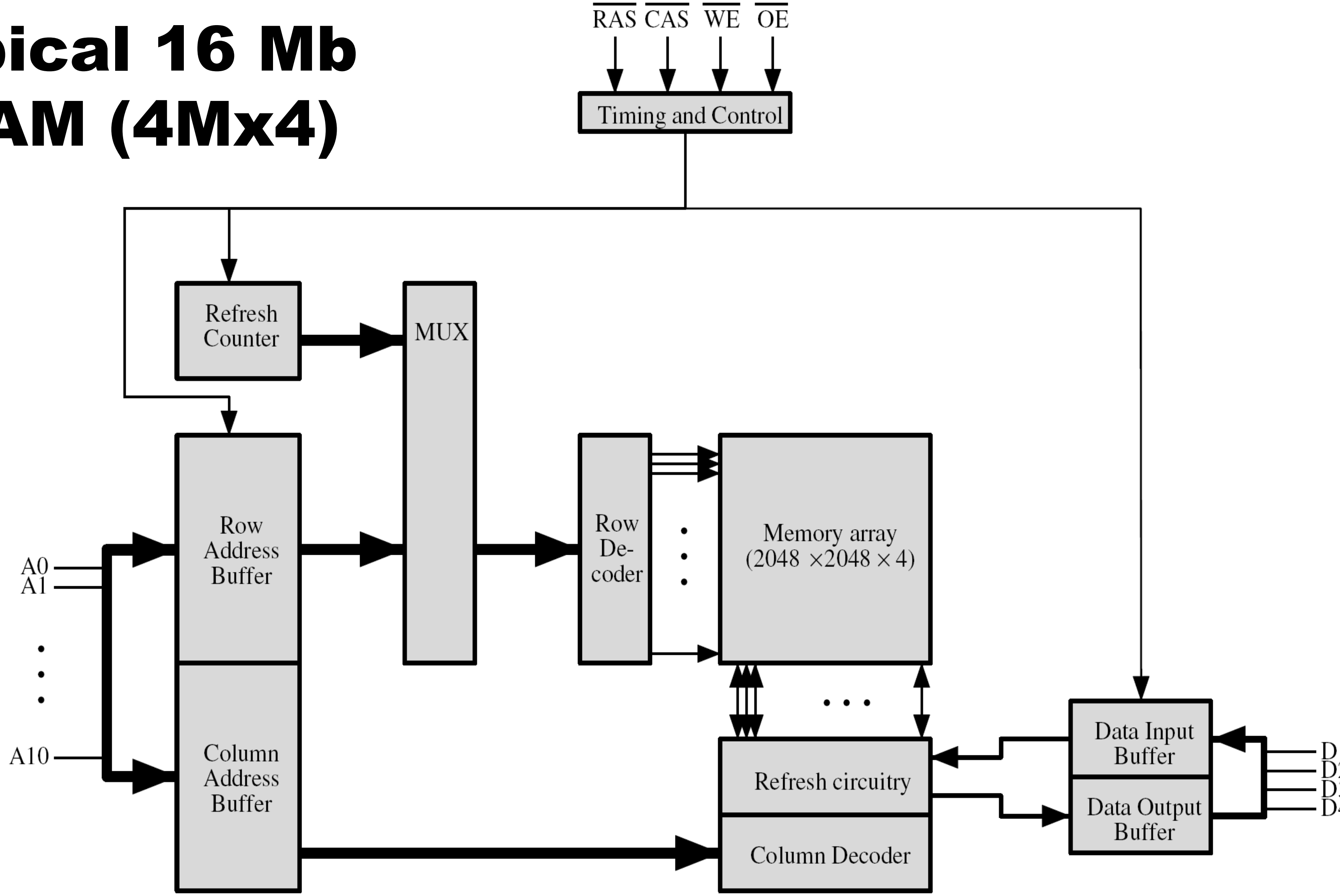
# Semiconductor Memory Types - Summary

| Memory Type | Category | Erasure | Write Mechanism | Volatility |
|---|---|---|---|---|
| Random-access memory (RAM) | Read-write memory | Electrically, byte-level | Electrically | Volatile |
| Read-only memory (ROM) | Read-only memory | Not possible | Masks | Nonvolatile |
| Programmable ROM (PROM) | | | Electrically | |
| Erasable PROM (EPROM) | Read-mostly memory | UV light, chip-level | | |
| Electrically Erasable PROM (EEPROM) | | Electrically, byte-level | | |
| Flash memory | | Electrically, block-level | | |

# Chip Logic

- Semiconductor memory comes in packaged chips.
- Each mem. chip contains an array of memory cells.
- Design issue: number of bits of data that maybe read/written at a time.
  - One extreme: 1-word-per-chip organization: physical arrangement of cells in the array is the same as logical arrangement of words in memory.
    - EX.: 1Mx16 memory = **One** 1Mx16 chip.
  - Other extreme: 1-bit-per-chip organization: data is read/written 1 bit at a time.
    - Ex.: 1Mx16 memory = **sixteen** 1Mx1 chips s.t. chip #1 holds bit #1 of each word, chip #2 holds bit #2 of each word, and so on.

# Typical 16 Mb DRAM (4Mx4)

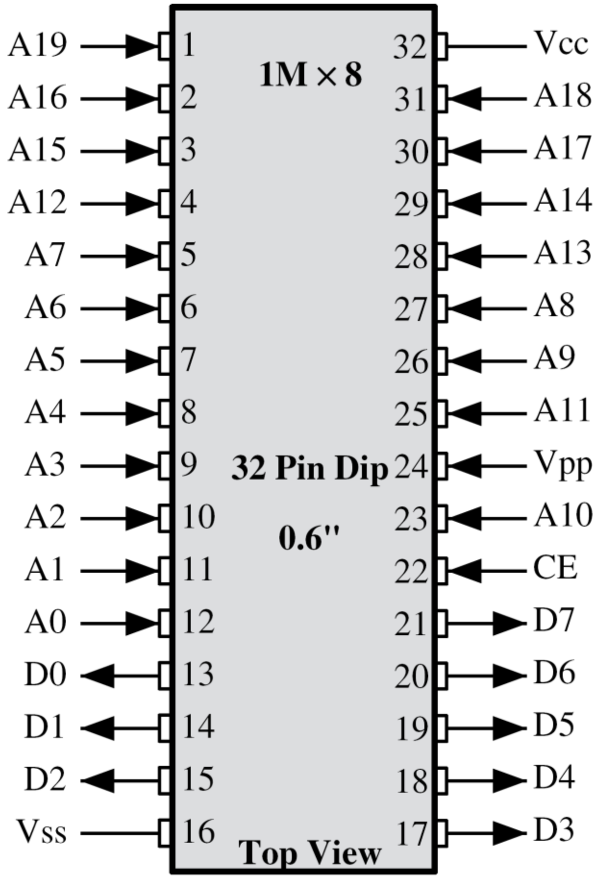



- Logically, 4 square arrays of 2048 x 2048 elements.
- Each horizontal line connects to the Select terminal of each cell in its row.
- Each vertical line connects to the Data in/Sense terminal of each cell in its column.
- Reduces number of address pins
  - Multiplex row address and column address
  - 11 pins to address ($2^{11}$=2048)
  - Adding one more pin doubles range of values so x4 capacity

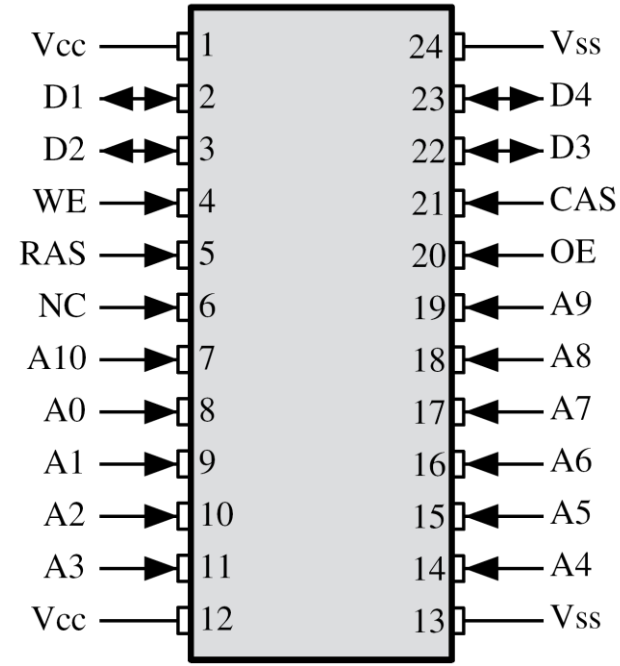
# Refreshing

- Refresh circuit included on chip.
- Disable chip.
- Count through rows.
- Data is read out and written back into the same location ➔ each cell is refreshed.
- Takes time.
- Slows down apparent performance.

# Chip Packaging




(a) 8 Mbit EPROM




(b) 16 Mbit DRAM

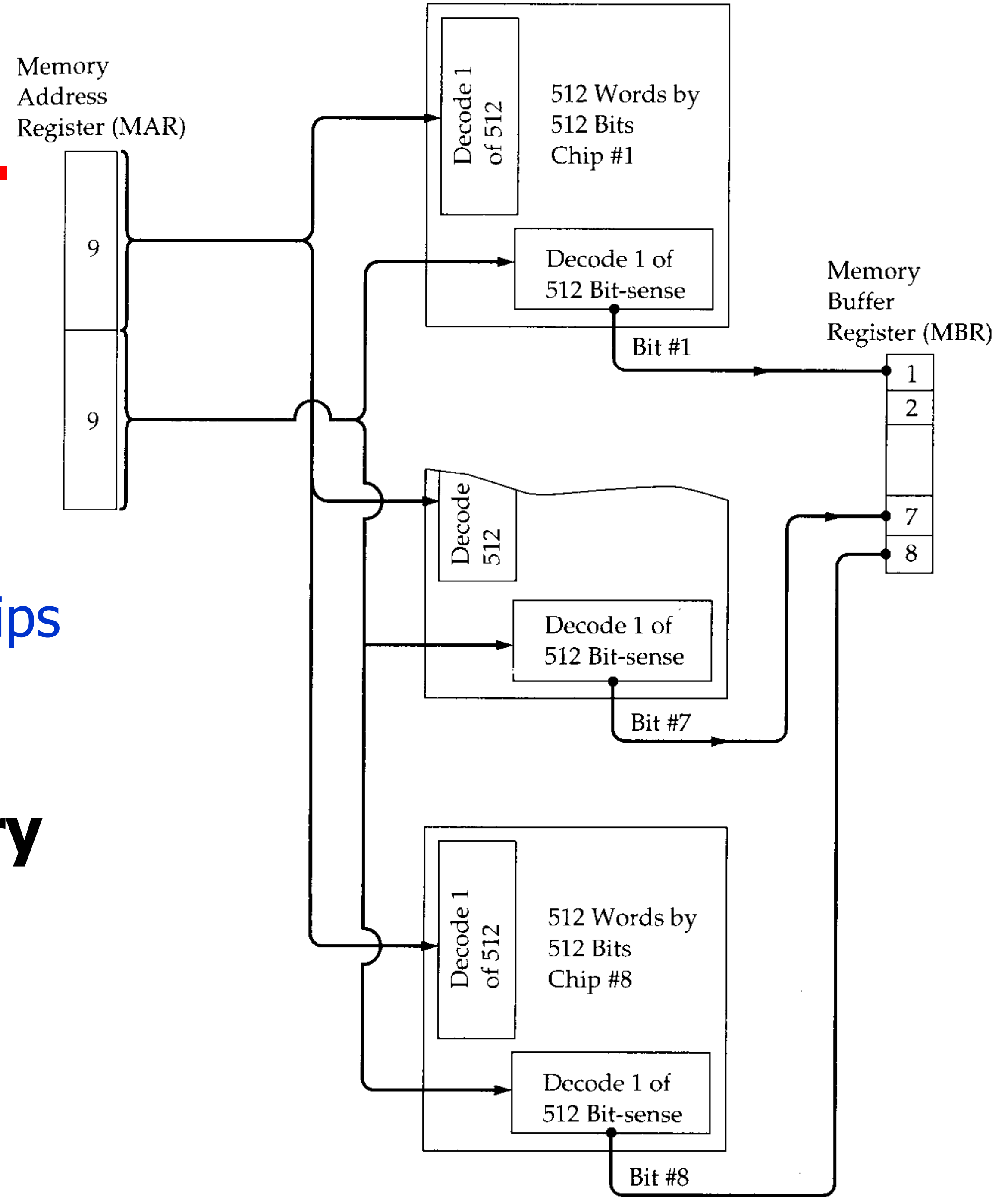
- 8-Mbit EPROM chip, 1M x 8.
- One-word-per-chip package.
- Address: A0-A19, Data: D0-D7
- Vcc: power, Vss: ground, CE: chip enable, Vpp: programming voltage.

- 16-Mbit DRAM, 4M x 4.
- Updatable ➔ data pins in/out.
- WE: Write Enable
- OE: Output Enable
- NC: No Connect ➔ even # of pins

# Module Organization

- Available: 256k x 1 chips

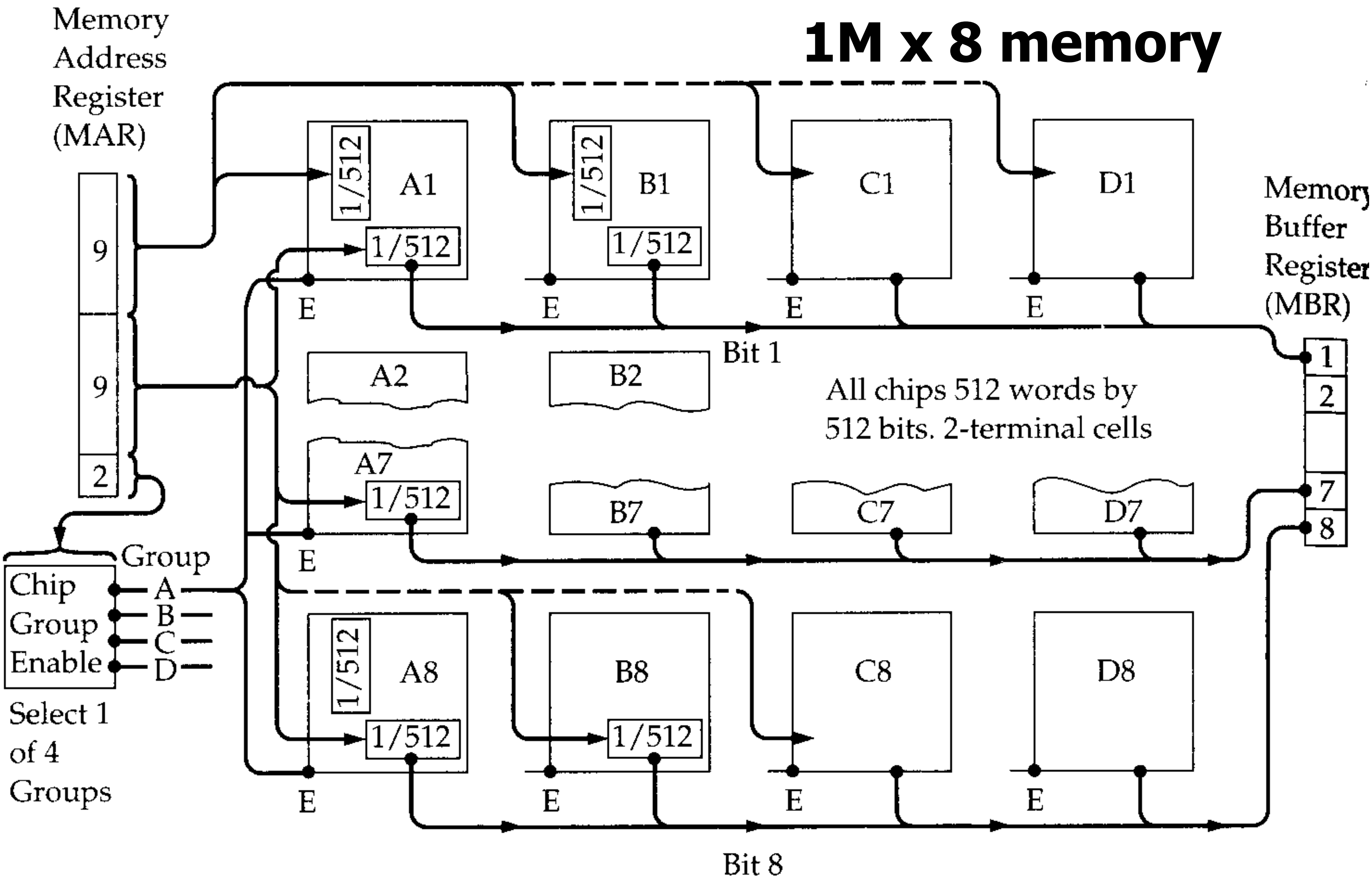
**256k x 8 memory**



# Module Organization (2)

- Available: 256k x 1-bit chips

**1M x 8 memory**



# Reading Material

- Stallings, Chapter 5:
  - Pages 159 – 169