1. A.
$$C = E^*B^*S = 128$$
 bytes

B.
$$CO = b = 2$$
 bits, stored in bits 0 -1
 $CI = s = 3$ bits, stored in bits 2-4
 $CT = m - s - b = 8$ bits, stored in 5-12

2. A. 0 0111 0001 1010

Block offset = 0x2 Index = 0x6 CT = 0x38

Cache Hit? Yes

Byte Returned = EB

3. A. 1 0110 1110 1000

Block offset = 0x0

Index = 0x2

CT = 0xB6

Cache Hit? Yes

Byte Returned = DC

- 4. The 8 addresses that will hit must contain tag B6 or BC and have index bits set to 010. These are 0x16E8, 0x16EA, 0x16E9, 0x16EB, 0x178B, 0x178B, 0x178B
- 5. The cache setup results in misses ¼ of the time.

dst array

	Col 0	Col 1	Col 2	Col 3
Row 0	M	Н	Н	Н
Row 1	M	Н	Н	Н
Row 2	M	Н	Н	Н
Row 3	M	Н	Н	Н

src array

	Col 0	Col 1	Col 2	Col 3
Row 0	М	Н	Н	Н
Row 1	М	Н	Н	Н
Row 2	М	Н	Н	Н
Row 3	М	Н	Н	Н