

Assume: $n = 14$ (virtual), $m = 12$ (physical), $P = 64$ (page size)

- How many Physical Pages are available? $2^{12}/2^6 = 2^6 = 64$
- How many Virtual Pages (Page Table Entries) are available? $2^{14}/2^6 = 2^8 = 256$
- For a virtual address, mark bits with VPN or VPO:



- For a physical address, mark bits with PPN or PPO:



- Given the virtual address 0x03d4, what are the:

0000 0011 1101 0100

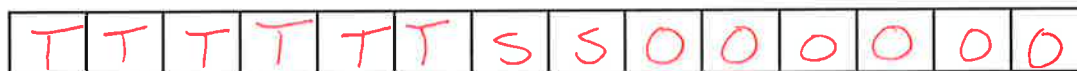
- VPN: 0x0F
- VPO: 0x14
- PPN: 0x00
- PPO: 0x14
- Physical Address:
1101010100
0x354

Page Table (first 16 entries)

| VPN | PPN | valid | VPN | PPN | valid |
|-----|-----|-------|-----|-----|-------|
| 00 | 28 | 1 | 08 | 13 | 1 |
| 01 | -- | 0 | 09 | 17 | 1 |
| 02 | 33 | 1 | 0A | 09 | 1 |
| 03 | 02 | 1 | 0B | -- | 0 |
| 04 | -- | 0 | 0C | -- | 0 |
| 05 | 16 | 1 | 0D | 2D | 1 |
| 06 | -- | 0 | 0E | 11 | 1 |
| 07 | -- | 0 | 0F | 0D | 1 |

Now we recognize that we must actually use a TLB to access the PPN. Assume the TLB is 4-way set associative with 16 total entries.

- For a virtual address, mark bits with Offset, TLB Set Index, or TLB Tag



- Given the virtual address 0x03d4, what are the:

- TLB Tag: 0x3
- TLB Set: 0x3
- TLB Offset: 0x14

TLB: 4-way, 16 entries, 4 sets

| set | tag | PPN | valid | tag | PPN | valid | tag | PPN | valid | tag | PPN | valid |
|-----|-----|-----|-------|-----|-----|-------|-----|-----|-------|-----|-----|-------|
| 0 | 03 | -- | 0 | 09 | 0D | 1 | 00 | -- | 0 | 07 | 02 | 1 |
| 1 | 03 | 2D | 1 | 02 | -- | 0 | 04 | -- | 0 | 0A | -- | 0 |
| 2 | 02 | -- | 0 | 08 | -- | 0 | 06 | -- | 0 | 03 | -- | 0 |
| → 3 | 07 | -- | 0 | 03 | 0D | 1 | 0A | 34 | 1 | 02 | -- | 0 |

- Given the current TLB state (next page), is the address 0x03d4 in the TLB (yes/no)?
- What are the: *generated*
 - PPN: 0x0D
 - PPO: 0x14
 - Physical Address: 0x354

Now assume the L1 cache is DM with 16 entries and 4-byte blocks

- For a physical address, mark bits with Offset, L1 Set Index, or L1 Tag

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| T | T | T | T | T | T | S | S | S | S | O | O |
|---|---|---|---|---|---|---|---|---|---|---|---|

L1 cache: DM, 4-byte block, 16 sets

- What are the L1 Tag, Set, and Offset associated with the physical address generated above?

- Tag: 0x0
- Set: 0x5
- Offset: 0x0

- Is the memory in cache (yes/no)?

- What value is returned given that memory accesses are to 1-byte words?

0x36

| set | tag | valid | blk0 | blk1 | blk2 | blk3 |
|-----|-----|-------|------|------|------|------|
| 0 | 19 | 1 | 99 | 11 | 23 | 11 |
| 1 | 15 | 0 | -- | -- | -- | -- |
| 2 | 1B | 1 | 0 | 2 | 4 | 8 |
| 3 | 36 | 0 | -- | -- | -- | -- |
| 4 | 32 | 1 | 43 | 6D | 8F | 9 |
| → 5 | 0D | 1 | 36 | 72 | F0 | 1D |
| 6 | 31 | 0 | -- | -- | -- | -- |
| 7 | 16 | 1 | 11 | C2 | DF | 3 |
| 8 | 24 | 1 | 3A | 0 | 51 | 89 |
| 9 | 2D | 0 | -- | -- | -- | -- |
| 10 | 2D | 1 | 93 | 15 | DA | 3B |
| 11 | 0B | 0 | -- | -- | -- | -- |
| 12 | 12 | 0 | -- | -- | -- | -- |
| 13 | 16 | 1 | 4 | 96 | 34 | 15 |
| 14 | 13 | 1 | 83 | 77 | 1B | D3 |
| 15 | 14 | 0 | -- | -- | -- | -- |