

Mémoire

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graph TD; Mem[Mémoire] <--> UC[Unité de Contrôle]; Mem <--> UAL[Unité Arithmétique et Logique]; subgraph CPU; UC <--> UAL; end; In[Entrées] --> UC; UAL --> Out[Sorties];
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The diagram illustrates the basic components of a computer system and their interactions. At the top is a light gray rectangular block labeled 'Mémoire' (Memory). Below it is a larger light gray rectangular block labeled 'CPU' on its right side. Inside the CPU block are two dark gray rectangular blocks: 'Unité de Contrôle' (Control Unit) on the left and 'Unité Arithmétique et Logique' (Arithmetic and Logic Unit) on the right. These two units are connected by a horizontal double-headed arrow. Below the CPU block are two light gray rectangular blocks: 'Entrées' (Inputs) on the left and 'Sorties' (Outputs) on the right. An upward-pointing arrow connects 'Entrées' to the 'Unité de Contrôle', and a downward-pointing arrow connects the 'Unité Arithmétique et Logique' to 'Sorties'. Additionally, vertical double-headed arrows connect the 'Mémoire' block to both the 'Unité de Contrôle' and the 'Unité Arithmétique et Logique'.

Unité
de
Contrôle

Unité
Arithmétique
et
Logique

CPU

Entrées

Sorties