Hsien-Hsin Sean Lee, Ph.D.

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https://hsienhsinlee.github.io/ LinkedIn Profile

EDUCATION

Massachusetts Institute of Technology, Cambridge, MA, USA
Executive MBA, MIT Sloan School of Management Exp. 2026

University of Michigan, Ann Arbor, MI, USA
Ph.D. in Computer Science and Engineering 2001
M.S.E. in Computer Science and Engineering 1994
Horace H. Rackham Distinguished Dissertation Award, University of Michigan.
Nominated by University of Michigan for ACM Doctoral Thesis Award.

National Tsing-Hua University, Hsinchu, Taiwan
B.S. in Electrical Engineering 1990
Valedictorian of the Class 1990

EMPLOYMENT

Intel Corporation, MA
Intel Fellow (Technology VP), System Architecture & Engineering, Office of the CTO Aug 2022 - Present

- Advanced development for future AI/ML workload-driven accelerators, heterogeneous datacenter architectures, system software stack, and performance/power optimization with emerging technologies.
- Development of dynamic auto-tuning and optimization framework.
- Benchmarking, pre-silicon simulation and PnP projection methodology and corporate strategy.
- Technology incubation for Confidential AI systems.

Meta / Facebook, Inc., Cambridge, MA
SysML Area Research Lead, Facebook AI Research (FAIR) March 2020 - Aug 2022
Research Lead, AI Infrastructure Research Jan 2019 - Feb 2020

- Built a new research team from scratch, specializing in Systems for ML at Facebook Boston site.
- High-efficiency personalized recommendation system designs.
- Processing-near-memory and emerging memory technology pathfinding for AI workloads.
- Sustainable, carbon-aware computing and machine learning.
- Privacy-preserving and secure machine learning.
- Academic research engagement with universities worldwide.

Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC), Hsinchu, Taiwan
Deputy Director, Design Methodology and Kits Development Division April 2012 - Jan 2019

- Directed 6 departments (155 R&D staff across Taiwan, China, and US) developing IC design methodology, EDA tool features, and process design kits (PDK) for all TSMC customers.
- Led the IC design ecosystem enablement across TSMC R&D, EDA partners (Synopsys, Cadence, Mentor, ANSYS, etc.), and fabless design houses.
- Technology owner of design collateral for all TSMC process nodes and integration/packaging technologies (2.5D/3DIC).
- Technology owner of EDA tool certification programs for physical design sign-off tools, custom design flow, and SPICE simulators.

- Technology owner of machine learning applications to improve the quality of physical verification.

Georgia Institute of Technology, Atlanta, GA
Associate Professor (Tenured), School of Electrical and Computer Engineering July 2008 - June 2014
Assistant Professor, School of Electrical and Computer Engineering Aug 2002 - June 2008

- Green data centers (NSF, State of Georgia.)
- 3D-IC architecture, design-for-test, physical design, & prototyping (DoD, NSF, SRC MARCO centers.)
- Emerging memory architecture (IBM, Intel.)
- Transactional memory and speculative multithreading (NSF.)
- Secure processor architecture (NSF, DoE.)
- FPGA-based accelerators and system-wide monitoring (NSF.)
- Initiated a GT course on Multicore and GPU programming for video games.
- Adjunct faculty member of joint degree programs at Shanghai Jiao Tong University (2011) and Korea University (2008-2010.)

Agere Systems, Atlanta, GA
Architecture Manager, StarCore DSP Technology Center (Agere and Motorola) July 2001 - August 2002

- Managed 10 CPU/DSP architects from Lucent/Agere and Motorola.
- Led development of a 1GHz StarCore DSP architecture for 3G infrastructure, including the VLES ISA, architecture simulators, and performance benchmarking.

Intel Corporation, CA
Researcher, Programming Systems Lab, Microprocessor Research Labs May 1999 - July 2001
Senior Processor Architect, Microprocessor Division 6 October 1995 - April 1999

- Pathfinding for next-generation IA64/EPIC architecture.
- Performance architect for Katmai (Pentium-III) and Timna (integrated CPU/GPU.)
- Coded and optimized Microsoft Direct3D 6.1 API using SSE ISA (at assembly level.)
- Owner of Intel 3D Graphics Geometry Performance Roadmap.
- Pentium III SSE/prefetch instruction definition and microarchitecture development.
- Pentium III post-silicon validation.

HONOR AND AWARDS

- **IEEE Fellow**, Class of 2017. *Citation: for Contributions to 3D Integrated Circuits and Computer Architecture.*
- 10-year Most Significant Paper Award. *International Test Conference (ITC)*, 2017. (Paper 3D19)
- MICRO Hall of Fame, ACM/IEEE International Symposium on Microarchitecture.
- HPCA Hall of Fame, IEEE International Symposium on High Performance Computer Architecture.
- Top Picks. IEEE Micro Top Picks from the Computer Architecture Conferences of 2010, 2022. (Paper MM5, ML6, ML14)
- Honorable Mention. IEEE Micro Top Picks from the Computer Architecture Conferences of 2020, 2021. (Paper ML19, ML23)
- Class of 1934 Course Survey Teaching Effectiveness Award, Georgia Tech, 2012.
- Best Paper Award. *The ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS 2011)*, NY, 2011. (Paper SA1)
- IBM Faculty Award, 2011.
- NSF CAREER Award, 2007.
- ECE Outstanding Junior Faculty Award, Georgia Tech, 2006.

- Department of Energy Early CAREER Principal Investigators Award, 2005.
- Best Paper Award. *The 2nd Watson Conference on Interaction Between Architecture, Circuits and Compilers ($P = AC^2$)*, NY, 2005. (Paper uA5)
- Best Paper Award. *The 2004 ACM/IEEE International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES-2004)*, Washington DC, 2004. (Paper SA19)
- Horace H. Rackham Distinguished Dissertation Award, University of Michigan, 2001.
- Best Paper Award. *The 33rd ACM/IEEE International Symposium on Microarchitecture (MICRO-33)*, Monterey, CA, 2000. (Paper MM12)
- Intel Foundation Fellowship, 2000-2001.
- University of Michigan Research Fellowship, 1993.
- Valedictorian of the Class 1990, National Tsing-Hua University, 1990.
- Chancellor Mei Yi-Chi Memorial Award, National Tsing-Hua University, 1989.

RESEARCH SUPERVISION

Ph.D. Dissertation Supervised

- **Joshua Bruce Fryman**, *SoftCache Architecture*, College of Computing, Georgia Institute of Technology, (Co-advised with Umakishore Ramachandran), August 2005. Current position: **Intel Fellow at Intel Corp**, Hillsboro, OR.
- **Weidong Larry Shi**, *Architectural Support for Protecting memory Integrity and Confidentiality*, College of Computing, Georgia Institute of Technology, April 2006. Current position: **Associate Professor**, Computer Science Department, **University of Houston**, Houston, TX.
- **Taeweon Suh**, *Integration and Evaluation of Cache Coherence Protocols for Multiprocessor SOCs*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2006. Current position: **Professor**, Department of Computer Science and Engineering, **Korea University**, Seoul, South Korea.
- **Kiran Puttaswamy**, *Designing High-Performance Microprocessors in 3-D Integration Technology*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (Co-advised with Gabriel Loh), December 2007. Current position: DV Lead at CPU Condor Computing Corporation, Austin, TX.
- **Chinnakrishnan Ballapuram**, *Semantic-Oriented Low Power Architecture*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2008. Current position: **Senior Director at Western Digital**, CA.
- **Mrinmoy Ghosh**, *Microarchitectural Techniques to Reduce Energy Consumption in the Memory Hierarchy*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2009. Current position: Senior Principal Engineer at Samsung, San Jose, CA.
- **Dong Hyuk Woo**, *Designing Heterogeneous Many-Core Processors to Provide High Performance Under Limited Power Budget*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2010. Current position: **Senior Vice President at Samsung**, San Jose, CA.
- **Nak Hee Seong**, *A Reliable, Secure Phase-Change Memory as Main Memory*, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2012. Current position: **Vice President at Samsung Electronics**, S. Korea.
- **Dean L. Lewis**, *Design for Pre-bond Testability in 3D Integrated Circuits*, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2012. Current position: Test and Characterization Engineer at IBM, Burlington, VT.

- **Jen-Cheng Huang**, *Efficient Simulation Techniques for Large-scale Applications*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (Co-advised with Hyesoon Kim), 2015. Current position: Computer Architect at Nvidia, CA.
- **Sungkap Yeo**, *Holistic Power Optimization for Datacenters*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (defense chaired by Tom Conte after I left), 2015. Current position: Software Engineer at Google, Pittsburgh, PA.

Master's Thesis Supervised

- Prateek Tandon, *High-Performance Advanced Encryption Standard (AES) Security Co-Processor Design*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2003. Current position: Principal Software Engineer, Microsoft, Seattle, WA.
- Aniket Naik, *Efficient Conditional Synchronization for Transactional Memory Based System*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (Co-advised with Milos Prvulovic), August 2006. Current position: Engineering Manager, Nvidia Corporation, Santa Clara, CA.
- **Fayez Mohamood**, *DLL-conscious Instruction Fetching for SMT Processors*, School of Electrical and Computer Engineering, Georgia Institute of Technology, August 2006. Current position: **Founder and CEO, Bluecore**, New York, NY.
- Richard M. Yoo, *Adaptive Transaction Scheduling for Transactional Memory Systems*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2008. Current position: **Chief Technology Officer at Lunit**, Seoul, South Korea.
- Pratik Marolia, *Watermarking FPGA Bitstream for IP Protection*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2008. Current position: Software Engineer at Google, Mountain View, CA.
- Vikas Rangaswamy Vasisht, *Architectural Support for Autonomic Protection Against Stealth by Rootkit Exploits*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2008. Current position: Performance Architect, Rivos, Inc., Austin, TX.
- Manoj Balanageswaran Athreya, *Subverting Linux On-the-fly using Hardware Virtualization Technology*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2010. Current position: Engineer, Apple, Cupertino, CA.

Undergraduate Researchers Supervised

- **Ilya (Khorosh) Tillis**, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2011. Current position: **Director of Product Development, Google**.
- Xiaodong Wang, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2011. Current position: Research Scientist, Facebook, Menlo Park, CA.
- Gregory Diamos, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2006. Current position: **Founder and CTO of, Lamini AI**, Palo Alto, CA.
- **June Paik** (Joonho Baek), School of Electrical and Computer Engineering, Georgia Institute of Technology, 2006. Current position: **Founder and CEO, Furiosa AI**, Seoul, Korea.
- Anirudh Saria, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2004. Current position: Senior Program Manager, Microsoft, Redmond, WA.

PROFESSIONAL SERVICE

Professional Community

- Industry Advisory Board Member, Department of Computer Science, University of Central Florida, 2021 - Present.
- IEEE Fellows Committee, 2018, 2019.

- Search Committee Chair for IEEE Micro Editor-in-Chief, 2018.
- Executive Committee Member, IEEE Technical Committee on Computer Architecture, 2017 - 2019.
- Industry Advisory Board Member, IEEE Computer Society, 2016 - Present.

Editorial Boards

- Editorial-in-Chief, *IEEE Micro Magazine*, 2024 - Present.
- Editorial Board Member, *IEEE Micro Magazine*, 2016 - 2023.
- Guest Editor, *IEEE Micro Special Issue on Commercial Products*, 2021.
- Guest Editor, *IEEE Micro Special Issue on Automotive Computing*, 2018.
- Associate Editor, *IEEE Transactions on Computers (IEEE TC)*, 2012 - 2015.
- Associate Editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, 2010 - 2013.
- Associate Editor, *ACM Transactions on Architecture and Code Optimization (ACM TACO)*, 2009 - 2015.

Major Conference/Workshop Organizers

- Program Subcommittee Chair, AI/ML System and Platform Design, *Design Automation Conference (DAC)*, 2023, 2024, 2025.
- Program Track Chair, Hardware Systems and Architectures for Artificial Intelligence, *International Conference on Computer-Aided Design (ICCAD)*, 2023.
- Program Co-Chair, *IEEE International Symposium on Secure and Private Execution Environment Design (SEED)*, 2022.
- Program Chair of Industry Track, *the 48th ACM/IEEE International Symposium on Computer Architecture (ISCA-48)*, Valencia, Spain, 2021.
- Program Co-Chair, *the 49th ACM/IEEE International Symposium on Microarchitecture (MICRO-49)*, Taipei, Taiwan, 2016.
- Workshop Co-Organizer, *the CLEAR Workshop on Computing Landscapes for Environmental Accountability and Responsibility collocated with ISCA-48*, 2021.
- Workshop Co-Chair, *International Workshop on Parallelism in Mobile Platforms (PRISM) collocated with ISCA*, 2013-2018.
- Steering Committee, *the IEEE International Symposium on Workload Characterization (IISWC 2011)*, 2011-Present.
- General Chair, *the IEEE International Symposium on Workload Characterization (IISWC 2010)*, Atlanta, GA, 2010.
- Tutorial and Workshop Chair, *the 43rd International Symposium on Microarchitecture (MICRO-43)*, Atlanta, GA, 2010.

Major Technical Program Committee

I served as a program committee member for more than 100 conferences and workshops. Highlights are:

- IEEE MICRO Top Picks: 2013, 2014, 2016, 2017, 2018.
- International Symposium on Computer Architecture (ISCA): 2006, 2008, 2012, 2014, 2015, 2018, 2019, 2020, 2021 (PC Chair, Industry Track)
- International Symposium on Microarchtiecture (MICRO): 2010, 2014, 2015, 2016 (Program Co-Chair), 2020, 2021.
- International Conference on High-Performance Computer Architecture (HPCA): 2007, 2016, 2021.

- International Conference on Compiler, Architectures, Synthesis for Embedded Systems (CASES): 2004, 2005, 2006, 2007, 2008.
- International Conference on Computer Design (ICCD): 2005, 2006, 2007, 2008, 2009, 2011, 2012.
- Design, Automation and Test in Europe (DATE): 2013, 2014, 2015.
- Asia and South Pacific Design Automation Conference (ASP-DAC): 2012, 2013, 2014.

Keynote Speeches and Key Conference Panelists

- Plenary Speaker: "Technological Challenges of Social Network Computing" in *International Conference on Electronics, Information, and Communication*, Jeju, Korea, 2022.
- IEDM Panelist: "Is Hardware/Software Co-design a Necessary Evil of Symbiotic Partner" in *the 67th Annual IEEE International Electron Devices Meeting*, 2021.
- Keynote Speech: "Challenges of Modern Computing on Social Network Platform" in *Research Summit at the Center for Unstoppable Computing*, University of Chicago, 2021.
- NSF Keynote Speech: "When Memory Meets ML on Social Network Platform" in *NSF Workshop on Processing-In-Memory Technology*, National Science Foundation, 2021.
- ARM DevSummit 2001 Panelist: "How Edge AI is Reshaping the World Now and in the Near Future" in ARM DevSummit 2021. (with David Hsu, Odin Shen, Wei-Fen Lin.)
- ISCA Panelist: "Data Center Architecture" in *the 47th ACM/IEEE International Symposium on Computer Architecture (ISCA-47)*, 2020. (with David Brooks and Christina Delimitrou.)
- ECE Distinguished Lecture Series: "Machine Learning on Social Network Platform" in George Washington University, Washington D.C., 2020.
- CASPA Keynote Speech: "The Computing Frontiers of Social Network" in *Chinese American Semiconductor Professional Association(CASPA) 2019 Annual Conference*, Fremont, CA, 2019.
- ISPLED Keynote Speech: "The Computing Frontiers of Social Network" in *ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED-2019)*, Lausanne Switzerland, 2019.
- DAC Panelist: "Will the Era of AI Drive Emerging Technologies to Overtake CMOS?" in *Design Automation Conference (DAC-55)*, San Francisco, CA, 2018. (with An Chen, Geoffrey Burr, Meng-Fan Marvin Chang, and Kaushik Roy.)
- ISSCC Panelist: "Can Artificial Intelligence Replace My Job? The Dawn of a New IC Industry with AI" in *International Solid-State Circuits Conference (ISSCC-2018)*, San Francisco, CA, 2018. (with Bill Dally, Georges Gielen, Antun Domic, Seung Hoon Tong, and Dario Gil.)
- ISCA Panelist: "Is the Death of Moore's Law Making Computer Architecture Livelier Than Ever?" in *the 44th ACM/IEEE International Symposium on Computer Architecture (ISCA-44)*, Toronto, Canada, 2017. (with Mark Hill, Sandhya Dwarkadas, and Babak Falsafi.)
- ISSCC Forum Speaker: "Ecosystem of Design for Security" in *Design Forum of Designing Secure Systems: Manufacturing, Circuits and Architectures, International Solid-State Circuits Conference (ISSCC-2016)*, San Francisco, CA, 2016.
- Distinguished Speaker Colloquium, "3D Integration" in *the Computer & Information Science & Engineering Department*, University of Florida, Gainesville, FL, March 5, 2010.

SCHOLARLY ACCOMPLISHMENTS

Invention Disclosure

I hold **42 US issued patents** in the areas of memory subsystem, secure non-volatile memory, 3D-IC, and physical design.

Publication (by areas)

[3DIC Design and Test]

3D1. Tianjian Li, Yan Han, Hsien-Hsin S. Lee, and Li Jiang. "Fault Clustering Technique for 3D Memory BISR," In *ACM/IEEE Design Automation & Test in Europe*, Lausanne, Switzerland, March, 2017.

3D2. Daehyun Kim, Krit Athikulwongse, Michael B. Healy, Mohammad M. Hossain, Moongon Jung, Ilya Khorosh, Gokul Kumar, Young-Joon Lee, Dean L. Lewis, Tzu-Wei Lin, Chang Liu, Shreepad Panth, Mohit Pathak, Minzhen Ren, Guanhao Shen, Taigon Song, Dong Hyuk Woo, Xin Zhao, Joungho Kim, Ho Choi, Gabriel H. Loh, Hsien-Hsin S. Lee, Sung Kyu Lim. "Design and Analysis of 3D-MAPS (3D Massively Parallel Processor with Stacked Memory." In *IEEE Transactions on Computers*, 64(1), pp.112-125, 2015.

3D3. Dong Hyuk Woo, Nak Hee Seong, and Hsien-Hsin S. Lee. "Pragmatic Integration of An SRAM Row Cache in Heterogeneous 3D DRAM Architecture using TSV." In *IEEE Transactions on Very Large Scale Integrated Circuits and Systems*, Vol.21, No.1, pp.1-13, January 2013.

3D4. Dae Hyun Kim, Krit Athikulwongse, Michael B. Healy, Mohammad M. Hossain, Moongon Jung, Ilya Khorosh, Gokul Kumar, Young-Joon Lee, Dean L. Lewis, Tzu-Wei Lin, Chang Liu, Shreepad Panth, Mohit Pathak, Minzhen Ren, Guanhao Shen, Taigon Song, Dong Hyuk Woo, Xin Zhao, Joungho Kim, Ho Choi, Gabriel H. Loh, Hsien-Hsin S. Lee, and Sung Kyu Lim. "3D-MAPS: 3D Massively Parallel Processor with Stacked Memory." In *Technical Digest of the IEEE International Solid-State Circuits Conference (ISSCC)*, pp.188 - 190, San Francisco, CA, 2012.

3D5. Hong Jun Choi, Young Jin Park, Hsien-Hsin Lee, and Cheol Hong Kim. "Adaptive Dynamic Frequency Scaling for Thermal-Aware 3D Multi-core Processors." In the *Proceedings of the 12th International Conference on Computational Science and Its Applications*, pp.602-612, Salvador de Bahia, Brazil, 2012.

3D6. Xiaodong Wang, Dilip Vasudevan, and Hsien-Hsin S. Lee. "Global Built-In Self-Repair for 3-D Memories with Redundancy Sharing and Parallel Testing." In *IEEE International 3D System Integration Conference (3DIC-12)*, Osaka, Japan, 2012.

3D7. Dean L. Lewis, Shreepad Panth, Xin Zhao, Sung Kyu Lim, and Hsien-Hsin S. Lee. "Designing 3D Test Wrappers for Pre-bond and Post-bond Test of 3D Embedded Cores." In *Proceedings of the XXIX IEEE International Conference on Computer Design (ICCD-11)*, pp.90 - 95, University of Massachusetts, Amherst, USA, October, 2011.

3D8. Xin Zhao, Dean Lewis, Hsien-Hsin S. Lee, and Sung Kyu Lim, "Low-Power Clock Tree Design for Pre-Bond Testing of 3D Stacked ICs." In *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol.30, No.5, pp.732-745, 2011.

3D9. Dong Hyuk Woo, Nak Hee Seong, and Hsien-Hsin S. Lee. "Heterogeneous Die Stacking of SRAM Row Cache and 3-D DRAM: An Empirical Design Evaluation." In *Proceedings of the 54th IEEE International Midwest Symposium on Circuits and Systems*, pp.1 - 4, Seoul, Korea, August, 2011. (An invited paper.)

3D10. Dong Hyuk Woo, Nak Hee Seong, Dean L. Lewis, and Hsien-Hsin S. Lee. "An Optimized 3D-Stacked Memory Architecture by Exploiting Excessive, High-Density TSV Bandwidth." In *Proceedings of the 16th IEEE International Symposium on High-Performance Computer Architecture (HPCA-16)*, pp.429-440, Bangalore, India, January, 2010. (Acceptance rate = 18%)

3D11. Michael B. Healy, Krit Athikulwongse, Rohan Goel, Mohammad M. Hossain, Dae Hyun Kim, Young-Joon Lee, Dean L. Lewis, Tzu-Wei Lin, Chang Liu, Moongon Jung, Brian Ouellette, Mohit Pathak, Hemant Sane, Guanhao Shen, Dong Hyuk Woo, Xin Zhao, Gabriel H. Loh, Hsien-Hsin S. Lee, and Sung Kyu Lim. "Design and Analysis of 3D-MAPS: A Many-Core 3D Processor with Stacked Memory." In *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, California, September, 2010.

3D12. Dean Lewis, Michael Healy, Mohammad Hossain, Tzu-Wei Lin, Mohit Pathak, Hemant Sane, Sung Kyu Lim, Gabriel Loh, and Hsien-Hsin S. Lee. "Design and test of 3D-MAPS, a 3D Die-Stack Many-Core Processor." In *the First IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits (poster)*, Austin, Texas, November, 2010.

3D13. Hsien-Hsin S. Lee and Krishnendu Chakrabarty. "Test Strategies for 3D Integrated Circuits." In *IEEE Design & Test of Computers, Special Issue on 3D IC Design and Test*, vol.26, no.5, pp.26-35, September/October, 2009.

3D14. Xin Zhao, Dean L. Lewis, Hsien-Hsin S. Lee, and Sung Kyu Lim. "Pre-bond Testable Low-Power Clock Tree Design for 3D Stacked ICs" In *Proceedings of the 2009 International Conference on Computer-Aided Design (ICCAD-09)*, pp.184-190, San Francisco, CA, November, 2009. (**Nominated for the Best Paper Award.**)

3D15. Dean L. Lewis and Hsien-Hsin S. Lee. "Architectural Evaluation of 3D Stacked RRAM Caches" In *Proceedings of the IEEE International 3D Systems Integration Conference (3DIC-09)*, pp.1-4. San Francisco, CA, September, 2009.

3D16. Dean L. Lewis and Hsien-Hsin S. Lee. "Testing Circuit-Partitioned 3D IC Designs." In *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI-09)*, pp.139-144, Tampa, FL, May, 2009.

3D17. Dean L. Lewis, Sudhakar Yalamanchili, and Hsien-Hsin S. Lee. "High Performance Non-blocking Switch Design in 3D Die-Stacking Technology." In *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI-09)*, pp.25-30, Tampa, FL, May, 2009.

3D18. Dong Hyuk Woo, Joshua B. Fryman, Allan D. Knies, Marsha Eng, and Hsien-Hsin S. Lee. "POD: A 3D-integrated Broad-Purpose Acceleration Layer." In *IEEE MICRO special issue on Accelerator Architectures*, pp.28-40, July/August, 2008.

3D19. Dean L. Lewis, and Hsien-Hsin S. Lee, "A Scan-Island Based Design Enabling Pre-bond Testability in Die-Stacking Microprocessors." In *Proceedings of the International Test Conference (ITC 2007)*, pp. 1-8, Santa Clara, CA, October, 2007. (**ITC-2017 10-year Most Significant Paper Award**)

3D20. Michael Healy, Mario Vittes, Mongkol Ekpanyapong, Chinnakrishnan Ballapuram, Sung Kyu Lim, Hsien-Hsin S. Lee, and Gabriel H. Loh, "Multi-Objective Microarchitectural Floorplanning For 2D and 3D ICs." In *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol.26, No.1, pp.38-52, 2007.

[Energy Efficient Design]

EE1. Mrinmoy Ghosh, Simon Ford, Emre Ozer, Stuart Biles, and Hsien-Hsin S. Lee. "Way Guard: A Segmented Counting Bloom Filter Approach to Reducing Energy for Set-Associative Caches." In *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED-09)*, pp.165-170, San Francisco, CA, August, 2009. (**Selected as one of seven papers of ISLPED highlight for publicity and press.**)

EE2. Hrishikesh Amur, Ripal Nathuji, Mrinmoy Ghosh, Karsten Schwan, and Hsien-Hsin S. Lee. "IdlePower: Application-Aware Management of Processor Idle States." In *Workshop on Managed Many-Core Systems (MMCS) co-located with ACM/IEEE International Symposium on High Performance Distributed Computing (HPDC)*, Boston, MA, June, 2008.

EE3. Chinnakrishnan S. Ballapuram, Ahmad Sharif, and Hsien-Hsin S. Lee, "Exploiting Access Semantics and Program Behavior to Reduce Snoop Power in Chip Multiprocessors." In *Proceedings of the 13th*

ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XIII), pp.60-69, Seattle, WA, 2008. (acceptance rate = 31/127, 24.4%)

EE4. Chinnakrishnan S. Ballapuram and Hsien-Hsin S. Lee, "Improving TLB Energy for Java Applications on JVM." In *Proceedings of the International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS VIII)*, pp.218-223, Samos, Greece, 2008.

EE5. Mrinmoy Ghosh and Hsien-Hsin S. Lee, "Virtual Exclusion: An Architectural Approach to Reducing Leakage Energy in Caches for Multiprocessor Systems." In *Proceedings of the 13th IEEE International Conference on Parallel and Distributed Systems (ICPADS-07)*, Hsinchu, Taiwan, December, 2007.

EE6. Dong Hyuk Woo, Mrinmoy Ghosh, Emre Ozer, Stuart Biles and Hsien-Hsin S. Lee, "Reducing Energy of Virtual Cache Synonym Lookup using Blooming Filters." In *Proceedings of the International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES'06)*, pp.179-189, Seoul, Korea, October, 2006. (Regular paper acceptance rate = 24.3%, 25/103)

EE7. Chinnakrishnan S. Ballapuram, Kiran Puttaswamy, Gabriel H. Loh and Hsien-Hsin S. Lee, "Entropy-based Low Power Data TLB Design." In *Proceedings of the International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES'06)*, pp.304-311, Seoul, Korea, October, 2006. (Short paper acceptance rate = 39.8%, 41/103)

EE8. Mrinmoy Ghosh and Hsien-Hsin S. Lee, "DRAMdecay: Using Decay Counters to Reduce Energy Consumption in DRAMs." In *Proceedings of the 3rd Watson Conference on Interaction between Architecture, Circuits and Compilers (PAC^2)*, Yorktown Heights, NY, October, 2006.

EE9. Mrinmoy Ghosh, Emre Ozer, Stuart Biles, and Hsien-Hsin S. Lee, "Efficient System-on-Chip Energy Management with a Segmented Bloom Filter." In *Proceedings of the Architecture of Computing Systems (ARCS'05)*, pp.283-297, Frankfurt, Germany, March 2006. (acceptance rate = 21%)

EE10. Chinnakrishnan S. Ballapuram, Hsien-Hsin S. Lee, and Milos Prvulovic, "Synonymous Address Compaction for Energy Reduction in Data TLB." In *Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED-05)*, pp.357-362, San Diego, California, August 2005. (acceptance rate=22%, 53/233)

EE11. Mrinmoy Ghosh, Weidong Shi, and Hsien-Hsin S. Lee, "CoolPression — A Hybrid Significance Compression Technique for Reducing Energy in Caches." In *Proceedings of the IEEE International System-On-Chip Conference (SOCC-2004)*, pp. 399 - 402, Santa Clara, California, September, 2004.

EE12. Yuvraj S. Dhillon, Abdulkadir U. Diril, Abhijit Chatterjee, and Hsien-Hsin S. Lee, "An Algorithm for Achieving Minimum Energy Consumption in CMOS Circuits Using Multiple Supply and Threshold Voltages at the Module Level." In *Digest of Technical Papers of the International Conference on Computer-Aided Design (ICCAD-03)*, pp.693-700, San Jose, California, November 2003. (acceptance rate = 26%, 130/490)

EE13. Joshua B. Fryman, Chad M. Huneycutt, Hsien-Hsin S. Lee, Kenneth M. Mackenzie and David E. Schimmel, "Energy Efficient Network Memory for Ubiquitous Devices." In *IEEE MICRO special issue on Power Complexity Aware Design*, pp. 60-70, September/October 2003.

EE14. Hsien-Hsin S. Lee and Chinnakrishnan S. Ballapuram, "Energy Efficient D-TLB and Data Cache using Semantic-Aware Multilateral Partitioning." In *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED'03)*, pp. 306-311, Seoul, Korea, August 2003. (acceptance rate = 24.4%, 54/221)

EE15. Hsien-Hsin S. Lee, Joshua B. Fryman, A. Utku Diril, and Yuvraj S. Dhillon, "The Elusive Metric for Low-Power Architecture Research." In *Workshop on Complexity-Effective Design (WCED-03) held in conjunction with the 30th ACM/IEEE International Symposium on Computer Architecture (ISCA-30)*, San Diego, California, June 2003. (acceptance rate=25%)

EE16. Hsien-Hsin S. Lee and Gary S. Tyson, "Region-based Caching: an Energy-Delay Efficient Memory Architecture for Embedded Processors." In *Proceedings of the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES'00)*, pp.120-127, San Jose, California, November, 2000.

[**Memory Systems**]

MM1. Nak Hee Seong, Sungkap Yeo, and Hsien-Hsin S. Lee. "Tri-Level-Cell Phase Change Memory: Toward an Efficient and Reliabla Memory System." In *Proceedings of?the 40th International Symposium on Computer Architecture (ISCA-40)*. Pp.440-451, Tel-Aviv, Israel, June, 2013.

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[**Generic Microarchitecture**]

uA1. Fayez Mohamood, Mrinmoy Ghosh, and Hsien-Hsin S. Lee. "DLL-Conscious Instruction Fetch Optimization for SMT Processors." In *Journal of Systems Architecture*, 54, pp.1089-1100, 2008.

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uA3. Fayez Mohamood, Michael Healy, Sung Kyu Lim, and Hsien-Hsin S. Lee, "A Floorplan-Aware Dynamic Inductive Noise Controller for Reliable Processor Design." In *Proceedings of the ACM/IEEE International Symposium on Microarchitecture (MICRO-39)*, pp. 3-14, Orlando, Florida, December, 2006. (acceptance rate = 24.1%, 42/174)

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GP6. Ahmad Sharif and Hsien-Hsin S. Lee. "Total Recall: A Debugging Framework for GPUs." In *Proceedings of the ACM SIGGRAPH/Eurographics Workshop of Graphics Hardware (GH-08)*, pp.13-20, Sarajevo, Bosnia-Herzegovina, June, 2008.

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SA2. Jun Yang, Lan Gao, Youtao Zhang, Marek Chrobak, and Hsien-Hsin S. Lee. "A Low-Cost Memory Remapping Scheme for Address Bus Protection" In *Journal of Parallel and Distributed Computing*, vol.70, issue 5, pp.443-457, May 2010.

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SA5. Weidong Shi, Chenghuai Lu, and Hsien-Hsin S. Lee, "Memory-centric Security Architecture." Invited article. In *Transactions of High Performance Embedded Architectures and Compilers*, Vol.1, pp.95-115, 2007. Springer Verlag.

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[**FPGA**]

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[**Performance Evaluation**]

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PE2. Hsien-Hsin Lee, Youfeng Wu, and Gary Tyson, "Quantifying Instruction-Level Parallelism Limits on an EPIC Architecture." In *Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2000)*, pp.21-27, Austin, Texas, April, 2000.

PE3. Eric L. Boyd, Waqar Azeem, Hsien-Hsin Lee, Tien-Pao Shih, Shih-Hao Hung, and Edward S. Davidson, "A Hierarchical Approach to Modeling and Improving the Performance of Scientific Applications on the KSR1." In *Proceedings of the 1994 International Conference on Parallel Processing (ICPP-94)*, pp.188-192, St. Charles, Illinois, August, 1994.

[**High-Efficiency, Sustainable, and Privacy-Preserving Machine Learning Systems**]

ML1. Haiyang Huang, Newsha Ardalani, Anna Sun, Liu Ke, Shruti Bhosale, Hsien-Hsin S. Lee, Carole-Jean Wu, Benjamin C. Lee. "Toward Efficient Inference for Mixtures of Experts." In the 38th Annual Conference on Neural Information Processing System (NeurIPS'24), Vancouver, Canada, December 2024.

ML2. Trishita Tiwari, Suchin Gururangan, Chuan Guo, Weizhe Hua, Sanjay Kariyappa, Udit Gupta, Wenjie Xiong, Kiwan Maeng, Hsien-Hsin S. Lee, G. Edward Suh. "Information Flow Control in Machine Learning Through Modular Model Architecture." In the 33rd USENIX Security Symposium, Philadelphia, PA, August, 2024.

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