3D SPHINX :
Stackable Processor using Heterogeneous INtegration and eXecution

April 21, 2011

1 Executive Summary

2 Relevance and Impact

- Prototyping activities for a 3-die stack will be performed in two phases corresponding to two tick-tock cycles.
- Pathway demonstration for the integration of interlayer liquid cooling for the 3D high performance ICs.

3 Technical Rationale and Approaches

3.1 3D SPHINX Architecture Concept

To fulfill and demonstrate the technical requirements described in this RFP and address future challenges for 3D-integrated heterogeneous multi-core architecture, for this research prototype, we propose **3D SPHINX**— a *Stackable Processor using Heterogeneous INtegration and eXecution*, a scalable accelerator-based architecture exploiting heterogeneous stacking using 3D die-stacking. In this implementation, we introduce several extensible design concepts into one single architecture including stacking die layers fabricated with disparate process technology nodes, integration of heterogeneous execution model using accelerators with standardized interface, and allowing more dies to be stacked as a scalable solution in the future.

Figure 1 illustrates the 3D architectural diagram of our proposed 3D SPHINX multi-core architecture. The prototype we plan to design and fabricate will consist of three die layers including two processing layers shown at the bottom stacked with one memory layer on the top. The architecture is partitioned in a modular manner in order to enable future stacking of additional processing layers and/or memory layers. The following sections will detail the architectural partitioning in 3D, inter-layer interface, and how does our 3D SPHINX meet the design objectives.

3.1.1 Processing and Memory Layers

The 3D SPHINX architecture contains two difference device layers: processing layer and memory layer. As depicted in Figure 1, each processing layer is composed of two general-purpose processor cores, two specially tailored accelerators of different functionality, and at least one bank of the level 2 cache. We call the cores and accelerators the *computing plane*. The rest of the memory components are generally referred to as the *uncore* part. As can be seen, the design of the processing layers are

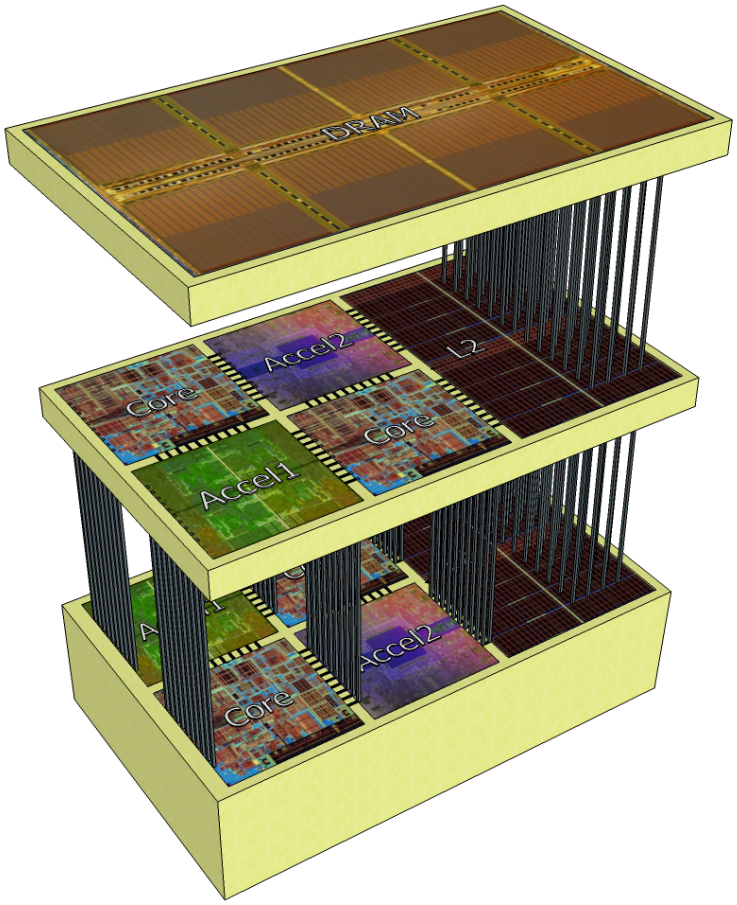


Figure 1: 3D SPHINX Architecture

almost symmetric except that their floorplans are slightly different to demonstrate heterogeneous execution to be discussed later when describing our design objectives. The cores and accelerators across two layers are placed in an interleaved pattern on purpose. As such, each processor core is paired up with one particular type of accelerator vertically via inter-die vias. This alternated core-accelerator placement in Figure 1 is the outcome of the 3D thermal density consideration related to our overall cooling strategy. We assume that the processor core will become idle when its vertically-neighbored accelerator carries out the computation and vice versa. Therefore, each vertical pair will not be fully activated simultaneously, thereby reducing both the power and thermal density.

Another consideration of this interleaved placement is with respect to the extensibility of the computing plane. Currently, the computing plane is organized in an N-by-M grid (N=M=2 is shown) with interleaved cores and accelerators. The same interleaving placement can easily and regularly be applied to future, larger computing plane as N and M are increased when larger die footprint is available as the fabrication process continues to shrink.

We propose to use the LEON open core (SPARC V8) from Gaisler Research for our processor core. We plan to explore the types of accelerators, which will likely be an ASIC core for typical data-parallel media applications. We will also consider and evaluate the possibility of implementing a more broad-purpose co-processor [13] for our accelerator. The cores, accelerators, and L2 banks will be connected with a 3D ring bus and data coherence will be maintained across the ring. This interconnect structure and the link operation upon which it is based is discussed in the next section.

3.1.2 Interconnection Model and Scalable Interface

The provision of a scalable (size), extensible (across technology generations), adaptable (across distinct IP modules) interconnect fabric requires i) a standardized interface to connect to a network, ii) a supporting point-to-point switched network, and iii) the ability to configure both.

Standardized Interface: We propose to use or adapt the Open Core Protocol (OCP) - an industry standard specification for interfacing IP blocks [1]. OCP compliant interfaces will connect IP blocks such as the Leon core to the SPHINX network. Our design approach will be to use the base OCP protocol which is based on read/write memory transactions, and selectively add additional optional OCP functionality such as burst transactions, and support for threads and tags depending on the specific IP end point modules and performance behaviors to be demonstrated, e.g., for accelerators vs. memory. The OCP standard only defines interfaces across a master-slave link and does not specify switched operation. Therefore OCP adapters will translate the OCP interface transactions to SPHINX network packets extending OCP transactions across multiple die and multiple modules on a die. This translation overhead in the network adapters is the price of design re-use and increased design productivity - for example in this case die re-use across multiple stacks. Georgia Tech will renew its membership in the OCP-IP consortium to utilize OCP tools in its design flows.

Interdie Network:. The inter-die interconnect is based on a unidirectional, point-to-point, packet-based link. Each link operates asynchronously enabling clock-domain crossings and the packet-based operation enables composition of links to form networks across multiple die. The link model is influenced by several industry standards [1, 3, 10, 11] and is comprised of of three groups of signals - data, control and optional test signals. A channel can be constructed with two links traversing opposite directions. The main attributes of this link are

1. **Variable Width:** Link widths are negotiated at power-up and established in byte-wide increments. This is a well known technique that is employed in several high speed networking standards.

2. **Asynchronous Operation:** Multiple die may operate at different clock rates either due to power and thermal management considerations or due to die shrink across a technology generations - a "tick" operation.

3. **Configurable Link Layer Protocol:** All inter-die links use the same physical layer (PHY) protocol. The PHYs are intended to be configurable to enable use with different link layer protocols. For example, the L2 cache interbank network can use the same physical layer as the core-to-accelerator interface. This will make it easier for third-party die to be designed to fit into an existing 3D platform advancing interoperability across design generations (a "tock" step). Robustness is achieved with link level CRC and automated retry across a link.

4. **Extensible:** Optional microarchitecture optimizations can be layered on top of the base physical layer and tap into OCP end point abstractions as desired.

The packet-based communication enables scalable communication across die. In this prototype we restrict ourselves to 3D ring topologies for both intra-die and inter-die communication although the packet design will support more complex switched 3D topologies. Ring topologies capture the necessary components of 3D scalability with simple, fast routers with ordering properties that simplify coherence and consistency management. The use of a configurable link layer enables the use *optional* extensions and optimizations. For example, optional bits in the packet may be defined and used as fields which identify virtual channels to preserve ordering and message priorities, e..g.,

for coherence an consistency operations. A number of such optimizations exposed by the OCP interfaces are also candidates for extension across the network. However, in this program, our goal is to keep the physical design as simple as possible, while demonstrating design room for such higher level (microarchitecture) optimizations that can be subsequently explored.

This program will explore different options in year 1 before settling on design to be implemented in the prototypes. Such a separation between the physical layer (standardized) and the data link layer (configurable) enables distinct IP generations or designs to communicate across the same physical layer substrate

3.1.3 Design Objectives

- **Performance.**
  To achieve the targeted 15% to 25% performance improvement over a 2D counterpart design, the 3D SPHINX will exploit the following key benefits enabled by 3D integration: (i) stacking memory directly on processing logic, (ii) reduced wire length using structure folding, and (iii) high-speed and high-density inter-die vias. By simply stacking system memory on top of the logic and integrating the memory controller on die [2, 8], the average memory access latency can be substantially reduced leading to overall performance improvement. To take further advantage of 3D, structure folding which reduces signal drive can be implemented. In particular, as depicted in Figure 1, we propose to bank-partition the L2 cache across die layers in our 3D SPHINX architecture as depicted in Figure 1. Such 3D design strategy partition an SRAM cache array by folding the bank (or called bank stacking [9, 12]) and cut down the wire RC delay of a 2D layout of cache banks. This reduction is due much to the small vertical dimension of TSV, therefore, data transfer between any two layers in a 3D design can be achieved within one single hop as studied in [5, 7]. Depending on the TSV technology, the typical distance between two adjacent die layers is between 12 microns [4] to 50 microns, shorter than one FO4. In other words, it will be feasible to design a "TSV elevator" which can transport data from the top memory layer to any processing layer below it, and vice versa, within one clock cycle for the 3D SPHINX. In contrast, the same access needs to traverse across multiple cache banks in a 2D cache design, inevitably increasing the latency. As shown in [9], folding an SRAM structure can effectively reduce the wire length, thereby improving the access latency for 3D caches. Moreover, such partitioning scheme could also reduce the area overhead required for a multi-ported cache by employing smaller, 3D banks.

  Another 3D feature to exploit for performance is the via density. It is known that off-chip memory bandwidth will eventually be limited by the available package pin count and its corresponding I/O power consumption. By exploiting 3D TSV, this limitation will be easily circumvented for their much higher density. More than 2x performance gain has been demonstrated in [14] by re-designing the DRAM interface and using wide TSV bus to fetch data at a much larger granularity than a regular cache line size. The design essentially leverages the basic property of (i) TSV bandwidth to eliminate trailing-edge effect and (ii) short TSV depth to transfer data at very high speed. We will investigate the trade-off among TSV density, area overhead, and design alteration for the 3D SPHINX to achieve our performance goal.

  On the other hand, the same wide TSV bus design can be applied to the interface between each processor core and its corresponding accelerator across die layers to further accelerate the data transfer [4, 13].

- **Tick Model Demonstration.**

To facilitate Intel's *tick model* allowing disparate process technologies to be independently applied to each die layer for a 3D-stacked design, our 3D SPHINX will demonstrate this viability with two features in our design approach. Both require a scalable interface design across die layers. The first demonstration is via the memory interface standardization interface, in particular, the system memory and each L2 bank placed on each individual processing layer. Our goal is to define a uniform interface to enable seamless stacking of future system memory layers, either fabricated using process shrink or new memory technologies (*e.g.,* PCM or STT-RAM) with no design change.

Secondly, we will demonstrate the tick model across the processing layers in 3D SPHINX using a globally asynchronous and locally synchronous (GALS) execution model. In our 3-layer architecture, the bottom two processing layers will be designed and clocked at different frequencies to demonstrate heterogeneous integration. The heterogeneity could either come from die layers fabricated by disparate process technologies or from two speed bins. Such integration will increase the overall post-bond yield by allowing stacking processing layers running at different speeds. Similarly, to enable this integration style we require a uniform and scalable interface design to synchronize the communication between the processor core and the accelerator. **HHL : To add more**

- **Tock Model Demonstration.**

  For Intel's *tock model* demonstration, the 3D SPHINX architecture proposes two heterogeneous accelerator designs, each stacked with a common core ISA placed in an interleaved fashion in 3D. This design choice is aimed at inherently showcasing the tock model with architectural changes without taping out another brand new design. Again, to be able to stack different types of accelerators on top of a processor core, the interface should be defined scalable and broad-purpose to facilitate different types of accelerator integration. Basically, the acceleration function can be treated like an API call or an ISA plug-in employed in DSP or embedded system design. We need to find the common input and output for these accelerators and standardize the signal interface for architectural scalability. Our goal is to investigate and design such unified interface for the two accelerators in the 3D SPHINX to implicitly realize the tock model within one single design.

3.2 Three-Tier Design

3.2.1 Design Methodology

Our 3D SPHINX architecture contains three tiers, the first two based on a Tezzaron 2-tier, and the second based on a third party 2D IC. These two are then bonded with TSVs by our assembly team. We will leverage our CAD tool capabilities to design the layout for both the 2-tier 3D IC and 1-tier 2D IC, separately. The 2D IC design can be done with readily available tools from Cadence, Synopsis, and Mentor. The 2-tier 3D IC design can also be done with our existing CAD tools based on these vendor tools, enhanced with custom point tools to handle TSVs and 2-tier stack that is shown in Figure 2. Our main tasks are as follows:

- **Tool enhancement.** The above tool flow needs to be further enhanced to design our 3-tier 3D SPHINX. Most of our 3D sign-off analysis tools can only handle 2-tier face-to-face 3D IC and need to be extended to deal with both face-to-face and face-to-back bonding in the full-stack 3D SPHINX. The entire set of tools including full-stack extraction, timing, power, clock, power and signal integrity, thermal, and design verification need to be revisited. In

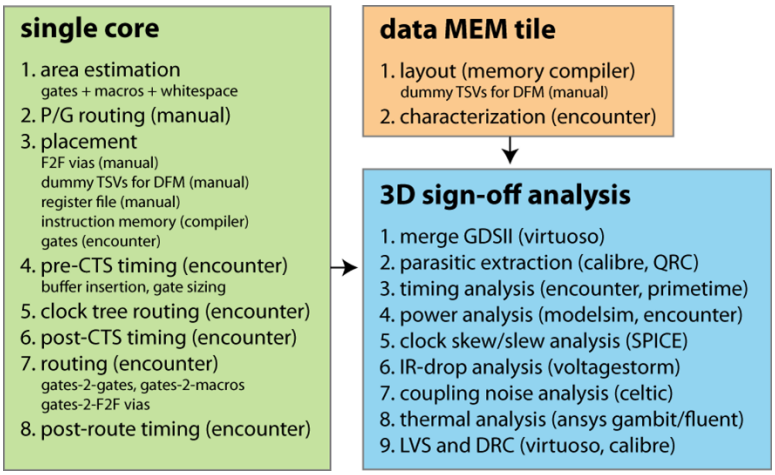


Figure 2: 3D-IC Design Flow

addition, layout optimization tools including buffering and sizing for timing and power closure will need to be enhanced to handle 3-tier.

- **New tool addition.** Full-stack mechanical stress and electro-migration analysis caused by TSVs based on Ansys, Abaqus, and Comsol will be added. We plan to extend the tools to design and verify full-stack clock and power delivery networks and scan chains for pre/post-bond testing.

- **3D floorplanning.** 3D floorplanning is an effective means to explore architecture and design space of 3D SPHINX during an early stage of the project. The goal is to evaluate a given 3D floorplan in terms of performance, power, reliability, and yield metrics, and return feedback to our architect team and design team on the strength and weakness of the given floorplan solution so that they can improve/fix them easily.

- **Circuit design support.** Our design team will deploy a variety of DFT circuit elements to enable pre/post-silicon and pre/post-bond testing for 3D SPHINX. Our CAD tools will need to be tailored to accommodate these DFT elements and provide feedback in terms of overhead.

- **Chip/package tool integration.** All of the tools above are focused on chip design. Our packaging team requires its own set of tools from CST, Agilent, Ansys for analysis and optimization. We plan to build a bridge between our chip-based and package-based tool chains to co-design and co-optimize 3D SPHINX and its package for better power and signal delivery.

The custom design components are described as follows.

3.2.2 Circuits for Power Delivery and Supply Noise Sensing for 3D SPHINX

Our goal is to design on-chip power delivery network with minimum number of TSVs and allow different voltage for each tier. The independent voltage domains for the tiers also helps provide power to the tiers during pre-bond test. The independent 2D power delivery network for each tier will be derived from a global 3D PDN using integrated voltage converter and regulator modules

(VRM). The design options to be explored here are either few complex centralized converters or more simple distributed converters. The control circuits for VRM will be built to provide options for on-chip voltage scaling. The power gating transistors will be included in the core and memory modules to drive active power management. The power gating transistors will also allow us to control the power demand during testing to limit the Ldi/dt and IR drop. We will use regularly placed distributed decaps for our design.

3.2.3 3D Interface Design

The 3D interface in our design includes the micro-bumps in the face-to-face bonded 3D Tezzaron stack, TSVs and solder-bumps in the connection between Tezzaron die-stack and memory die (3rd tier), and the TSVs or wire-bonds in the final system. Circuit design considerations for the interface will focus on robust and low-latency signal communication. We envision that the signal delay through the face-to-face connections will be minimal and may not require additional considerations. The challenge will be the communication through the TSV and solder-bumps that will connect our Tezzaron stack and MOSIS die. The design trade-off is reliability (more and redundant TSVs) versus speed (more capacitance). We also need to consider whether ESD protection circuits will be required at the interfaces to prevent gate damage during pre-bond probing. Our plan is to include in-built signal recovery and slew correction to improve signal integrity. Duty-cycle correction may also become necessary if we are sending clock through interface for synchronization. The capacitive loads of the vias can clearly limit the achievable performance and power dissipation. We plan to explore low-swing signaling to partially alleviate this challenge depending on the resistance the bonding material. Level shifter (or level shifting latches) can be used across the interface to perform communication across voltage domains.

3.2.4 Clocking for 3D SPHINX

Our clocking strategy will be to design independent clock network for each tier. We will use off-chip source and on-chip Voltage-Controlled-Oscillator (VCO) with integrated Delay-Locked-Loop (DLL) based clock source embedded in each tier. The De-skewing technique will be used while distributing clocks in each tier. Synchronizing the two DLLs will be problem if we plan to run the tiers in same frequency (particularly tier 1 and tier 2) and use synchronous clocking. This is because of the unpredictability of the voltage and thermal conditions of each tier. We will evaluate the option of spine based as well as H-tree type distribution architecture. The independent clock tree for each tier will also help testability of individual tiers so that each tier can be tested without other tiers. Separating the PDN for the clock buffers will be considered for safer design practice if pad allocation permits.

3.3 Design for Testability

We need to enable test and on-chip characterization of (i) each tier of the 2-tier Tezzaron test-chip, (ii) the memory tier before bonding, (iii) the assembled and bonded 3-tier system before packaging, and (iv) full system test with different benchmark applications. Our objective is to build significant on-chip instrumentation that will allow us to successfully test and characterize all the above steps.

3.3.1 Characterization of Supply Noise

The supply noise behavior of our prototype system is critical to characterize. We aim to design high-speed (100s MHz) but low-resolution ADCs to characterize high-frequency supply variations

while low-speed but higher-resolution ones for low-frequency (transient IR drop) variations. The second option will be to use delay based sensors for supply noise characterization to simplify the design. Our main goal is to characterize how the supply noise profile varies from tier to tier and whether noise propagates across tiers. We will perform frequency domain post-processing of the data to understand how 3D integration modulates the supply noise behavior (e.g. principal frequency of first, second, and third droop, how the resonant frequency changes from tier-to-tier) and whether the supply noise coupling exists across tiers.

3.3.2 Interface Characterization

The design of the interface circuits will also include specific circuits for interface characterization. The first objective is to characterize the RC parameters of interfaces. We will exploit our recent work to perform DC test for resistance variation. The resistance variation will be captured in terms voltage and converted to digital output either using ADCs or VCO (and counter). The RC property of can be characterized by incorporating the interface either as a capacitive load or as a serial part (both R and C) of the oscillator. We next plan to characterize the maximum data rate that can be reliably sustained across a 3D interface. The goal will be to drive the interface through specialized ring-oscillators with controllable frequency and monitor (frequency-to-digital-converters) signal at the other end. The interface circuits to drive at-speed logic tests (or delay tests) by designing in-built circuits to drive required test vectors at each interface point.

3.3.3 Delay and Temperature Sensor

We also incorporate in-built delay sensor to localize pos-fabrication performance bottlenecks to understand what determine 3D prototypes performance - interface or logic tiers or memory tiers. The delay sensing will be performed using replica path approach (with minimal invasion to the original layout of the core). The delay sensors will be correlated to at-speed test to understand whether the physical property or the logical considerations limit the performance. The delay sensor will be extended to temperature sensing. The differential delay sensor (a temperature sensitive and one temperature insensitive delay sensor)can be used to improve the accuracy of temperature sensing. Signal post-processing (low-pass filter) can be used to improve the sensing accuracy.

3.4 Power Delivery Network and Characterization

Power delivery is one of the major challenges in 3D stacked ICs. This is mainly due to the smaller footprint (= fewer P/G bumps) and higher device density (= more current demand per P/G bump and P/G TSV) in 3D ICs. This problem is exacerbated by the large area overhead involved with the 3D PDN. In order to tackle these unique power delivery issues and facilitate faster mainstream acceptance of 3D ICs, industry first needs to understand the electrical and mechanical properties of P/G TSVs and other elements in the PDN of 3D ICs and their packaging substrate. Second, industry also needs circuit-level and physical design-level solutions to detect and alleviate power supply noise problem both on-chip and on-package. Third, reliability and manufacturability issues in the PDN caused by various sources including TSV stress, electro-migration, mechanical defects, etc., need to be thoroughly investigated. Lastly, chip/package co-analysis and co-design is essential to ensure that the overall system meets the stringent requirement on power delivery of 3D SPHINX. We will investigate the following areas during the development of our prototype.

3.4.1 PDN Models Considering Chip and Package

The proposed effort will develop PDN models considering chip and package simultaneously and considering non-idealities in the TSVs. Our approach will concentrate on the following specific problems:

- **Modeling of the P/G TSVs.** We model the process induced variability and defects in P/G TSVs such as variation in diameters/oxide thickness, TSV-to-TSV misalignment, weak short or weak open defects in TSVs, and the time-varying reliability of P/G TSVs considering electro-migration and mechanical reliability caused by TSV stress.
- **Co-modeling of PDN in the chip and package.** P/G TSVs are utilized in both the 3D IC and the packaging substrate in 3D SPHINX, but their size and pitch are different and require different process technologies. In addition, their neighboring elements are different: on-chip TSVs are surrounded by silicon substrate, devices, and on-chip wires, while on-package through vias are surrounded by organic/ceramic/silicon substrate, bumps/balls, and on-package wires. Our goal is to model electrical and mechanical properties of these elements used for package-to-chip power delivery for 3D ICs.
- **PDN Reliability Models.** The coupled simulation framework will be used to model the effects of process-induced and/or time-dependent variations in resistance, capacitance, and inductance of the P/G TSVs on the reliability of the P/G network. The PDN models are coupled to the power models for different dies in 3D SPHINX. We will characterize the IR and Ldi/dt noise in the entire 3D stack, individual dies, and the chip/package interface. Characterization of the die-to-die and die-to-package coupling of the PDN noise will receive specific attention.

3.4.2 PDN Reliability Analysis Considering Circuit and Physical Design

Our chip/package PDN models will be used to perform a comprehensive analysis of the interaction between the PDN reliability and circuit/physical design solutions for 3D SPHINX. Our 3D physical design tools being developed is leveraged in this analysis. The two major PDN circuit design options to be investigated in this work are (i) shared (PDN of all tiers are shared) vs. non-shared (different 2D PDN network for different tiers) PDNs on the system (chip and package) level IR and Ldi/dt noise; and (ii) the die-to-die and die-to-package noise coupling. The filtering properties of the die-package interface will be studied by quantifying the noise leaking from the die into the package and vice versa. Assuming a fixed die-area (*i.e.*, 3D footprint), the non-shared PDN design will consider two cases: (i) all the different PDNs are supplied from off-chip, therefore significantly reducing the number of P/G bumps/TSVs available for each tier and (ii) only a single global P/G PDN is designed for the entire stack, and the local PDNs are derived from this global network using voltage regulators. . This approach will allow us to understand the impact of IR drop due to the TSVs. We study both centralized (few complex regulators for each tier) and distributed (a larger number but simpler distributed voltage regulators) voltage regulators to create different PDN design options for the 3D stack. We consider the interaction of the above chip-level PDN design options and package-level PDN/voltage regulator solutions. In addition, we consider the effects of the following physical design factors in the above PDN options: (i) the number of the P/G TSVs considering different power profile for individual dies; (ii) P/G TSV sizing (whether a single large P/G TSV or a group of small P/G TSVs is more efficient); (iii) the P/G TSVs to signal TSVs ratios on supply noise (due to the coupling of signal to P/G TSV), congestion, area,

and delay; and (iv) the interaction of 3D clock delivery network and 3D PDN in 3D SPHINX. One major issue we will address is the coupling between signal and P/G TSV due to slow wave effect at low frequencies causing a slowly decaying waveform (RC effect) and the coupling between the TSVs and transistors through silicon. The chip-package anti-resonance and its effect on signal integrity will be quantified as well through simulations. A low impedance path from the voltage regulator on the package to the 3D stack will be designed and the role of the die and package in generating the first, second and third droops in the die power supply will be studied through simulations. Another important aspect is the effect of temperature on the DC IR drop due to joule heating effects. This has shown to create a 10% increase in IR drop for 3D stacked dies. This effect will be quantified through simulations for 3D SPHINX.

3.4.3 PDN Fabrication and Testing Plans

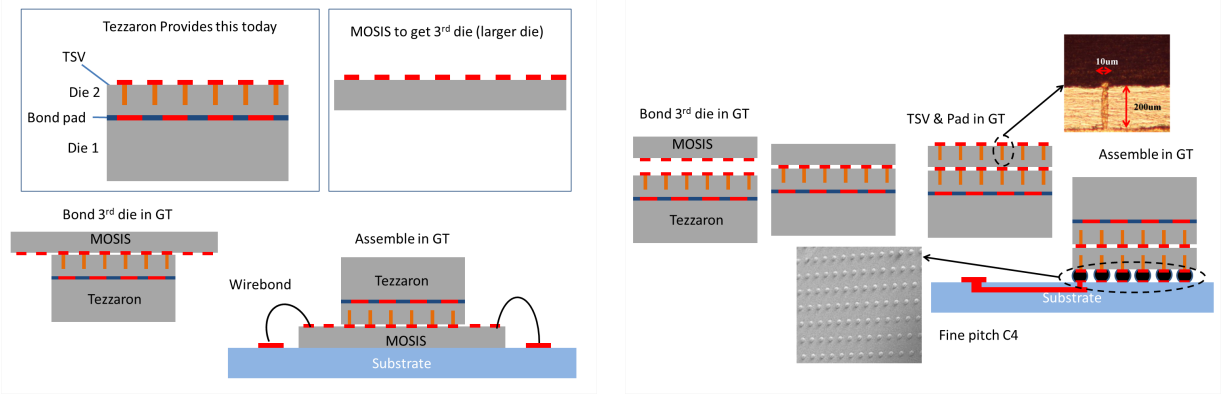
The models and analysis performed in previous two tasks are used to drive design, fabrication, and measurement plans to study what kinds of PDN solutions are the most robust for different power profiles of the chip and package solutions for 3D SPHINX. Our goal is to develop on-chip PDN characterization methods to understand the interaction of PDN solutions (*e.g.*, shared/non-shared, distributed/clustered TSVs, etc.) and power profile of different dies. Our past experience of 2D and 3D chip design with Tezzaron/MOSIS will drive this task. The specific design challenges and focus are:

- **Tunable power profile for each die.** We will design activity/power tunable circuits (*e.g.*, inverter chain with programmable capacitors, or ring-oscillator of different length) and distribute it across the tiers to create a tunable power profile for the dies. Our goal is to tune both the average power for IR analysis and transient profile for Ldi/dt analysis in 3D SPHINX.
- **On-chip PDN noise measurement techniques.** The focus here is to design circuits/methods that can isolate the effects of Ldi/dt and IR noise as well as power supply variation of each die in 3D SPHINX due to power variation in that die and due to other dies in the 3D package (due to die-to-die coupling). We will use spectral sensing techniques, where the sensed supply noise over time will be decomposed in the frequency domain to understand the time-scale of different noise events. Using the modeling framework described earlier, we correlate this time-scale to different sources of variations.

3.5 Assembly and Packaging

Full 3D prototyping capabilities will be exercised in a step-wise manner in this program with each step enabling to a generational advance in system architecture and performance. The prototyping will be a combination of in-house routine and innovative processes, and third-party capabilities for those components or processes which are too costly, complex, or time consuming to perform internally given time and budget constraints. The prototyping innovations we will demonstrate include (i) in-house stacking of third-party CMOS die manufactured at different foundries using different technologies (heterogeneous die integration), (ii) in-house fabrication of TSVs using a post-CMOS fabrication (combining routine fabrication steps and Georgia Tech's innovation), (iii) in-house fabrication of novel, low-capacitance TSVs featuring low-k liners (leading to high-speed and lower energy signal links), (iv) path-finding demonstration of fine pitch chip bonding, and (v) path-finding demonstrations for the integration of novel cooling within the 3D stack. For the most part, the in-house prototyping innovations have already been created in other programs. We will

leverage an enormous existing investment in facilities and expertise, and use the funds from this program to explore the integration.



(a) Packaging V1

(b) Packaging V2

Figure 3: Bonding and Packaging for 3D SPHINX

The prototyping activities for the 3-die stack will be performed in two phases corresponding to two tick-tock cycles. We will also outline the generational changes which would occur on additional cycles (which are beyond the time and budget anticipated in this program). The first phase, Figure 3(a), provides a low-risk, rapid turn-around, 3-die chip stack to demonstrate the architectural benefits and benchmarking of 3D SPHINX system. The prototype will feature a 2-die stack using the Tezzaron multi-project-wafer (MPW) run with 130 nm CMOS technology. The third die will be fabricated separately in a different technology node. The three-die stack will have Tezzaron TSVs in one die. It will flip-chip attached to a third die by Georgia Tech. Normally, flip-chip metallurgy would be processed when the die is in wafer-form. However, in this case a separate processing jig will be designed because we will unlikely be able to procure chips in wafer-form. The first-level interconnect technology between the chip stack and the package substrate is through wire-bond from the third die which has a larger footprint than the Tezzaron stack. This first phase prototype technology will be adequate for the system power, speed, and cooling requirements, yet demonstrates our ability to stack heterogenous chips fabricated in disparate technology nodes. It also paves the way for the introduction of additional speed, power, and cooling in future generations, shown in Figure 3(b). The substrate will be fabricated at Georgia Tech using a two-layer, thin-film, inorganic technology (one or two layers of fine-line copper or gold wiring on a silicon substrate) so that the 3D stack can be powered and tested.

The second phase prototype anticipates higher speed, power, and density connections between the 3D stack and the substrate. As depicted Figure 3(b), post-CMOS TSVs will be fabricated at Georgia Tech in the third die. The stack will be flip-chip attached to the Georgia Tech produced substrate. The first-layer package will be fine line wiring with flip-chip metallization (additional layer of metal patterning). The TSV will be created using deep-trench reactive ion etching with novel copper filling methods. Demonstrations will be made for higher performance TSV technologies with low-k liners for future high-speed vertical interconnect.

Future phases of process advancements can be envisioned and will be outlined in this program with physical demonstrations. The advances include: higher density, scalable TSVs, advances in the density and layers in the first-level package substrate, and inter-layer cooling. These advances will be planned for 3D generations for higher clock speed, chip power, and cooling needs to coincide with future technology/architecture tick-tock cycles.

4 Statement of Work and Schedule

4.1 Schedule and Milestones

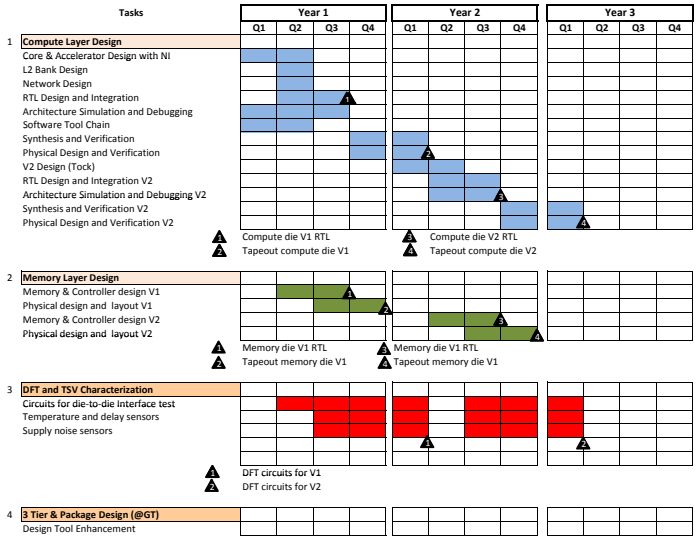


Figure 4: Schedule and Milestones

The overall program schedule and major milestones are presented in Figure 4. There are 7 major tasks, each with several sub-tasks listed as shown. Milestones for each task are also numbered on the schedule.

4.2 Success Criteria

4.3 Deliverables

The program deliverables will demonstrate the ability of the 3D SPHINX design concepts to deliver a modular architecture for 3D systems that supports composition of modules across technology generations (a tick) and designs within a technology generation (a tock). The major deliverables in support of this demonstration are the following.

1. A 3 die stack (version 1 or V1) comprised of two compute layers and one memory layer wire bonded to the package. All three die will be fabricated in the same technology node (130 nm) and delivered in a test set-up providing functional and performance data.

2. A 3 die stack (version 2 or V2) using the same die for the compute layers but integrated and packaged with a memory die fabricated at a different technology node (90nm or 65 nm). The package will be delivered in a test set-up providing functional and performance data.

3. All software (for design, test, and simulation) will be made available open source. Note that in particular much of this software development (especially the CAD extensions) are supported by parallel and independentlt funded efforts.

4. All hardware designs will be made available as open source modules.

5. Writings documenting new processes, techniques, and insights will be published in conference and journal proceedings and/or as GT technical reports.

Milestone deliverables marking technical progress at the granularity of a quarter are presented in the schedule in Section 4.1.

5 Fabrication and Assembly Facilities

5.1 Georgia Tech In-House capabilities

The Georgia Tech Nanotechnology Research Center (NRC) is an open user facility that serves nearly 700 unique researchers annually and has a full complement of processing capabilities. Georgia Tech is one of the world leaders in nanoscience and nanotechnology research. As the premier nanotechnology research facility in the region, the Nanotechnology Research Center already serves more than 500 researchers per year, with nearly 40 percent of these coming from other universities, colleges, companies, and government labs.

The Georgia Tech Nanotechnology Research Center consists of the Pettit Microelectronics Building and the newly completed Marcus Nanotechnology Building. The Marcus Building cleanroom has an innovative combination of traditional inorganic cleanroom space adjacent to a cleanroom designed for research at the interface between life sciences and nanotechnology. These areas are physically connected to allow for research samples to be transferred between them. More importantly, this connectivity will foster novel designs and applications through interdisciplinary research collaboration.

The GT NRC is a member of the Nanotechnology Infrastructure Network (NNIN), an integrated geographically-diverse partnership of 14 university-based laboratories supported by National Science Foundation.

The GT NRC maintains over 140 research tools and provides access and technical support to the broad user community. The facilities include optical lithography (spin-coaters and mask aligners), mask making capabilities, nano-patterning via state-of-the-art electron beam lithography, thin film deposition (thermal growth, low-pressure chemical vapor deposition, plasma enhanced chemical vapor deposition, atomic layer deposition, and electron-cyclotron resonance deposition), reactive ion etching, inductively coupled plasma etching, electron-beam evaporators, filament evaporators, radio frequency sputtering, direct current sputtering, packaging facilities (dicing saws, probe stations, lapping tools, polishing tools, wirebonders, and flip-chip aligners), micro-scale printing tools, jet-printing tools, imaging and analysis tools (scanning electron microscopes, atomic force microcroscopy, focused ion beam sectioning, and optical microscopy), and metrology tools (profilometry, ellipsometry, refractometry, energy dispersive x-ray analysis, mass spectroscropmetry, x-ray diffraction, x-ray photoelectron spectroscopy, quartz crystal microbalance, and raman spectroscopy). The PIs have access to additional processing and characterization tools including nuclear magnetic resonance spectroscopy, infrared spectroscopy, and high frequency test stations.

5.1.1 TSV process?

5.1.2 Integration

5.1.3 Packaging?

5.2 Potential Foundry Partners

We are currently exploring the collaboration opportunities of our foundry partners for fabrication.

5.2.1 Tezzaron

Our favorite choice of fabrication is the 3D process of Tezzaron and their foundry partner (GLOBALFOUNDRIES) whom our team members have worked with in their prior 3D prototyping project. Most importantly, Tezzaron is currently way ahead of the curve in terms of the following reasons.

- Easy/cheap access to the fab line: offer MPW runs with MOSIS twice a year at relatively low cost (around $1500 per 1mm2 as of spring 2011).
- Size of TSVs: 1.2um diameter and 6um height, which is several times smaller compared with IBM and IMEC (5-10um diameter and 20-50um height).
- Yield: 99.9% according to the CEO Bob Patti.
- Good track record: have manufactured several successful 3D ICs.
- Roadmap: have plans up update device technology from 130nm to 65nm and offer 3 and 4 tier stacking in late 2011, according to the CEO.

Through DARPA's 3D MPW program, Lee and Lim's 3D-MAPS 64-core processor was manufactured using this service with logic CMOS done by GLOBALFOUNDRIES (Chartered) 0.13μm process and TSV/bonding performed by Tezzaron.

5.2.2 ITRI and TSMC

In addition to the first option, we are also assessing the potential option of using manufacturing and integration service provided by Industrial Technology Research Institute (ITRI). ITRI, a foundation and technology incubator based in Hsin-Chu, Taiwan, provides 90nm CMOS shuttle service from Taiwan Semiconductor Manufacturing Company (TSMC) for their 3D-IC research and development. The die stacking and bonding (currently limited to two die layers face-to-back), TSV fabrication, and post processing will be performed inside ITRI. ITRI will also provide TSMC IP including embedded DRAM (logic-process eDRAM) for satisfying our design requirement. Moreover, based on their partnership with a commercial CAD tool company, ITRI can provide us their established, complete 3D design flow which they used to design their current 3D ICs According to their current projection, ITRI will be able to provide 65nm process (TSMC shuttle service) with three die stack integration around the time we tape out our design.

5.2.3 Hynix?

6 Proposal Team

Our team includes eight members from Georgia Tech specialized in computer architecture, physical design, CAD tools, testing, power distribution, fabrication, and packaging. All of them have been heavily engaged in 3D stacked ICs research for many years, and had done physical design, prototyping, fabrication, and packaging in their respective 3D IC projects. Before their qualifications are described, we first highlight critical 3D-IC projects related to this Prototype RFP.

6.1 Highlight of Prior 3D-IC Projects

6.1.1 3D-MAPS Many-Core Prototype

Lee and Lim led a team designed and taped out a two-layer 64-core processor called *3D-MAPS* [4,6] in March 2010 using GLOBALFOUNDRIES (Chartered) 130nm process and TSV process and bonding provided by Tezzaron through the DARPA MPW run. The two-layer 3D chip contins

64 cores on one die and 256KB scratchpad SRAM on another, totalling 33M transistors. Around 50,000 face-to-face vias were employed for power and signals to achieve 71.9 GB/s bandwidth at 277MHz core frequency. It also uses 50,000 TSV, each 1.2μ in diameter, for off-chip power delivery and signal I/O. At 1.5V, the 5mmx5mm 3D chip stack consumes up to 6.2W. The power density is 24W/cm2, and a special cooling mechanism is employed in the package. The RTL-to-GDSII tool chain is based on commercial tools from Synopsys, Cadence, and Mentor Graphics. Since these tools can only handle 2D ICs, we have developed plug-ins to handle TSVs and 3D stacking. The chip is being bonded by Tezzaron and will be packaged by Amkor. The same team is currently working on *3D-MAPS V2* featuring 128 cores and 2Gbit DRAM, a 5-die stack to be taped out in May 2011.

6.1.2 Packaging and Cooling Technologies

Bakir and Kohl have extensive experience in 3D IC technology demonstration, packaging, and cooling. They have demonstrated numerous TSV technologies with diameters ranging from 50 μm down to 100 nm. Moreover, they have demonstrated fine-pitch solder and copper-copper chip-to-chip bonding. In the 3D prototype we propose, both TSVs and fine pitch bonding and assembly are critical elements. The PIs also have extensive experience with integration of novel on-chip cooling in 3D ICs and have won numerous paper awards on their research.

6.2 Team Profile

Muhannad Bakir. Muhannad S. Bakirs areas of interest include three-dimensional (3D) electronic system integration, advanced cooling and power delivery for 3D systems, biosensors and their integration with CMOS circuitry, carbon based interconnect networks, and nanofabrication technology. He is the editor of a book entitled Integrated Interconnect Technologies for 3D Nanoelectronic Systems (Artech House, 2009) and is the author/coauthor of more than 70 journal publications and conference proceedings, 5 book chapters, 12 US patents. Dr. Bakir received an Intel Ph.D Fellowship (2002) and is the Associate Director of the Georgia Tech Interconnect and Packaging Center (IPC). His projects include multi-mode I/O for 3D and chip-to-substrate attachment. In particular, significant advances have been made in the co-design of inter-layer chip cooling and layer-to-layer stacking for 3D.

Abhibit Chatterjee. Abhijit Chatterjee is a Professor in the School of Electrical and Computer Engineering at Georgia Tech and a Fellow of the IEEE. He received his Ph.D in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 1990. Chatterjee received the NSF Research Initiation Award in 1993 and the NSF CAREER Award in 1995. He has received four Best Paper Awards and three Best Paper Award nominations. In 1996, he received the Outstanding Faculty for Research Award from the Georgia Tech Packaging Research Center, and in 2000, he received the Outstanding Faculty for Technology Transfer Award, also given by the Packaging Research Center. Chatterjee has published over 350 papers in refereed journals and meetings and has 12 patents. He co-founded Ardext Technologies Inc, a test solutions company and served as Chairman and Chief Scientist from 2000 - 2002. He is currently directing research at Georgia Tech in mixed-signal/RF design and test funded by NSF, SRC, MARCO-DARPA and industry.

Paul A. Kohl Paul A. Kohl received a Ph.D. from the University of Texas in 1978 and was employed at AT&T Bell laboratories until 1989. He held a number of positions at Bell Labs including the creation and supervision of an Advanced Packaging Group to explore high-density memory-processor modules on silicon. He is currently a Regents Professor at Georgia Tech, Director

of the Interconnect Focus Center, and founding Director in the SRC Interconnect and Packaging Center of Excellent at Georgia Tech (now past Director). His research interests include materials and structures for electronic packaging and interconnect. He holds some of the original patents on porous low-k dielectrics created from thermal decomposition of thermally labile groups and received the Callinan Award from the ECS for the work. He has made numerous contribution of low-loss transmission line structures for chip-to-chip communications including the use of air-clad dielectrics with no loss. Numerous advances in chip and package approaches to metallization have been made. He has published more than 200 journal papers on the subject and holds 51 US Patents, mostly in the areas of metallization and dielectric materials. He is past Editor-in-Chief of the Journal of the Electrochemical Society (1995 to 2008) and Electrochemical and Solid-State Letters (1998-2003). Dr. Kohl is Vice President of the Electrochemical Society (2011-2014) and President elect (2014-2015). Recent work has focused on high-bandwidth, low-loss, air-clad transmission line structure for chip-to-chip communication, novel cooling methods for electronic systems, and power.

Hsien-Hsin S. Lee (PI). Hsien-Hsin Lee had a PhD from University of Michigan, Ann Arbor. He was a processor architect at Intel (1995-2001) and managed the architecture team at Agere/Motorola's StarCore DSP Center. He started 3D-IC research in 2004 at Georgia Tech and is the lead Principal Investigator for the 3D SPHINX project. Sponsored by FCRP's GSRC and C2S2 centers, Department of Defense, and National Science Foundation, Lee had led several research projects in 3D architecture, physical design, design-for-test, and prototyping. In the 3D-MAPS project mentioned above, Lee's responsibility is the architecture definition and design, 3D partitioning, RTL development, DFT, test plan, software and simulator, and post-silicon validation. Currently, Lee and his team are working with ITRI, Taiwan, to design a two-layer 3D chip to be fabricated using TSMC's shuttle service (90nm) and ITRI's TSV process. Lee will be responsible for the 3D SPHINX architecture ad physical design.

Sung Kyu Lim. Sung Kyu Lim had a PhD from UCLA. Lim's responsibility includes physical design, CAD tools, DFT, thermal analysis, power distribution and clock synthesis.

Saibal Mukhopadhyay. Saibal Mukhopadhyay have been involved in successful tape-out of four test-chips from University (as a lead designer in two and as a faculty supervisor in two). Further he has designed one test-chip during his industrial tenure at IBM T. J. Watson. Measurement results from his different test-chips have been published in all of the three premier circuit conferences: - International Solid State Circuit Conference (ISSCC, 2007), Symposium of VLSI Circuits (VLSI Ckt, 2007), and Custom Integrated Circuits Conference (CICC, 2010, faculty, and five (5) papers in premier circuit journal - IEEE Journal of Solid State Circuits (JSSC). His particular custom circuit design experience includes: SRAM, on-chip sensors (leakage, device mismatch), logic circuits, analog bias generators (body-bias, voltage reference), and circuits for on-chip clocking (VCO, clock delivery, etc. 200MHz-1GHz). He has designed/supervised test-chip design in following technologies: 130nm RF-CMOS, 150nm FD/SOI (MIT), 180nm CMOS, and sub-45nm SOI. PI Mukhopadhyay will be involved in defining and supervising the circuit design and design-for-testability problems.

Madhavan Swaminathan. Madhavan Swaminathan is the Joseph M. Pettit Professor in Electroncis and Director of the Interconnect and Packaging Center. His areas of interest include power delivery, CAD, high frequency mesurements, test and package integration. He has over 325 publications and 22 patents in this area and is the principal author of the book "Power Integrity Modeling and Design for Semiconductors and Systems", Prentice Hall, 2007 and co-editor of "Introduction to System on Package - Miniaturization of the Entire System", McGraw Hill, 2008. He will be focusing on power distribution, TSV characterization and package integration in this proposal.

Sudhakar Yalamanchili. Sudhakar Yalamanchili has been involved in the development of high performance multiprocessor interconnection networks since the early 1990's when his group

taped out Ariadne - a fully self-timed, reliable wormhole router. Since then this work has grown to include reliable and reconfigurable communication and computation where he has been the PI on projects funded by NSF, DARPA, DOE and ONR. His is currently Co-PI of a project funded by the FCRP's Interconnect Focus Center to explore the limiting impact of 3D interconnects on multicore architectures. In the last decade he has led the development of compiler and optimization infrastructures for heterogeneous computing notably as Co-PI for DARPA's XMONARCH TRIX compiler and PI for the current CPU-GPU targeted Ocelot infrastructure supported by IBM, NVIDIA, LogicBlox and NSF. He will be responsible for the development of the configurable link and interconnection network for 3D SPHINX, and the software tool chain.

7 Cost Proposal

TITLE: 3D SPHINX Stackable Processor using Heterogeneous INtegration and eXecution					
PRINCIPAL INVESTIGATOR / PROJECT DIRECTOR	No. of Months	12	12	12	
A. SENIOR PERSONNEL: PI/PD, Co-PI's, Faculty and Other Senior Associates					
(List each separately with title, A.7. show number in brackets)		Period 1	Period 2	Period 3	TOTAL
1. Professors (no time charged)		$0	$0	$0	$0
7. (1) TOTAL SENIOR PERSONNEL (1-6)		$0	$0	$0	$0
B. OTHER PERSONNEL (SHOW NUMBERS IN BRACKETS)					
1. ( ) POST DOCTORAL ASSOCIATES		$0	$0	$0	$0
2. ( ) OTHER PROFESSIONALS		$0	$0	$0	$0
3. (10) GRADUATE STUDENTS (Full-Time GRA appointment is 20 hours/week)		$284,400	$241,740	$246,575	$772,715
4. ( ) UNDERGRADUATE STUDENTS		$0	$0	$0	$0
5. ( ) SECRETARIAL-CLERICAL		$0	$0	$0	$0
6. ( ) OTHER		$0	$0	$0	$0
TOTAL SALARIES AND WAGES (A+B)		$284,400	$241,740	$246,575	$772,715
Graduate Student Health Insurance		$2,275	$1,934	$1,973	$6,182
C. FRINGE BENEFITS (IF CHARGED AS DIRECT COSTS)		$0	$0	$0	$0
TOTAL SALARIES, WAGES AND FRINGE BENEFITS (A+B+C)		$286,675	$243,674	$248,547	$778,897
D. PERMANENT EQUIPMENT (LIST ITEM AND DOLLAR AMOUNT FOR EACH ITEM EXCEEDING $1,000)					
		$0	$0	$0	$0
TOTAL PERMANENT EQUIPMENT		$0	$0	$0	$0
E. TRAVEL	1. DOMESTIC (INCL. CANADA AND U.S. P	$6,000	$6,000	$6,000	$18,000
	2. FOREIGN	$0			$0
F OTHER DIRECT COSTS					
1. MATERIALS AND SUPPLIES		$ 30,000	$ 172,500	$ 142,500	$345,000
2. PUBLICATION COSTS/DOCUMENT DISSEMINATION					$0
3. CONSULTANT SERVICES					$0
4. CLEANROOM ACCESS FEES (2 students)		$28,000	$28,000	$28,000	$84,000
5. SUBCONTRACTS					$0
	<25K				$0
	<25K				$0
	>25K	$0	$0	$0	$0
	>25K	$0	$0	$0	$0
TOTAL Subcontract		$0	$0	$0	$0
					$0
6. OTHER	Tuition cost	$148,366	$160,235	$173,054	$481,656
G. TOTAL OTHER DIRECT COSTS		$206,366	$360,735	$343,554	$910,656
TOTAL DIRECT COSTS (A THROUGH G)		$499,041	$610,409	$598,102	$1,707,552
H. INDIRECT COSTS (57.1 % overhead)	BASE:	$350,675	$450,174	$425,047	$1,225,897
Excluding tuition charges, equipment, and subcontract costs over $25K each					
TOTAL INDIRECT COSTS		$0	$0	$0	$0
I. TOTAL DIRECT AND INDIRECT COSTS		$499,041	$610,409	$598,102	$1,707,552

Figure 5: Anticipated Budget

We plan to place all intellectual property developed in this program in the public domain including offering software developed under this program under an open source license. Accordingly the anticipated budget is provided in Figure 5. Note that these budgets are preliminary and while we feel they are accurate, they have not been officially certified by Georgia Tech's Office of Sponsored Programs. Should this program be funded, we do not anticipate deviations from this budget unless requested by Intel (for example if the work is to be peformed under as sponsored contract).

7.1 Budget Justification

The specific elements of the budget are described in more detail below.

1. **Personnel:** In year 1 we will have 12 graduate research assistants engaged in the project. This number will drop to 10 for years 2 and 3. This increased workload in year 1 is primarily due to the RTL design and increased modeling and debugging demands. After year 1 we will have a reasonable stable RTL from which to we will generate the V2 design. The first year will also see increased workload in getting the software tool chains installed, stablilized

(stuctured to interact with the test fixtures) as well as setting up the probe station. Such tasks are one time tasks. We also note that we are obtaining significant leverage from existing research funding at GT in CAD Tools for 3D Design (PI: SK. Lim), in satisfying the unique needs of the SHINX CAD tool infrastructure.

2. **Travel:** The budget includes approximately 5 person trips ($1200/trip) each year for travel to Intel sites for interaction with Intel engineers.

3. **Cleanroom Costs:** The cleanroom costs are budgeted at approximately $14K per student per year for two graduate students. This cost includes access and use of cleanroom facilities, the bonder, two boxes of dummy silicon wafers and related packaging materials and supplies.

4. **Tuition:**As required by the Institute, tuition remission is assessed at $1030.32 per month for each graduate student.

5. **Materials and Supplies:** This category includes several items.

   (a) Two Die Stack: We have budgeted $37,500 for each two die stack based on anticipated costs. Exact expense formulas cannot be released at this time due to some confidentiality issues. However, we are confident that the estimates are reliable.

   (b) Third Die Fabrication: We have proposed an aggressive strategy for fabricating the third die. Costs are difficult to estimate exactly at this time. We have budgeted $100,000 per die (one die each for V1 and V2).

   (c) Daughter Cards: We have budgeted $10K for sets of daughter cards upon which to mount the packaged 3 die stack. This cost will most likely drop as we plan to design the cards in house.

   (d) Motherboards: We have budgeted $5K for a motherboard for each version. This motherboard will host the daughter card and FPGA-based interface. Should a PCIe based daughter card solution serve our testing and demonstration needs, we will not need to have these motherboards designed and fabricated.

   (e) Probe Cards: We have budgeted $20K each for two probe cards for testing the two-die stack and memory die with our probe station.

   (f) Packaging: No packaging costs are incurred as these activities are being performed in-house.

Note that the M & S purchases are spread across project years. For example, in year 1 we will acquire a probe card and the daughter cards for the 3-die stacks for SPHINX V1 while the remaining fabrication and assembly costs for V1 are incurred in year 2.

References

[1] Open core protocol. http://www.ocpip.org/.

[2] B. Black, M. Annavaram, N. Brekelbaum, J. DeVale, L. Jiang, G. H. Loh, D. McCauley, P. Morrow, D. W. Nelson, D. Pantuso, P. Reed, J. Rupley, S. Shankar, J. Shen, and C. Webb. Die Stacking (3D) Microarchitecture. In *Proceedings of the 39th International Symposium on Microarchitecture*, 2006.

[3] Brian Holden and Jay Trodden and Don Anderson . *HyperTransport 3.1 Interconnect Technology*. Mindshare Inc., first edition, 2008.

[4] M. B. Healy, K. Athikulwongse, R. Goel, M. M. Hossain, D. H. Kim, Y. J. Lee, D. L. Lewis, T.-W. Lin, C. Liu, M. Jung, B. Ouellette, M. Pathak, H. Sane, G. Shen, D. H. Woo, X. Zhao, G. H. Loh, H.-H. S. Lee, and S. K. Lim. Design and analysis of 3D-MAPS: A many-core 3D processor with stacked memory. In *2010 IEEE Custom Integrated Circuits Conference (CICC)*, 2010.

[5] J. Kim, C. Nicopoulos, D. Park, R. Das, Y. Xie, V. Narayanan, M. Yousif, and C. Das. A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures. In *Proceedings of the International Symposium on Computer Architecture*, 2007.

[6] D. L. Lewis, M. B. Healy, M. Hossain, T.-W. Lin, M. Pathak, H. Sane, S. K. Lim, G. Loh, and H.-H. S. Lee. Design and Test of 3D-MAPS, a 3D Die-Stack Many-Core Processor. In *IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits*, 2010.

[7] F. Li, C. Nicopoulos, T. Richardson, Y. Xie, N. Vijaykrishnan, and M. Kandemir. Design and Management of 3D Chip Multiprocessors using Network-in-Memory. In *Proceedings of the International Symposium on Computer Architecture*, 2006.

[8] C. Liu, I. Ganusov, M. Burtscher, and S. Tiwari. Bridging the Processor-Memory Performance Gap with 3D IC Technology. *IEEE Design & Test of Computers*, 22(6):556–564, 2005.

[9] K. Puttaswamy and G. H. Loh. 3d-integrated sram components for high-performance microprocessors. *IEEE Transactions on Computers*, 58(10):1369–1381, 2009.

[10] R. Maddox and G. Singh and R. Safranek and R. Colwell . *Weaving High Performance Multiprocessor Fabric: Architectural Insights to the Intel QuickPath Interconnect*. Intel Press, first edition, 2010.

[11] Ravi Budruk and Don Anderson and Tom Shanley . *PCI Express System Architecture*. Mindshare Inc., first edition, 2008.

[12] P. Reed, G. Yeung, and B. Black. Design Aspects of a Microprocessor Data Cache using 3D Die Interconnect Technology. In *Proceedings of the 2005 International Conference on Integrated Circuit and Technology*, 2006.

[13] D. H. Woo, J. B. Fryman, A. D. Knies, M. Eng, and H.-H. S. Lee. POD: a 3D-integrated Broad-purpose Acceleration Layer. *IEEE MICRO special issue on Accelerator Architectures*, 28(4):28–40, July/August 2008.

[14] D. H. Woo, N. H. Seong, D. L. Lewis, and H.-H. S. Lee. An Optimized 3D-Stacked Memory Architecture by Exploring Excessive, High-Density TSV Bandwidth. In *Proceedings of the 16th International Symposium on High-Performance Computer Architecture*, 2010.