Hsien-Hsin Sean Lee, Ph.D.

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EDUCATION

University of Michigan, Ann Arbor, MI
Ph.D. in Computer Science and Engineering 2001
Dissertation Title: *Improving Energy and Performance of Data Cache Architectures by Exploiting Memory Reference Characteristics.*
Horace H. Rackham Distinguished Dissertation Award, University of Michigan.
Nominated by University of Michigan for ACM Doctoral Thesis Award.

University of Michigan, Ann Arbor, MI
M.S.E. in Computer Science and Engineering 1994

National Tsing-Hua University, Hsinchu, Taiwan
B.S. in Electrical Engineering 1990
Valedictorian of the Class 1990

EMPLOYMENT

Facebook Inc., Cambridge, MA
Research Head, SysML Boston, Facebook AI Research March 2020 - Present
Research Head, AI Infrastructure Research Jan 2019 - Feb 2020

- Build a new research team from scratch focusing on computing systems for machine learning at Boston.
- Lead a dozen of researchers to perform on high-efficiency, high-throughput, and privacy-preserving machine learning research for datacenter infrastructure and wearable devices.
- Establish academic relations with universities worldwide.

Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC), Hsinchu, Taiwan April 2012 - Jan 2019
Deputy Director, Design Methodology and Kits Development Division

- Manage 6 departments (155 R&D staff across Taiwan, China, and US) developing IC design methodology and process design kits (PDK) for all TSMC customers.
- Lead design enablement across TSMC R&D, EDA (Synopsys, Cadence, Mentor, ANSYS, etc.), and fabless design houses.
- Technology owner of design collaterals for all TSMC process nodes and integration/packaging technologies (2.5D/3DIC.)
- Technology owner of EDA tool certification programs for physical design sign-off tools, custom design flow, and SPICE simulators.
- Technology owner of Machine Learning applications to improve efficiency and quality of physical design methodology.

Georgia Institute of Technology, Atlanta, GA
Associate Professor (Tenured), School of Electrical and Computer Engineering July 2008 - June 2014
Assistant Professor, School of Electrical and Computer Engineering Aug 2002 - June 2008

- Green data centers (NSF, State of Georgia)
- 3D-IC architecture, design-for-test, physical design, & prototyping (DoD, NSF, SRC MARCO centers)
- Emerging memory architecture (IBM, Intel)
- Transactional memory and speculative multithreading (NSF)

- Secure processor architecture (NSF, DoE)
- FPGA-based accelerators and system-wide monitoring (NSF)
- Adjunct faculty member of joint degree program at Shanghai Jiao Tong University (2011) and Korea University (2008-2010).

Agere Systems, Atlanta, GA July 2001 - August 2002
Architecture Manager, StarCore DSP Technology Center of Agere Systems and Motorola, Inc.

- Managed 10 CPU/DSP architects from Lucent/Agere and Motorola.
- Owner of a 1GHz StarCore DSP architecture design for 3G infrastructure, including the VLES ISA, architecture simulators, and performance benchmarking.

Intel Corporation, Santa Clara, CA May 1999 - July 2001
Researcher, Programming Systems Lab, MRL

- Research on computation reuse of IA64 architecture.
- Exploitation of instruction-level parallelism for advanced Itanium architecture.

Intel Corporation, Folsom, CA October 1995 - April 1999
Senior Processor Architect, Microprocessor Division 6

- Performance architect for Timna and Katmai (Pentium-III).
- Pentium III post-silicon validation.
- Pentium III SSE/prefetch instruction definition and microarchitecture development.
- Coded Microsoft Direct3D 6.1 API using SSE ISA (assembly level).
- Owner of Intel 3D Geometry Performance Roadmap.

HONOR AND AWARDS

- **IEEE Fellow**, 2017. *Citation: for contributions to 3D integrated circuits and computer architecture.*
- **10-year Most Significant Paper Award**. *International Test Conference (ITC)*, 2017. (Paper 3D19)
- Class of 1934 Course Survey Teaching Effectiveness Award, Georgia Tech, 2012.
- **Best Paper Award**. *The ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS 2011)*, NY, 2011. (Paper SA1)
- IBM Faculty Award, 2011.
- **NSF CAREER Award**, 2007.
- ECE Outstanding Junior Faculty Award, Georgia Tech, 2006.
- **Department of Energy Early CAREER Principal Investigators Award**, 2005.
- **Best Paper Award**. *The 2nd Watson Conference on Interaction Between Architecture, Circuits and Compilers ($P = AC^2$)*, NY, 2005. (Paper uA5)
- **Best Paper Award**. *The 2004 ACM/IEEE International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES-2004)*, Washington DC, 2004. (Paper SA19)
- **Horace H. Rackham Distinguished Dissertation Award**, University of Michigan, 2001.
- **Best Paper Award**. *The 33rd ACM/IEEE International Symposium on Microarchitecture (MICRO-33)*, Monterey, CA, 2000. (Paper MM12)
- Intel Foundation Fellowship, 2000-2001.
- University of Michigan Research Fellowship, 1993.
- **Valedictorian of the Class 1990** of National Tsing-Hua University, 1990.
- **Chancellor Mei Yi-Chi Memorial Award**, National Tsing-Hua Univeristy, 1989.

PROFESSIONAL SERVICE

Professional Societies

- Industry Advisory Board Member, Department of Computer Science, University of Central Florida, 2021 - Present.
- IEEE Fellows Committee, 2018, 2019.
- Search Committee Chair for IEEE Micro Editor-in-Chief, 2018.
- Executive Committee Member, IEEE Technical Committee on Computer Architecture, 2017 - 2019.
- Industry Advisory Board Member, IEEE Computer Society, 2016 - Present.
- Fellow, IEEE, M'96, SM'06, F'17.
- Senior Member, ACM, M'99, SM'09.
- Member, Tau Beta Pi Engineering Honor Society.

Editorial Boards

- Editorial Board Member, *IEEE Micro Magazine*, 2016 - Present.
- Guest Editor, *IEEE Micro Special Issue on Commercial Products*, 2021.
- Guest Editor, *IEEE Micro Special Issue on Automotive Computing*, 2018.
- Associate Editor, *IEEE Transactions on Computers (IEEE TC)*, 2012 - 2015.
- Associate Editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, 2010 - 2013.
- Associate Editor, *ACM Transactions on Architecture and Code Optimization (ACM TACO)*, 2009 - 2015.

Major Conference/Workshop Organizers

- Program Chair of Industry Track, *the 48th ACM/IEEE International Symposium on Computer Architecture (ISCA-48)*, Valencia, Spain, 2021.
- Program Co-Chair, *the 49th ACM/IEEE International Symposium on Microarchitecture (MICRO-49)*, Taipei, Taiwan, 2016.
- Workshop Co-Chair, *International Workshop on Parallelism in Mobile Platforms (PRISM) collocated with ISCA*, 2013-2018.
- Student Travel Grant/Award Chair, *the 39th ACM/IEEE International Symposium on Computer Architecture (ISCA-39)*, Portland, OR, 2012.
- Steering Committee, *the IEEE International Symposium on Workload Characterization (IISWC 2011)*, 2011-Present.
- General Chair, *the IEEE International Symposium on Workload Characterization (IISWC 2010)*, Atlanta, GA, 2010.
- Workshop Co-Organizer, *Invited Workshop on Technology-Architecture Interaction: Emerging Technologies and their Impact on Computer Architecture, in conjunction with MICRO-43*, Atlanta, GA, 2010.
- Tutorial and Workshop Chair, *the 43rd International Symposium on Microarchitecture (MICRO-43)*, Atlanta, GA, 2010.
- Registration Chair, *the 42nd International Symposium on Microarchitecture (MICRO-42)*, New York City, 2009.
- Audio/Video Co-chair, *Embedded System Week (ESWEEK)*, Atlanta, GA, 2008.

Major Technical Program Committee

I served as a program committee member for more than 90 conferences and workshops. Here are the highlights:

- IEEE MICRO Top Picks: 2013, 2014, 2016, 2017, 2018.
- International Symposium on Computer Architecture (ISCA): 2006, 2008, 2012, 2014, 2015, 2018, 2019, 2020, 2021 (PC Chair, Industry Track)
- International Symposium on Microarchtiecture (MICRO): 2010, 2014, 2015, 2016 (Program Co-Chair), 2020, 2021.
- International Conference on High-Performance Computer Architecture (HPCA): 2007, 2016, 2021.
- International Conference on Compiler, Architectures, Synthesis for Embedded Systems (CASES): 2004, 2005, 2006, 2007, 2008.
- International Conference on Computer Design (ICCD): 2005, 2006, 2007, 2008, 2009, 2011, 2012.
- Design, Automation and Test in Europe (DATE): 2013, 2014, 2015.
- Asia and South Pacific Design Automation Conference (ASP-DAC): 2012, 2013, 2014.

TEACHING

Ph.D. Dissertation Supervised

- **Joshua Bruce Fryman**, *SoftCache Architecture*, College of Computing, Georgia Institute of Technology, (Co-advised with Umakishore Ramachandran), August 2005. Current position: **Senior Principal Engineer and Engineering Manager at Intel Corp**, Hillsboro, OR.
- **Weidong Larry Shi**, *Architectural Support for Protecting memory Integrity and Confidentiality*, College of Computing, Georgia Institute of Technology, April 2006. Current position: **Associate Professor**, Computer Science Department, **University of Houston**, Houston, TX.
- **Taeweon Suh**, *Integration and Evaluation of Cache Coherence Protocols for Multiprocessor SOCs*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2006. Current position: **Professor**, Department of Computer Science and Engineering, **Korea University**, Seoul, South Korea.
- **Kiran Puttaswamy**, *Designing High-Performance Microprocessors in 3-D Integration Technology*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (Co-advised with Gabriel Loh), December 2007. Current position: Staff Engineer at Esperanto Technologies, Austin, TX.
- **Chinnakrishnan Ballapuram**, *Semantic-Oriented Low Power Architecture*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2008. Current position: **Director of Mobile Business Unit at Micron Technology**, CA.
- **Mrinmoy Ghosh**, *Microarchitectural Techniques to Reduce Energy Consumption in the Memory Hierarchy*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2009. Current position:Performance and Capacity Engineer at Facebook, Menlo Park, CA.
- **Dong Hyuk Woo**, *Designing Heterogeneous Many-Core Processors to Provide High Performance Under Limited Power Budget*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2010. Current position: **Technical Lead Manager (edgeTPU) at Google**, Mountain View, CA.
- **Nak Hee Seong**, *A Reliable, Secure Phase-Change Memory as Main Memory*, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2012. Current position: **Vice President at Samsung Electronics**, S. Korea.

- **Dean L. Lewis**, *Design for Pre-bond Testability in 3D Integrated Circuits*, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2012. Current position: Design Engineer at IBM, Burlington, VT.
- **Jen-Cheng Huang**, *Efficient Simulation Techniques for Large-scale Applications*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (Co-advised with Hyesoon Kim), 2015. Current position: Computer Architect at NVidia, CA.
- **Sungkap Yeo**, *Holistic Power Optimization for Datacenters*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (defense chaired by Tom Conte after I left), 2015. Current position: Software Engineer at Google, Pittsburgh, PA.

Master's Thesis Supervised

- Prateek Tandon, *High-Performance Advanced Encryption Standard (AES) Security Co-Processor Design*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2003. Current position: Principal Software Engineer, Microsoft, Seattle, WA.
- Aniket Naik, *Efficient Conditional Synchronization for Transactional Memory Based System*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (Co-advised with Milos Prvulovic), August 2006. Current position: Engineering Manager, Nvidia Corporation, Santa Clara, CA.
- **Fayez Mohamood**, *DLL-conscious Instruction Fetching for SMT Processors*, School of Electrical and Computer Engineering, Georgia Institute of Technology, August 2006. Current position: **Founder and CEO, Bluecore**, New York, NY.
- Richard M. Yoo, *Adaptive Transaction Scheduling for Transactional Memory Systems*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2008. Current position: Senior Software Engineer at Google, Cambridge, MA.
- Pratik Marolia, *Watermarking FPGA Bitstream for IP Protection*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2008. Current position: Senior System Architect at Intel Corporation, Hillsboro, OR.
- Vikas Rangaswamy Vasisht, *Architectural Support for Autonomic Protection Against Stealth by Rootkit Exploits*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2008. Current position: CPU Performance Architect, Intel Corporation, Austin, TX.
- Manoj Balanageswaran Athreya, *Subverting Linux On-the-fly using Hardware Virtualization Technology*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2010. Current position: Engineer, Apple, Cupertino, CA.

SCHOLARLY ACCOMPLISHMENTS

Invention Disclosure

I hold **31 US issued patents** in the areas of memory subsystem, secure non-volatile memory, 3D-IC, and physical design.

Publication

[Datacenter, Cloud, and Multi-core Computing]

DC1. Sungkap Yeo, Mohammad M. Hossain, Jen-Cheng Huang, and Hsien-Hsin S. Lee. "ATAC: Ambient Temperature-Aware Capping for Power Efficient Datacenters." In *Proceedings of the ACM Symposium on Cloud Computing*, pp.17.1-17.14, Seattle, WA, 2014.

DC2. Sungkap Yeo and Hsien-Hsin S. Lee. "Peeling the Power Onion of Data Centers." Chapter Three In *Energy Efficient Thermal Management of Data Centers* by Yogendra Joshi and Pramod Kumar (Editors), pp.137-168, Springer, 2012.

DC3. Mohammad M. Hossain, Jen-Cheng Huang, and Hsien-Hsin S. Lee. "Migration Energy-Aware Workload Consolidation in Enterprise Clouds." In *Proceedings of?the IEEE International Conference on Cloud Computing Technology and Science*, pp.405-410, December, 2012.

DC4. Sungkap Yeo and Hsien-Hsin S. Lee. "SimWare: A Holistic Warehouse-scale Computer Simulator." In *IEEE Computer Special Issue on Modeling and Simulation of Smart and Green Computing Systems*, Vol. 35, No. 9, pp.48-55, 2012.

DC5. Sungkap Yeo and Hsien-Hsin S. Lee. "Using Mathematical Modeling in Provisioning a Heterogeneous Cloud Computing Environment." In *IEEE Computer*, Vol. 44, No. 8, pp. 55-62, August, 2011.

DC6. Mrinmoy Ghosh, Ripal Nathuji, Min Lee, Karsten Schwan, and Hsien-Hsin S. Lee. "Symbiotic Scheduling for Shared Caches in Multi-Core Systems Using Memory Footprint Signature." In *Proceedings of the 40th IEEE International Conference on Parallel Processing (ICPP-2011)*, Taipei, Taiwan, pp.11 - 20, September, 2011. (Acceptance rate = 22%, 81/363)

DC7. Sung Woo Chung, Hsien-Hsin S. Lee, and Woo Hyong Lee. "Architecture/OS Support for Embedded Multi-core Systems." In *The Computer Journal*, vol.53, no.8, pp.1134-1135, 2010.

DC8. Dong Hyuk Woo and Hsien-Hsin S. Lee. "PROPHET: Goal-Oriented Provisioning for Highly Tunable Multicore Processors in Cloud Computing." In *ACM SIGOPS Operating Systems Review special issue on the Interaction among the OS, Compilers, and Multicore Processors*, Vol.43, Issue 2, pp.102-103, April, 2009.

DC9. Michael Healy, Hsien-Hsin S. Lee, Gabriel H. Loh, and Sung Kyu Lim. "Thermal optimization in Multigranularity Multi-Core Floorplanning." In *Proceedings of the 14th IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC'09)*, pp.43-48, Yokohama, Japan, January, 2009.

DC10. Dong Hyuk Woo and Hsien-Hsin S. Lee. "Extending Amdahl's Law for Energy-Efficient Computing in the Many-Core Era." In *IEEE Computer*, Vol.41, No.12, pp.24-31, December, 2008.

DC11. Richard M. Yoo and Hsien-Hsin S. Lee, "Adaptive Transaction Scheduling for Transactional Memory Systems." In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA) in the Special Track on Hardware and Software Techniques to Improve the Programmability of Multicore Machines*, pp. 169-178, Munich, Germany, 2008.

DC12. Richard M. Yoo, Yang Ni, Adam Welc, Bratin Saha, Ali-Reza Adl-Tabatabai, and Hsien-Hsin S. Lee, "Kicking the Tires of Software Transactional Memory: Why the Going Gets Tough." In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA) in the Special Track on Hardware and Software Techniques to Improve the Programmability of Multicore Machines*, pp.265-274, Munich, Germany, 2008.

DC13. Richard M. Yoo and Hsien-Hsin S. Lee. "Helper Transactions: Enabling Thread-Level Speculation via A Transactional Memory System." In *Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures (PESPMA) in Conjunction with ACM/IEEE International Symposium on Computer Architecture (ISCA-35)*, Beijing, China, June 2008.

DC14. Taeweon Suh, Daehyun Kim, and Hsien-Hsin S. Lee, "Cache Coherence Support for Non-Shared Bus Architecture on Heterogeneous MP SoCs." In *Proceedings of the 42nd Design Automation Conference (DAC-42)*, pp.553-558, Anaheim, California, June 2005. (acceptance rate=20%)

DC15. Taeweon Suh, Hsien-Hsin S. Lee, and Douglas M. Blough, "Integrating Cache Coherence Protocols for Heterogeneous Multiprocessor Systems. Part 2." In *IEEE MICRO special issue on Embedded Systems: Architecture, Design and Tools*, pp.70-78, September/October 2004.

DC16. Taeweon Suh, Hsien-Hsin S. Lee, and Douglas M. Blough, "Integrating Cache Coherence Protocols for Heterogeneous Multiprocessor Systems. Part 1." In *IEEE MICRO special issue on Embedded Systems: Architecture, Design and Tools*, pp.33-41, July/August 2004.

DC17. Taeweon Suh, Douglas M. Blough and Hsien-Hsin S. Lee, "Supporting Cache Coherence in Heterogeneous Multiprocessor Systems." In *Proceedings of the Design Automation and Test in Europe Conference (DATE'04)*, pp.1150-1155, Paris, France, February 2004. (acceptance rate = 23.2%, 181/780)

[**GPU and Heterogeneous Architecture**]

GP1. Jen-Cheng Huang, Joo Hwan Lee, Hyesoon Kim, and Hsien-Hsin S. Lee. "GPUMech: GPU Performance Modeling Technique Based on Interval Analysis." In *Proceedings of the 47th IEEE/ACM International Symposium on Microarchitecture (MICRO-47)*, pp.268-279, Cambridge, England, December, 2014.

GP2. Jen-Cheng Huang, Lifeng Nai, Hyesoon Kim, and Hsien-Hsin S. Lee. "TBPoint: Reducing Simulation Time for Large Scale GPGPU Kernels." In *Proceedings of the 28th International Parallel and Distributed Processing Symposium (IPDPS)*, pp.437-446, Phoenix, AZ, 2014.

GP3. Hong Jun Choi, Dong Oh Son, Seung Gu Kang, Jong Myon Kim, Hsien-Hsin S. Lee, and Cheol Hong Kim. "An Efficient Scheduling Scheme Using Estimated Execution Time for Heterogeneous Computing Systems." In *Journal of Supercomputing*, 65(2), pp.886-902, 2013.

GP4. Abderrahim Benquassmi, Eric Fontaine, and Hsien-Hsin S. Lee. "Parallelization of Katsevich CT Image Reconstruction Algorithm on Generic Multi-Core Processors and GPGPU." In *GPU Computing GEMS, Section 10 Medical Imaging, Chapter 31*, Wen-Mei Hwu (editor-in-chief), pp.659-677, Morgan Kaufmann Publishers, 2011.

GP5. Dong Hyuk Woo and Hsien-Hsin S. Lee. "COMPASS: A Programmable Data Prefetcher Using Idle GPU Shaders." In *Proceedings of the 16th IEEE International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XV)*, pp.297-309, Pittsburgh, PA, March, 2010. (Acceptance rate = 17.7%, 32/181)

GP6. Ahmad Sharif and Hsien-Hsin S. Lee. "Total Recall: A Debugging Framework for GPUs." In *Proceedings of the ACM SIGGRAPH/Eurographics Workshop of Graphics Hardware (GH-08)*, pp.13-20, Sarajevo, Bosnia-Herzegovina, June, 2008.

GP7. Eric Fontaine and Hsien-Hsin S. Lee, "Optimizing Katsevich Image Reconstruction Algorithm on Multicore Processors." In *Proceedings of the 13th IEEE International Conference on Parallel and Distributed Systems (ICPADS-07)*, Hsinchu, Taiwan, December, 2007.

GP8. Dong Hyuk Woo, Joshua B. Fryman, Allan D. Knies, Marsha Eng, and Hsien-Hsin S. Lee, "POD: A Parallel On-Die Architecture." In *Proceedings of the 11th Annual Workshop on High Performance Embedded Computing (HPEC)*, Lexington, Massachusetts, September, 2007. (**Award Session**)

GP9. Dong Hyuk Woo, Joshua B. Fryman, Allan D. Knies, and Hsien-Hsin S. Lee. "Chameleon: Virtualizing Idle Acceleration Cores of A Heterogeneous Multi-Core Processor for Caching and Prefetching." In *ACM Transactions on Architecture and Code Optimization*, vol.7, no.1, pp.1-35, April, 2010.

[**Security Architecture and Dependable Systems**]

SA1. Jen-Cheng Huang, Matteo Monchiero, Yoshio Turner, and Hsien-Hsin S. Lee. "Ally: OS-Transparent Packet Inspection Using Sequestered Cores." In *Proceedings of the ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS-11)*, pp. 1 - 11, Brooklyn, NY, October, 2011. (Acceptance rate = 32%, 20/62) (**Best Paper Award of ANCS-11**.)

SA2. Jun Yang, Lan Gao, Youtao Zhang, Marek Chrobak, and Hsien-Hsin S. Lee. "A Low-Cost Memory Remapping Scheme for Address Bus Protection" In *Journal of Parallel and Distributed Computing*, vol.70, issue 5, pp.443-457, May 2010.

SA3. Vikas R. Vasisht and Hsien-Hsin S. Lee. "SHARK: Architectural Support for Autonomic Protection Against Stealth by Rootkit Exploits." In *Proceedings of the 41st ACM/IEEE International Symposium on Microarchitecture (MICRO-41)*, pp.106-116, Lake Como, Italy, November, 2008. (Acceptance rate = 19%, 40/210.)

SA4. Weidong Shi and Hsien-Hsin S. Lee, "Accelerating Memory Decryption and Authentication with Frequent Value Prediction." In *Proceedings of the ACM International Conference on Computing Frontiers (CF'07)*, pp.35-46, Ischia, Italy, May, 2007.

SA5. Weidong Shi, Chenghuai Lu, and Hsien-Hsin S. Lee, "Memory-centric Security Architecture." Invited article. In *Transactions of High Performance Embedded Architectures and Compilers*, Vol.1, pp.95-115, 2007. Springer Verlag.

SA6. Dong Hyuk Woo and Hsien-Hsin S. Lee, "Analyzing Performance Vulnerability due to Resource Denial-of-Service Attack on Chip Multiprocessors." In *Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMPMSI) in conjunction with the 13th International Symposium on High-Performance Computer Architecture (HPCA-13)*, Phoenix, Arizona, February, 2007.

SA7. Weidong Shi, and Hsien-Hsin S. Lee, "Authentication Control Point and its Implications for Secure Processor Design." In *Proceedings of the ACM/IEEE International Symposium on Microarchitecture (MICRO-39)*, pp.103-112, Orlando, Florida, December, 2006. (acceptance rate = 24.1%, 42/174)

SA8. Chenghuai Lu, Tao Zhang, Weidong Shi, and Hsien-Hsin S. Lee, "M-TREE: A High Efficiency Security Architecture for Protecting Integrity and Privacy of Software." In *Journal of Parallel and Distributed Computing, Special Issue on Security in Grid and Distributed Systems*, Vol.66, Issue 9, pp.1116-1128, 2006. (acceptance rate =12.2%, 10/82.)

SA9. Weidong Shi, Hsien-Hsin S. Lee, Richard M. Yoo, and Alexandra Boldyreva, "A Digital Rights Enabled Graphics Processing System." In *Proceedings of the ACM SIGGRAPH/Eurographics Workshop of Graphics Hardware*, pp.17-26, Vienna, Austria, September 2006. (acceptance rate = 31.1%, 14/45)

SA10. Lan Gao, Jun Yang, Marek Chrobak, Youtao Zhang, San Nguyen, and Hsien-Hsin S. Lee, "A Low-cost Memory Remapping Scheme for Address Bus Protection." In *Proceedings of the 15th International Conference on Parallel Architecture and Compilation Techniques (PACT'06)*, pp.74-83, Seattle, WA, September 2006. (acceptance rate = 25.6%, 30/117)

SA11. Weidong Shi, Hsien-Hsin S. Lee, Laura Falk, and Mrinmoy Ghosh, "An Integrated Framework for Dependable and Revivable Architecture Using Multicore Processors." In *Proceedings of the 33rd International Symposium on Computer Architecture (ISCA-33)*, pp.102-113, Boston, MA, June 2006. (acceptance rate = 13%, 31/231)

SA12. Weidong Shi, Joshua B. Fryman, Guofei Gu, Hsien-Hsin S. Lee, Youtao Zhang, and Jun Yang, "InfoShield: A Security Architecture for Protecting Information Usage in Memory." In *Proceedings of the 12th International Conference on High Performance Computer Architectures (HPCA-12)*, pp.225-234, Austin, Texas, February 2006. (acceptance rate=14%)

SA13. Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu, and Mrinmoy Ghosh, "Towards the Issues in Architectural Support for Protection of Software Execution." In *ACM SIGARCH Computer Architecture News*, Vol. 33, Issue 1, pp.6-15, March 2005.

SA14. Weidong Shi, Chenghuai Lu, and Hsien-Hsin S. Lee, "Memory-centric Security Architecture." In *Proceedings of the 2005 International Conference on High Performance Embedded Architectures and Compilers (HiPEAC 2005)*, pp.153 - 168, Barcelona, Spain, November 2005. (acceptance rate=20.2%, 17/84)

SA15. Weidong Shi, Hsien-Hsin S. Lee, Guofei Gu, Mrinmoy Ghosh, Laura Falk, and Trevor Mudge, "Intrusion Tolerant and Self-recoverable Network Service System Using Security Enhanced Chip Multiprocessor." In *Proceedings of the 2nd IEEE International Conference on Autonomic Computing (ICAC-05)*, pp.263-273, Seattle, WA, June 2005. (acceptance rate of regular papers = 16.7%, 25/150)

SA16. Weidong Shi, Hsien-Hsin S. Lee, Mrinmoy Ghosh, Chenghuai Lu, and Alexandra Boldyreva, "High Efficiency Counter Mode Security Architecture via Prediction and Precomputation." In Proceedings of the 32nd International Symposium on Computer Architecture (ISCA-32), pp.14-24, Madison, Wisconsin, June 2005. (acceptance rate = 23.2%, 45/194)

SA17. Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu and Tao Zhang, "Attacks and Risk Analysis for Hardware Supported Software Copy Protection Systems." In *Proceedings of the 4th ACM Workshop on Digital Right Management (DRM'2004)*, pp.54-62, Washington D.C., October 2004.

SA18. Weidong Shi, Hsien-Hsin S. Lee, Mrinmoy Ghosh, and Chenghuai Lu, "Architectural Support for High Speed Authentication of Shared Memory in Multiprocessor Systems." In *Proceedings of the International Conference on Parallel Architecture and Compilation Techniques (PACT'04)*, pp. 123 - 134, Antibes Juan-les-Pins, France, September 2004. (acceptance rate = 18.8%, 23/122)

SA19. Xiaotong Zhuang, Tao Zhang, Hsien-Hsin S. Lee and Santosh Pande, "Hardware Assisted Control Flow Obfuscation for Embedded Processors." In *Proceedings of the International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES'04)*, pp. 292 - 302, Washington D.C., September 2004. (acceptance rate=25.2%, 31/123) . (**Best Paper Award of CASES 2004**.)

SA20. Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu, and Mrinmoy Ghosh, "Toward the Issues in Architectural Support for Protection of Software Execution." In *Workshop on Architectural Support for Security and Anti-Virus (WASSA) in conjunction with the 11th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-XI)*, pp.1-9, Boston, Massachusetts, October 2004.

[Energy Efficient Design]

EE1. Mrinmoy Ghosh, Simon Ford, Emre Ozer, Stuart Biles, and Hsien-Hsin S. Lee. "Way Guard: A Segmented Counting Bloom Filter Approach to Reducing Energy for Set-Associative Caches." In *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED-09)*, pp.165-170, San Francisco, CA, August, 2009. (**Selected as one of seven papers of ISLPED highlight for publicity and press.**)

EE2. Hrishikesh Amur, Ripal Nathuji, Mrinmoy Ghosh, Karsten Schwan, and Hsien-Hsin S. Lee. "IdlePower: Application-Aware Management of Processor Idle States." In *Workshop on Managed Many-Core Systems (MMCS) co-located with ACM/IEEE International Symposium on High Performance Distributed Computing (HPDC)*, Boston, MA, June, 2008.

EE3. Chinnakrishnan S. Ballapuram, Ahmad Sharif, and Hsien-Hsin S. Lee, "Exploiting Access Semantics and Program Behavior to Reduce Snoop Power in Chip Multiprocessors." In *Proceedings of the 13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XIII)*, pp.60-69, Seattle, WA, 2008. (acceptance rate = 31/127, 24.4%)

EE4. Chinnakrishnan S. Ballapuram and Hsien-Hsin S. Lee, "Improving TLB Energy for Java Applications on JVM." In *Proceedings of the International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS VIII)*, pp.218-223, Samos, Greece, 2008.

EE5. Mrinmoy Ghosh and Hsien-Hsin S. Lee, "Virtual Exclusion: An Architectural Approach to Reducing Leakage Energy in Caches for Multiprocessor Systems." In *Proceedings of the 13th IEEE International Conference on Parallel and Distributed Systems (ICPADS-07)*, Hsinchu, Taiwan, December, 2007.

EE6. Dong Hyuk Woo, Mrinmoy Ghosh, Emre Ozer, Stuart Biles and Hsien-Hsin S. Lee, "Reducing Energy of Virtual Cache Synonym Lookup using Blooming Filters." In *Proceedings of the International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES'06)*, pp.179-189, Seoul, Korea, October, 2006. (Regular paper acceptance rate = 24.3%, 25/103)

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ML2. Udit Gupta, Young Geun Kim, Sylvia Lee, Jordan Tse, Hsien-Hsin S. Lee, Gu-Yeon Wei, David Brooks, Carole-Jean Wu. "Chasing Carbon: The Elusive Environmental Footprint of Computing." In *Proceedings of the IEEE International Symposium on High-Performance Computer Architecture (HPCA-27)*, Seoul, South Korea, February, 2021.

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BG1. Carole-Jean Wu, David Brooks, Udit Gupta, Hsien-Hsin Sean Lee, and Kim Hazelwood. "Deep Learning: It's Not All About Recognizing Cats and Dogs", ACM SIGARCH Blog, November, 2019.

BG2. Hsien-Hsin Sean Lee. "The First Trillion-Transistor Chip: A New Design Space", ACM SIGARCH Blog, August, 2019.