Hsien-Hsin Sean Lee (李憲信), Ph.D.

lee.sean@gmail.com Tel: 1-650-709-9452 (Cell)
https://hsienhsinlee.github.io/ LinkedIn Profile

EDUCATION

University of Michigan, Ann Arbor, USA
Ph.D. in Computer Science and Engineering 2001
Dissertation Title: *Improving Energy and Performance of Data Cache Architectures by Exploiting Memory Reference Characteristics.*
Horace H. Rackham Distinguished Dissertation Award, University of Michigan.
Nominated by University of Michigan for ACM Doctoral Thesis Award.

University of Michigan, Ann Arbor, USA
M.S.E. in Computer Science and Engineering 1994

National Tsing-Hua University, Hsinchu, Taiwan
B.S. in Electrical Engineering 1990
Valedictorian of the Class 1990 (90級畢業生致答詞代表)

EMPLOYMENT

Facebook Inc., Cambridge, MA
Area Research Lead, Facebook AI Research March 2020 - Present
Research Head, AI Infrastructure Research Jan 2019 - Feb 2020

- Build a new research team from scratch specialized in computing systems at Boston.
- Lead a group of researchers to perform on high-efficiency, high-throughput, and privacy-preserving machine learning research for datacenter infrastructure and explore new technologies for on-device AI.
- Establish academic relations with universities worldwide.

Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC), Hsinchu, Taiwan April 2012 - Jan 2019
Deputy Director, Design Methodology and Kits Development Division

- Manage 6 departments (155 R&D staff across Taiwan, China, and US) developing IC design methodology and process design kits (PDK) for all TSMC customers.
- Lead design enablement across TSMC R&D, EDA (Synopsys, Cadence, Mentor, ANSYS, etc.), and fabless design houses.
- Technology owner of design collaterals for all TSMC process nodes and integration/packaging technologies (2.5D/3DIC).
- Technology owner of EDA tool certification programs for physical design sign-off tools, custom design flow, and SPICE simulators.
- Technology owner of machine learning applications to improve the quality of physical verification.

Georgia Institute of Technology, Atlanta, GA
Associate Professor (Tenured), School of Electrical and Computer Engineering July 2008 - June 2014
Assistant Professor, School of Electrical and Computer Engineering Aug 2002 - June 2008

- Green data centers (NSF, State of Georgia).
- 3D-IC architecture, design-for-test, physical design, & prototyping (DoD, NSF, SRC MARCO centers).
- Emerging memory architecture (IBM, Intel).
- Transactional memory and speculative multithreading (NSF).
- Secure processor architecture (NSF, DoE).

- FPGA-based accelerators and system-wide monitoring (NSF).
- Adjunct faculty member of joint degree program at Shanghai Jiao Tong University (2011) and Korea University (2008-2010).

Agere Systems, Atlanta, GA July 2001 - August 2002
Architecture Manager, StarCore DSP Technology Center of Agere Systems and Motorola, Inc.

- Managed 10 CPU/DSP architects from Lucent/Agere and Motorola.
- Owner of a 1GHz StarCore DSP architecture design for 3G infrastructure, including the VLES ISA, architecture simulators, and performance benchmarking.

Intel Corporation, Santa Clara, CA May 1999 - July 2001
Researcher, Programming Systems Lab, MRL

- Research on computation reuse of IA64 architecture.
- Exploitation of instruction-level parallelism for advanced Itanium architecture.

Intel Corporation, Folsom, CA October 1995 - April 1999
Senior Processor Architect, Microprocessor Division 6

- Performance architect for Timna and Katmai (Pentium-III).
- Pentium III post-silicon validation.
- Pentium III SSE/prefetch instruction definition and microarchitecture development.
- Coded Microsoft Direct3D 6.1 API using SSE ISA (assembly level).
- Owner of Intel 3D Geometry Performance Roadmap.

HONOR AND AWARDS

- IEEE Fellow, class of 2017. *Citation: for contributions to 3D integrated circuits and computer architecture.*
- 10-year Most Significant Paper Award. *International Test Conference (ITC)*, 2017. (Paper 3D19)
- Class of 1934 Course Survey Teaching Effectiveness Award, Georgia Tech, 2012.
- Best Paper Award. *The ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS 2011)*, NY, 2011. (Paper SA1)
- IBM Faculty Award, 2011.
- Honorable Mention. IEEE Micro Top Picks from the Computer Architecture Conferences of 2020. (Paper ML5)
- Top Pick. IEEE Micro Top Picks from the Computer Architecture Conferences of 2010. (Paper MM5)
- NSF CAREER Award, 2007.
- ECE Outstanding Junior Faculty Award, Georgia Tech, 2006.
- Department of Energy Early CAREER Principal Investigators Award, 2005.
- Best Paper Award. *The 2nd Watson Conference on Interaction Between Architecture, Circuits and Compilers ($P = AC^2$)*, NY, 2005. (Paper uA5)
- Best Paper Award. *The 2004 ACM/IEEE International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES-2004)*, Washington DC, 2004. (Paper SA19)
- Horace H. Rackham Distinguished Dissertation Award, University of Michigan, 2001.
- Best Paper Award. *The 33rd ACM/IEEE International Symposium on Microarchitecture (MICRO-33)*, Monterey, CA, 2000. (Paper MM12)
- Intel Foundation Fellowship, 2000-2001.
- University of Michigan Research Fellowship, 1993.

- Valedictorian of the Class 1990, National Tsing-Hua University, 1990. (90級畢業生致答詞代表)
- Chancellor Mei Yi-Chi Memorial Award, National Tsing-Hua University, 1989. (梅貽琦紀念獎章)

COURSES TAUGHT and DEVELOPED

- **ECE2030 Introduction to Computer Systems.** I designed a few creative term projects (in different semesters) to help students to solve real and interesting logic and computer design problems and to understand machine-level operations using MIPS assembly programming. For example, one project asked students to design a decryption algorithm using MIPS assembly languages by reverse-engineering the ciphertext that I provided. Another example is a project to find the perfect number (equivalent to the summation of its own factors) for a given range. Both projects require algorithmic designs at the machine instruction level. Students learn not only how to program at machine level assembly languages, but also brainstorm ideas with respect to how to accelerate their programs for higher efficiency.
- **ECE3055 Computer Architectures and Operating Systems.** I offered this course every other year based on the materials developed by several other faculty including myself.
- **ECE4100/6100 Advanced Computer Architecture.** I renovated the materials and designed new course projects to increase students' understanding on crucial microarchitectural modules in modern microprocessors and familiarize them with the design tools. The projects include an instruction cache enhanced with victim cache (in structural Verilog model), an Alpha 21264-like tournament hybrid branch predictor (in behavioral Verilog model), latest branch predictors (*e.g.,* perceptron predictor, O-GEHL predictor, etc.), and a dynamic instruction scheduler (in behavioral Verilog model), and a MOESI cache coherence protocol (in C/C++). These projects imitate how these crucial microarchitectural modules were designed in a real processor design team and help students drive the algorithm-level concepts learned in class into functional designs at the logic gate level.
- **ECE4893 Multicore and GPU Programming for Video Games.** Dr. Aaron Lanterman and I designed this new course to respond to the timely demand for computer engineers in the GPU, 3D gaming, and parallel application industries. This class focuses on the hardware architecture design and programming model for the emerging multi-core processors and GPGPUs. Several mini-projects based on widely used API (Microsoft Direct3D), shader language (HLSL/Cg), and development environment (Microsoft XNA) were designed to enrich students' experiences and develop their programming skills on these special purpose processors. The projects were designed to run on the latest Nvidia GeForce graphics cards and Cell Blades in the Cell Center of Competence.
- **ECE7102 RISC Architectures.** This course was completely renovated to focus on latest developments in microarchitecture research. In addition, in-depth design details of commercial high-performance microprocessors such as EPIC from Intel/HP and Pentium 4 from Intel were also incorporated into the course materials. Simplescalar, the most popular architecture simulator adopted in academia was used in this course. Programming assignments based on Simplescalar were designed for students to learn how to perform microarchitecture research by using this toolkit.
- **CS8001 Computer Architecture Seminar.** Computer architecture faculty from both ECE and CS co-managed this weekly meeting to discuss the latest research and industry trend in the general area of computer architecture. I was one of the most senior faculty members among them to organize this reading group since 2002. It became a credit course for those who are doing or interested in computer architecture research.
- **CS8803 Language and Compiler for Embedded Systems.** Dr. Santosh Pande of CS and I developed this course for a dual-degree master program offered by Georgia Tech and Korea University. The course targets higher education in embedded software for engineers from Korean industry including Samsung, LG, and Korean Telecom. I developed several course modules and class projects emphasizing on the design of instruction set architecture for embedded system, high performance techniques for exploiting instruction-level parallelism (ILP) in embedded software, code compression techniques, real-time scheduling for embedded systems, and embedded security issues. Two projects developed for

this course. The first project is to build a control-flow graph for given VLIW codes and find the ILP for them; the second one is to implement and evaluate the compression efficiency for a few code compression techniques including one similar to the method used by IBM CodePack and one dictionary-based compression algorithm.

- **ECE8833 Polymorphic and Many-Core Computer Architecture.** I developed this special topic course with an intent to replace the existent ECE7102. The content covers classical work in computer architecture as well as the latest, emerging issues and research topics in the field. The students are required to form a two- to three-people's team and propose a research project for their term project.

RESEARCH SUPERVISION

Ph.D. Dissertation Supervised

- **Joshua Bruce Fryman**, *SoftCache Architecture*, College of Computing, Georgia Institute of Technology, (Co-advised with Umakishore Ramachandran), August 2005. Current position: **Senior Principal Engineer and Engineering Manager at Intel Corp**, Hillsboro, OR.
- **Weidong Larry Shi**, *Architectural Support for Protecting memory Integrity and Confidentiality*, College of Computing, Georgia Institute of Technology, April 2006. Current position: **Associate Professor**, Computer Science Department, **University of Houston**, Houston, TX.
- **Taeweon Suh**, *Integration and Evaluation of Cache Coherence Protocols for Multiprocessor SOCs*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2006. Current position: **Professor**, Department of Computer Science and Engineering, **Korea University**, Seoul, South Korea.
- **Kiran Puttaswamy**, *Designing High-Performance Microprocessors in 3-D Integration Technology*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (Co-advised with Gabriel Loh), December 2007. Current position: Senior Staff Verification Lead at Esperanto Technologies, Austin, TX.
- **Chinnakrishnan Ballapuram**, *Semantic-Oriented Low Power Architecture*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2008. Current position: **Director of Mobile Business Unit at Micron Technology**, CA.
- **Mrinmoy Ghosh**, *Microarchitectural Techniques to Reduce Energy Consumption in the Memory Hierarchy*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2009. Current position: Performance and Capacity Engineer at Facebook, Menlo Park, CA.
- **Dong Hyuk Woo**, *Designing Heterogeneous Many-Core Processors to Provide High Performance Under Limited Power Budget*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2010. Current position: **Technical Lead Manager (edgeTPU) at Google**, Mountain View, CA.
- **Nak Hee Seong**, *A Reliable, Secure Phase-Change Memory as Main Memory*, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2012. Current position: **Vice President at Samsung Electronics**, S. Korea.
- **Dean L. Lewis**, *Design for Pre-bond Testability in 3D Integrated Circuits*, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2012. Current position: Test and Characterization Engineer at IBM, Burlington, VT.
- **Jen-Cheng Huang**, *Efficient Simulation Techniques for Large-scale Applications*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (Co-advised with Hyesoon Kim), 2015. Current position: Computer Architect at NVidia, CA.
- **Sungkap Yeo**, *Holistic Power Optimization for Datacenters*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (defense chaired by Tom Conte after I left), 2015. Current position: Software Engineer at Google, Pittsburgh, PA.

Master's Thesis Supervised

- Prateek Tandon, *High-Performance Advanced Encryption Standard (AES) Security Co-Processor Design*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2003. Current position: Principal Software Engineer, Microsoft, Seattle, WA.
- Aniket Naik, *Efficient Conditional Synchronization for Transactional Memory Based System*, School of Electrical and Computer Engineering, Georgia Institute of Technology, (Co-advised with Milos Prvulovic), August 2006. Current position: Engineering Manager, Nvidia Corporation, Santa Clara, CA.
- **Fayez Mohamood**, *DLL-conscious Instruction Fetching for SMT Processors*, School of Electrical and Computer Engineering, Georgia Institute of Technology, August 2006. Current position: **Founder and CEO, Bluecore**, New York, NY.
- Richard M. Yoo, *Adaptive Transaction Scheduling for Transactional Memory Systems*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2008. Current position: Devices Security Lead at Verily Life Sciences, an Alphabet subsidiary, San Francisco, CA.
- Pratik Marolia, *Watermarking FPGA Bitstream for IP Protection*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2008. Current position: Software Engineer at Google, Mountain View, CA.
- Vikas Rangaswamy Vasisht, *Architectural Support for Autonomic Protection Against Stealth by Rootkit Exploits*, School of Electrical and Computer Engineering, Georgia Institute of Technology, December 2008. Current position: Server Performance Architect, AMD, Austin, TX.
- Manoj Balanageswaran Athreya, *Subverting Linux On-the-fly using Hardware Virtualization Technology*, School of Electrical and Computer Engineering, Georgia Institute of Technology, April 2010. Current position: Engineer, Apple, Cupertino, CA.

Undergraduate Researchers Supervised

- **Ilya (Khorosh) Tillis**, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2011. Current position: **Director, GitHub, Microsoft**, Raleigh, NC.
- Xiaodong Wang, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2011. Current position: Research Scientist, Facebook, Menlo Park, CA.
- Gregory Diamos, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2006. Current position: Engineering Lead, Landing AI, CA.
- **June Paik** (Joonho Baek), School of Electrical and Computer Engineering, Georgia Institute of Technology, 2006. Current position: **Founder and CEO, Furiosa AI**, Seoul, Korea.
- Anirudh Saria, School of Electrical and Computer Engineering, Georgia Institute of Technology, 2004. Current position: Senior Program Manager, Microsoft, Redmond, WA.

UNIVERSITY APPOINTED SERVICE

- Search Committee Member for the *Rhesa "Ray" S. Farmer, Jr. Distinguished Chair in Embedded Computer Systems*, 2006.
- Chair of the Computer Engineering Curriculum Subcommittee, October 2009 - 2011.
- Search Committee Member for ECE School Chair, 2011 - Present.

PROFESSIONAL SERVICE

Professional Community

- Industry Advisory Board Member, Department of Computer Science, University of Central Florida, 2021 - Present.
- IEEE Fellows Committee, 2018, 2019.
- Search Committee Chair for IEEE Micro Editor-in-Chief, 2018.
- Executive Committee Member, IEEE Technical Committee on Computer Architecture, 2017 - 2019.
- Industry Advisory Board Member, IEEE Computer Society, 2016 - Present.

Editorial Boards

- Editorial Board Member, *IEEE Micro Magazine*, 2016 - Present.
- Guest Editor, *IEEE Micro Special Issue on Commercial Products*, 2021.
- Guest Editor, *IEEE Micro Special Issue on Automotive Computing*, 2018.
- Associate Editor, *IEEE Transactions on Computers (IEEE TC)*, 2012 - 2015.
- Associate Editor, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, 2010 - 2013.
- Associate Editor, *ACM Transactions on Architecture and Code Optimization (ACM TACO)*, 2009 - 2015.

Major Conference/Workshop Organizers

- Program Chair of Industry Track, *the 48th ACM/IEEE International Symposium on Computer Architecture (ISCA-48)*, Valencia, Spain, 2021.
- Program Co-Chair, *the 49th ACM/IEEE International Symposium on Microarchitecture (MICRO-49)*, Taipei, Taiwan, 2016.
- Workshop Co-Organizer, *the CLEAR Workshop on Computing Landscapes for Environmental Accountability and Responsibility collocated with ISCA-48*, 2021.
- Workshop Co-Chair, *International Workshop on Parallelism in Mobile Platforms (PRISM) collocated with ISCA*, 2013-2018.
- Steering Committee, *the IEEE International Symposium on Workload Characterization (IISWC 2011)*, 2011-Present.
- General Chair, *the IEEE International Symposium on Workload Characterization (IISWC 2010)*, Atlanta, GA, 2010.
- Tutorial and Workshop Chair, *the 43rd International Symposium on Microarchitecture (MICRO-43)*, Atlanta, GA, 2010.

Major Technical Program Committee

I served as a program committee member for more than 100 conferences and workshops. Highlights are:

- IEEE MICRO Top Picks: 2013, 2014, 2016, 2017, 2018.
- International Symposium on Computer Architecture (ISCA): 2006, 2008, 2012, 2014, 2015, 2018, 2019, 2020, 2021 (PC Chair, Industry Track)
- International Symposium on Microarchtiecture (MICRO): 2010, 2014, 2015, 2016 (Program Co-Chair), 2020, 2021.
- International Conference on High-Performance Computer Architecture (HPCA): 2007, 2016, 2021.
- International Conference on Compiler, Architectures, Synthesis for Embedded Systems (CASES): 2004, 2005, 2006, 2007, 2008.

- International Conference on Computer Design (ICCD): 2005, 2006, 2007, 2008, 2009, 2011, 2012.
- Design, Automation and Test in Europe (DATE): 2013, 2014, 2015.
- Asia and South Pacific Design Automation Conference (ASP-DAC): 2012, 2013, 2014.

Keynote Speeches and Key Conference Panelists

- Keynote Speech: "Challenges of Modern Computing on Social Network Platform" in *Research Summit at the Center for Unstoppable Computing*, University of Chicago, 2021.
- NSF Keynote Speech: "When Memory Meets ML on Social Network Platform" in *NSF Workshop on Processing-In-Memory Technology*, National Science Foundation, 2021.
- ISCA Panelist: "Data Center Architecture" in *the 47th ACM/IEEE International Symposium on Computer Architecture (ISCA-47)*, 2020. (with David Brooks and Christina Delimitrou)
- ECE Distinguished Lecture Series: "Machine Learning on Social Network Platform" in George Washington University, Washington D.C., 2020.
- CASPA Keynote Speech: "The Computing Frontiers of Social Network" in *Chinese American Semiconductor Professional Association(CASPA) 2019 Annual Conference*, Fremont, CA, 2019.
- ISPLED Keynote Speech: "The Computing Frontiers of Social Network" in *ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED-2019)*, Lausanne Switzerland, 2019.
- DAC Panelist: "Will the Era of AI Drive Emerging Technologies to Overtake CMOS?" in *Design Automation Conference (DAC-55)*, San Francisco, CA, 2018. (with An Chen, Geoffrey Burr, Meng-Fan Marvin Chang, and Kaushik Roy.)
- ISSCC Panelist: "Can Artificial Intelligence Replace My Job? The Dawn of a New IC Industry with AI" in *International Solid-State Circuits Conference (ISSCC-2018)*, San Francisco, CA, 2018. (with Bill Dally, Georges Gielen, Antun Domic, Seung Hoon Tong, and Dario Gil.)
- ISCA Panelist: "Is the Death of Moore's Law Making Computer Architecture Livelier Than Ever?" in *the 44th ACM/IEEE International Symposium on Computer Architecture (ISCA-44)*, Toronto, Canada, 2017. (with Mark Hill, Sandhya Dwarkadas, and Babak Falsafi.)
- ISSCC Forum Speaker: "Ecosystem of Design for Security" in *Design Forum of Designing Secure Systems: Manufacturing, Circuits and Architectures, International Solid-State Circuits Conference (ISSCC-2016)*, San Francisco, CA, 2016.
- Distinguished Speaker Colloquium, "3D Integration" in *the Computer & Information Science & Engineering Department*, University of Florida, Gainesville, FL, March 5, 2010.

RESEARCH GRANTS

Research Grants from Federal Agency

GF1. **National Science Foundation (NSF):** "ITR: Toward Autonomous Computing Platforms: System-Wide Hardware/Software Performance Monitoring and Adaptation." Co-PI with Sally McKee (Cornell), $814,000 (Lee's allocation: $407,000.) 10/2003 - 09/2009.

GF2. **National Science Foundation (NSF):** "ITR: Morphable Software Services: Self-Modifying Programs for Distributed Embedded Systems Organization: National Science Foundation." Co-PI with Karsten Schwan , Tucker Balch, Greg Eisenhauer, Santosh Pande, Calton Pu. (Lee was listed as a senior personnel.) $1,033,775. (Lee's allocation: $147,683.) 10/2003 - 05/2007.

GF3. **US Department of Energy (DoE) Early CAREER PI Award:** "Toward Highly Secure and Autonomic Computing Systems: A Hierarchical Approach." PI, $299,755. 08/2005 - 08/2009. (Georgia Tech Office of VP of Research supplemented with $15,000.)

GF4. **National Science Foundation (NSF):** "CAREER: Introspective Computing - A Multicore Approach to Availability, Reliability, and Security." PI, $400,000. 06/2007 - 05/2012. (Georgia Tech Office of VP of Research supplemented with $25,000 and one research assistant for the project period.)

GF5. **National Science Foundation (NSF):** "CPA: Parallel-On-Demand — A Broad Purpose 3D-Integrated Performance Acceleration Layer for General Purpose Processors." PI, $255,000. 07/2008 - 8/2012.

GF6. **National Science Foundation (NSF):** "CCLI-Phase 1 Exploratory: Problem-Based Learning of Multithreaded Programming." PI, $54,843. 01/2009 - 08/2010.

GF7. **US Department of Defense (DoD):** "Design, Fabrication, and Testing of 3D-MAPS: A Massively Parallel Processor with 3D Stacked Memory." PI with Sung Kyu Lim and Gabriel Loh. $941,543. (Lee's allocation: $313,848.) 05/2009 - 04/2011.

GF8. **National Science Foundation (NSF):** "II-NEW: GreenIT: Testbeds for Real-time Data Center and Platform Energy and Thermal Management." Co-PI with Karsten Schwan, Yogendra Joshi, Hyesoon Kim, and Saibal Mukhopadhyay. $410,000 (Lee's allocation $82,000.) 03/2010 - 02/2011.

GF9. **National Science Foundation (NSF):** "CSR: A Unified Many-Core Architecture for Enabling Speculative Multithreading and Transactional Memory." PI, $351,831. 08/2010 - 07/2013.

GF10. **US Department of Defense (DoD):** "3D-MAPS V2: A Massively Parallel Processor with 3D Stacked Memory." PI with Sung Kyu Lim. $295,776. (Lee's allocation: $147,888.) 08/2011 - 09/2012.

Research Grants from Industry and Others

GI1. **CERCS Industry Research Fund:** "Semantics-Oriented Low-power Architecture." PI, $40,000. 10/2002 - 12/2003.

GI2. **Intel Corporation:** "Equipment grant for embedded computing research." Co-PI with Karsten Schwan. $25,000. 01/2004.

GI3. **Semiconductor Research Corporation's MARCO Centers GSRC/C2S2:** "High Performance 3D Microarchitecture Design." PI with Sung Kyu Lim and Gabriel Loh. $210,000 (Lee's allocation: $70,000.) 07/2005 - 08/2006.

GI4. **Intel Corporation:** "Curriculum Development Addressing Multi-Core Platform Issues." Co-PI with Ada Gavrilovska, Karsten Schwan, and Matt Wolf. $78,168 (Lee's allocation: $16,000.) 01/2006 - 04/2007.

GI5. **Semiconductor Research Corporation's MARCO Center C2S2:** "High Performance 3D Microarchitecture Design." PI with Sung Kyu Lim and Gabriel Loh. $450,000 (Lee's allocation: $150,000.) 08/2006 - 07/2009.

GI6. **Intel Corporation:** "Parallelizing Applications for Intel Multicore Processors." Co-PI with Ada Gavrilovska. $50,000 (Lee's allocation: $25,000.) 01/2007 - 04/2007.

GI7. **Intel Corporation:** "Collaborative Multi-core Training." Co-PI with Ada Gavrilovska, Karsten Schwan, and Matt Wolf. $38,500. (Lee's allocation: $9,625.) 08/2007 - 07/2008.

GI8. **Intel Corporation:** "Curriculum Development Addressing Multi-Core Platform Issues." Co-PI with Ada Gavrilovska, Karsten Schwan, and Matt Wolf. $80,000 (Lee's allocation: $20,000.) 01/2008 - 12/2008.

GI9. **Intel Corporation:** "Accelerating Medical Image Reconstruction for Multicore Processors." PI, $25,000. 01/2008 - 12/2008.

GI10. **Intel Corporation:** "Thread Fairness in the Larrabee Architecture." Co-PI with Hyesoon Kim. $45,000 (Lee's allocation: $22,500.) 09/2008 - 08/2009.

GI11. **Georgia Tech Focused Research Program (FRP):** "GreenIT: IT Technologies for Green Computing." Co-PI with Sudhakar Yalamanchili, Ada Gavrilovska, Yogendra Joshi, Hyesoon Kim, Saibal Mukhopadhyay, Karsten Schwan. $75,000 (Lee's allocation: $15,000.) 08/2009 - 04/2010.

GI12. **Intel Corporation:** "Thread Fairness in the Larrabee Architecture (Phase II)." Co-PI with Hyesoon Kim. $45,000 (Lee's allocation: $22,500.) 01/2010 - 08/2012.

GI13. **Intel Corporation:** "Exploiting Memory Hierarchy for Heterogeneous Multi-Core Systems: A Holistic Approach." PI, $80,000. 04/2010 - 08/2012.

GI14. **Intel Corporation:** "Curriculum Development: Intel Atom in Embedded Systems Courses." Co-PI with Ada Gavrilovska, Santosh Pande, Karsten Schwan, Matt Wolf, and Sudhakar Yalamanchili. $70,000 (Lee's allocation $11,500.) 01/2011 - 04/2012.

GI15. **Industrial Technology Research Institute (ITRI), Taiwan:** "Accelerated Computing Using 3-D Integration Technology." PI, $70,000. 08/2011 - 07/2012.

GI16. **IBM Corporation:** "Architectural Exploration for Emerging Memory Technologies." PI, $45,000. 2011. (through IBM Faculty Award.)

SCHOLARLY ACCOMPLISHMENTS

Invention Disclosure

I hold **33 US issued patents** in the areas of memory subsystem, secure non-volatile memory, 3D-IC, and physical design.

Publication (by areas)

[3DIC Design and Test]

3D1. Tianjian Li, Yan Han, Hsien-Hsin S. Lee, and Li Jiang. "Fault Clustering Technique for 3D Memory BISR," In *ACM/IEEE Design Automation & Test in Europe*, Lausanne, Switzerland, March, 2017.

3D2. Daehyun Kim, Krit Athikulwongse, Michael B. Healy, Mohammad M. Hossain, Moongon Jung, Ilya Khorosh, Gokul Kumar, Young-Joon Lee, Dean L. Lewis, Tzu-Wei Lin, Chang Liu, Shreepad Panth, Mohit Pathak, Minzhen Ren, Guanhao Shen, Taigon Song, Dong Hyuk Woo, Xin Zhao, Joungho Kim, Ho Choi, Gabriel H. Loh, Hsien-Hsin S. Lee, Sung Kyu Lim. "Design and Analysis of 3D-MAPS (3D Massively Parallel Processor with Stacked Memory." In *IEEE Transactions on Computers*, 64(1), pp.112-125, 2015.

3D3. Dong Hyuk Woo, Nak Hee Seong, and Hsien-Hsin S. Lee. "Pragmatic Integration of An SRAM Row Cache in Heterogeneous 3D DRAM Architecture using TSV." In *IEEE Transactions on Very Large Scale Integrated Circuits and Systems*, Vol.21, No.1, pp.1-13, January 2013.

3D4. Dae Hyun Kim, Krit Athikulwongse, Michael B. Healy, Mohammad M. Hossain, Moongon Jung, Ilya Khorosh, Gokul Kumar, Young-Joon Lee, Dean L. Lewis, Tzu-Wei Lin, Chang Liu, Shreepad Panth, Mohit Pathak, Minzhen Ren, Guanhao Shen, Taigon Song, Dong Hyuk Woo, Xin Zhao, Joungho Kim, Ho Choi, Gabriel H. Loh, Hsien-Hsin S. Lee, and Sung Kyu Lim. "3D-MAPS: 3D Massively Parallel Processor with Stacked Memory." In *Technical Digest of the IEEE International Solid-State Circuits Conference (ISSCC)*, pp.188 - 190, San Francisco, CA, 2012.

3D5. Hong Jun Choi, Young Jin Park, Hsien-Hsin Lee, and Cheol Hong Kim. "Adaptive Dynamic Frequency Scaling for Thermal-Aware 3D Multi-core Processors." In the *Proceedings of the 12th International Conference on Computational Science and Its Applications*, pp.602-612, Salvador de Bahia, Brazil, 2012.

3D6. Xiaodong Wang, Dilip Vasudevan, and Hsien-Hsin S. Lee. "Global Built-In Self-Repair for 3-D Memories with Redundancy Sharing and Parallel Testing." In *IEEE International 3D System Integration Conference (3DIC-12)*, Osaka, Japan, 2012.

3D7. Dean L. Lewis, Shreepad Panth, Xin Zhao, Sung Kyu Lim, and Hsien-Hsin S. Lee. "Designing 3D Test Wrappers for Pre-bond and Post-bond Test of 3D Embedded Cores." In *Proceedings of the XXIX IEEE International Conference on Computer Design (ICCD-11)*, pp.90 - 95, University of Massachusetts, Amherst, USA, October, 2011.

3D8. Xin Zhao, Dean Lewis, Hsien-Hsin S. Lee, and Sung Kyu Lim, "Low-Power Clock Tree Design for Pre-Bond Testing of 3D Stacked ICs." In *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol.30, No.5, pp.732-745, 2011.

3D9. Dong Hyuk Woo, Nak Hee Seong, and Hsien-Hsin S. Lee. "Heterogeneous Die Stacking of SRAM Row Cache and 3-D DRAM: An Empirical Design Evaluation." In *Proceedings of the 54th IEEE International Midwest Symposium on Circuits and Systems*, pp.1 - 4, Seoul, Korea, August, 2011. (An invited paper.)

3D10. Dong Hyuk Woo, Nak Hee Seong, Dean L. Lewis, and Hsien-Hsin S. Lee. "An Optimized 3D-Stacked Memory Architecture by Exploiting Excessive, High-Density TSV Bandwidth." In *Proceedings of the 16th IEEE International Symposium on High-Performance Computer Architecture (HPCA-16)*, pp.429-440, Bangalore, India, January, 2010. (Acceptance rate = 18%)

3D11. Michael B. Healy, Krit Athikulwongse, Rohan Goel, Mohammad M. Hossain, Dae Hyun Kim, Young-Joon Lee, Dean L. Lewis, Tzu-Wei Lin, Chang Liu, Moongon Jung, Brian Ouellette, Mohit Pathak, Hemant Sane, Guanhao Shen, Dong Hyuk Woo, Xin Zhao, Gabriel H. Loh, Hsien-Hsin S. Lee, and Sung Kyu Lim. "Design and Analysis of 3D-MAPS: A Many-Core 3D Processor with Stacked Memory." In *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, California, September, 2010.

3D12. Dean Lewis, Michael Healy, Mohammad Hossain, Tzu-Wei Lin, Mohit Pathak, Hemant Sane, Sung Kyu Lim, Gabriel Loh, and Hsien-Hsin S. Lee. "Design and test of 3D-MAPS, a 3D Die-Stack Many-Core Processor." In *the First IEEE International Workshop on Testing Three-Dimensional Stacked Integrated Circuits (poster)*, Austin, Texas, November, 2010.

3D13. Hsien-Hsin S. Lee and Krishnendu Chakrabarty. "Test Strategies for 3D Integrated Circuits." In *IEEE Design & Test of Computers, Special Issue on 3D IC Design and Test*, vol.26, no.5, pp.26-35, September/October, 2009.

3D14. Xin Zhao, Dean L. Lewis, Hsien-Hsin S. Lee, and Sung Kyu Lim. "Pre-bond Testable Low-Power Clock Tree Design for 3D Stacked ICs" In *Proceedings of the 2009 International Conference on Computer-Aided Design (ICCAD-09)*, pp.184-190, San Francisco, CA, November, 2009. (**Nominated for the Best Paper Award.**)

3D15. Dean L. Lewis and Hsien-Hsin S. Lee. "Architectural Evaluation of 3D Stacked RRAM Caches" In *Proceedings of the IEEE International 3D Systems Integration Conference (3DIC-09)*, pp.1-4. San Francisco, CA, September, 2009.

3D16. Dean L. Lewis and Hsien-Hsin S. Lee. "Testing Circuit-Partitioned 3D IC Designs." In *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI-09)*, pp.139-144, Tampa, FL, May, 2009.

3D17. Dean L. Lewis, Sudhakar Yalamanchili, and Hsien-Hsin S. Lee. "High Performance Non-blocking Switch Design in 3D Die-Stacking Technology." In *Proceedings of the IEEE Computer Society Annual Symposium on VLSI (ISVLSI-09)*, pp.25-30, Tampa, FL, May, 2009.

3D18. Dong Hyuk Woo, Joshua B. Fryman, Allan D. Knies, Marsha Eng, and Hsien-Hsin S. Lee. "POD: A 3D-integrated Broad-Purpose Acceleration Layer." In *IEEE MICRO special issue on Accelerator Architectures*, pp.28-40, July/August, 2008.

3D19. Dean L. Lewis, and Hsien-Hsin S. Lee, "A Scan-Island Based Design Enabling Pre-bond Testability in Die-Stacking Microprocessors." In *Proceedings of the International Test Conference (ITC 2007)*, pp. 1-8, Santa Clara, CA, October, 2007. (**ITC-2017 10-year Most Significant Paper Award**)

3D20. Michael Healy, Mario Vittes, Mongkol Ekpanyapong, Chinnakrishnan Ballapuram, Sung Kyu Lim, Hsien-Hsin S. Lee, and Gabriel H. Loh, "Multi-Objective Microarchitectural Floorplanning For 2D and 3D ICs." In *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol.26, No.1, pp.38-52, 2007.

[Energy Efficient Design]

EE1. Mrinmoy Ghosh, Simon Ford, Emre Ozer, Stuart Biles, and Hsien-Hsin S. Lee. "Way Guard: A Segmented Counting Bloom Filter Approach to Reducing Energy for Set-Associative Caches." In *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED-09)*, pp.165-170, San Francisco, CA, August, 2009. (**Selected as one of seven papers of ISLPED highlight for publicity and press.**)

EE2. Hrishikesh Amur, Ripal Nathuji, Mrinmoy Ghosh, Karsten Schwan, and Hsien-Hsin S. Lee. "IdlePower: Application-Aware Management of Processor Idle States." In *Workshop on Managed Many-Core Systems (MMCS) co-located with ACM/IEEE International Symposium on High Performance Distributed Computing (HPDC)*, Boston, MA, June, 2008.

EE3. Chinnakrishnan S. Ballapuram, Ahmad Sharif, and Hsien-Hsin S. Lee, "Exploiting Access Semantics and Program Behavior to Reduce Snoop Power in Chip Multiprocessors." In *Proceedings of the 13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XIII)*, pp.60-69, Seattle, WA, 2008. (acceptance rate = 31/127, 24.4%)

EE4. Chinnakrishnan S. Ballapuram and Hsien-Hsin S. Lee, "Improving TLB Energy for Java Applications on JVM." In *Proceedings of the International Symposium on Systems, Architectures, Modeling and Simulation (SAMOS VIII)*, pp.218-223, Samos, Greece, 2008.

EE5. Mrinmoy Ghosh and Hsien-Hsin S. Lee, "Virtual Exclusion: An Architectural Approach to Reducing Leakage Energy in Caches for Multiprocessor Systems." In *Proceedings of the 13th IEEE International Conference on Parallel and Distributed Systems (ICPADS-07)*, Hsinchu, Taiwan, December, 2007.

EE6. Dong Hyuk Woo, Mrinmoy Ghosh, Emre Ozer, Stuart Biles and Hsien-Hsin S. Lee, "Reducing Energy of Virtual Cache Synonym Lookup using Blooming Filters." In *Proceedings of the International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES'06)*, pp.179-189, Seoul, Korea, October, 2006. (Regular paper acceptance rate = 24.3%, 25/103)

EE7. Chinnakrishnan S. Ballapuram, Kiran Puttaswamy, Gabriel H. Loh and Hsien-Hsin S. Lee, "Entropy-based Low Power Data TLB Design." In *Proceedings of the International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES'06)*, pp.304-311, Seoul, Korea, October, 2006. (Short paper acceptance rate = 39.8%, 41/103)

EE8. Mrinmoy Ghosh and Hsien-Hsin S. Lee, "DRAMdecay: Using Decay Counters to Reduce Energy Consumption in DRAMs." In *Proceedings of the 3rd Watson Conference on Interaction between Architecture, Circuits and Compilers (PAC^2)*, Yorktown Heights, NY, October, 2006.

EE9. Mrinmoy Ghosh, Emre Ozer, Stuart Biles, and Hsien-Hsin S. Lee, "Efficient System-on-Chip Energy Management with a Segmented Bloom Filter." In *Proceedings of the Architecture of Computing Systems (ARCS'05)*, pp.283-297, Frankfurt, Germany, March 2006. (acceptance rate = 21%)

EE10. Chinnakrishnan S. Ballapuram, Hsien-Hsin S. Lee, and Milos Prvulovic, "Synonymous Address Compaction for Energy Reduction in Data TLB." In *Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED-05)*, pp.357-362, San Diego, California, August 2005. (acceptance rate=22%, 53/233)

EE11. Mrinmoy Ghosh, Weidong Shi, and Hsien-Hsin S. Lee, "CoolPression — A Hybrid Significance Compression Technique for Reducing Energy in Caches." In *Proceedings of the IEEE International System-On-Chip Conference (SOCC-2004)*, pp. 399 - 402, Santa Clara, California, September, 2004.

EE12. Yuvraj S. Dhillon, Abdulkadir U. Diril, Abhijit Chatterjee, and Hsien-Hsin S. Lee, "An Algorithm for Achieving Minimum Energy Consumption in CMOS Circuits Using Multiple Supply and Threshold Voltages at the Module Level." In *Digest of Technical Papers of the International Conference on Computer-Aided Design (ICCAD-03)*, pp.693-700, San Jose, California, November 2003. (acceptance rate = 26%, 130/490)

EE13. Joshua B. Fryman, Chad M. Huneycutt, Hsien-Hsin S. Lee, Kenneth M. Mackenzie and David E. Schimmel, "Energy Efficient Network Memory for Ubiquitous Devices." In *IEEE MICRO special issue on Power Complexity Aware Design*, pp. 60-70, September/October 2003.

EE14. Hsien-Hsin S. Lee and Chinnakrishnan S. Ballapuram, "Energy Efficient D-TLB and Data Cache using Semantic-Aware Multilateral Partitioning." In *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED'03)*, pp. 306-311, Seoul, Korea, August 2003. (acceptance rate = 24.4%, 54/221)

EE15. Hsien-Hsin S. Lee, Joshua B. Fryman, A. Utku Diril, and Yuvraj S. Dhillon, "The Elusive Metric for Low-Power Architecture Research." In *Workshop on Complexity-Effective Design (WCED-03) held in conjunction with the 30th ACM/IEEE International Symposium on Computer Architecture (ISCA-30)*, San Diego, California, June 2003. (acceptance rate=25%)

EE16. Hsien-Hsin S. Lee and Gary S. Tyson, "Region-based Caching: an Energy-Delay Efficient Memory Architecture for Embedded Processors." In *Proceedings of the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES'00)*, pp.120-127, San Jose, California, November, 2000.

[Memory Systems]

MM1. Nak Hee Seong, Sungkap Yeo, and Hsien-Hsin S. Lee. "Tri-Level-Cell Phase Change Memory: Toward an Efficient and Reliabla Memory System." In *Proceedings of?the 40th International Symposium on Computer Architecture (ISCA-40)*. Pp.440-451, Tel-Aviv, Israel, June, 2013.

MM2. Sungkap Yeo, Nak Hee Seong, and Hsien-Hsin S. Lee. "Can Multi-Level Cell PCM Be Reliable and Usable? Analyzing the Impact of Resistance Drift." In the 10th Annual Workshop on Duplicating, Deconstructing and Debunking in conjunction with the 39th International Symposium on Computer Architecture, Portland, OR, June, 2012.

MM3. Nak Hee Seong, Dong Hyuk Woo, Vijayalakshmi Srinivasan, Jude A. Rivers, and Hsien-Hsin S. Lee. "SAFER: Stuck-At-Fault Error Recovery for Memories." In *Proceedings of the 43rd ACM/IEEE International Symposium on Microarchitecture (MICRO-43)*, pp.115-124, Atlanta, Georgia, December, 2010. (Acceptance rate = 18%, 45/248)

MM4. Ahmad Sharif and Hsien-Hsin S. Lee, "Data Prefetching by Exploiting Global and Local Access Patterns." In *Journal of Instruction-Level Parallelism, Special Issue: The First JILP Data Prefetching Championship (DPC-1)*, Volume 13, 2011. ISSN 1942-9525.

MM5. Nak Hee Seong, Dong Hyuk Woo, and Hsien-Hsin S. Lee. "Security Refresh: Prevent Malicious Wear-out and Increase Durability for Phase-Change Memory with Dynamically Randomized Address Mapping." In *IEEE MICRO special issue on Top Picks from the Computer Architecture Conferences of 2010*, pp.119-127, January/February, 2011.

MM6. Nak Hee Seong, Dong Hyuk Woo, and Hsien-Hsin S. Lee. "Security Refresh: Prevent Malicious Wear-out and Increase Durability for Phase-Change Memory with Dynamically Randomized Address Mapping." In *Proceedings of the 37th IEEE International Symposium on Computer Architecture (ISCA-37)*, pp.383-394, Saint-Malo, France, June, 2010. (Acceptance rate = 18%, 44/245)

MM7. Ahmad Sharif and Hsien-Hsin S. Lee. "Data Prefetching Mechanism by Exploiting Global and Local Access Patterns" In *The First Journal of Instruction-Level Parallelism Data Prefetching Championship (DPC-1) in conjunction with the 15th IEEE International Symposium on High Performance Computer Architecture (HPCA-15)*, Raleigh, North Carolina, February, 2009.

MM8. Mrinmoy Ghosh and Hsien-Hsin S. Lee, "Smart Refresh: An Enhanced Memory Controller Design for Reducing Energy in Conventional and 3D Die-Stacked DRAMs." In *Proceedings of the 40th IEEE/ACM International Symposium on Microarchitecture (MICRO-40)*, pp.134-145, Chicago, IL, December, 2007. (acceptance rate = 35/166 = 21%)

MM9. Xiaotong Zhuang and Hsien-Hsin S. Lee, "Reducing Cache Pollution via Dynamic Data Prefetch Filtering." In *IEEE Transactions on Computers*, Vol.56, No.1, pp.18-31, January, 2007.

MM10. Xiaotong Zhuang and Hsien-Hsin S. Lee, "A Hardware Based Cache Pollution Filtering Mechanism for Aggressive Prefetches." In *Proceedings of the International Symposium on Parallel Processing (ICPP-03)*, pp.286-293, Kaohsiung, Taiwan, October 2003. (acceptance rate = 20% in architecture track)

MM11. Hsien-Hsin S. Lee, Gary S. Tyson, and Matthew K. Farrens, "Bandwidth Utilization using Eager Writeback." *Journal of Instruction-Level Parallelism*, Vol. 4, 2001.

MM12. Hsien-Hsin S. Lee, Gary S. Tyson, and Matthew K. Farrens, "Eager Writeback - a Technique for Improving Bandwidth Utilization." In *Proceedings of the 33rd ACM/IEEE International Symposium on Microarchitecture (MICRO-33)*, pp.11-21, Monterey, California, December, 2000. (**Best Paper Award of MICRO-33**.)

MM13. *Intel Architecture Software Optimization Reference Manual*, Intel Literature Center, order number: 245127-001, August, 1998. (Author of Chapter 6: Optimizing Cache Utilization for Pentium III Processor, pp.6-1 to pp.6-30, and Appendix A: The Mathematics of Prefetch Scheduling Distance, pp.F-1 to pp.F-12.)

[**Generic Microarchitecture**]

uA1. Fayez Mohamood, Mrinmoy Ghosh, and Hsien-Hsin S. Lee. "DLL-Conscious Instruction Fetch Optimization for SMT Processors." In *Journal of Systems Architecture*, 54, pp.1089-1100, 2008.

uA2. Eric Fontaine and Hsien-Hsin S. Lee. "Bicephaly: Maximizing Bandwidth by Duplexing Power and Data. In *Workshop on Wild and Crazy Ideas (WACI-VI) in conjunction with the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS XIII)*, Seattle, WA, 2008.

uA3. Fayez Mohamood, Michael Healy, Sung Kyu Lim, and Hsien-Hsin S. Lee, "A Floorplan-Aware Dynamic Inductive Noise Controller for Reliable Processor Design." In *Proceedings of the ACM/IEEE International Symposium on Microarchitecture (MICRO-39)*, pp. 3-14, Orlando, Florida, December, 2006. (acceptance rate = 24.1%, 42/174)

uA4. Mongkol Ekpanyapong, Jacob Minz, Thaisiri Watewai, Hsien-Hsin S. Lee, and Sung Kyu Lim, "Profile-Guided Microarchitectural Floorplanning for Deep Submicron Processor Design." In *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol.25, No.7, pp.1289-1300, July, 2006.

uA5. Fayez Mohamood, Mrinmoy Ghosh and Hsien-Hsin S. Lee, "DLL-Conscious Instruction Fetch Optimization for SMT Processors." In *Proceedings of the 2nd Watson Conference on Interaction Between Architecture, Circuits and Compilers ($P = AC^2$)*, pp.143-152, Yorktown Heights, New York, September 2005. . (**Best Paper Award of $P = AC^2$.**)

uA6. Mongkol Ekpanyapong, Sung Kyu Lim, Chinnakrishnan Ballapuram, and Hsien-Hsin S. Lee, "Wire-driven Microarchitectural Design Space Exploration," In *Proceedings of the 2005 IEEE International Symposium on Circuits and Systems (ISCAS-05)*, pp.1867-1870, Kobe, Japan, May 2005.

uA7. Mongkol Ekpanyapong, Pinar Korkmaz, and Hsien-Hsin S. Lee, "Choice Predictor for Free." In *Proceedings of the 9th IEEE Asia-Pacific Computer Systems Architecture Conference (ACSAC-2004)*, pp.399 - 413, Beijing, China, September 2004.

uA8. Mikhail Smelyanskiy, Scott A. Mahlke, Edward S. Davidson, and Hsien-Hsin S. Lee, "Predicate-aware Scheduling: A Technique for Reducing Resource Constraints." In *Proceedings of the First Annual IEEE/ACM Inernational Symposium on Code Generation and Optimization (CGO-2003)*, pp.168-177, Fisherman's Wharf, San Francisco, California, March 2003. (acceptance rate =35.4%)

uA9. Hsien-Hsin S. Lee, Mikhail Smelyanskiy, Chris J. Newburn, and Gary S. Tyson, "Stack Value File: Custom Microarchitecture for the Stack." In *Proceedings of the 7th IEEE International Symposium on High Performance Computer Architecture (HPCA-7)*, pp.5-14, Monterrey, Mexico, January, 2001. (acceptance rate = 23.6%, 26/110)

uA10. Paul Zagacki, Deep Buch, Emile Hsieh, Daniel Melaku, Vladimir Pentkovski, and Hsien-Hsin Lee, "Architecture of a 3D Software Stack for Peak Pentium III Processor Performance." *Intel Technology Journal*, Volume 3, Issue 2, May, 1999.

[**Physical Design**]

PD1. Hsien-Hsin S. Lee, "IC Design Challenges and Opportunities for Advanced Process Technology," In *Proceedings of 2015 International Symposium on VLSI Design, Automation, and Test (VLSI-DAT)*, Hsinchu, Taiwan, April, 2015.

PD2. Michael B. Healy, Fayez Mohamood, Hsien-Hsin S. Lee, and Sung Kyu Lim. "Integrated Microarchitectural Floorplanning and Runtime Controller for Inductive Noise Mitigation." In *ACM Transactions on Design Automation of Electronic Systems*, Volume 16, Issue 4, pp.46:1-25, 2011.

PD3. Michael Healy, Fayez Mohamood, Hsien-Hsin S. Lee and Sung Kyu Lim, "A Unified Methodology for Power Supply Noise Reduction in Modern Microarchitecture Design." In *Proceedings of the 13th IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC'08)*, pp.611-616, Seoul, Korea, 2008.

PD4. Fayez Mohamood, Michael Healy, Sung Kyu Lim, and Hsien-Hsin S. Lee, "Noise-Direct: A Technique for Power Supply Noise Aware Floorplanning Using Microarchitecture Profiling." In *Proceedings of the 12th Asia and South Pacific Design Automation Conference (ASP-DAC'07)*, pp.786-791, Yokohama, Japan, January, 2007. (acceptance rate = 32.1%, 131/408)

PD5. Michael Healy, Mario Vittes, Mongkol Ekpanyapong, Chinnakrishnan Ballapuram, Sung Kyu Lim, Hsien-Hsin S. Lee, and Gabriel H. Loh, "Microarchitectural Floorplanning Using Performance and Temperature Tradeoff." In *Proceedings of the Design, Automation and Test in Europe (DATE-06)*, pp.1288-1293, Munich, Germany, March 2006. (acceptance rate = 17%)

PD6. Mongkol Ekpanyapong, Jacob R. Minz, Thaisiri Watewai, Hsien-Hsin S. Lee, and Sung Kyu Lim, "Profile-Guided Microarchitectural Floorplanning for Deep Submicron Processor Design." In *Proceedings of the 41st Design Automation Conference (DAC-2004)*, pp.634 -639, San Diego, California, June 2004. (acceptance rate = 21%, 163/785)

[Datacenter, Cloud, and Multi-core Computing]

DC1. Sungkap Yeo, Mohammad M. Hossain, Jen-Cheng Huang, and Hsien-Hsin S. Lee. "ATAC: Ambient Temperature-Aware Capping for Power Efficient Datacenters." In *Proceedings of the ACM Symposium on Cloud Computing*, pp.17.1-17.14, Seattle, WA, 2014.

DC2. Sungkap Yeo and Hsien-Hsin S. Lee. "Peeling the Power Onion of Data Centers." Chapter Three In *Energy Efficient Thermal Management of Data Centers* by Yogendra Joshi and Pramod Kumar (Editors), pp.137-168, Springer, 2012.

DC3. Mohammad M. Hossain, Jen-Cheng Huang, and Hsien-Hsin S. Lee. "Migration Energy-Aware Workload Consolidation in Enterprise Clouds." In *Proceedings of?the IEEE International Conference on Cloud Computing Technology and Science*, pp.405-410, December, 2012.

DC4. Sungkap Yeo and Hsien-Hsin S. Lee. "SimWare: A Holistic Warehouse-scale Computer Simulator." In *IEEE Computer Special Issue on Modeling and Simulation of Smart and Green Computing Systems*, Vol. 35, No. 9, pp.48-55, 2012.

DC5. Sungkap Yeo and Hsien-Hsin S. Lee. "Using Mathematical Modeling in Provisioning a Heterogeneous Cloud Computing Environment." In *IEEE Computer*, Vol. 44, No. 8, pp. 55-62, August, 2011.

DC6. Mrinmoy Ghosh, Ripal Nathuji, Min Lee, Karsten Schwan, and Hsien-Hsin S. Lee. "Symbiotic Scheduling for Shared Caches in Multi-Core Systems Using Memory Footprint Signature." In *Proceedings of the 40th IEEE International Conference on Parallel Processing (ICPP-2011)*, Taipei, Taiwan, pp.11 - 20, September, 2011. (Acceptance rate = 22%, 81/363)

DC7. Sung Woo Chung, Hsien-Hsin S. Lee, and Woo Hyong Lee. "Architecture/OS Support for Embedded Multi-core Systems." In *The Computer Journal*, vol.53, no.8, pp.1134-1135, 2010.

DC8. Dong Hyuk Woo and Hsien-Hsin S. Lee. "PROPHET: Goal-Oriented Provisioning for Highly Tunable Multicore Processors in Cloud Computing." In *ACM SIGOPS Operating Systems Review special issue on the Interaction among the OS, Compilers, and Multicore Processors*, Vol.43, Issue 2, pp.102-103, April, 2009.

DC9. Michael Healy, Hsien-Hsin S. Lee, Gabriel H. Loh, and Sung Kyu Lim. "Thermal optimization in Multigranularity Multi-Core Floorplanning." In *Proceedings of the 14th IEEE/ACM Asia South Pacific Design Automation Conference (ASP-DAC'09)*, pp.43-48, Yokohama, Japan, January, 2009.

DC10. Dong Hyuk Woo and Hsien-Hsin S. Lee. "Extending Amdahl's Law for Energy-Efficient Computing in the Many-Core Era." In *IEEE Computer*, Vol.41, No.12, pp.24-31, December, 2008.

DC11. Richard M. Yoo and Hsien-Hsin S. Lee, "Adaptive Transaction Scheduling for Transactional Memory Systems." In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA) in the Special Track on Hardware and Software Techniques to Improve the Programmability of Multicore Machines*, pp. 169-178, Munich, Germany, 2008.

DC12. Richard M. Yoo, Yang Ni, Adam Welc, Bratin Saha, Ali-Reza Adl-Tabatabai, and Hsien-Hsin S. Lee, "Kicking the Tires of Software Transactional Memory: Why the Going Gets Tough." In *Proceedings of the 20th ACM Symposium on Parallelism in Algorithms and Architectures (SPAA) in the Special Track on Hardware and Software Techniques to Improve the Programmability of Multicore Machines*, pp.265-274, Munich, Germany, 2008.

DC13. Richard M. Yoo and Hsien-Hsin S. Lee. "Helper Transactions: Enabling Thread-Level Speculation via A Transactional Memory System." In *Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures (PESPMA) in Conjunction with ACM/IEEE International Symposium on Computer Architecture (ISCA-35)*, Beijing, China, June 2008.

DC14. Taeweon Suh, Daehyun Kim, and Hsien-Hsin S. Lee, "Cache Coherence Support for Non-Shared Bus Architecture on Heterogeneous MP SoCs." In *Proceedings of the 42nd Design Automation Conference (DAC-42)*, pp.553-558, Anaheim, California, June 2005. (acceptance rate=20%)

DC15. Taeweon Suh, Hsien-Hsin S. Lee, and Douglas M. Blough, "Integrating Cache Coherence Protocols for Heterogeneous Multiprocessor Systems. Part 2." In *IEEE MICRO special issue on Embedded Systems: Architecture, Design and Tools*, pp.70-78, September/October 2004.

DC16. Taeweon Suh, Hsien-Hsin S. Lee, and Douglas M. Blough, "Integrating Cache Coherence Protocols for Heterogeneous Multiprocessor Systems. Part 1." In *IEEE MICRO special issue on Embedded Systems: Architecture, Design and Tools*, pp.33-41, July/August 2004.

DC17. Taeweon Suh, Douglas M. Blough and Hsien-Hsin S. Lee, "Supporting Cache Coherence in Heterogeneous Multiprocessor Systems." In *Proceedings of the Design Automation and Test in Europe Conference (DATE'04)*, pp.1150-1155, Paris, France, February 2004. (acceptance rate = 23.2%, 181/780)

[GPU and Heterogeneous Architecture]

GP1. Jen-Cheng Huang, Joo Hwan Lee, Hyesoon Kim, and Hsien-Hsin S. Lee. "GPUMech: GPU Performance Modeling Technique Based on Interval Analysis." In *Proceedings of the 47th IEEE/ACM International Symposium on Microarchitecture (MICRO-47)*, pp.268-279, Cambridge, England, December, 2014.

GP2. Jen-Cheng Huang, Lifeng Nai, Hyesoon Kim, and Hsien-Hsin S. Lee. "TBPoint: Reducing Simulation Time for Large Scale GPGPU Kernels." In *Proceedings of the 28th International Parallel and Distributed Processing Symposium (IPDPS)*, pp.437-446, Phoenix, AZ, 2014.

GP3. Hong Jun Choi, Dong Oh Son, Seung Gu Kang, Jong Myon Kim, Hsien-Hsin S. Lee, and Cheol Hong Kim. "An Efficient Scheduling Scheme Using Estimated Execution Time for Heterogeneous Computing Systems." In *Journal of Supercomputing*, 65(2), pp.886-902, 2013.

GP4. Abderrahim Benquassmi, Eric Fontaine, and Hsien-Hsin S. Lee. "Parallelization of Katsevich CT Image Reconstruction Algorithm on Generic Multi-Core Processors and GPGPU." In *GPU Computing GEMS, Section 10 Medical Imaging, Chapter 31*, Wen-Mei Hwu (editor-in-chief), pp.659-677, Morgan Kaufmann Publishers, 2011.

GP5. Dong Hyuk Woo and Hsien-Hsin S. Lee. "COMPASS: A Programmable Data Prefetcher Using Idle GPU Shaders." In *Proceedings of the 16th IEEE International Conference on Architectural Support for*

Programming Languages and Operating Systems (ASPLOS XV), pp.297-309, Pittsburgh, PA, March, 2010. (Acceptance rate = 17.7%, 32/181)

GP6. Ahmad Sharif and Hsien-Hsin S. Lee. "Total Recall: A Debugging Framework for GPUs." In *Proceedings of the ACM SIGGRAPH/Eurographics Workshop of Graphics Hardware (GH-08)*, pp.13-20, Sarajevo, Bosnia-Herzegovina, June, 2008.

GP7. Eric Fontaine and Hsien-Hsin S. Lee, "Optimizing Katsevich Image Reconstruction Algorithm on Multicore Processors." In *Proceedings of the 13th IEEE International Conference on Parallel and Distributed Systems (ICPADS-07)*, Hsinchu, Taiwan, December, 2007.

GP8. Dong Hyuk Woo, Joshua B. Fryman, Allan D. Knies, Marsha Eng, and Hsien-Hsin S. Lee, "POD: A Parallel On-Die Architecture." In *Proceedings of the 11th Annual Workshop on High Performance Embedded Computing (HPEC)*, Lexington, Massachusetts, September, 2007. (**Award Session**)

GP9. Dong Hyuk Woo, Joshua B. Fryman, Allan D. Knies, and Hsien-Hsin S. Lee. "Chameleon: Virtualizing Idle Acceleration Cores of A Heterogeneous Multi-Core Processor for Caching and Prefetching." In *ACM Transactions on Architecture and Code Optimization*, vol.7, no.1, pp.1-35, April, 2010.

[Security Architecture and Dependable Systems]

SA1. Jen-Cheng Huang, Matteo Monchiero, Yoshio Turner, and Hsien-Hsin S. Lee. "Ally: OS-Transparent Packet Inspection Using Sequestered Cores." In *Proceedings of the ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS-11)*, pp. 1 - 11, Brooklyn, NY, October, 2011. (Acceptance rate = 32%, 20/62) (**Best Paper Award of ANCS-11**.)

SA2. Jun Yang, Lan Gao, Youtao Zhang, Marek Chrobak, and Hsien-Hsin S. Lee. "A Low-Cost Memory Remapping Scheme for Address Bus Protection" In *Journal of Parallel and Distributed Computing*, vol.70, issue 5, pp.443-457, May 2010.

SA3. Vikas R. Vasisht and Hsien-Hsin S. Lee. "SHARK: Architectural Support for Autonomic Protection Against Stealth by Rootkit Exploits." In *Proceedings of the 41st ACM/IEEE International Symposium on Microarchitecture (MICRO-41)*, pp.106-116, Lake Como, Italy, November, 2008. (Acceptance rate = 19%, 40/210.)

SA4. Weidong Shi and Hsien-Hsin S. Lee, "Accelerating Memory Decryption and Authentication with Frequent Value Prediction." In *Proceedings of the ACM International Conference on Computing Frontiers (CF'07)*, pp.35-46, Ischia, Italy, May, 2007.

SA5. Weidong Shi, Chenghuai Lu, and Hsien-Hsin S. Lee, "Memory-centric Security Architecture." Invited article. In *Transactions of High Performance Embedded Architectures and Compilers*, Vol.1, pp.95-115, 2007. Springer Verlag.

SA6. Dong Hyuk Woo and Hsien-Hsin S. Lee, "Analyzing Performance Vulnerability due to Resource Denial-of-Service Attack on Chip Multiprocessors." In *Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMPMSI) in conjunction with the 13th International Symposium on High-Performance Computer Architecture (HPCA-13)*, Phoenix, Arizona, February, 2007.

SA7. Weidong Shi, and Hsien-Hsin S. Lee, "Authentication Control Point and its Implications for Secure Processor Design." In *Proceedings of the ACM/IEEE International Symposium on Microarchitecture (MICRO-39)*, pp.103-112, Orlando, Florida, December, 2006. (acceptance rate = 24.1%, 42/174)

SA8. Chenghuai Lu, Tao Zhang, Weidong Shi, and Hsien-Hsin S. Lee, "M-TREE: A High Efficiency Security Architecture for Protecting Integrity and Privacy of Software." In *Journal of Parallel and Distributed Computing, Special Issue on Security in Grid and Distributed Systems*, Vol.66, Issue 9, pp.1116-1128, 2006. (acceptance rate =12.2%, 10/82.)

SA9. Weidong Shi, Hsien-Hsin S. Lee, Richard M. Yoo, and Alexandra Boldyreva, "A Digital Rights Enabled Graphics Processing System." In *Proceedings of the ACM SIGGRAPH/Eurographics Workshop of Graphics Hardware*, pp.17-26, Vienna, Austria, September 2006. (acceptance rate = 31.1%, 14/45)

SA10. Lan Gao, Jun Yang, Marek Chrobak, Youtao Zhang, San Nguyen, and Hsien-Hsin S. Lee, "A Low-cost Memory Remapping Scheme for Address Bus Protection." In *Proceedings of the 15th International Conference on Parallel Architecture and Compilation Techniques (PACT'06)*, pp.74-83, Seattle, WA, September 2006. (acceptance rate = 25.6%, 30/117)

SA11. Weidong Shi, Hsien-Hsin S. Lee, Laura Falk, and Mrinmoy Ghosh, "An Integrated Framework for Dependable and Revivable Architecture Using Multicore Processors." In *Proceedings of the 33rd International Symposium on Computer Architecture (ISCA-33)*, pp.102-113, Boston, MA, June 2006. (acceptance rate = 13%, 31/231)

SA12. Weidong Shi, Joshua B. Fryman, Guofei Gu, Hsien-Hsin S. Lee, Youtao Zhang, and Jun Yang, "InfoShield: A Security Architecture for Protecting Information Usage in Memory." In *Proceedings of the 12th International Conference on High Performance Computer Architectures (HPCA-12)*, pp.225-234, Austin, Texas, February 2006. (acceptance rate=14%)

SA13. Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu, and Mrinmoy Ghosh, "Towards the Issues in Architectural Support for Protection of Software Execution." In *ACM SIGARCH Computer Architecture News*, Vol. 33, Issue 1, pp.6-15, March 2005.

SA14. Weidong Shi, Chenghuai Lu, and Hsien-Hsin S. Lee, "Memory-centric Security Architecture." In *Proceedings of the 2005 International Conference on High Performance Embedded Architectures and Compilers (HiPEAC 2005)*, pp.153 - 168, Barcelona, Spain, November 2005. (acceptance rate=20.2%, 17/84)

SA15. Weidong Shi, Hsien-Hsin S. Lee, Guofei Gu, Mrinmoy Ghosh, Laura Falk, and Trevor Mudge, "Intrusion Tolerant and Self-recoverable Network Service System Using Security Enhanced Chip Multiprocessor." In *Proceedings of the 2nd IEEE International Conference on Autonomic Computing (ICAC-05)*, pp.263-273, Seattle, WA, June 2005. (acceptance rate of regular papers = 16.7%, 25/150)

SA16. Weidong Shi, Hsien-Hsin S. Lee, Mrinmoy Ghosh, Chenghuai Lu, and Alexandra Boldyreva, "High Efficiency Counter Mode Security Architecture via Prediction and Precomputation." In Proceedings of the 32nd International Symposium on Computer Architecture (ISCA-32), pp.14-24, Madison, Wisconsin, June 2005. (acceptance rate = 23.2%, 45/194)

SA17. Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu and Tao Zhang, "Attacks and Risk Analysis for Hardware Supported Software Copy Protection Systems." In *Proceedings of the 4th ACM Workshop on Digital Right Management (DRM'2004)*, pp.54-62, Washington D.C., October 2004.

SA18. Weidong Shi, Hsien-Hsin S. Lee, Mrinmoy Ghosh, and Chenghuai Lu, "Architectural Support for High Speed Authentication of Shared Memory in Multiprocessor Systems." In *Proceedings of the International Conference on Parallel Architecture and Compilation Techniques (PACT'04)*, pp. 123 - 134, Antibes Juan-les-Pins, France, September 2004. (acceptance rate = 18.8%, 23/122)

SA19. Xiaotong Zhuang, Tao Zhang, Hsien-Hsin S. Lee and Santosh Pande, "Hardware Assisted Control Flow Obfuscation for Embedded Processors." In *Proceedings of the International Conference on Compilers, Architecture, Synthesis for Embedded Systems (CASES'04)*, pp. 292 - 302, Washington D.C., September 2004. (acceptance rate=25.2%, 31/123) . (**Best Paper Award of CASES 2004**.)

SA20. Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu, and Mrinmoy Ghosh, "Toward the Issues in Architectural Support for Protection of Software Execution." In *Workshop on Architectural Support for Security and Anti-Virus (WASSA) in conjunction with the 11th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-XI)*, pp.1-9, Boston, Massachusetts, October 2004.

[FPGA]

FP1. Taeweon Suh, Shih-Lien L. Lu, and Hsien-Hsin S. Lee, "An FPGA Approach to Quantifying Coherence Traffic Efficiency on Multiprocessor Systems" In *Proceedings of the 17th IEEE International Conference on Field Programmable Logic and Applications (FPL 2007)*, pp. 47-53, Amsterdam, The Netherlands, August, 2007. (acceptance rate = 21%) (**Nominated for the Best Paper Award**.)

FP2. Taeweon Suh, Hsien-Hsin S. Lee, Shih-Lien Lu, and John Shen, "Coherence Traffic Considered Harmful - An FPGA Approach to Quantifying Coherence Traffic Efficiency on Multiprocessor Systems," In *International Symposium on Field-Programmable Gate Arrays (FPGA 2007)*, Monterey, California, February 2007. (poster paper.)

FP3. Taeweon Suh, Hsien-Hsin S. Lee. Shih-Lien Lu, and John Shen, "Initial Observations of Hardware/Software Co-Simulation using FPGA in Architecture Research," In *Workshop on Architecture Research using FPGA Platforms (WARFP-2006) in conjunction with International Symposium on High-Performance Computer Architecture (HPCA-12)*, Austin, Texas, 2006.

FP4. Taeweon Suh, Hsien-Hsin S. Lee, Sally A. McKee, and Martin Schulz, "Evaluating System-wide Monitoring Capsule Design Using Xilinx Virtex-II Pro FPGA," In *Workshop on Architecture Research using FPGA Platforms (WARFP-2005) in conjunction with International Symposium on High-Performance Computer Architecture (HPCA-11)*, San Francisco, CA, 2005.

FP5. Martin Schulz, Brian S. White, Sally A. McKee, Hsien-Hsin S. Lee, and Jurgen Jeitner, "Owl: Next Generation System Monitoring." In *Proceedings of the ACM Computing Frontiers 2005*, pp.116-124, Ischia, Italy, May 2005.

FP6. Martin Schulz, Brian White, Sally A. McKee, and Hsien-Hsin Lee, "A Vision for Next Generation System Monitoring." In *Workshop on Hardware Performance Monitor Design and Functionality in conjunction with International Symposium on High-Performance Computer Architecture (HPCA-11)*, San Francisco, CA, 2005.

FP7. Christopher R. Clark, Ripal Nathuji, and Hsien-Hsin S. Lee, "Using an FPGA as a Prototyping Platform for Multi-core Processor Applications," In *Workshop on Architectural Research using FPGA Platforms (WARFP-2005) in conjunction with International Symposium on High-Performance Computer Architecture (HPCA-11)*, San Francisco, CA, 2005.

[**Performance Evaluation**]

PE1. Richard M. Yoo, Hsien-Hsin S. Lee, Han Lee, and Kingsum Chow, "Hierarchical Means: Single Number Benchmarking with Workload Cluster Analysis." In *Proceedings of the 2007 IEEE International (IISWC-2007)*, pp.204-213, Boston, MA, September, 2007.

PE2. Hsien-Hsin Lee, Youfeng Wu, and Gary Tyson, "Quantifying Instruction-Level Parallelism Limits on an EPIC Architecture." In *Proceedings of the IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2000)*, pp.21-27, Austin, Texas, April, 2000.

PE3. Eric L. Boyd, Waqar Azeem, Hsien-Hsin Lee, Tien-Pao Shih, Shih-Hao Hung, and Edward S. Davidson, "A Hierarchical Approach to Modeling and Improving the Performance of Scientific Applications on the KSR1." In *Proceedings of the 1994 International Conference on Parallel Processing (ICPP-94)*, pp.188-192, St. Charles, Illinois, August, 1994.

[**High-Efficiency and Privacy-Preserving Machine Learning Systems**]

ML1. Liu Ke, Xuan Zhang, Jinin So, Jong-Geon Lee, Shin-Haeng Kang, Sukhan Lee, Songyi Han, Yeongon Cho, Jin Hyun Kim, Yongsuk Kwon, Kyungsoo Kim, Jin Jung, Ilkwon Yun, Sung Joo Park, Hyunsun Park, Joonho Song, Jeonghyeon Cho, Kyomin Sohn, Nam Sung Kim, and Hsien-Hsin S. Lee. "Near-Memory Processing in Action: Accelerating Personalized Recommendation with AxDIMM." To appear in *IEEE MICRO Special Issue on Processing-In-Memory*, November/December, 2021.

ML2. Udit Gupta, Samuel Hsia, Jeff Zhang, Mark Wilkening, Javin Pombra, Hsien-Hsin S. Lee, Gu-Yeon Wei, Carole-Jean Wu, and David Brooks. "Co-designing Models and Hardware to Jointly Optimize Recommendation Quality and Performance." To appear in *Proceedings of the 54th ACM/IEEE International Symposium on Microarchitecture (MICRO-54)*, Athens, Greece, October, 2021.

ML3. Brandon Reagen, Woo-Seok Choi, Yeongil Ko, Vincent T. Lee, Hsien-Hsin S. Lee, Gu-Yeon Wei, David Brooks. "Cheetah: Optimizing and Accelerating Homomorphic Encryption for Private Inference." In *Proceedings of the IEEE International Symposium on High-Performance Computer Architecture (HPCA-27)*, Seoul, South Korea, February, 2021.

ML4. Udit Gupta, Young Geun Kim, Sylvia Lee, Jordan Tse, Hsien-Hsin S. Lee, Gu-Yeon Wei, David Brooks, Carole-Jean Wu. "Chasing Carbon: The Elusive Environmental Footprint of Computing." In *Proceedings of the IEEE International Symposium on High-Performance Computer Architecture (HPCA-27)*, Seoul, South Korea, February, 2021.

ML5. Udit Gupta, Samuel Hsia, Vikram Saraph, Xiaodong Wang, Brandon Reagen, Gu-Yeon Wei, Hsien-Hsin S. Lee, David Brooks, and Carole-Jean Wu. "DeepRecSys: A System for Optimizing End-to-End At-Scale Neural Recommendation Inference." In *Proceedings of the 47th ACM/IEEE International Symposium on Computer Architecture (ISCA-47)*, Valencia, Spain, 2020.

ML6. Liu Ke, Udit Gupta, Carole-Jean Wu, Benjamin Cho, Mark Hempstead, Brandon Reagen, Xuan Zhang, David Brooks, Vikas Chandra, Utku Diril, Amin Firoozshahian, Bill Jia, Kim Hazelwood, Hsien-Hsin S. Lee, Meng Li, Bert Maher, Dheevatsa Mudigere, Maxim Naumov, Martin Scharz, Mikhail Smelyanksiy, an Xiaodong Wang. "RecNMP: Accelerating Personalized Recommendation with Near-Memory Processing." In *Proceedings of the 47th ACM/IEEE International Symposium on Computer Architecture (ISCA-47)*, Valencia, Spain, 2020.

ML7. Udit Gupta, Carole-Jean Wu, Xiaodong Wang, Maxim Naumov, Brandon Reagen, David Brooks, Bradford Cottel, Kim Hazelwood, Mark Hempstead, Bill Jia, Hsien-Hsin S. Lee, Andrey Malevich, Dheevatsa Mudigere, Mikhail Smelyanskiy, Liang Xiong, and Xuan Zhang, "The Architectural Implications of Facebook's DNN-based Personalized Recommendation." In *Proceedings of the 26th IEEE International Symposium on High-Performance Computer Architecture (HPCA-26)*, San Diego, CA, February, 2020.

ML8. Lifeng Nai, Yinglong Xia, Ching-Yung Lin, Bo Hong, and Hsien-Hsin S. Lee. "Cache-conscious Graph Collaborative Filtering on Multi-socket Multicore Systems". In *Proceedings of the 11th ACM Conference on Computing Frontiers*, Article No. 32, Cagliari, Italy, 2014.

ML9. Richard M. Yoo, Han Lee, Kingsum Chow, and Hsien-Hsin S. Lee, "Constructing a Non-Linear Model with Neural Networks For Workload Characterization." In *Proceedings of the 2006 IEEE International Symposium on Workload Characterization (IISWC-06)*, pp.150-159, San Jose, California, October, 2006.

Blog Articles

BG1. Carole-Jean Wu, David Brooks, Udit Gupta, Hsien-Hsin Sean Lee, and Kim Hazelwood. "Deep Learning: It's Not All About Recognizing Cats and Dogs", ACM SIGARCH Blog, November, 2019.

BG2. Hsien-Hsin Sean Lee. "The First Trillion-Transistor Chip: A New Design Space", ACM SIGARCH Blog, August, 2019.