PROJECT SUMMARY

Addressing **3D** IC Design Challenges through a Cross-Disciplinary **A**rchitecture, **T**esting, and **E**DA Approach

Three-dimensional integrated circuits (3D ICs) are attractive options for overcoming the barriers in interconnect scaling, offering an opportunity to continue the CMOS performance trend. The benefits of 3D ICs include: (i) higher packing density and smaller footprint due to the addition of a third dimension to the conventional two-dimensional layout; (ii) higher performance due to reduced average interconnect length; (iii) lower interconnect power consumption due to the reduction in total wiring length; and (iv) support for realization of mixed-technology chips.

Even though 3D integrated circuits show great benefits, there are several challenges for the adoption of 3D architectures. First, there are few commercially available EDA tools and design methodologies for 3D integrated circuits. Second, 3d testing remains to be an unexplore area. Third, design space exploration at the architectural level is essential to fully take advantage of the 3D integration technologies and build a high performance, reliable, and low power 3D IC design. The research will be be conducted in collaboration with our industrial partners, including IBM, Intel, Freescale, Qualcomm, Seagate, Synopsys.

Intellectual merit: Key contributions expected from this research are:

Broader Impact: The success of this research is likely to have a significant influence on the design of next generation 3D architectures. The results from this research will foster new research directions in several areas of 3D architecture design, which is expected to be the main design paradigm for future high performance archiitectures. Through collaboration with our leading industry partners, we envision direct transfer of many ideas to industry. The outcome of this research would, therefore, have a direct impact on future 3D designs. Undergraduate and graduate students, involved in this research, will get versatile training in several areas to prepare them for the next generation IT workforce. Moreover, the tools and techniques developed in this research will be used in teaching existing and new courses. Finally, the tools will be available through our Web site for use by other educators, researchers and industrial practitioners.

PROJECT DESCRIPTION

1 Introduction

The objective of this proposed research project includes two tasks:

- **3D Architecture**: we will explore new 3D architecture, as well as utilizing 3D technology to improve system reliability.
- **3D EDA Tools**: we will develop EDA design tools for researchers and industrial practitioners designing three-dimensional integrated circuits;
- **3D Testing**: We will investigate testing techniques that are specifically for 3D chips.

As technology scales, the International Technology Roadmap for Semiconductors projects that on-chip communications will require new design approaches to achieve system level performance targets. Aggressive scaling of process technologies has enabled feature sizes to shrink continuously. While the performance of gates has been improving, interconnects have become a major performance bottleneck [1, 2, 8], because global interconnects do not scale accordingly with technologies. Consequently, intermediate and global interconnects of current microprocessors contribute to a major portion of power consumption and also serve as impediments for better performance. Hence, many research efforts are devoted to seeking solutions which can overcome the limitation of wiring requirements for present and future chip designs.

Three-dimensional integrated circuits (3D ICs) [13, 19, 31] are attractive options for overcoming the barriers in interconnect scaling, offering an opportunity to continue the CMOS performance trend. In a three-dimensional (3D) chip, multiple device layers are stacked together with direct vertical interconnects tunnelling through them. (Figure 1 shows a conceptual 2-layer 3D integrated circuit) [**?**]. The direct vertical interconnects are called *inter-wafer vias* or *die-to-die (d2d) vias*. Consequently, one of the most important benefits of a 3D chip over a traditional two-dimensional (2D) design is the reduction on global interconnect [34, 36]. Other benefits of 3D ICs include: (i) higher packing density and smaller footprint due to the addition of a third dimension to the conventional two-dimensional layout [42, 45]; (ii) higher performance due to reduced average interconnect length; (iii) lower interconnect power consumption due to the reduction in total wiring length [33, 48, 57]; and (iv) support for realization of mixed-technology chips [40].

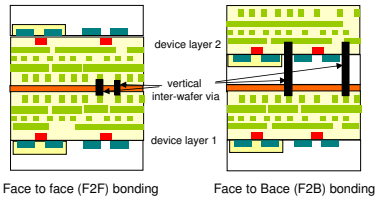


Figure 1: A conceptual 3D IC: two device layers are stacked together with direct vertical interconnects tunnelling through them

Even though 3D integrated circuits show great benefits, there are several challenges for the adoption of 3D architectures. First, there are no commercially available EDA tools and design methodologies for 3D integrated circuits [16]. Second, the move from 2D to 3D architecture could accentuate the thermal concerns due to the increased power densities that result from placing one logic block over another in the multi-layered 3D stack [28, 29]. Third, design space exploration at the architectural level is essential to fully take advantage of the 3D integration technologies and build a high performance 3D IC chip.

The absence of EDA tools that explore design space for three-dimensional integrated circuits are affecting researchers and industrial practitioners in their quest for the adoption of this new technology. New opportunities brought by 3D technology can result in innovations in new architecture design for future many-core CMP (Chip multiprocessor).

The proposed project will fill this critical void through the creation of a hierachical design automation toolset, which interface with commercially available EDA design flows. Also, the project will study the impact of 3D technology on architecture design and provides guidelines for future 3D architecture design. Finally we will study the 3D testing techniques.

2 Related Work

The work related to this proposal can be divided into three main groups: those related to system and architecture level design exploration for 3D IC, those related to 3D EDA tools development, and those related to testing. In the

following paragraphs, we discuss each of those in detail and explain how the proposed research differs from them or complements them.

- **System-level and architecture level design exploration for 3D ICs**
  Early work on 3D integrated circuits has been in the system-level modeling and analysis. To predict the reduction on wire-length and the improved performance in 3D ICs, numerical models have been developed for various forms of 3D integration technology [7] [35] [59]. Since interconnect power consumption is becoming an important portion of the total power consumption, the opportunities for reducing power dissipation using 3D integration were also investigated [32]. The impact of the through via density on the performance was investigated [49]. The energy, thermal, and performance of 3D designs under a given timing constraint were also studied [17]. Analysis of applying 3D technology on FPGA design were conducted [37] [56]. These work have done a comprehensive system-level analysis of the benefits using 3D integration, including the reduction of the wiring length, improved performance, and reduced power consumption. However, it also shows that the increased power density (due to stacking) can cause higher temperature [58] [54], which is often considered a major hindrance for the adoption of 3D integration.
  In mircoarchitecture level, a number of approaches have been proposed to explore the design space in 3D microprocessors [11] [44] [51]. Black et al. [11] provided an overview of the potential benefits of designing an Intel IA32 processor in 3D technology, even though the design details for each components were not disclosed. Loh et al. [51] [52] [53] investigated the 3D implementation of important components in microprocessors, such as instruction schedulers, register files, and arithmetic units. Specific to 3D memory design, a 3D shared memory is fabricated. In this shared memory system design, six memory modules are distributed into three device layers and high data bandwidth is achieved by connecting broadcast bus in both horizontal and vertical directions (3D vertical interconnects). As for cache design, Loh et al. [50] has shown a custom 3D implementation of caches using face-to-face stacking. However, it didn't fully explore all design options and thus the design itself may not be the optimal one.
- **EDA Design Tools for 3D ICs**
  To efficiently exploit the benefits of 3D technologies, design techniques and methodologies to support 3D designs are imperative. 3D IC design is fundamentally related to the topological arrangement of logic blocks. Therefore, physical design tools for 3D circuits are important for the adoption of 3D technology. New placement and routing tools are necessary to optimize 3D circuits to take full advantages of the additional floorplanning/placement/routing dimension. As shown by system-level analysis [58] [54], a major concern in the adoption of 3D technology is the increased on-chip temperature. Therefore, physical design tools for 3D circuits have to be thermal aware. Recent efforts have focused on developing tools for supporting custom 3D layouts and placement tools [18]. In [20], the technology and testing issues were surveyed and a physical design framework for 3D ICs was presented. Thermal-driven floorplanning/placement/routing algorithms for 3D ICs have been proposed by various groups [15] [3] [86]. To help mitigate thermal issues, thermal vias (the vertical inter-wafer vias which are only for heat conducting purpose and don't carry electrical signals) can be inserted during floorplanning and placement steps [85] [82]. Another design metric, reliability, was also considered during 3D physical design steps [72] [46].
- **Testing**
  Krish, please put more here,
  Among all EDA challenges for 3D IC design, tools and methodologies for 3D IC testing are regarded as the No.1 challenge, according to a recent keynote speech [**?**] by Ted Vucurevich (CTO of Cadence Design System). However, research on testing for 3D ICs is still in its infancy. It is only recently that progress has been reported on the testing of 3D ICs. For example, Lewis et al. have proposed a scanisland based pre-bond test method to facilitate the testability of die-stacked microprocessors [**?**]. Wu et al. have proposed several 3D scan-chain design techniques [**?**]. In [?], the most efficient of these methods is based on a genetic algorithm (GA), which is targeted towards the ordering of scan cells for a single scan chain. However, a disadvantage of the GAbased approach is that it is limited to a single scan chain. Second, it does not provide any insights into lower bounds on wire length, and being a heuristic approach, it is difficult to evaluate its effectiveness.

3 Proposed Research

The project involves three different research tasks: architecture, EDA, testing. The following sections enumerate the proposed work for each part in detail.

4 3D Architecture

Sean/Vijay/Yuan/Krish
- Sean's DRAM stacking stuffs
- Yuan's MRAM stacking stuffs
- Yuan/Vijay, Reconfigurable logic stacking on uProcessor
- Vijay, low power/reliability?
- Krish, Microfluidic based thermal management?
- Sean, more ideas?

4.1 DRAM stacking

At the technology level, DRAM die-stacking directly on top of a processor is seemingly the most straightforward and effective approach to apply 3D integration as it leverages the advantages brought by fast, high-density, and low-power die-to-die vias to alleviate huge bandwidth demand for data-intensive applications. In particular, when the trend is heading for multi-core design, how to supply enough data into a processor with a massive number of on-die cores will become a major challenge for performance scalability. Traditional off-chip memory will not suffice due to the I/O pin limitation. According to ITRS' projection, the number of pins on a package will not continue to grow for the next decade. To use 3D DRAM stacking successfully for general-purpose high performance processors, there are a few research issues yet to be addressed to make such integration feasible and reliable.

The first concern is related to thermal dissipation. Typically, the power consumption of DRAM is lower, sometimes orders of magnitude lower, than that of a processor. Simply stacking DRAM on a processor without meticulous consideration will lead to an over-heated DRAM, which in turn result in data loss due to either thermally accelerated leakage or more frequent refresh requirements worsening the power consumption and performance. First of all, a reliable and accurate thermal model considering a 3D-integrated DRAM and processor needs to be constructed to simulate and understand the problem space. Secondly, we need to continue to explore low-power architectural techniques and alternative mechanisms such as microfluid channels to reduce the heat conduction to the DRAM layers. Integrating these channels into thermal analysis will help the planning and placement of these channels at the architectural planning stage. Nonetheless, these channels will compete routing space against die-to-die vias for enhancing bandwidth. How to balance the performance while providing thermal reliability will be addressed in this work. Additionally, we plan to investigate the refresh methods of the 3D DRAM. Note that, the capacity of 3D-integrated DRAM is limited by several factors, including the die size budget and the accessible technology (i.e., the maximum number of integratable layers). A recent study [10] shows that on an Intel Core 2 Duo footprint, the maximum stackable DRAM capacity is 64MB. In other words, these DRAMs will only be used as a larger cache, backed up by on-board conventional DRAM memory. The number of accesses to these DRAM caches, especially for the multi-core processors, will be much more frequent than that of a conventional DRAM. As our preliminary study showed [24], unnecessary redundant refresh operations can be eliminated by tracking the memory access history. We will explore such opportunities in the design of a DRAM-stacked multi-core processor to understand the implication of DRAM stacking. Combined with the MRAM study, we will obtain an overall evaluation and better understanding of the ideal single-chip 3D die-stacked memory hierarchy.

4.2 Stacking with Performance Acceleration Layers

Another architectural level application of 3D integration is to provide value added features on-demand for a baseline 2D implementation. For example, researchers have demonstrated "snap on" functionality that enables online performance monitoring and execution profiling [47] or perform dynamic instruction verification to ensure reliability for a planar processor [**?**]. Similarly, we argue that 3D integration can also enhance overall performance by providing an on-demand "snap on" performance layer for certain market segments without incurring much NRE cost. The previous 3D DRAM-on-processor is one example to support large memory bandwidth by taking the advantages of high-density die-to-die vias. Another particular performance snap-on layer we propose to investigate is to provide acceleration functionality by rethinking massive parallel processors (MPPs) such as MasPar [**?**, **?**] or Connection Machine [**?**] in 3D. The goal is to provide a 3D layer for those performance-oriented systems that target applications containing large data parallelism. A snap-on performance acceleration die layer can stack a large computational fabric on top of a

general-purpose processor, providing extra FLOPS needed instantly. The prior MPP machines share a common feature — using a control processor to orchestrate a large array consisting of simple SIMD processing elements to exploit data level parallelism. Architecturally, this PE array can be considered as an acceleration extension (a performance feature, but not a necessity) for exploiting data level parallelism. 3D enables the flexibility of integrating one or several performance acceleration layers (or none when not needed) on top of a baseline processor for fulfilling different performance demands or costs. Such performance acceleration layers can be made high density mainly consisting of data processing specialized units such as a SIMD array with simplified point-to-point communication links and local SRAM memory. We anticipate such a layer contains almost no control logic, and thus is highly complexity-effective, low power with little effort to implement. There are several issues, however, that need to be addressed. To design a snap-on performance acceleration layer in a seamless manner, in other words, make such stacking completely optional, involves further investigation at the system architecture level. In this research, we will focus on the following areas: (1) how to design interconnection interface between the processor and the acceleration layer to enable a seamless integration? (2) how to control the execution of the 3D acceleration layer using extended ISA? (3) what is the suitable, low-cost programming model? (4) how to resolve code compatibility and scalability? i.e., how to develop an architecture that is independent and resilient with or without the acceleration layer?

5 3D EDA

Even though we have done some previous work on 3D EDA tool development, it is hard to use stand-alone 3D EDA tools for real design. We have seen many existing work on 3D EDA tool development. However, there are two problems associated with current 3D EDA efforts:

- It is unrealistic to develop EDA tools for 3D from the scratch. Ideally, design companies want to keep their original 2D commercial EDA tool flow, and expect that the flow can be modified for 3D design with minimum change on tool interfacing and methodologies.
- Different companies may use different design tool flow. Therefore, one 3D design methodology modified for a particular company may not work for another company.

Realize these two major challenges, what we propose is to develop 3D design methodologies based on OpenAccess, and integrate our 3D physical design toolsets with OpenAccess.

5.1 OpenAccess

Current design environments consist of a large number of design tools which contain applications and related databases. It significantly involves incompatible file formats and syntaxes. Engineers in CAD field spend a large amount of time integrating them using thousands of lines of translator code. However, the resulting flows are fragile and error-prone. In addition, they are inefficient and make IC design cycle times longer. To address these problems, **OpenAccess (http://openeda.si2.org)** appears as a community effort to provide inter-operability, not just data exchange, among IC design tools. This process is implemented through an open standard data API and reference database which supports that API for IC design. The OpenAccess database give users the opportunity to build flows incorporating design tools from different sources to best satisfy their needs. Written by C++ language, the OpenAccess API is the interface to IC design data. The API and reference implementation provide a high performance, high capacity electronic design database.

The main advantages of OpenAccess approach to Integrated Circuit design include the following: Reduce translation steps in the CAD flow; Keep the integration of data and/or data semantics between tools transfer; Make the representation semantics more standard, avoiding conflicts in data representation and misinterpretation; Centralize accessibility of all design data, assuring completeness of the stored information. Realize ”plug’n’play” of tools from different vendors and proprietary applications in a flow.

There are several ways that our 3D toolset can interface with OpenAccess:

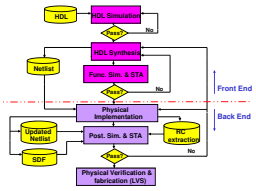


Figure 2: A general 2D EDA flow.

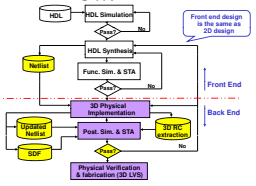


Figure 3: The modified 3D EDA flow. The major changes include 3D physical design, 3D RC extraction, and 3D LVS.

- file translation: data is extracted from OpenAccess using the API then rewritten to an data file that satisfy the application's requirement.
- data mapping: the application uses the OpenAccess API to access design data but then transfer it into a unique runtime model used by the application
- tight coupling: application modules work together in the same process using a common OpenAccess runtime model without conversions

5.2 Integration with Commercial EDA tools

A general 2D design flow is shown in Figure 2. 3D IC design is fundamentally related to the topological arrangement of logic blocks. Therefore, physical design tools play an important role in the adoption of 3D technologies.Based on our evaluation, we believe that the front end design may not need changes. We proposed a modified 3D design flow as shown in Figure 3.

The 3D physical design part, which includes 3D floorplanning, 3D placement, and 3D global routing, will be focusing on using OpenAccess database, such that the 3D physical design tool can be interfaced with any EDA flow. Figure 4 shows the concept of such OA-oriented approach.

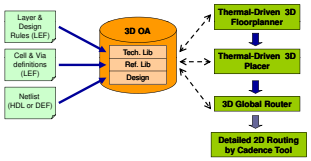


Figure 4: The 3D physical design tool will be developed based on using OpenAccess database, such that the 3D physical design tool can be interfaced with any EDA flow.

A major concern in the adoption of 3D architecture is the increased power densities that can result from placing one computational block over another in the multilayered 3D stack. Since power densities are already a major bottleneck in 2D architectures, the move to 3D architectures could accentuate the thermal problem. Even though 3D chips could offer some respite due to reduced interconnect power consumption (as a result of the shortening of many long wires), it is imperative to develop thermally aware physical design tools. For example, partition design to place highly loaded, active gates in layer close to the heat-sink.

We have already had experience on developing 3D physical design tools. For example, we have designed a thermal-aware floorplanner for a 3D microprocessors [**?**]. Our floorplanner is unique in that it accounts for the effects of the interconnect power consumption in estimating the peak temperatures. We developed a new 3D thermal estimation tool called *HS3D* [**?**] which is an extension of the original HotSpot tool, by including a variable number of additional levels, each composed of both a silicon layer and an inter-silicon "*glue*" material. To validate the multi-layer modeling, HS3D was compared to a commercial FEM tool, Flotherm, and showed an average temperature mis-estimation of 3^oC and a maximum deviation of 5^oC. The floorplanner used in this work is based on the B*-tree representation, which was proposed by Chang et al. [**?**]. A B*-tree is an ordered binary tree which can represent a non-slicing admissible floorplan. A simulated annealing engine is used to generate floorplanning solutions.

With the initial preliminary result [?, ?], we are very confident that the proposed 3D EDA tool flow will be very successful.

6 3D Testing Challenges

Krish/Sean/Yuan

Scan chain design

similarity bw MCM testing and 3D testing.

Core-based testing: Assuming a 3D SOC design, each core is a 2D IP core and they are stacking on several layers. It would be interesting to explore different TAM methods. would bus-based TAM still be the best? for example, the distance between two layers is very small (10um to 50 um), which may introduce a new TAM? what if each core itself is a 3D design (instead of stacking 2D cores onto multiple layers)? how does it affect TAM design.

6.1 Pre-bond Testability

Prior research thrusts proposed and studied several methods for partitioning their functions to exploit the benefits from 3D integration [10, 12, 30, 41, 50–52, 55]. In general, the partitioning schemes can be broadly classified into three categories: the technology level, architecure level, and circuits level.

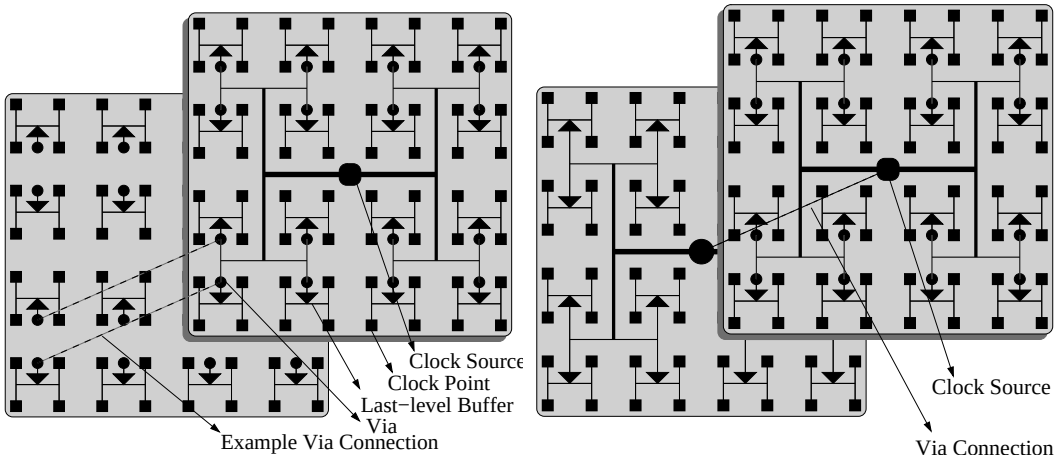
To make 3D designs commerically viable, it faces a major challenge: exponentially decreasing yield resulting from the integration of many distinct components. One naive testing strategy is bond-and-pray; that is, no testing is performed on the individual layer before they are bonded together. To enable the integration of a large number of die layers, however, this will not suffice economically. pre-bond testability becomes a necessity. Enabling pre-bond testability requires that eacy layer, independent of all other layers, maintain some basic level of functionality. In other words, each incomplete die must be tested invidually before bonding is applied. 3D partitioning at the technology level, each layer could be independently tested using existing test methods. For testing 3D designs partitioned at the architectural and circuits levels, different testing methods need to be considered as each layer will contain only partial, incomplete circuits, making pre-bond test very difficult if not prohibitively impossible.

The simplest mechanism would be to probe each die-to-die via individually, providing or observing test values as necessary. Unfortunately, this is not a viable solution as the number of vias on a given layer can vary from hundreds to even hundreds of thousands, which is beyond the capabilities of moden testers. Additionally, the process of actually making a connection with a test probe is a very stressful and damaging procedure, that in turn could damage die-to-die vias to the point where the neighboring die could not be successfully bonded post-layer-test. Beyond this challenge of incompleteness, several other concerns need to be properly addressed as well. First is the question of how pre-bond test fits into the larger testability picture. The extra hardware required for pre-bond test could potentially occupy space after bonding is done, leading to wasted resources. The pre-bond test hardware should be integrated into the post-bond test strategy. The second challenge is the state of the fundamental support nets including power, ground, and clock. These nets could exist as isolated, distributed islands on each die layer pre-bond. If they are not fully connected, test of the logic they support will become very difficult. The third challenge is regarding the test pads. In a traditional planar design, bond pads serve double-duty as test probe touchdown points and wire bond contacts for interfacing the chip to the outside world. In a 3D design, only bond pads on the top layer can play both roles. Any pads placed on lower layers only provide a test interface and are left hanging afterwards. Thus, test pads must be used very judiciously to control the area overheads.

Toward these issues, we propose to explore the following techniques to address testability for both architecture-partitioned and circuits-partitioned 3D implementations. One primary goal of this research is to provide a general framework for both pre-bond and post-bond tests for 3D circuits. In other words, we plan to identify new test strategies that can maximize the reuse of required pre-bond test hardware for post-bond tests in order to minimize the overheads of our 3D test mechanism.

In the case of architecture-partitioned 3D circuits, we will investigate the needed extra logic and their insertion points for enabling module-level tests. Note that, under such partitioning, a microarchitectural module could receive inputs from a different layer and output their results to another layer, while the complete functionality of the module is self-contained. The die-to-die vias are used as bounary interface to carry input and output singals between modules spread across different layers. Even though the complete functionality of the entire circuits is missing pre-bond, testing each module could be done by integrating specialized scan registers in place of these interface vias for each layer. The concept is similar to a test strategy called *Scan Islands* [9] employed by Alpha 21364. In essence, eacn isolated, incomplete architectural module on one layer can be treated as a test island. The isolation will be bridged by specialized scan registers pre-bond. During pre-bond test mode, these registers closed the borders of the islands, replacing incoming values with test values from the scan chain. For normal operations post-bond, these registers allowed data to flow freely between islands. One area we will explore is with regards to how to reuse these scan registers implemented for pre-bond test to enable a full-chip test after bonding is applied.

The functionality of on-die assets mostly relies on two main types of modules: SRAM-based blocks and arithmetic units. For example, more than 60% of the transistors on a modern processor were dedicated to various tables, register files, and caches based on SRAM. Due to the homogenity of these modules, to address DFT issues for circuits-partitioned designs, we will investigate the solutions for SRAM and simple units such as a parallel prefix adder. For the SRAM-based structures, processors often multi-port the SRAM to enable silmutaneous multiple reads or writes, which also leads to quadratic growth in area. As shown in prior studies, splitting ports into 3D layers can substantially reduce the footprint of the memory structure as well as shorten the wire length and wire load. Such circuits level partitioning leaves the cross-coupled inverter pair on one single layer with other ports and their decoders, drivers, and sense amplifiers on separate layers, creating a serious pre-bond challenge. To ensure testability, in this research, we try to address the questions: how to consider DFT in the early stage of partitioning while still maintaining the benefits of circuits level partitioning? Our basic idea is to create a closed circuit loop for the isolated, incomplete circuitry in the partitioning stage as a pre-bond testability requirement. For example, in the port-splitting SRAM, we can consider to implement at least one read port and one write port on the layer with no storage cell. As such, a test vector can be



(a) Power-optimized 3D clock tree (b) Desired 3D clock tree for DFT

Figure 5: H-Tree style 3D Clock Trees

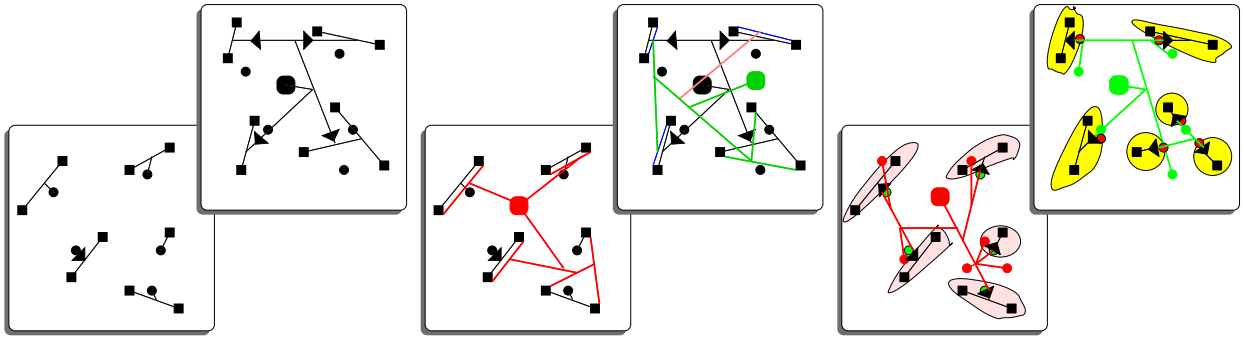
applied to the write port but will be read out immediately by the read port as these two ports, when the same address is enabled, form a loop between the input bitline of the write port and the output bitline of the read port. This has the effect of the write port placing a value on the internal nodes and the read port immediately reading it. This strategy will test all SRAM components including address decoder, write hardware, bitlines and wordlines, ports, and sense amplifiers. The latter four all participate directly in passing the test data, so it is easy to see how they are tested. The address decoders, on the other hand, are tested in a slightly indirect manner. Since the write decoder and all read decoders all should be receiving the same address and producing the same one-hot register entry, a fault in one of them will activate the wrong entry and produce an error on the output. Based on such DFT strategy, we will investigate testing methods for other SRAM based components that use circuits-partitioning.

6.2 3D Clocking Design For Pre-bond Test

As mentioned earlier, pre-bond testability requires each layer to maintain certain basic functionality. This implies that the hardcore components of each layer, e.g., power network, global reset, clock distribution, etc., must remain fully functional pre-bond for testing purposes. Pre-bond clock distribution is particularly challenging because this net is delicate (it must be designed for zero-skew operaion) but can also be costly (it is a global net that must constantly switching, consuming massiv amounts of routing area and dynamic power). In fact, from the perspective of design-for-test, this is a unique, new problem due to 3D integration.

To take testability, performance, and power all into account, ther are two competing goals in 3D clock design. On one hand, it is desired to have a clock network as shown in Figure 5(a) that maximizes the use of inter-die vias to reduce dynamic power and skew, as well as improve the routability. On the other hand, a fully connected clock on each layer as shown in Figure 5(b) is needed to provide source clock for pre-bond testing. A power-optimized design is usually less testable since the clock net on each layer can be highly segmented. Whereas a pre-bond testable design can be power-inefficient due to the redundancy in horizontal routing, diminishing the benefit obtained from 3D integration.

To find a clock that is both power efficient and testable pre-bond, we propose to investigate techniques that integrate both an optimized 3D clock tree and a separate clock tree structure for testability. Figure 6(a) shows an optimized 3D clock tree for a 2-layer 3D circuit, in which the bottom layer contains five isolated clock islands while the top layer contains an almost complete 2D clock tree. Such an optimized tree leverages the advantages of high-density, short-distance inter-die vias to complete the entire clock tree after bonding. Apparently, it will be difficult to perform pre-bond tests for the bottom layer due to these distributed yet unconnected clock islands. Our first approach is to perform individual clock routing for each die layer after the optimized 3D clock routing is finished. As shown in Figure 6(b), there are two additional semi-global routings performed for each individual layer. Pre-bond, these semi-global clock connects all clock points on just that layer. Post-bond, the 3D optimized clock tree synchronizes the chip



(a) Optimized 3D clock tree (b) Test clock approach (c) Redundant clocks approach

Figure 6: H-Tree style 3D Clock Trees

to achieve minimum power while meeting the skew requirement. Another approach we propose to investigate is shown in Figure 6(c). In this scheme, we will perform clock routing optimized for 3D, which will creates a almost complete planar tree in one layer with many clock islands on the rest of the layers.

7 Educational Aspects and Outreach Activities

This project will involve graduate and undergraduate students in all aspects of the research.

8 Project Management

The research team poses complementary skills required for the project. The PIs are well qualified for the proposed research with significant prior experience in various areas. Prof. Krish brings his extensive experience in testing domain; Prof. Narayanans expertise is in reliability, power aware systems/tools and emerging technologies; Prof. Xies expertise span areas of VLSI and architecture, as well as EDA domain, with extensive experience in 3D IC domain. Prof. Sean Lee's expertise is mainly in architecture, with many years' industry experience in Intel. The PIs will work in close coordination on different parts of this multi-disciplinary project. The integration of all these research components and tool will be a coordinated effort by all the investigators. The research will include four Ph.D. students. Detailed project milestones are given in Figure.

9 Results from Prior NSF Support

Krish's Prior NSF support;

Vijay's Prior NSF support;

Lee's prior research supported by NSF includes 1) *ITR CNS-0325536: Toward Autonomous Computing Platforms: System-Wide Hardware/ Software Performance Monitoring and Adaptation*, 10/2003-09/2008. This project focuses on developing a flexible, FPGA-assisted infrastructure for non-intrusive hardware monitoring across the entire system. The goal is to construct a self-adapting, self-aware system with the assistance of microarchitectural support and the FPGA. The outcomes of this work have been published in [14, 43, 62–71, 73–79, 87]. 2) *ITR CCF-0326396: Collaborative Research: Morphable Software Services: Self-Modifying Programs for Distributed Embedded Systems*, 10/2003-06/2007. (Lee was listed as a senior personnel.) The project investigated low-power processing techniques for sustaining collaborative morphable services under extreme, inaccessible conditions. Lee's focus was to develop power reduction techniques, primarily for memory subsystems. The outcomes of this work were published in [4–6, 21–27, 38, 39, 83]. 3) *CAREER CNS-0644096: Introspective Computing: A Multcore Approach to Availability, Reliability, and Security*, 06/2007-05/2012. This new project investigates an introspective multi-core procesor architecture that can perform fine-grained security introspection, instant low-overhead checkpoint, and fast, on-demand

rollback revovery. The goal is to provide a synergistic and holistic solution toward the challenges of achieving high availability, reliability, and securty for a comupting system.

Xie's current research is partly supported by: 1) NSF CNS 0454123: *SEAT – Soft Error Analysis Toolset* (co-PI). 06/2005-05/2008. This CRI (Computer Research Infrastructure) project aims at developing a soft error analysis toolset for hardware. Some of the results have been published [**?**, **?**, **?**, **?**, 60, 61, 80, 81, 84]. 2)NSF CAREER *CNS-0643902: Process Variation Aware Embedded System Synthesis*.01/2007-12/2011. This CAREER project aims at developing variation aware analysis and synthesis techniques for embedded system design. The project has resulted in a few publications, including ASP-DAC 2008 Best Paper Award Nomination. 3)(NSF): *CCF 0702617: HoDoo: Holistic Design of On-chip Interconnects*. 08/2007-07/2010. This project aims at developing high performance, low power, reliable on-chip network for future NoC architectures. 4)NSF *CNS 0720659: Hybrid Timing Analysis via Multi-mode Execution*. 01/2008-12/2010. This project aims at developing worst-case execution time analysis techniques for embedded systems that employ modern microarchitectures.

REFERENCES CITED

References

[1] V. Agarwal, M. S. Hrishikesh, S. W. Keckler, and D. Burger. Clock rate versus ipc: The end of the road for conventional microarchitectures. In *Computer Architecture, 2000. Proceedings of the 27th International Symposium on*, pages 248–259, 2000.

[2] D. H. Albonesi and I. Koren. Improving the memory bandwidth of highly-integrated, wide-issue, microprocessor-based systems. In *Parallel Architectures and Compilation Techniques., 1997. Proceedings. 1997 International Conference on*, pages 126–135, 1997.

[3] Karthik Balakrishnan, Vidit Nanda, Siddharth Easwar, and Sung Kyu Lim. Wire congestion and thermal aware 3d global placement. In *Proc. of Asia South Pacific Design Automation Conference (ASPDAC)*, pages 1131–1134, 2005.

[4] Chinnakrishnan S. Ballapuram, Hsien-Hsin S. Lee, and Milos Prvulovic. Synonymous Address Compaction for Energy Reduction in Data TLB. In *ISPLED'05: Proceedings of the 2005 ACM/IEEE International Symposium on Low Power Electronics and Design*, pages 357–362, San Diego, CA, 2005.

[5] Chinnakrishnan S. Ballapuram, Kiran Puttaswamy, Gabriel H. Loh, and Hsien-Hsin S. Lee. Entropy-based low power data tlb design. In *Proceedings of the ACM/IEEE International Conference on Compilers Architecture and Synthesis for Embedded Systems*, 2006.

[6] Chinnakrishnan S. Ballapuram, Ahmad Sharif, and Hsien-Hsin S. Lee. Exploiting access semantics and program behavior to reduce snoop power in chip multiprocessors. In *Proceedings of the 13th ACM Internatioanl Conference on Architectural Support for Programming Languages and Operating Systems*, 2008.

[7] K. Banerjee, S. Souri, P. Kapur, and K. Saraswat. 3d ics: A novel chip design for improving deep-submicrometer inteconnect performance and system-on-chip integration. In *Proc. of the IEEE, Special Issue, Interconnections-Addressing The Next Challenge of IC Technology*, volume 89, 2001.

[8] K. Bernstein. New dimension in performance. *EDA Forum*, 3(2), 2006.

[9] Dilip K. Bhavsar and Richard A. Davies. Scan islands - a scan partitioning architecture and its implementation on the alpha 21364 processor. In *VTS '02: Proceedings of the 20th IEEE VLSI Test Symposium*, page 16, Washington, DC, USA, 2002. IEEE Computer Society.

[10] B. Black, M. Annavaram, N. Brekelbaum, J. DeVale, L. Jiang, G. H. Loh, D. McCauley, P. Morrow, D. W. Nelson, D. Pantuso, P. Reed, J. Rupley, S. Shankar, J. Shen, and C. Webb. Die Stacking (3D) Microarchitecture. In *Proceedings of the 39th International Symposium on Microarchitecture*, 2006.

[11] B. Black, D. W. Nelson, C. Webb, and N. Samra. 3d processing technology and its impact on ia32 microprocessors. In *Proc. of 2004 IEEE International Conference on Computer Design (ICCD)*, pages 316–318, 2004.

[12] Bryan Black, Donald Nelson, Clair Webb, and Nick Samra. 3D Processing Technology and Its Impact on iA32 Microprocessors. In *Proceedings of the 22nd International Conference on Computer Design*, pages 316–318, 2003.

[13] J. Carson. The emergence of stacked 3d silicon and its impact on microelectronics systems integration. In *Innovative Systems in Silicon, 1996. Proceedings., Eighth Annual IEEE International Conference on*, pages 1–8, 1996.

[14] Christopher R. Clark, Ripal Nathuji, and Hsien-Hsin S. Lee. Using an FPGA as a Prototyping Platform for Multi-core Processor Applications. In *Workshop on Architecture Research using FPGA Platforms in conjunction with International Symposium on High-Performance Computer Architecture (WARFP-05)*, February 2005.

[15] J. Cong, J. Wei, and Y. Zhang. A thermal-driven floorplanning algorithm for 3d ics. In *Proc. of International Conference Computer-Aided Design (ICCAD)*, 2004.

[16] S. Das, A. Chandrakasan, and R. Reif. Design tools for 3-d integrated circuits. In *Design Automation Conference, 2003. Proceedings of the ASP-DAC 2003. Asia and South Pacific*, pages 53–56, 2003.

[17] S. Das, A. Chandrakasan, and R. Reif. Timing, energy, and thermal performance of three-dimensional integrated circuits. In *Proc. of the 13th ACM Great Lakes Symposium on VLSI (ISVLSI)*, 2004.

[18] S. Das, A. Fan, K. N. Chen, C. S. Tan, N. Checka, and R. Reif. Technology performance and computer-aided design of three-dimensional integrated circuits. In *Proc. of the 2004 International Symposium on Physical Design (ISPD)*, pages 108–115, 2004.

[19] W. R. Davis, J. Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A. M. Sule, M. Steer, and P. D. Franzon. Demystifying 3d ics: The pros and cons of going vertical. *IEEE Design & Test of Computers*, 22(6):498–510, 2005.

[20] Y. Deng and W. Maly. 2.5-Dimensional VLSI System Integration. In *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, number 6, pages 668–677, 2005.

[21] Yuvraj Singh Dhillon, Abdulkadir Utku Diril, Abhijit Chatterjee, and Hsien-Hsin Sean Lee. Algorithm for Achieving Minimum Energy Consumption in CMOS Circuits Using Multiple Supply and Threshold Voltages at the Module Level. In *ICCAD '03: Proceedings of the 2003 IEEE/ACM International Conference on Computer-Aided Design*, pages 693–700, 2003.

[22] Mongkol Ekpanyapong, Pinar Korkmaz, and Hsien-Hsin S. Lee. Choice Predictor for Free. In *Proceedings of the 9th Asia-Pacific Computer System Architecture Conference*, pages 399–413, September 2004.

[23] Joshua B. Fryman, Chad Huneycutt, Hsien-Hsin S. Lee, Kenneth M. Mackenzie, and David E. Schimmel. Energy-Efficient Network Memory for Ubiquitous Devices. *IEEE Micro special issue on Power Complexity Aware Design*, 23(5):60–70, September/October 2003.

[24] Mrinmoy Ghosh and Hsien-Hsin S. Lee. Smart refresh: An enhanced memory controller design for reducing energy in conventional and 3d die-stacked drams. In *Proceedings of the 40th International Symposium on Microarchitecture*, 2007.

[25] Mrinmoy Ghosh and Hsien-Hsin S. Lee. Virtual exclusion: An architectural approach to reducing leakage energy in caches for multiprocessor systems. In *Proceedings of the 13th IEEE International Conference on Parallel and Distributed Systems*, 2007.

[26] Mrinmoy Ghosh, Emre Ozer, Stuart Biles, and Hsien-Hsin S. Lee. Efficient System-on-Chip energy Management with a Segmented Bloom Filter. In *ARCS '06: Proceedings of the 19th International Conference on Architecture of Computing Systems*, pages 283–297, March 2006.

[27] Mrinmoy Ghosh, Weidong Shi, and Hsien-Hsin S. Lee. CoolPression — A Hybrid Significance Compression Technique for Reducing Energy in Caches. In *Proceedings of the IEEE International System-on-Chip Conference*, pages 399–402, September 2004.

[28] B. Goplen and S. S. Sapatnekar. Efficient thermal placement of standard cells in 3d ics using a force directed approach,. In *International Conference on Computer-Aided Design*, pages 86–89, 2003.

[29] B. Goplen and S. S. Sapatnekar. Thermal via placement in 3d ics,. In *International Symposium on Physical Design*, pages 167–174, 2004.

[30] S. Gupta, M. Hilbert, S. Hong, and R. Patti. Techniques for Producing 3D ICs with High-Density Interconnect. In *VMIC '04: Proceedings of the 21st International VLSI Multilevel Interconnection Conference*, Waikoloa Beach, HI, USA, 2004.

[31] B. Hoefflinger, S. T. Liu, and B. Vajdic. A three-dimensional cmos design methodology. *Electron Devices, IEEE Transactions on*, 31(2):171–173, 1984. 0018-9383.

[32] J. Joyner and J. Meindl. Opportunities for reduced power dissipation using 3d integration. In *Proc. of International Testing Conference (ITC)*, 2002.

[33] J. W. Joyner and J. D. Meindl. Opportunities for reduced power dissipation using three-dimensional integration. In *Interconnect Technology Conference, 2002. Proceedings of the IEEE 2002 International*, pages 148–150, 2002.

[34] J. W. Joyner, R. Venkatesan, P. Zarkesh-Ha, J. A. Davis, and J. D. Meindl. Impact of three-dimensional architectures on interconnects in gigascale integration. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 9(6):922–928, 2001. 1063-8210.

[35] J.W. Joyner, P. Zarkesh-Ha, and J.D. Meindl. A stochastic global net-length distribution for a three-dimensional system-on-a-chip (3D-SoC). In *Proc. 14th Annual IEEE International ASIC/SOC Conference*, September 2001.

[36] C. Kuan-Neng, M. J. Kobrinsky, B. C. Barnett, and R. Reif. Comparisons of conventional, 3-d, optical, and rf interconnects for on-chip clock distribution. *Electron Devices, IEEE Transactions on*, 51(2):233–239, 2004. 0018-9383.

[37] Young-Su Kwon, Payam Lajevardi, Frank Honor, and Anantha P. Chandrakasan. A 3-d fpga wire resource prediction model validated using a 3-d placement and routing tool. In *Proc. of System Level Interconnect Prediction workshop (SLIP)*, 2005.

[38] Hsien-Hsin S. Lee and Chinnakrishnan S. Ballapuram. Energy Efficient D-TLB and Data Cache using Semantic-Aware Multilateral Partitioning. In *ISPLED'03: Proceedings of the 2003 ACM/IEEE International Symposium on Low Power Electronics and Design*, pages 306–311, Seoul, Korea, August 2003.

[39] Hsien-Hsin S. Lee, Joshua B. Fryman, A. Utku Diril, and Yuvraj S. Dhillon. The Elusive Metric for Low-Power Architecture Research. In *Workshop on Complexity-Effective Design in conjunction with the 30th ACM/IEEE International Symposium on Computer Architecture (WCED-03)*, San Diego, California, June 2003.

[40] X. Lei, C. C. Liu, K. Hong-Seung, S. K. Kim, and S. Tiwari. Three-dimensional integration: Technology, use, and issues for mixed-signal applications. *Electron Devices, IEEE Transactions on*, 50(3):601–609, 2003. 0018-9383.

[41] F. Li, C. Nicopoulos, T. Richardson, Y. Xie, N. Vijaykrishnan, and M. Kandemir. Design and Management of 3D Chip Multiprocessors using Network-in-Memory. In *Proceedings of the International Symposium on Computer Architecture*, 2006.

[42] C. C. Liu, I. Ganusov, M. Burtscher, and S. Tiwari. Bridging the processor-memory performance gap with 3d ic technology. *IEEE Design & Test of Computers*, 22(6):556– 564, 2005.

[43] Chenghuai Lu, Tao Zhang, Weidong Shi, and Hsien-Hsin S. Le. "M-TREE: A High Efficiency Security Architecture for Protecting Integrity and Privacy of Software. *Journal of Parallel and Distributed Computing for a special issue on Security in Grid and Distributed Systems*, 66(9), 2006.

[44] J. Mayega, O. Erdogan, P. M. Belemjian, K. Zhou, J. F. McDonald, and R. P. Kraft. 3d direct vertical interconnect microprocessors test vehicle. In *Proc. of the 13th ACM Great Lakes symposium on VLSI (GLSVLSI)*, pages 141–146, 2003.

[45] I. Meikei, K. W. Guarini, V. Chan, K. Bernstein, R. Joshi, J. Kedzierski, and W. Haensch. Three dimensional cmos devices and integrated circuits. In *Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003*, pages 207–213, 2003.

[46] Jacob Minz, Eric Wong, and Sung Kyu Lim. Reliability-aware floorplanning for 3d circuits. In *Proc. of IEEE International SOC Conference*, 2005.

[47] Shashidhar Mysore, Banit Agrawal, Navin Srivastava, Sheng-Chih Lin, Kaustav Banerjee, and Timothy Sherwood. Introspective 3D Chips. In *Proceedings of the International Conference on Architectural Support for Programming Languages and Operating Systems*, 2006.

[48] A. Nahman, A. Fan, J. Chung, and R. Reif. Wire-length distribution of three-dimensional integrated circuits. In *Interconnect Technology, 1999. IEEE International Conference*, pages 233–235, 1999.

[49] Viet Nguyen and Philip Christie. The impact of interstratal interconnect density on the performance of 3d ics. In *Proc. of System Level Interconnect Prediction workshop (SLIP)*, 2005.

[50] Kiran Puttaswamy and Gabriel Loh. Implementing Caches in a 3D Technology for High Performance Processors. In *Proc. the International Conference on Computer Design (ICCD)*, October 2005.

[51] Kiran Puttaswamy and Gabriel Loh. Dynamic instruction schedulers in a 3-dimensional integration technology. In *Proc. Great Lakes Symopsium on VLSI (GLSVLSI)*, 2006.

[52] Kiran Puttaswamy and Gabriel Loh. The impact of 3-dimensional integration on the design of arithmetic units. In *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, 2006.

[53] Kiran Puttaswamy and Gabriel Loh. Implementing register files for high-performance microprocessors in a die-stacked (3d) technology. In *Proc. IEEE International Symposium on VLSI (ISVLSI)*, 2006.

[54] Kiran Puttaswamy and Gabriel Loh. Thermal analysis of a 3d die-stacked high-performance microprocessor. In *Proc. Great Lakes Symopsium on VLSI (GLSVSI)*, 2006.

[55] Kiran Puttaswamy and Gabriel H. Loh. Thermal Herding: Microarchitecture Techniques for Controlling Hotspots in High-Performance 3D-Integrated Processors. In *Proceedings of the 13th International Symposium on High-Performance Computer Architecture*, pages 193–204, 2007.

[56] A. Rahman, S. Das, R. Reif, and Anantha P. Chandrakasan. Wiring requirement and 3d integration technology for fpga. In *IEEE Trans. on VLSI Systems*, 2003.

[57] A. Rahman, A. Fan, and R. Reif. Comparison of key performance metrics in two- and three-dimensional integrated circuits. In *Interconnect Technology Conference, 2000. Proceedings of the IEEE 2000 International*, pages 18–20, 2000.

[58] A. Rahman, A. Fan, and R. Reif. Thermal analysis of 3d ics. In *Proc. International Testing Conference (ITC)*, 2001.

[59] A. Rahman and R. Reif. System-level performance evaluation of three-dimensional integrated circuits. *IEEE Trans. on VLSI Systems*, 8(6):671–678, 2005.

[60] R. Ramanarayanan, J. S. Kim, N. Vijaykrishnan, Y. Xie, and M. J. Irwin. Seat-la: A soft error analysis tool for combinational logic. In *IEEE International Conference on VLSI Design*, 2006.

[61] R. Ramanarayanan, R. Krishnan, N. Vijaykrishnan, Y. Xie, and M. J. Irwin. Temperature and voltage scaling effects on electrical masking,. In *The Second Workshop on System Effects of Logic Soft Errors*, 2006.

[62] Martin Schulz, Brian S. White, Sally A. McKee, Hsien-Hsin S. Lee, and Jurgen Jeitner. Owl: Next Generation System Monitoring. In *Proceedings of the ACM Computing Frontier 2005*, pages 116–124, 2005.

[63] Weidong Shi, Joshua B. Fryman, Guofei Gu, Hsien-Hsin S. Lee, Youtao Zhang, and Jun Yang. InfoShield: A Security Architecture for Protecting Information Usage in Memory. In *HPCA-12: Proceedings of the 12th International Symposium on High-Performance Computer Architecture*, pages 225–234, 2006.

[64] Weidong Shi and Hsien-Hsin S. Lee. Authentication control point and its implications for secure processor design. In *Proceedings of the 39th International Symposium on Microarchitecture*, pages 103–112, 2006.

[65] Weidong Shi and Hsien-Hsin S. Lee. Accelerating memory decryption and authentication with frequent value prediction. In *Proceedings of the ACM International Conference on Computing Frontiers*, pages 35–46, 2007.

[66] Weidong Shi, Hsien-Hsin S. Lee, Mrinmoy Ghosh, and Chenghuai Lu. Architectural Support for High Speed Protection of Memory Integrity and Confidentiality in Symmetric Multiprocessor Systems. In *PACT'04: Proceedings of International Conference on Parallel Architectures and Compilation Techniques*, pages 123–134, September 2004.

[67] Weidong Shi, Hsien-Hsin S. Lee, Mrinmoy Ghosh, Chenghuai Lu, and Alexandra Boldyreva. High Efficiency Counter Mode Security Architecture via Prediction and Precomputation. In *ISCA '05: Proceedings of the 32nd Annual International Symposium on Computer Architecture*, pages 14–24, 2005.

[68] Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu, and Mrinmoy Ghosh. Towards the issues in architectural support for protection of software execution. *SIGARCH Computer Architecture News*, 33(1):6–15, 2005.

[69] Weidong Shi, Hsien-Hsin S. Lee, Chenghuai Lu, and Tao Zhang. Attacks and Risk Analysis for Hardware Supported Software Copy Protection Systems. In *DRM '04: Proceedings of the 4th ACM workshop on Digital Rights Management*, pages 54–62, 2004.

[70] Weidong Shi, Hsien-Hsin S. Lee, Richard M. Yoo, and Alexandra Boldyreva. A digital right enabled graphics processing system. In *Proceedings of the ACM SIGGRAPH/Eurographics Workshop of Graphics Hardware*, pages 17–26, 2006.

[71] Weidong Shi, Chenghuai Lu, and Hsien-Hsin S. Lee. Memory-centric Security Architecture. In *Proceedings of the 2005 International Conference on High Performance Embedded Architectures and Compilers*, pages 153–168, 2005.

[72] P. Shiu and S. K. Lim. Multi-layer floorplanning for reliable system-on-package. In *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, 2004.

[73] Taeweon Suh, Douglas M. Blough, and Hsien-Hsin S. Lee. Supporting cache coherence in heterogeneous multiprocessor systems. In *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition Volume II (DATE'04)*, page 21150. IEEE Computer Society, 2004.

[74] Taeweon Suh, Daehyun Kim, and Hsien-Hsin S. Lee. Cache Coherence Support for Non-Shared Bus Architecture on Heterogeneous MP SoCs. In *Proceedings of the 42nd Design Automation Conference (DAC-42)*, pages 553–558, June 2005.

[75] Taeweon Suh, Hsien-Hsin S. Lee, and Douglas M. Blough. Integrating Cache Coherence Protocols for Heterogeneous Multiprocessor Systems, Part I. *IEEE Micro special issue on Embedded Systems: Architecture, Design and Tools*, pages 33–41, July/August 2004.

[76] Taeweon Suh, Hsien-Hsin S. Lee, and Douglas M. Blough. Integrating Cache Coherence Protocols for Heterogeneous Multiprocessor Systems, Part II. *IEEE Micro*, pages 70–78, September/October 2004.

[77] Taeweon Suh, Hsien-Hsin S. Lee, Shih-Lien Lu, and John Shen. Initial Observations of Hardware/Software Co-Simulation using FPGA in Architecture Research. In *Workshop on Architecture Research using FPGA Platforms in conjunction with International Symposium on High-Performance Computer Architecture (WARFP-06)*, February 2006.

[78] Taeweon Suh, Hsien-Hsin S. Lee, Sally A. McKee, and Martin Schulz. Evaluating System-wide Monitoring Capsule Design Using Xilinx Virtex-II Pro FPGA. In *Workshop on Architecture Research using FPGA Platforms in conjunction with International Symposium on High-Performance Computer Architecture (WARFP-05)*, February 2005.

[79] Taeweon Suh, Shih-Lien L. Lu, and Hsien-Hsin S. Lee. An fpga approach to quantifying coherence traffic efficiency on multiprocessor systems. In *Proceedings of the 17th International Conference on Field Programmable Logic and Applications*, 2007.

[80] B. Vaidyanathan, Y. Xie, N. Vijaykrishnan, and H. Zheng. Soft error analysis and optimizations of c-elements in asynchronous circuits. In *The Second Workshop on System Effects of Logic Soft Errors*, 2006.

[81] F. Wang and Y. Xie. An accurate and efficient model of electrical masking effect for se in combinatorial logic. In *The Second Workshop on System Effects of Logic Soft Errors*, 2006.

[82] Eric Wong and Sung Kyu Lim. 3d floorplanning with thermal vias. In *Proc. of Design, Automation and Test in Europe (DATE)*, 2006.

[83] Dong Hyuk Woo, Mrinmoy Ghosh, Emre Ozer, Stuart Biles, and Hsien-Hsin S. Lee. Reducing energy of virtual cache synonym lookup using bloom filters. In *Proceedings of the ACM/IEEE International Conference on Compilers Architecture and Synthesis for Embedded Systems*, 2006.

[84] S. Yang, W. Wolf, N. Vijaykrishnan, and Y. Xie. Reliability-aware soc voltage islands partition and floorplan. In *IEEE Computer Society Annual Symposium on Emerging VLSI Technologies and Architectures*, 2006.

[85] T. Zhang and S. Sapatnekar. Thermal via placement in 3d ics. In *Proc. of the ACM International Symposium on Physical Design (ISPD)*, pages 167–174, 2005.

[86] T. Zhang and S. Sapatnekar. Temperature-aware routing in 3d ics. In *Proc. of Asia South Pacific Design Automation Conference (ASPDAC)*, pages 309–314, 2006.

[87] Xiaotong Zhuang, Tao Zhang, Hsien-Hsin S. Lee, and Santosh Pande. Hardware Assisted Control Flow Obfuscation for Embedded Processors. In *Proceedings of the 2004 International Conference on Compilers, Architectures, Synthesis on Embedded Systems (CASES-04)*, Washington D.C., 2004.

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Five Related Publications

Yuan Xie, Gabriel Loh, Bryan Black, and Kerry Bernstein, "Design Space Exploration for 3D Architecture." ACM Journal of Emerging Technologies for Computer Systems, Vol. 2. No. 2, pp.65-103, April 2006.

Gabriel Loh, Yuan Xie, and Bryan Black. "Processor Design in Three-Dimensional Die-Stacking Technologies." IEEE Micro, Vol. 27. No. 3, pp.31-48, May/June 2007

Kim, J., C. Nicopoulos, D. Park, R. Das, Yuan Xie, N. Vijaykrishnan, C. R. Das. "A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures." Proceedings of the Annual International Symposium on Computer Architecture (ISCA), pp. 138-149, June 2007.

F. Li, C. Nicopoulos, T. Richardson, Yuan Xie, N. Vijaykrishnan, and M. Kandemir, "Design and Management of 3D Chip Multiprocessors using Network-in-memory." Proceedings of the Annual International Symposium on Computer Architecture (ISCA), pp. 130-141, June. 2006

W.-L. Hung, G. Link, Yuan Xie, N. Vijaykrishnan, and M. J. Irwin, "Interconnect and Thermal-aware Floorplanning for 3D Microprocessors." Proceedings of International Symposium on Quality Electronic Design (ISQED), pp. 98-104, March. 2006

Five Other Significant Publications

O. Ozturk, Feng Wang, M. Kandemir, Yuan Xie, "Optimal Topology Exploration for Application-Specific 3D Architectures." ; Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 390-395, Jan. 2006

Yuan Xie, W.Wolf, and H. Lekatsas. "Code Compression Using Variable-to-fixed Coding." IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 14. No. 5, pp.525-536, January. 2006.

W.L. Hung, X. Wu, Y. Xie, "Guaranteeing Performance Yield in High-Level Synthesis", In *IEEE International Conference on Computer Aids Design (ICCAD'06)*, 2006.

Y. Xie, W. Wolf, H. Lekatsas, "Code Compression for VLIW Processors Using Variable-to-fixed Coding", In *IEEE Transactions on VLSI*, Vol. 14, No.5, pp.525-536, 2006.

N.Vijaykrishnan, Y. Xie, "Reliability Concerns in Embedded System Designs", In *IEEE Computer*, Vol.39, No.1, pp.118-120, 2006.

Synergistic Activities

Associate Editor, IEEE Transaction on VLSI, 2007-

Guest co-Editor, ACM Journal of Emerging Technologies for Computer Systems (JETC) Special Issues on 3D ICs.

Technical Program Committee Member: LCTEC 2008, DAC 2008, ASP-DAC 2008, ISLPED 2007-2008, Computing Frontiers 2007, Nano-Net 2006, CASES 2006, GLSVLSI 2006-2008,

Honors and Awards

ASP-DAC Best Paper Award Nomination, 2008

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Chun-Hui Outstanding Overseas Scholar Award, Chinese Ministry of Education, 2006

ICCADBest Paper Award Nomination, 2006

SRC (Semiconductor Research Corporations) Inventor Recognition Awards, 2002

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Graduate Advisors

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Students

Current Students: 6 Ph.D. students, 1 M.S. student;

Graduated student: 2 Ph.D. and 1 M.S.

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