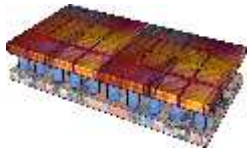
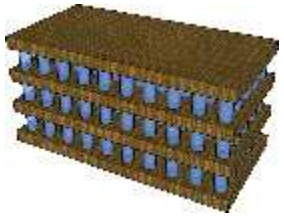
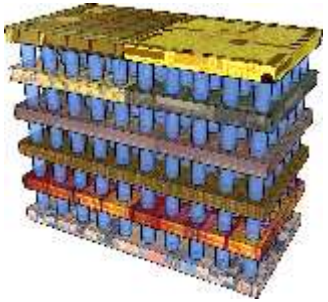
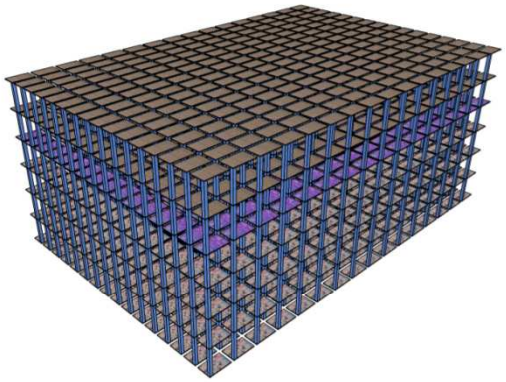
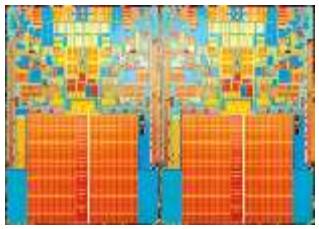
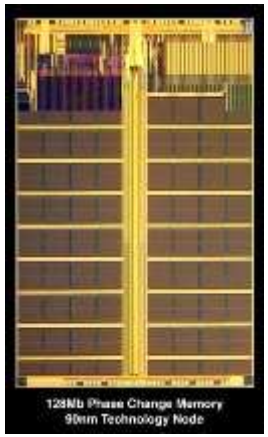








Workshop on Architecting Memory Technologies
ASPLOS XV, 2010

So Little Bandwidth, So Many Memories



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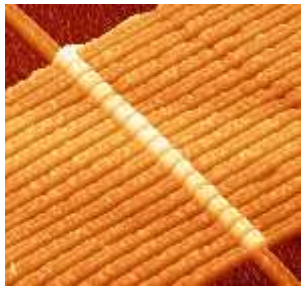
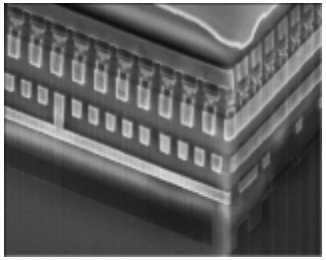
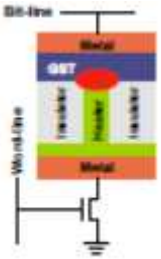

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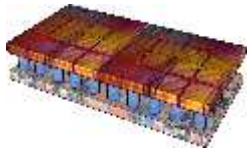
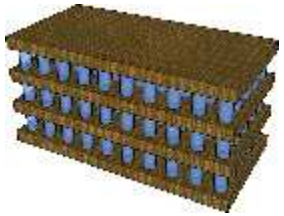
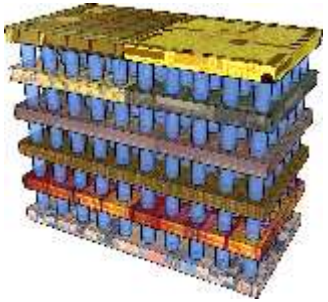
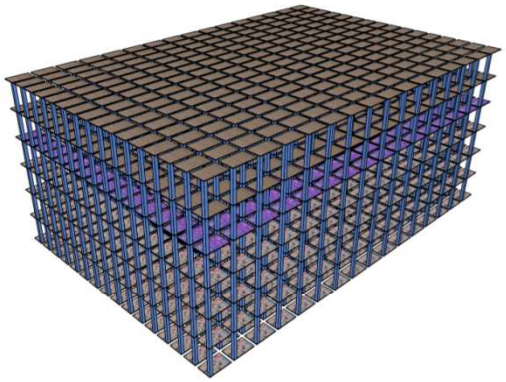

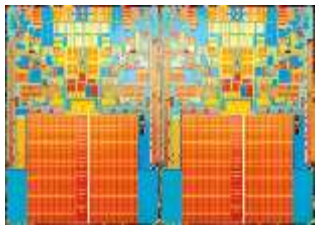

Workshop on Architecting Memory Technologies
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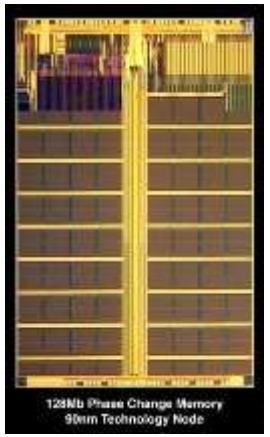
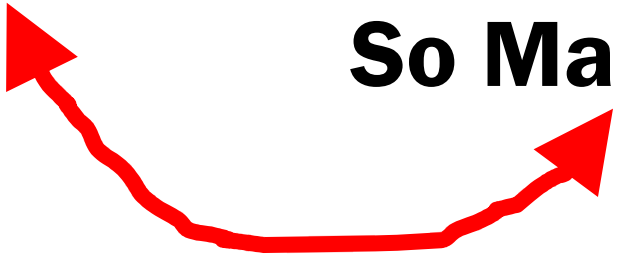
So Little Bandwidth, So Many Memories





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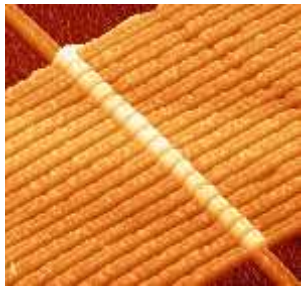
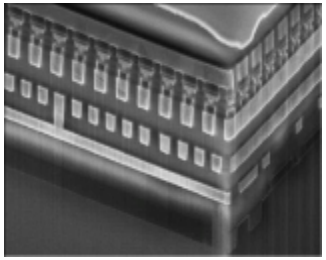
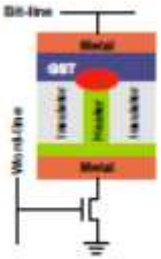

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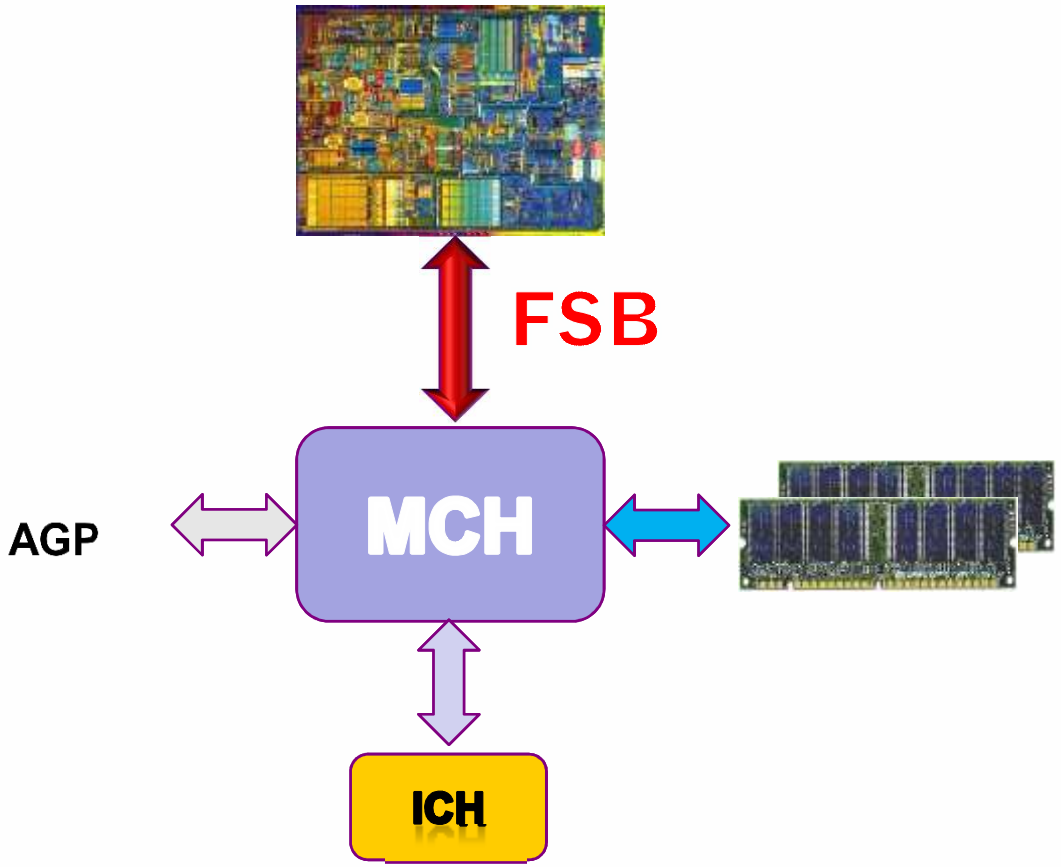
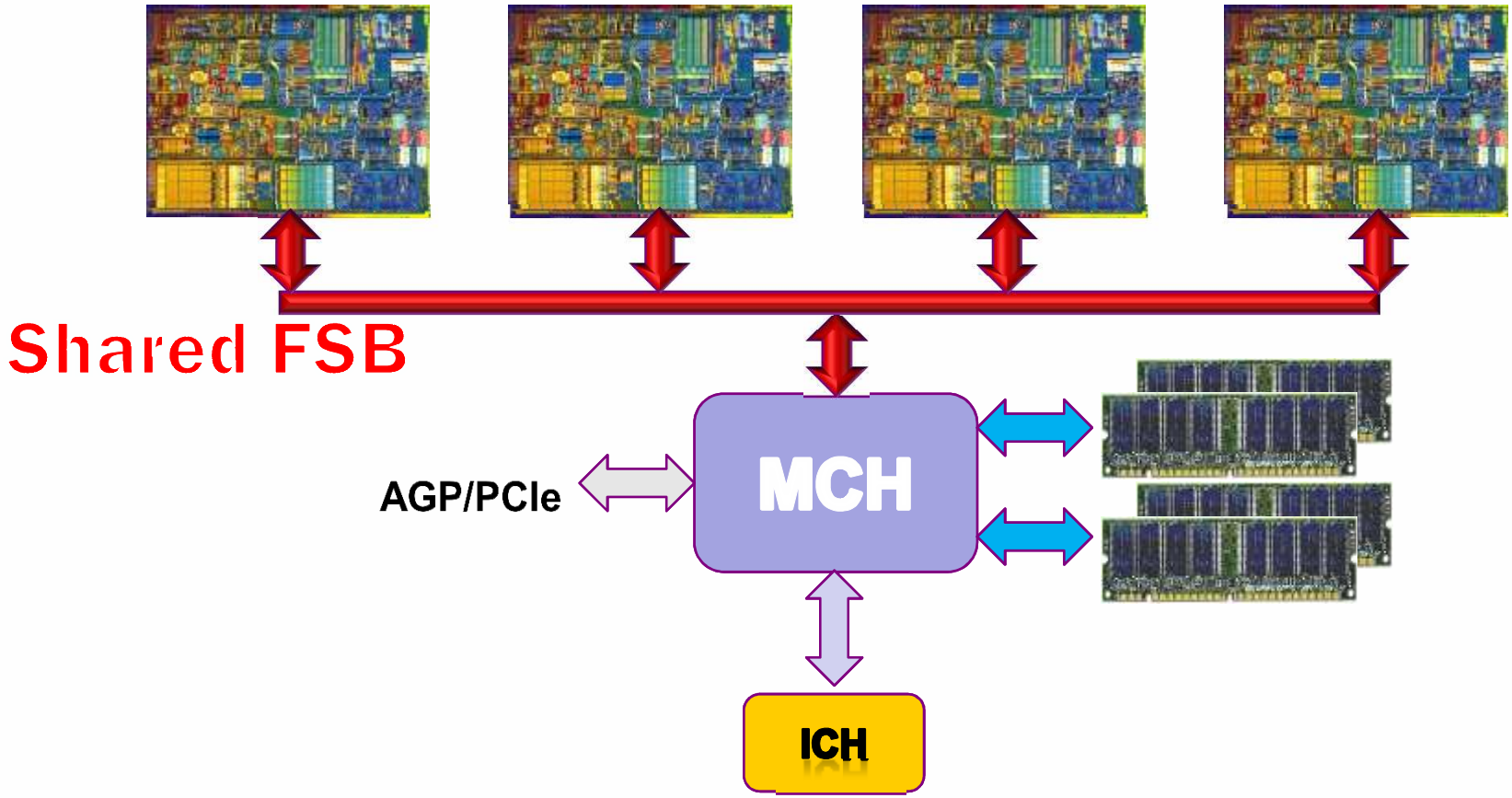
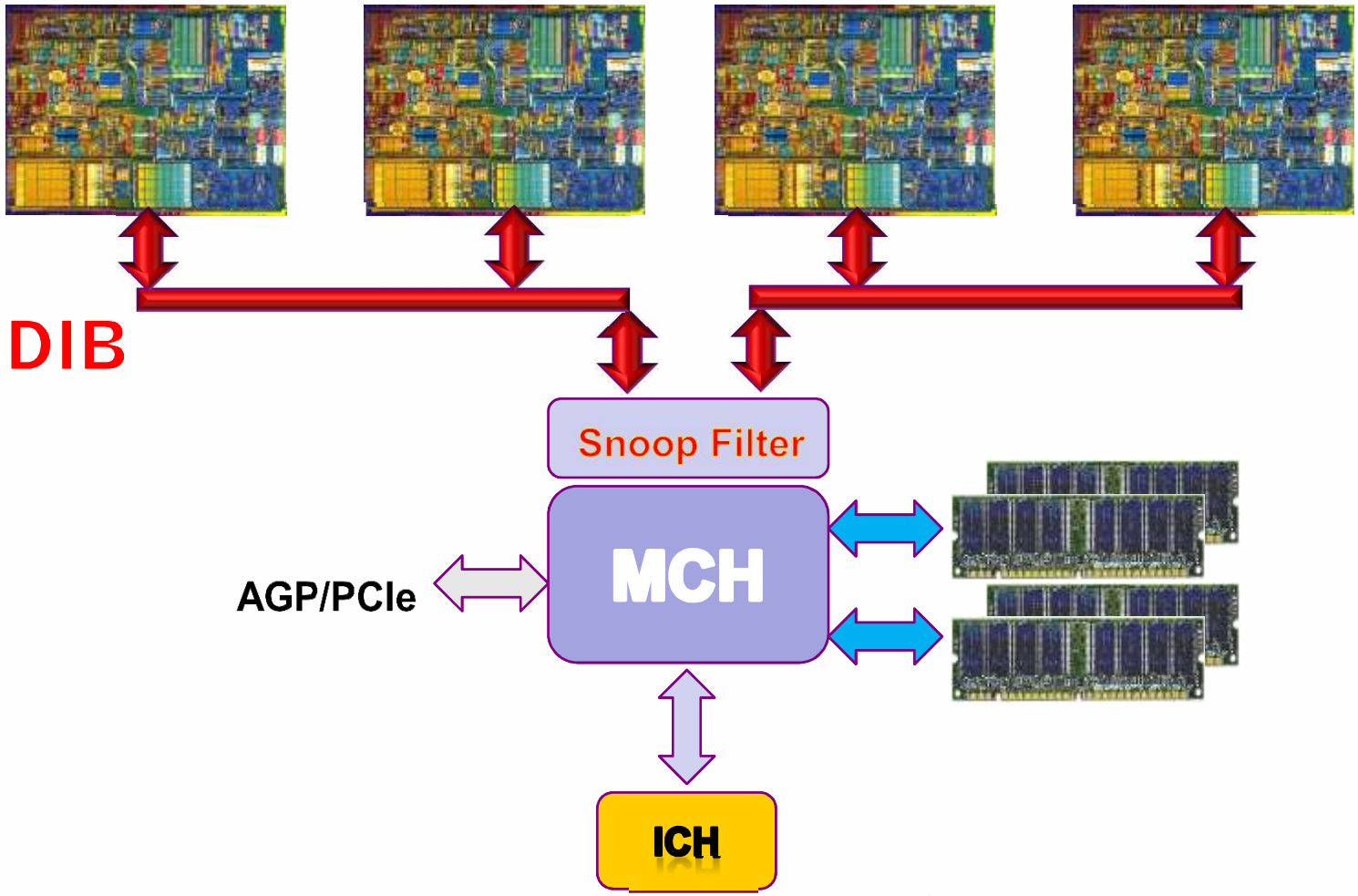
Once Upon A Time … .. .



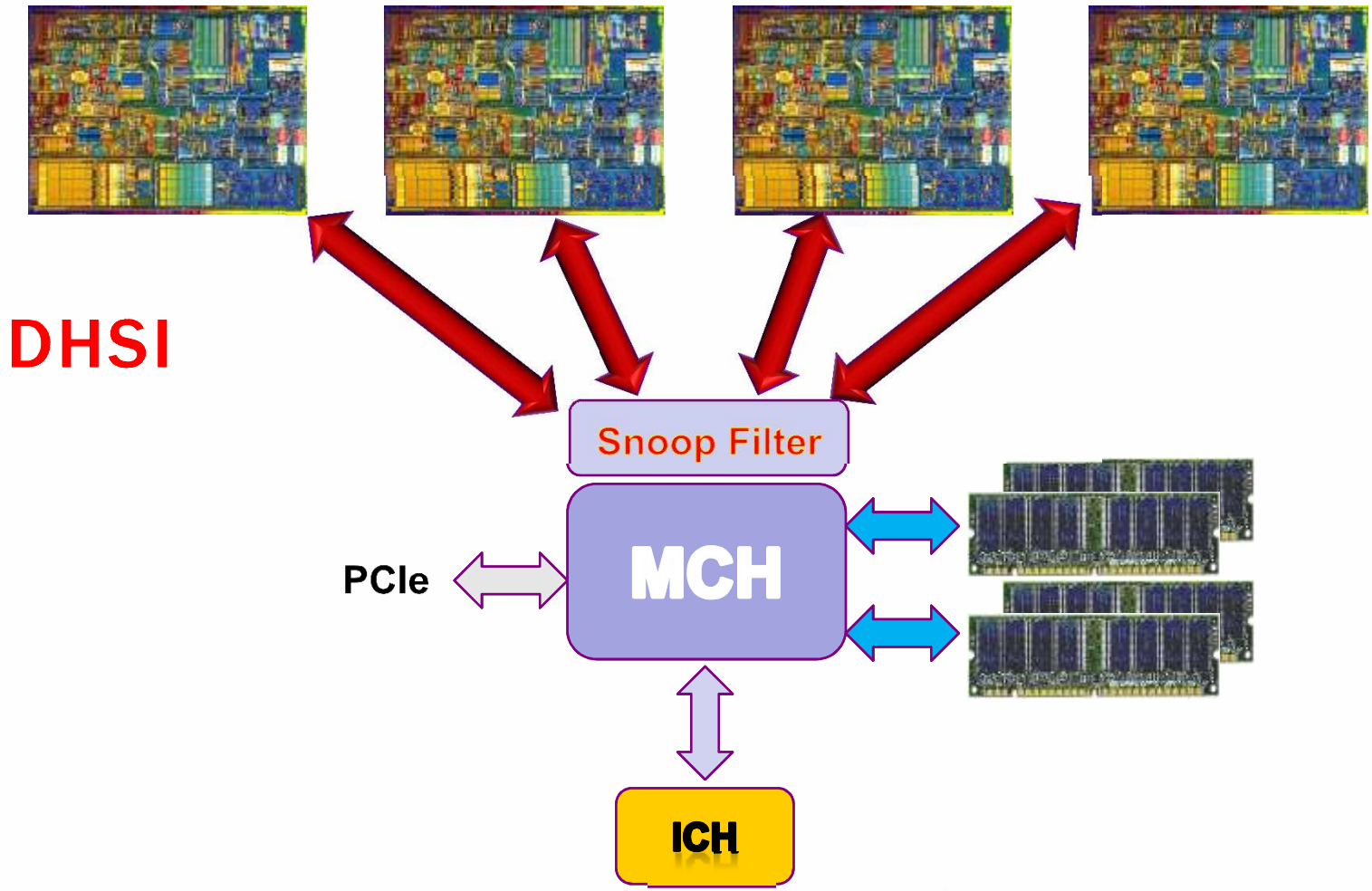
Evolution of Memory Bandwidth



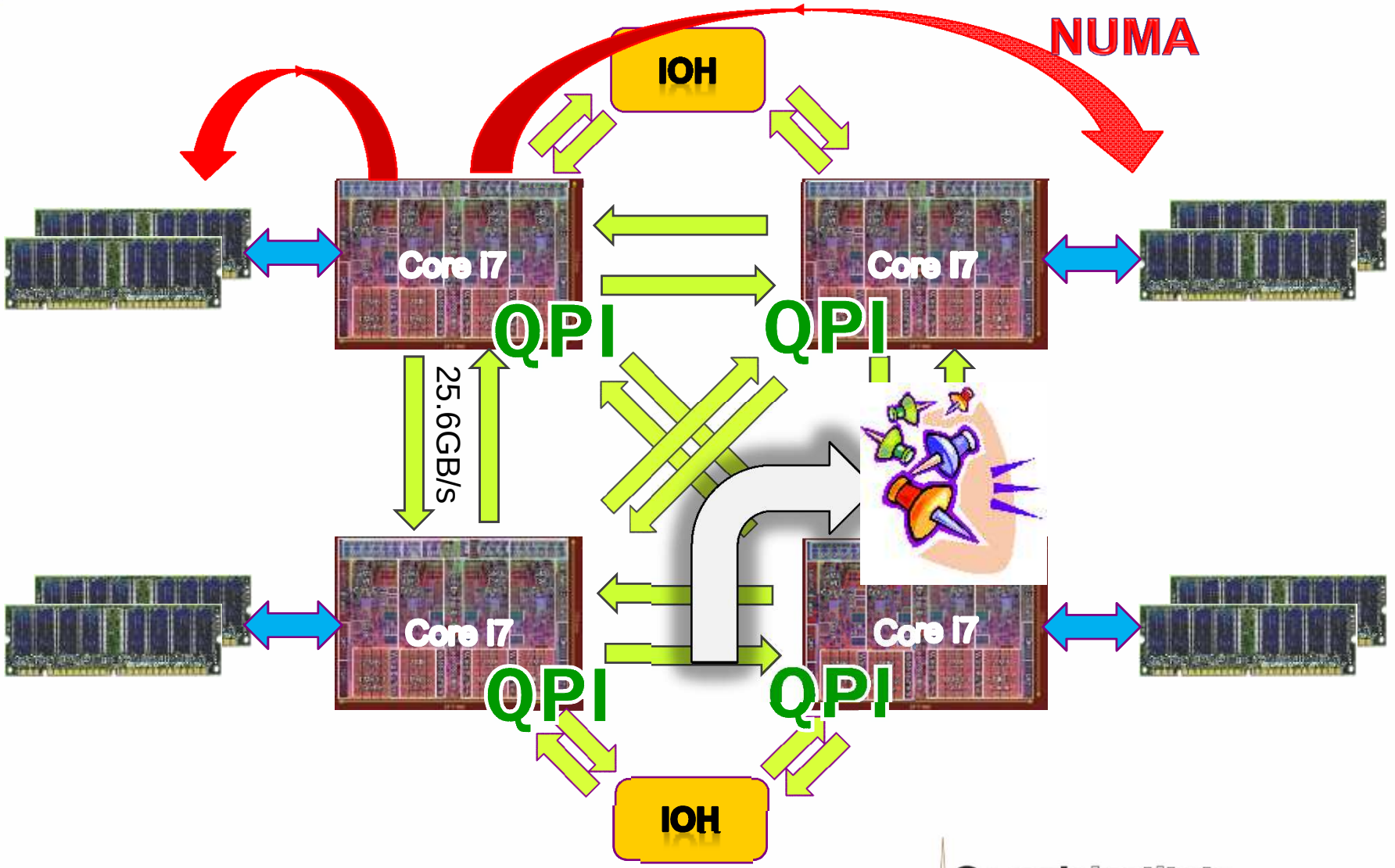
Evolution of Memory Bandwidth



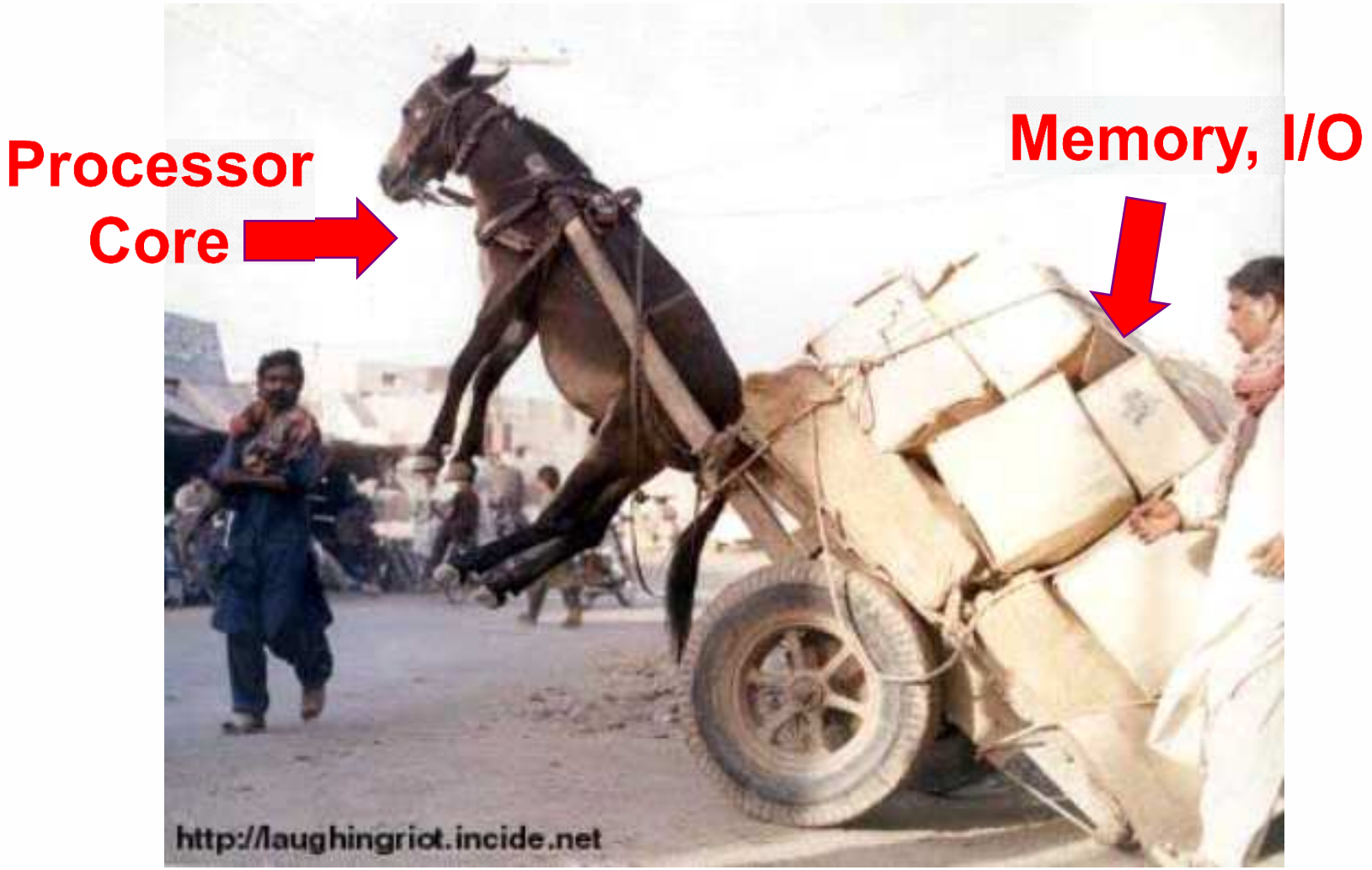
Evolution of Memory Bandwidth



Evolution of Memory Bandwidth

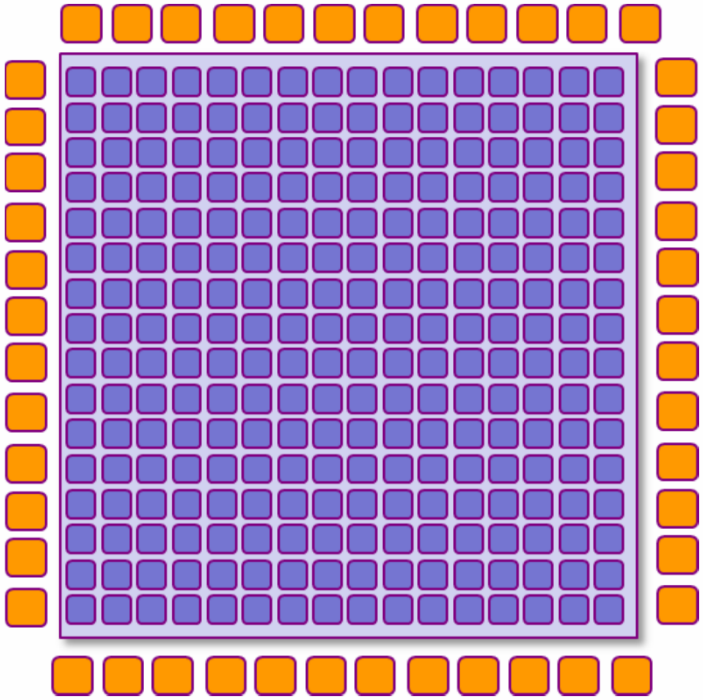


An Unbalanced System



Source: Bob Colwell keynote ISCA'29 2002

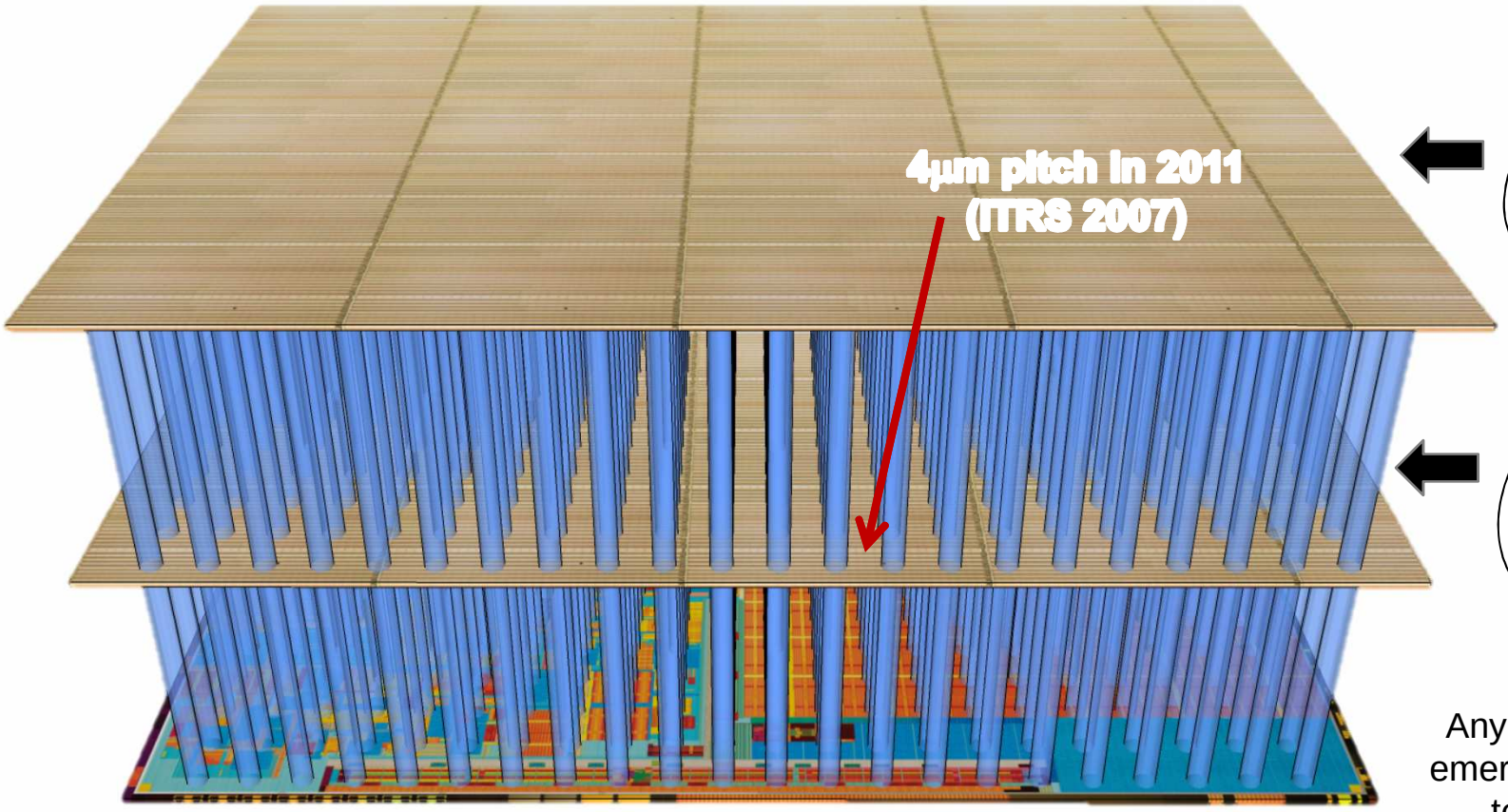
Bandwidth Wall on Conventional Processors

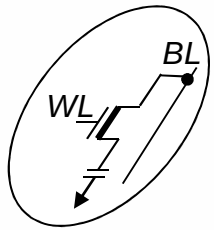


- DDR3 ~ 40mW per pin
- 1024 data pins ~ **40W**
- 4096 data pins ~ **160W**

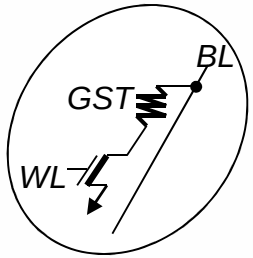
- ITRS predicts slow growth in pin count
  - 2/3 for **Power and ground**, 1/3 for **Signal I/O**
  - Limited by physical metal properties and cost

3D Memory-Stacked Processor





Or

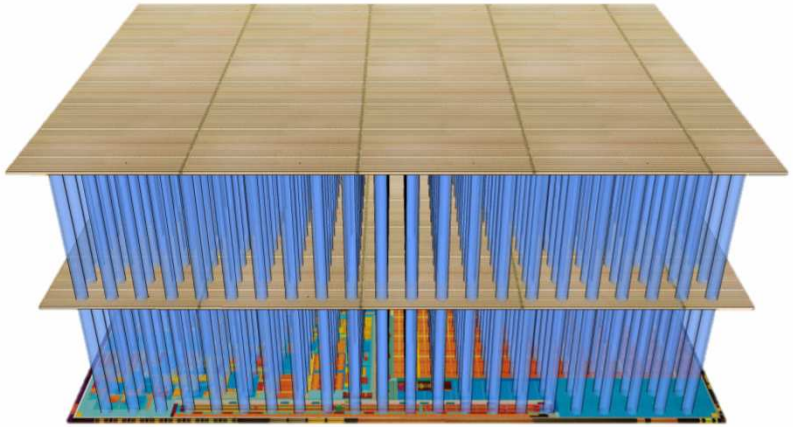


Or

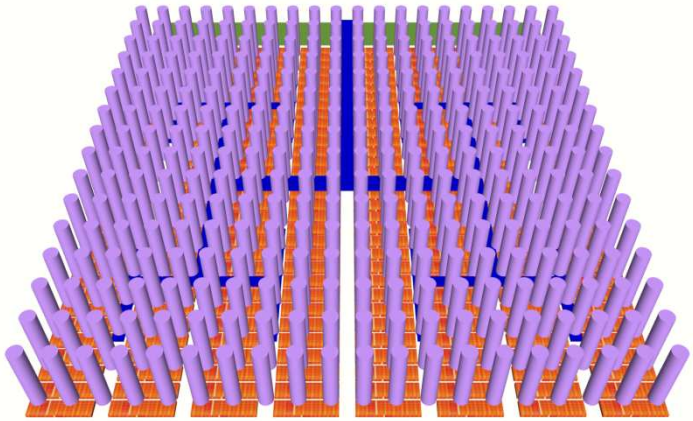
Any high-density emerging memory technology

Via Bandwidth Potential of 3D-IC

- High f2f via/TSV frequency
- High f2f via/TSV bandwidth

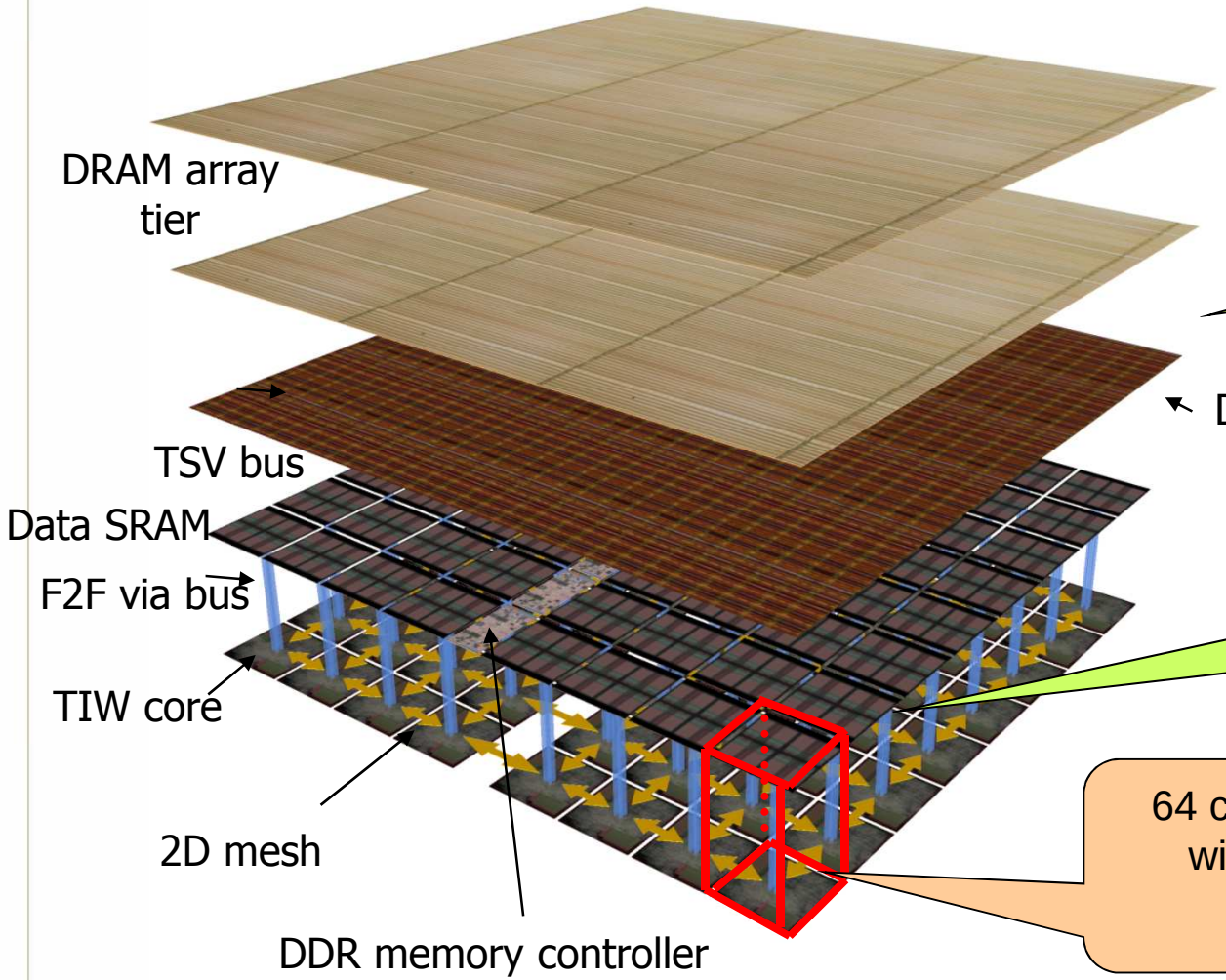


- Dense f2f via/TSV provides many independent channels
- Short f2f via/TSV improve
  - Latency
  - Power
  - For both signal and clock



- 1 ~ 10s TB/sec or even higher

3D-MAPS Prototype @Georgia Tech



Optimized 3D DRAM design by moving peripheral logic to one separate die tier. (Tezzaron)

8 SRAM tiles share one memory controller.

64 cores, each communicates with its private scratchpad memory tile thru TSV

PIs: H.-H. S. Lee, S. Lim, and G. Loh

Bandwidth Potential of 3D-MAPS

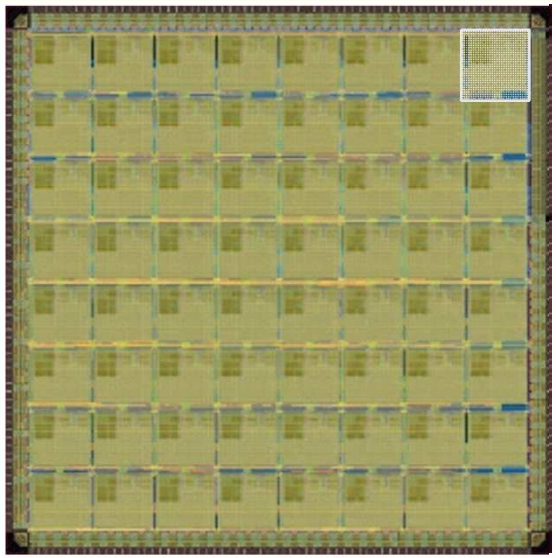
3D-MAPS Specification

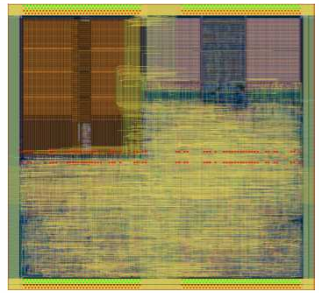
Number of cores = 64 (5-stage, 2-way VLIW, in-order)
Clock frequency = 266MHz
Supply voltage = 1.5V
Power consumption = 4 to 7W (64 cores + 64 mem tiles)
Core-to-core communication: 2D-mesh (message passing)

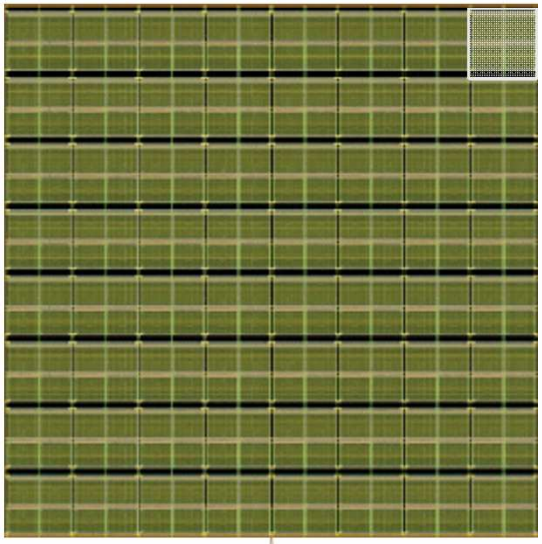
Memory model: 4KB SRAM scratchpad per core
Memory access: 1 to 4 Byte/cycle
Core to memory communication: F2F vias

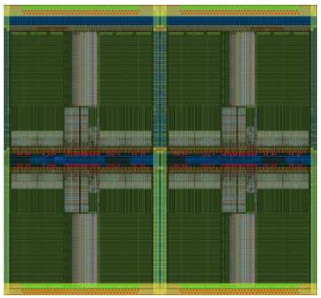
Data Bandwidth

Benchmark	DBW	DBW(a)
String search	1.60Nf	27.2 GB/s
Matrix multiply	2.00Nf	34.0 GB/s
AES standard	2.92Nf	49.7 GB/s
Histogram	4.00Nf	68.1 GB/s
Sobel detector	2.00Nf	34.0 GB/s
K-means	2.66Nf	45.3 GB/s
Median filter	2.18Nf	37.1 GB/s
Motion est.	0.67Nf	11.4 GB/s









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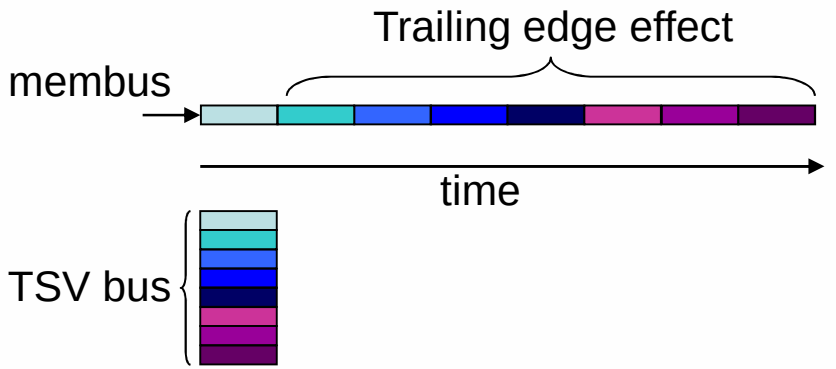
Revisiting Prior Architectural "False Truth"

- Common wisdom

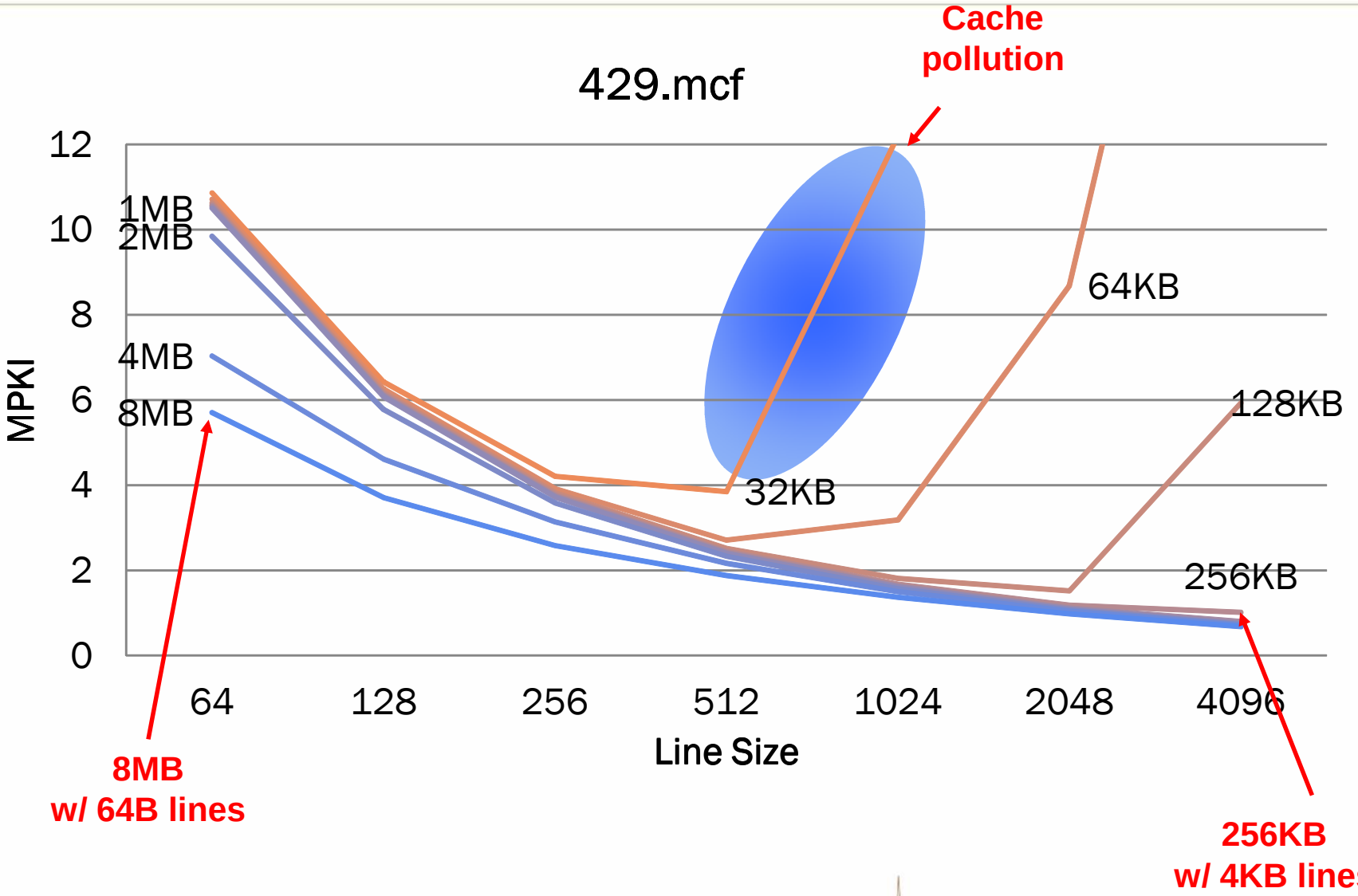
  Bandwidth problems can be cured with money, latency problems are harder because the speed of light is fixed —you can't bribe God.

- We challenge this to ameliorate "latency" using bandwidth

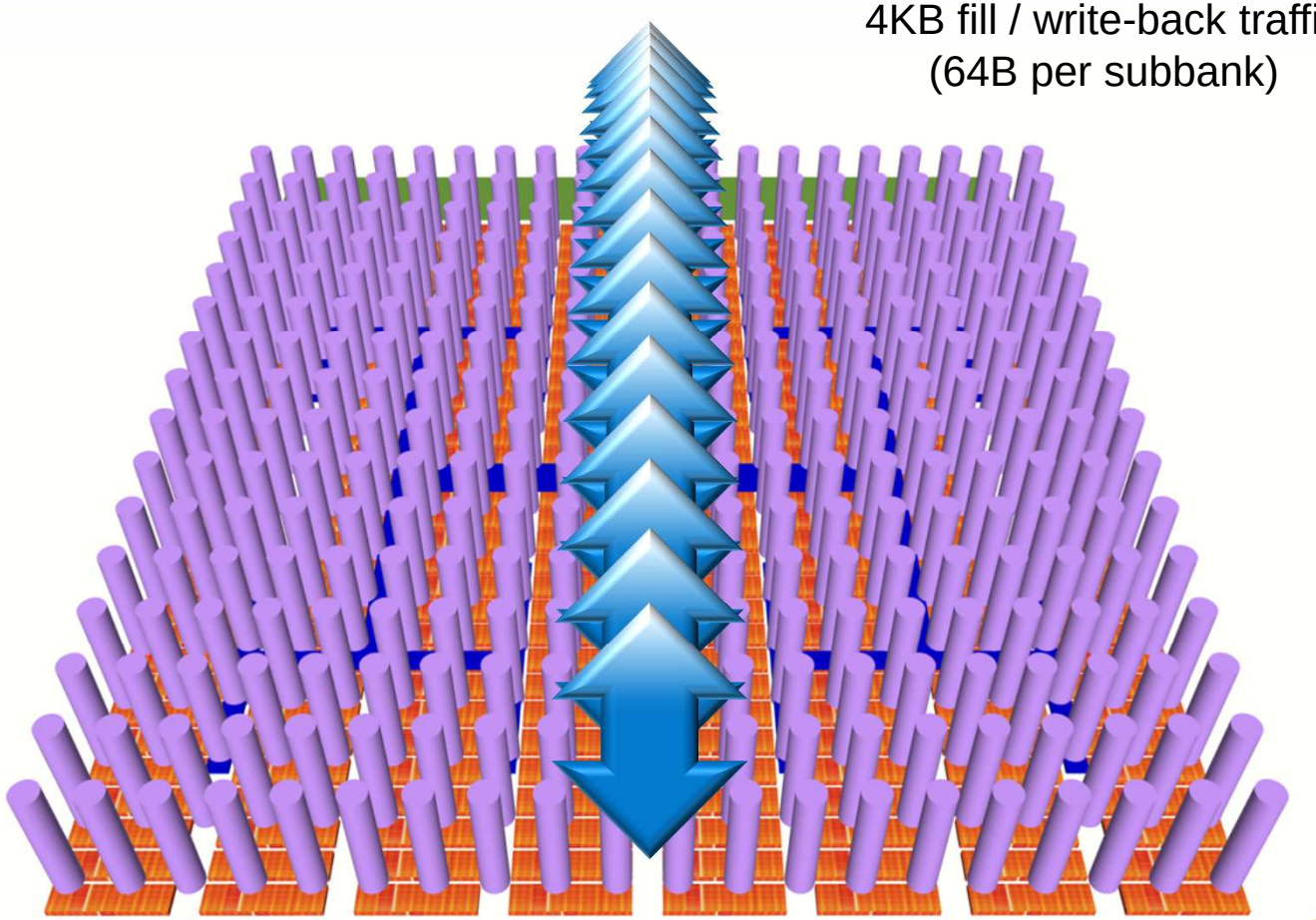
- TSV or F2F vias
  - Are fast (< 1FO4)
  - Are high density
  - Eliminate trailing-edge



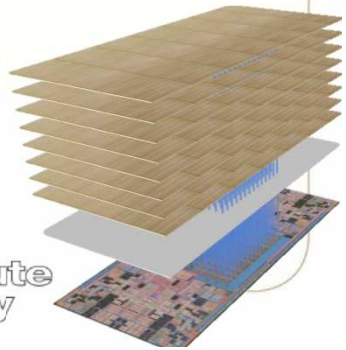
Revisiting Cache Line Size



SMART-3D: L2 and 3D DRAM



- Greater than 2x speedup for single- and multi-core.
- Avg 48% energy saving



In HPCA-16, 2010

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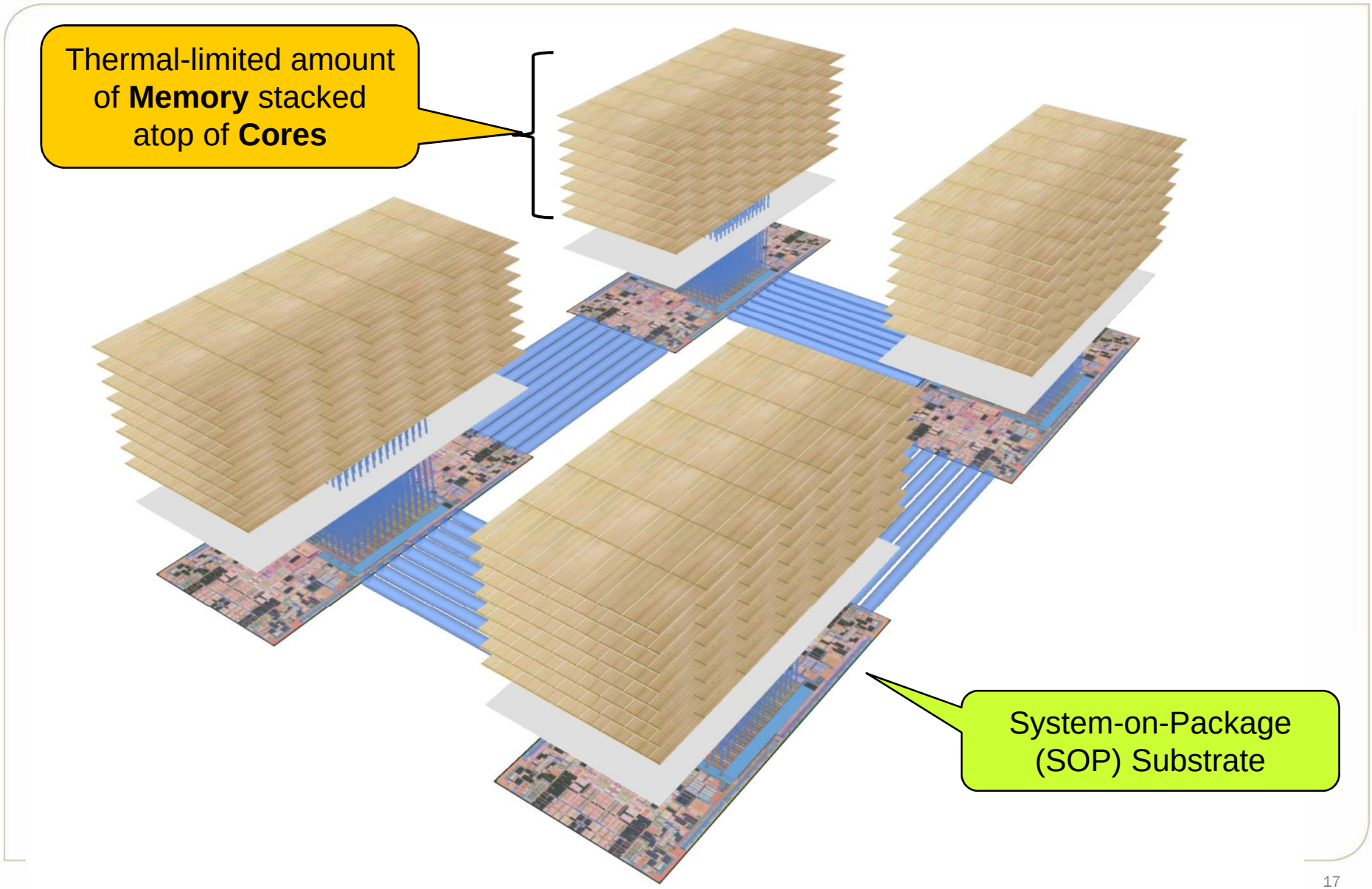
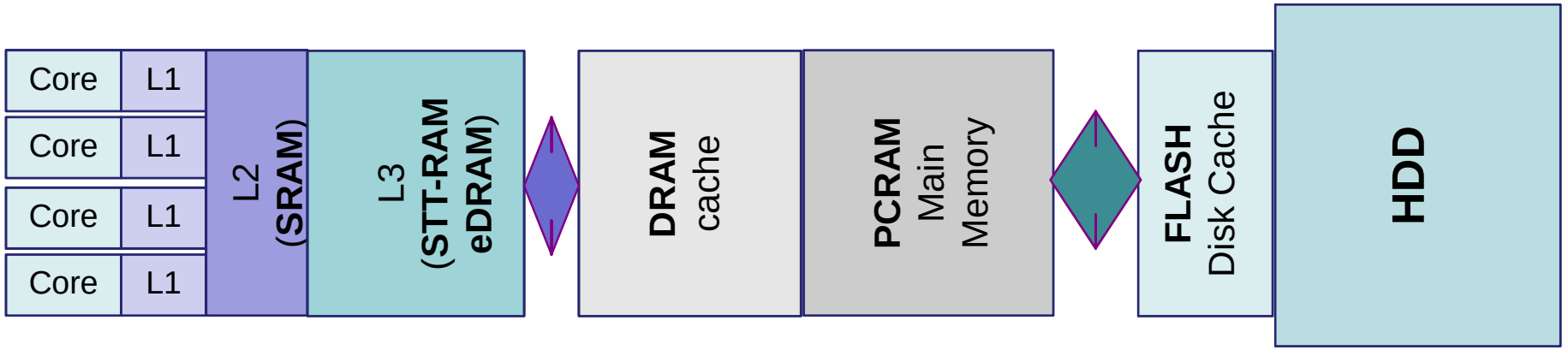
Prospect of Future 3D NUMA Many-Core



So Many Memories, So Many Hierarchies

Memory Type	DRAM	6T SRAM	NOR FLASH	PCM	MRAM	STT-RAM	FeRAM	Memristor
Volatility	Volatile	Volatile	NVM	NVM	NVM	NVM	NVM	NVM
Cell Size (F^2)	6 - 12	50 -80	7 - 11	5 - 8	16-40	6-20	Large	scalable
Read	Destructive	Partial Destructive	Non-Destructive	Non-Destructive	Non-Destructive	Non-Destructive	Destructive	Non-Destructive
Erase Granularity	Direct	Direct	Block	Direct	Direct	Direct	Direct	Direct
Write/Erase/Read Time	50ns/50ns/50ns	8ns/8ns/8ns	1µs/1-100ms/60ns	10ns/50ns/20ns	30ns/30ns/30ns	20ns/20ns/20ns	80ns/80ns/80ns	??
Programming Energy	Medium	Medium	High	Medium	Medium	Low	Medium	Low?
Write/Read Endurance	~∞/~∞	~∞/~∞	10^6/~∞	10^8~10^{12}/~∞	$10^{12}/10^{12}$	$10^{15}/10^{15}$ (?)	$10^{12}/10^{12}$	10^7/?
Multi-Level Cell	No	No	Yes	Yes	stacking	stacking	No	stacking
Cost per bit	Low	High	Medium	Low	??	??	High	??
Supply Voltage	3V	<1V	6-8V	1.5-3V	3V	<1.5V	2-3V	<1.5V?



Example of Memory Hierarchy with Many Memories

- Co-optimize: density, speed, reliability, and read/write power
- Some memories can co-locate at the same level
- Probably no one-size-fits-all

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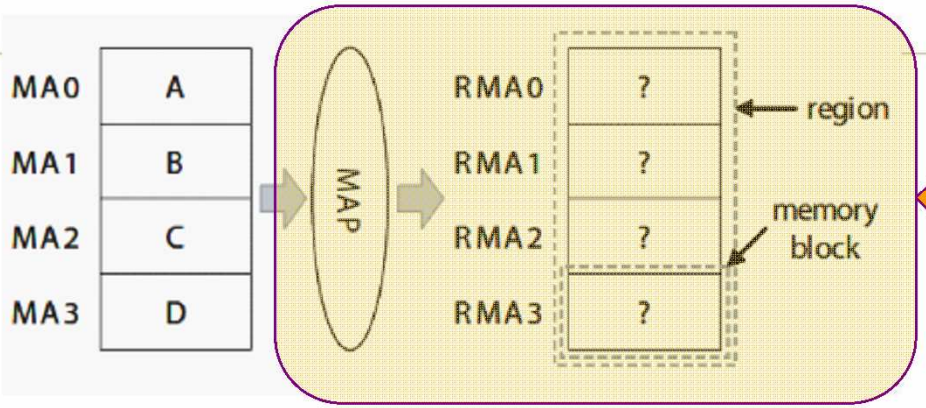
Reliability and Resilience Issues

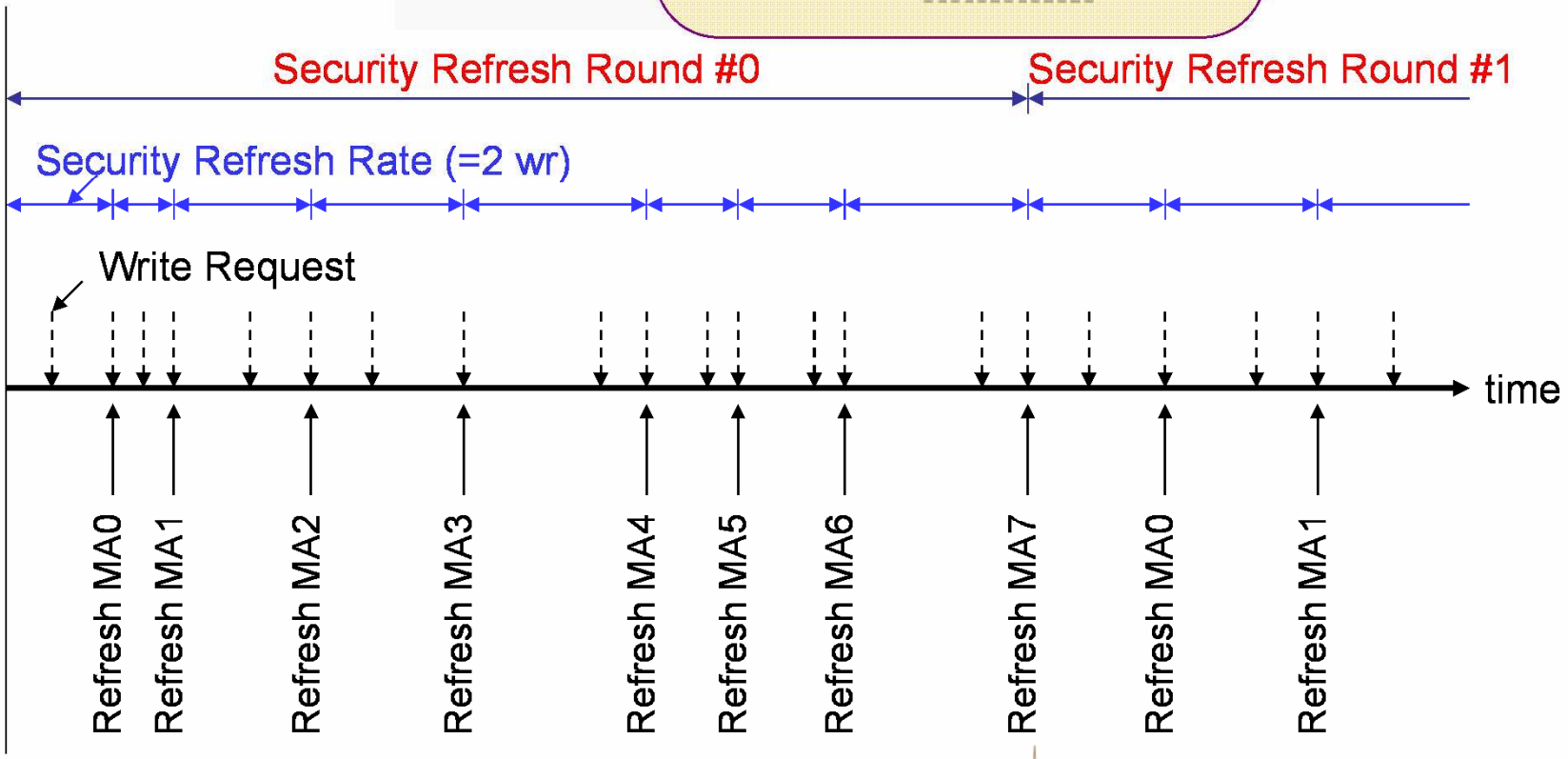
- Write endurance
  - Eliminating redundant writes
  - Wear-leveling
    - Behavior of average application (a slew of prior work)
    - Worst case or malicious behavior [Security Refresh, ISCA-37,2010]
- In the face of faults
  - Fault-aware
  - Resilient operations
- Disturbance
  - Proximity disturbance
  - Read disturbance

Security Refresh for PCM

MA: Phys mem addr

RMA: Refreshed PCM addr

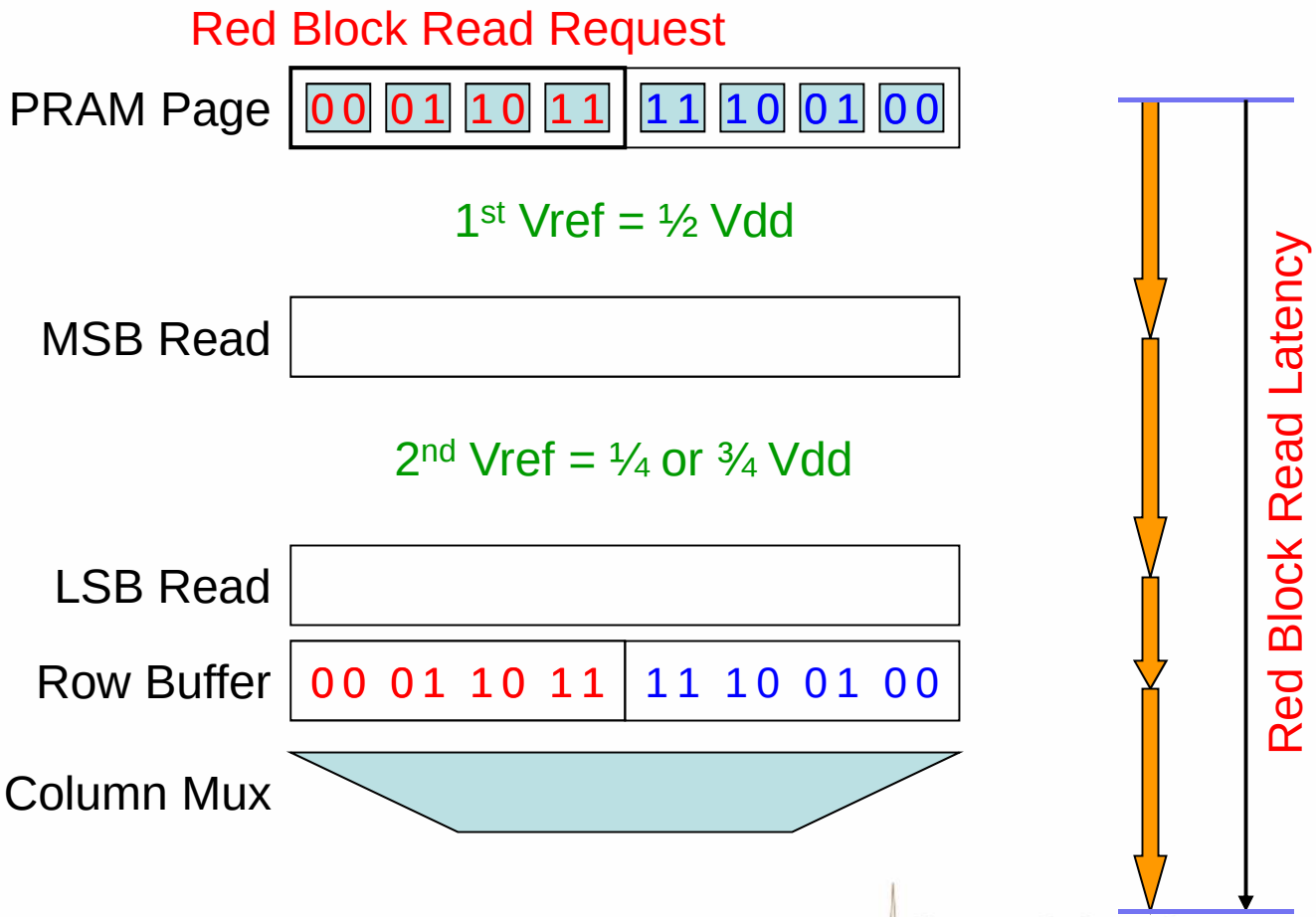




Assume 8 blocks in the region

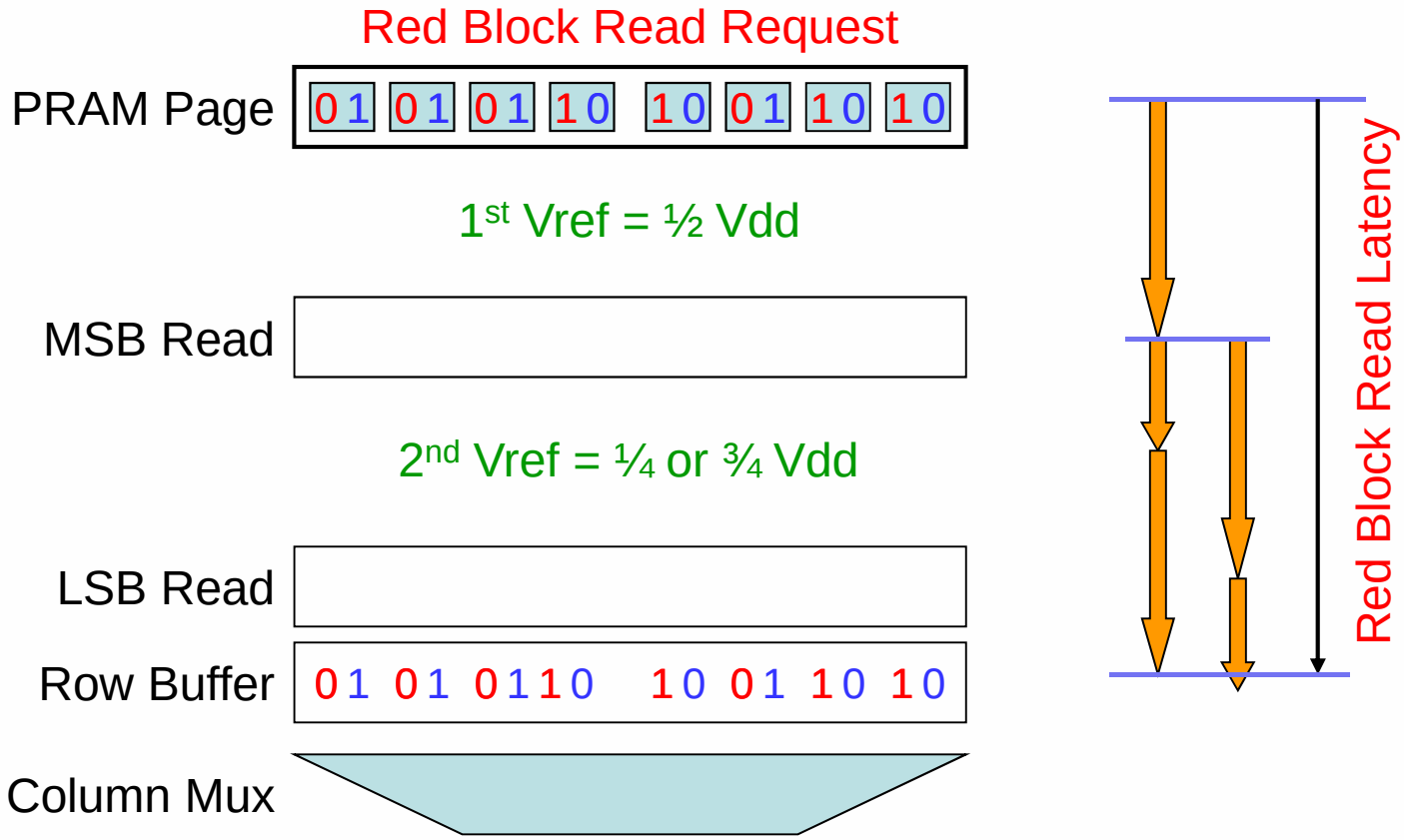
MLC Density vs. Read Performance

- Serial sensing (storing 2-bit per MLC)
- Allocating data in sequential manner



MLC Density vs. Read Performance

- Stride the bit pattern of data across MLC cells



- How does the system map the MFU lines to “Red” MSB location?



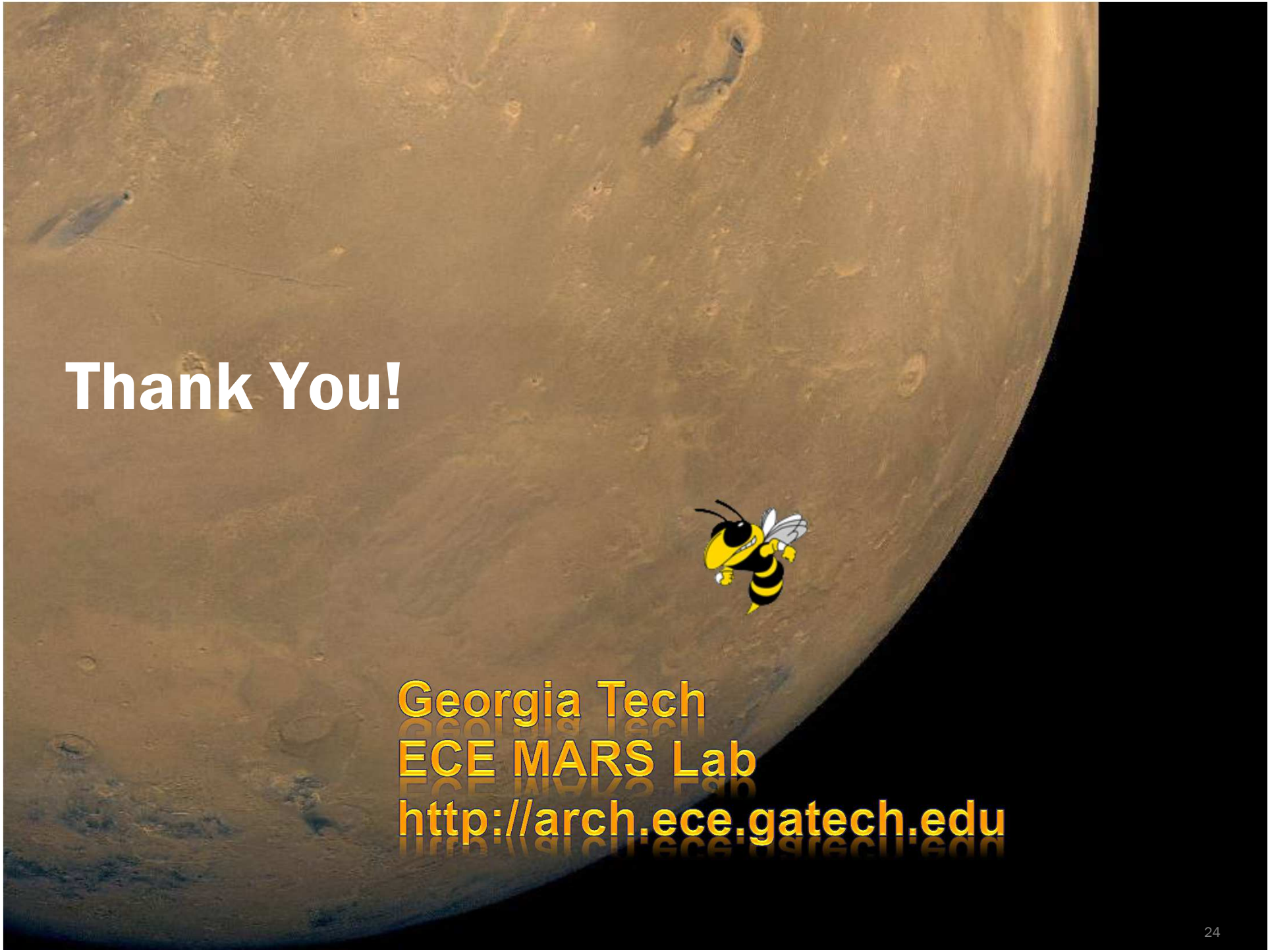
Summary

Bandwidth wall

- 3D can provide a short-term balanced system
- Should we move instructions rather than data?

Several emerging memory technologies

+ New opportunities, yet new challenges, too
+ Process-scalable, non-volatile, High-density
+ Better memory hierarchy
– Reliability
– Cost? Can we produce volume?


Thank You!
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