2007 Summary Statement

Hsien-Hsin Sean Lee, Ph.D.
Assistant Professor
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA 30332
leehs@gatech.edu

1 Introduction

Hsien-Hsin Sean Lee joined the School of Electrical and Computer Engineering of Georgia Tech as an assistant professor in fall, 2002. He received his Ph.D. degree in Electrical Engineering and Computer Science from the University of Michigan at Ann Arbor. Before joining Georgia Tech, he spent more than 5 years in the microprocessor and DSP industry (Intel Corporation and Agere's StarCore DSP Center) designing state-of-the-art microprocessor architectures and compiler technologies and managing engineering teams, in product development groups as well as in research labs.

2 General Summary

2.1 Research

Dr. Lee's research program focuses on several emerging areas in computer architecture including secure processor architecture, low-power microarchitecture, integration issues for system-on-chips, and 3D-integrated processor design issues.

For his research thrusts in secure computing, Dr. Lee and his PhD students investigated and addressed a wide spectrum of challenges from the perspective of processor architects. First, they examined the integration of security support to achieve a tamper-resistant and tamper-evident processor without compromising execution performance. They proposed prediction and precomputation techniques based on *counter mode* encryption (ISCA-32, JPDC-06, CF-07). In addition, they also studied the enabling techniques for supporting security in symmetric multiprocessors (PACT-13). To provide software confidentiality and integrity for shared libraries, Dr. Lee and his team proposed a *memory-centric security architecture* or MESA (HiPEAC-05) which protects instruction and data usage on a per-memory segment basis. They also analyzed the digital right management issues (DRM-04, GH-06) and their implications in designing processor architecture, in particular, for the application of the growing virtual properties trading over the network. To address the information leakage issues through the vulnerability that exhibits in common program semantics, they proposed *InfoShield* to enforce security policies when using and propagating sensitive information in user level codes with low-cost microarchitectural support to check violation at runtime (HPCA-13). They also examined new leakage issues due to side channel attacks at the microarchitectural level (WASSA-04, CAN-05, MICRO-39), and proposed several microarchitectural techniques to obfuscate the plaintext addresses on the bus (CASES-04, PACT-15). Their CASES work was awarded the Best Paper by the conference. More recently, Dr. Lee and his team proposed *Introspective Computing* that utilizes the emerging multicore processors to provide constant monitoring, instant checkpointing, and fast self-recovery. The goal is to provide high availability, reliability and self-healing capability with a new programming model on a multicore processor (ICAC-05, ISCA-33).

For their research thrusts in low-power architectures, Dr. Lee and his students developed architectural techniques for reducing power consumption in memory hierarchies. First, they proposed a semantic-aware multi-lateral partitioning scheme to address data TLB power (ISLPED-03). The technique exploits the advantage of small stack footprint that requires just one or two address translations throughout a program's lifetime. They further improved the d-TLB energy savings with their address compaction scheme (ISLPED-05) and an entropy-based TLB design (CASES-06). Dr. Lee also investigated the ideal supply and threshold voltage assignment for a given circuit delay requirement using Lagrange multiplier and a gradient search algorithm (ICCAD-03). Later, collaborating with ARM, they proposed counting Bloom filters inside cache hierarchy to predict L2 misses and address power consumption of synonym lookups in L1 (ARCS-06, CASES-06).

In their work on multiprocessor system-on-chips, Dr. Lee and his PhD student sought for techniques to integrate heterogeneous processors that support incompatible cache coherence protocols. They first proposed

a series of methodology and optimization techniques to integrate several invalidation-based protocols for a shared-bus architecture in a low-cost, seamless manner (DATE-04, IEEE MICRO 04). They then continued to address similar issues by proposing bypassing and book-keeping schemes inside the memory controller for non-shared-bus SoC systems to achieve the same goal (DAC-42).

For their research activities in high-performance 3D microarchitecture, Drs. Lee, Lim, and Loh's team first investigated the performance impact due to wire delays, power, and thermal profile and proposed new floorplanning methods to address them (DAC-41, DATE-06, IEEE TCAD 06, IEEE TCAD 07). Then they worked on the reliability issue due to high-frequency inductive noise and proposed a streamlined design methodology to advocate their *design for the average case* with a dynamic response system to handle the worst case. As such, a large quantity of decoupling capacitance can be substantially reduced when aggressive clocking gating is applied. In the first step of their design flow, profile feedback was collected to quantify the switching behavior which is used for a noise-aware floorplanner for facilitating the average inductive noise (ASPDAC-07). A power-pin aware dynamic control was proposed to handle the worse case current swing (MICRO-39). More recently, Dr. Lee and his team are investigating per-bond design-for-testability issues for 3D-integrated processor with 3D modules. The idea is based on scan islands used in Alpha processor (ITC-07).

Dr. Lee was granted several research awards from different funding agencies over the last 5 years. In 2002, he shared 2 ITR awards from the NSF. The first award ($814,000) with McKee from Cornell investigates system-wide monitoring for performance and security. The second award ($1,033,775, listed as senior staff) shared with 5 other faculty from CoC studied low-power architecture for distributed mobile devices. Dr. Lee received a Department of Energy Early CAREER PI Award ($299,775) to study a highly secure and autonomic computing system. He also received an NSF CAREER Award ($400,000) to investigate an *Introspective Computing Architecture* using emerging Multicore processors. With Dr. Lim (ECE) and Dr. Loh (CoC), they were awarded by MARCO/FCRP ($660,000) to study high performance 3D microarchitecture based on die stacking technology. Dr. Lee also received Intel's multicore curriculum development award ($78,168) and Intel's multicore imaging application development award ($50,000) with 2 other faculty.

2.2 Teaching

Dr. Lee has taught ECE2030 Introduction to Computer Engineering, ECE3055 Computer Architecture and Operating Systems, ECE4100/ECE6100 Advanced Computer Architecture, and ECE7102 RISC Architecture. These are the core courses of computer engineering from Introduction to Computer Engineering, to entry-level processor architecture and operating systems up to the most advanced microarchitecture course. He keeps renovating the course materials to follow the design of modern industry-standard computer architecture and developed several new, challenging Verilog-based lab projects. The coverage emphasizes dynamic out-of-order processors, static scheduling processors, to the most recent contemporary multithreaded, multicore processors. Many students who took Dr. Lee's senior/graduate level architecture courses had successfully landed positions at processor powerhouses such as Intel and AMD. To fulfill the growing demand for multimedia, 3D graphics, and gaming industries, Dr. Lee is currently working with Dr. Aaron Lanterman and Dr. David Bader (CoC) for developing a new course emphasizing general-purpose graphics processor and game design slated for Fall 2007.

2.3 Service

Dr. Lee has supervised 10 Ph.D. students since 2002. He also served as a Ph.D. proposal and defense committee member for more than 20 students in ECE and the College of Computing. Three Ph.D.s were awarded under Dr. Lee's supervision: Dr. Joshua Fryman is currently a senior researcher with Intel Microprocessor Technology Labs working on next generation many-core architectures. Dr. Weidong Shi joined Motorola Research Labs working on digital rights management issues for their future mobile phones. Dr. Taeweon Suh is with Intel's Digital Enterprise Group at Oregon working on architectural design space exploration using FPGA. Dr. Lee was appointed as one of the four members serving the Farmer Chair Search Committee and successfully recruited Prof. Wayne Wolf from Princeton University.

For service outside Georgia Tech, Dr. Lee served as a program committee member for more than 25 international conferences and workshops in the areas of processor architecture, embedded, and system-on-chip systems including ISCA-33, HPCA-13, ICCD (2005-2007), CASES (2004-2007). He also served as the Workshop and Tutorial Chair for MICRO-39, and co-organized a workshop WISA-06 in conjunction with HPCA-12. Dr. Lee

constantly served as a reviewer for numerous refereed conferences and journal publications including *IEEE Transactions* and *ACM Transactions*. He is the the Associate Editor of the *International Journal of Embedded Systems* from 2004 to 2007.

3 Five Major Intellectual Products

- High Performance Secure Architecture. Dr. Lee and his students investigated a tamper-resistant and tamper-evident processor to provide seamless security support without compromising performance. They proposed a new integrity and data privacy protection mechanism called M-TREE. (C. Lu, T. Zhang, W. Shi, and H.-H. S. Lee. M-TREE: A High Efficiency Security Architecture for Protecting Integrity and Privacy of Software." In *Journal of Parallel and Distributed Computing (JPDC) for a special issue on Security in Grid and Distributed Systems*, Vol. 66, issue 9, pp.1116-1128, 2006.) Subsequently, they applied prediction mechanisms to enable precomputation of decryption pad for counter-mode security architecture. (W. Shi, H.-H. S. Lee, M. Ghosh, C. Lu, and A. Boldyreva. High Efficiency Counter Mode Security Architecture via Prediction and Precomputation. In *Proceedings of the 32nd International Symposium on Computer Architecture (ISCA-32)*, pp.14-24, 2005.)
- Dependable and Revivable Multicore Architecture. Dr. Lee and his students designed a remote attack-immune and self-healing system called *Indra* using the emerging multicore processors. The focus of this work examines the security monitoring, fast checkpoint and recovery mechanisms. (W. Shi, H.-H. S. Lee, L. Falk, and M. Ghosh. An Integrated Framework for Dependable and Revivable Architecture Using Multicore Processors. In *Proceedings of the 33rd International Symposium on Computer Architecture (ISCA-33)*, pp. 102-113, 2006.)
- Integration of Heterogeneous Multiprocessor SoC. Dr. Lee and his student investigated the cache coherence integration issues for heterogeneous multiprocessor system-on-chips for both shared-bus and non-shared-bus architectures with incompatible coherence protocols. (T. Suh, H.-H. S. Lee, and D. M. Blough. Integrating Cache Coherence Protocols for Heterogeneous Multiprocessor Systems. Part 1. In *IEEE MICRO special issue on Embedded Systems: Architecture, Design and Tools*, pp.33-41, July/August 2004. T. Suh, D. Kim, and H.-H. S. Lee. Cache Coherence Support for Non-Shared Bus Architecture on Heterogeneous MP SoCs. In *Proceedings of the 42nd Design Automation Conference (DAC-42)*, pp.553-558, 2005.)
- Inductive Noise Aware Processor Design. Dr. Lee and his student studied the high-frequency inductive noise in power-efficient processors with Dr. Lim's research group. They proposed an average-case design methodology including a noise-aware floorplanner and a dynamic noise control microarchitecture. The floorplanner is based on profiled dynamic switching behavior of microarchitecture blocks. (F. Mohamood, M. Healy, S. K. Lim, and H.-H. S. Lee. Noise-Direct: A Technique for Power Supply Noise Aware Floorplanning Using Microarchitecture Profiling. In *Proceedings of the 12th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.786-791, Yokohama, Japan, 2007.) Next, they proposed a dynamic inductive noise evaluation hardware to adaptively control the level of clock-gating, making the circuits operation more reliable. (F. Mohamood, M. Healy, S. K. Lim, and H.-H. S. Lee. A Floorplan-Aware Dynamic Inductive Noise Controller for Reliable Processor Design. In *Proceedings of the 39th ACM/IEEE International Symposium on Microarchitecture (MICRO-39)*, pp.3-14, Orlando, FL, December, 2006.)
- High-Performance 3D Microarchitecture Design. Dr. Lee and his students investigated design challenges for 3D-IC die stacked processors together with Dr. Lim and Dr. Loh. First, they proposed a profile-driven methodology aiming to reduce the unscalable wire delay. (M. Ekpanyapong, J. R. Minz, T. Watewai, H.-H. S. Lee, and S. K. Lim. Profile-Guided Microarchitectural Floorplanning for Deep Submicron Processor Design. In *Proceedings of the 41st Design Automation Conference (DAC-41)*, pp. 634-639, San Diego, CA, 2004.) Further, they extended the methodology to take performance, power and thermal profile into account to formulate a multi-objective microarchitectural floorplanner. (M. Healy, M. Vittes, M. Ekpanyapong, C. Ballapuram, S. K. Lim, H.-H. S. Lee, and G. H. Loh. Microarchitectural Floorplanning Under Performance and Temperature Tradeoff. In *Proceedings of the Design, Automation and Test in Europe (DATE-06)*, pp.1288-1293, Munich, Germany, 2006) and applied it to 3D-integrated circuits. (M. Healy, M. Vittes, M. Ekpanyapong, C. Ballapuram, S. K. Lim, H.-H. S. Lee, and G. H. Loh. Multi-Objective Microarchitectural Floorplanning For 2D and 3D ICs. In *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 1, pp.38-52, 2007.) Dr. Lee also developed a novel DFT technique for 3D-integrated processors. (D. L. Lewis and H.-H. S. Lee. A Scan-Island Based Design Enabling Pre-bond Testability in Die-Stacked Microprocessors. In *Proceedings of the International Test*

Conference (ITC-07), Santa Clara, CA, 2007.)