
# Design Report – Team 01

## ELETENG311: Electrical Engineering Design II

*Design of a Pocket Power Supply*

Hrichik Sircar
Kees Albers-Connolly
Kili Miyamoto
Timothy Aguana Cabrera
Department of Electrical, Computer, & Software Engineering

# Abstract

This report explores the design process, performance and the motivation behind the proof of concept of a DC-DC converter. The DC-DC converter is a flyback transformer, a switch mode power supply, that has been designed  to provide a dynamic voltage and power to the load based on the user's input to the converter. The flyback converter's design and performance were validated and assessed respectively and the details of which will be included in this report.

# Introduction

Bench-top power supplies are an important tool in the development and testing of electronic circuits. A typical supply such as the GW3323 provides low voltages and currents set by the user at its isolated outputs. This is achieved with a 50Hz transformer with multiple taps to step down the 230V AC mains supply and a series type linear regulator to regulate to the DC voltage as set by the user.

The drawbacks of these power supplies result not from their performance but their physical properties. A large transformer is required because of the low frequency of the mains supply, which adds considerable weight and volume to the device. Significant heatsinks for the output linear regulator are also needed, further increasing these properties.

There is therefore motivation to miniaturize the power supply in order to both save space and increase versatility due to its miniature size that allows it to be easily carried and used at different locations, provided there is a DC power source available as its input.

In order to miniaturise the benchtop power supply, the fundamental properties of magnetics and high frequency switching which is commonly used in SMPS designs will be used. A proposed design would be to use a high frequency isolation transformer in order to miniaturise the size of the transformer needed and consequently reduce copper losses. Power will be transferred through the magnetic field generated by the inductance of the transformer which switches at a predetermined period, of which the duty cycle directly translates to the voltage and current to the output. To add controllability like that of benchtop power supplies, a digital means of communication between the user and the analog circuitry will be designed with the use of a microcontroller and appropriate firmware to achieve this functionality. To prevent harm to the user, the input and output sections of the PCB will be isolated in order to prevent the user from being a return path to the primary. This isolation will be achieved by the magnetic coupling of the transformer, integrated circuits (ICs) and PCB design techniques. Lastly an over voltage protection circuit design will be included to shut down the device to protect components from over voltage damage.

This report will explore the design process and support the design decisions supported with the relevant fundamentals of the analog and digital circuitry involved. Additionally documentation such as oscilloscope screenshots and proteus (digital simulator of firmware) measurements will be included in order to show the validity and the effect of design improvements implemented on the device.

# The Proposed Design

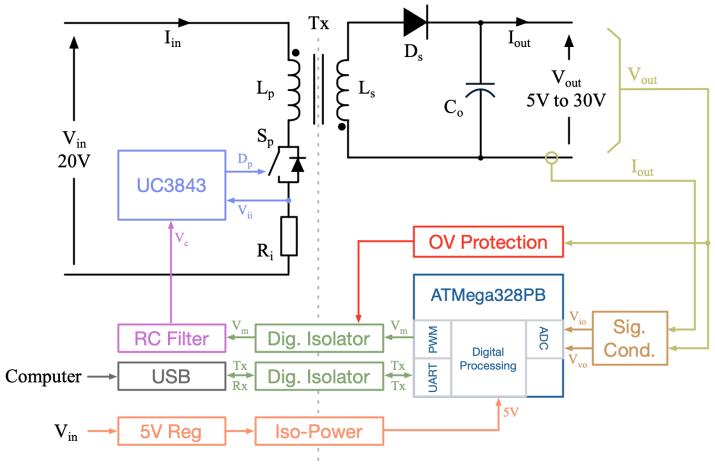



Fig. 1: A conceptual system diagram [1]

The proposed design will utilize switching in order to regulate the power/energy transferred to the output from the input. The switching is done using a MOSFET (a voltage controlled switch) to control the current going through the inductor/transformer. A key property of inductors is that they can store energy. The switch Sp is closed to pass current through the inductor which accumulates energy and stores it in a magnetic field. After a certain amount of time the switch is opened, and the energy in the inductor has no other path to travel except across to the output through the transformer. By controlling the duration (Duty cycle) of the switching, the output power and the voltage can be controlled.

The MOSFET is controlled by the UC3843, a controller that reads the voltage at the current sense resistor $R_i$ representative of the current (note: the current is linearly increasing as long as the inductor is not fully charged) through the inductor and is fed a voltage reference generated by the ATMega328P microcontroller, if the current sense voltage is lower than the voltage reference the UC3843 outputs a voltage to turn the MOSFET on, if the current sense voltage is higher then it stops outputting and after a certain period of time it resumes outputting. For the user to be able to control the output voltage without altering the circuit component values, a feedback circuitry is established with the microcontroller which takes in the output voltage and forms a closed loop control. The output voltage is compared with the user's input and the difference (error) is used to calculate an appropriate voltage reference. The microcontroller will output a voltage PWM waveform that is passed through a filter to achieve an average voltage between 1-4V that is fit to be fed to the UC3843.

In order to prevent damage to the circuitry and to the user, parts of the circuit will be isolated from each other and an OVP (over voltage protection) circuit will be implemented. In the design isolation is achieved by using a digital isolator located between the ATMega328P and UC3843. The PCB has a large gap between the input and output circuits for further isolation.. The OVP is designed so that if the output voltage exceeds 34V, the UC3843 will not output keeping the MOSFET switched off.

Table 1: Design Specifications

| Parameter | Value |
|---|---|
| Input Voltage | 20 $V_{DC}$ |
| Output Voltage Range | 5 $V_{DC}$ to 30 $V_{DC}$ |
| Load Regulation | 5% |
| Maximum Output Power | 12 W |
| Output Voltage Ripple | 100 mV or Less |
| Efficiency | 80% or Better for Over 5 W |
| Switching Frequency | 100 kHz |
| Isolation Rating | 500 V or more |
| Over Voltage Protection | 32 V |
| Converter Topology | Flyback |
| Information Displayed to User on PC | Output Voltage |
| User Setpoints | Output Voltage |
| PCB Technology | Double Layer with PTH |

# The Hardware Design

## Design Calculations

To calculate the inductance required for the primary winding it is necessary to determine the relationship between power and inductance., The energy in an inductor can be found by the equation of $E_{Lp} = \frac{1}{2}L_p I^2_{Lp-pk}$ which is equivalent to $\frac{V_{in}}{2Lp}D^2T_s^2$ as $I_{Lp-pk}$ can be determined by the equation $\frac{V_{in}}{L_p}D * T_s$ and from substitution the two equations can be shown to be equivalent. Power is Joules/sec therefore it can be calculated by simply multiplying either of the equivalent equations with the switching frequency; $E_{lp} * f_{switch}$. $L_P \leq \frac{V_{in}^2}{2f_s P_{out(max)}}D^2_{max}$ the following relationship can be extracted from rearrangement, the inductance of the primary winding is needed to be equal or less than the RHS in order to satisfy the maximum power output (12W in this case), as $E_{Lp}$ is a function of $I_{Lp-pk}$ and a lower $L_P$ means a higher achievable $I_{Lp-pk}$ therefore higher achievable output power.

To simplify the design of the device the maximum duty cycle was set to 0.5 and the flyback transformer is designed to operate in DCM (discontinuous mode) to fully utilize components. This means the integral of the voltage at the primary winding must be 0 indicating all energy accumulated is transferred over; $\int_0^{T_s} V_{Lp}dt = V_{in}DT_s - nV_{out}D'T_s = 0$. The turns ratio, $n$, is the ratio between $\frac{N_p}{N_s}$ where $N_x$ is the number of coil turns at the primary or secondary winding of the transformer. In order to simplify the design the turns ratio was selected to be 1 to guarantee DCM and therefore both $L_p$ and $L_s$ will be the same. To guarantee DCM the following equation, $n \geq \frac{V_{in}D}{V_{out}(1-D)}$ can be derived from the equivalent integral expression above and to validate the design at rated loads simulation software such as MATLAB and LTspice were used, the results of which can be found in table 2 and table 3.

As per the specifications, the output ripple voltage must be lower or equal to that of the specified output ripple. Using an equation, $C_o \geq \frac{1}{2\Delta V_{out}}\frac{(nI_{LP(pk)} - I_{out})^2}{nI_{LP(pk)}}D'T_s$ , derived by Duleepa J. Thrimathiwana (2022) in their lectures the minimum output capacitor was calculated to be 35uF. A 100uF was then selected to be used, to minimise the output ripple at the cost of response time

In order for the circuit to switch at the switching frequency, a MOSFET is implemented due to its higher switching speeds, voltage and current ratings. The FQP13N10 MOSFET was implemented in the circuit as

when the inductor is transferring energy the switch must withstand the reflected output voltage and the input voltage combined ideally with a margin of safety. In addition, its conduction and switching losses are also low. As for its implementation a high gate drive current was used in order to discharge/charge the parasitic capacitances of the mosfet, a 15 ohm resistor was used to drive the MOSFET gate at a current of 1-1.3A (dependent on UC3843 output).

In order to filter the input and output signals of the flyback converter from high frequency noise, decoupling capacitors were used to create a low impedance path. All capacitors have a parasitic factor called ESL (Effective series inductance), usually modern capacitors have ESLs ranging from 10nH to 100 nH. ESL affects the filtering response of the capacitors as past the 'knee' frequency (more commonly known as the resonant frequency), the reactance of the capacitor increases. Therefore decoupling capacitors are placed in parallel to provide additional short impedance paths for higher frequency responses past each capacitor. To decide the capacitor values for the design the aforementioned ESL range, common capacitance value and knee frequencies were used to evaluate. The equation for a given knee frequency is as follows:

$$\frac{1}{2*\pi\sqrt{C*ESL}}$$

Through Matlab the following short script was ran:

```
Best_case_ESL = 10E-09;
Worst_case_ESL = 100E-09;
Capacitance_to_be_used = 100E-9;
Best_case_Knee_frequency = 1/(2*pi*sqrt(Capacitance_to_be_used*Best_case_ESL));
Worst_case_Knee_frequency = 1/(2*pi*sqrt(Capacitance_to_be_used*Worst_case_ESL));
```

Which yielded decoupling capacitors values of 47uF, 100n and 68n (for both input and output).

With regards to the characteristics of the flyback transformer a suitable diode needs to be implemented at the output to block during the on-state of the MOSFET. A schottky diode was used due to its quick transition time and low forward voltage which helps with lowering transition and conduction loss. The schottky diode used in the circuit is the SDT5H100P5 which has a maximum reverse bias of 100V. From the table below, it can be seen that the maximum reverse bias voltage experienced by the diode is 50V, well within the specifications.

Table 2: Calculated Open-loop values.

| Parameter | Value | Unit | Value | Unit | Value | Unit | Value | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{out}$ | 5 | V | 12.5 | V | 20 | V | 30 | V |
| $P_{out}$ | 1.5 | W | 6.75 | W | 12 | W | 12 | W |
| $R_{load}$ | 16.6667 | Ω | 23.15 | Ω | 33.33 | Ω | 75 | Ω |
| Max D for DCM | 0.1768 | | 0.375 | | 0.5 | | 0.5 | |
| Operating D | 0.1677 | | 0.3558 | | 0.4743 | | 0.4743 | |
| DCM Achieved | Yes | | Yes | | Yes | | Yes | |
| Max $V_{SP}$ | 25 | V | 32.5 | V | 40 | V | 50 | V |
| Peak $I_{in}$ = $I_{LP}$ | 0.89 | A | 1.9 | A | 2.53 | A | 2.53 | A |
| RMS $I_{in}$ = $I_{LP}$ | 0.21 | A | 0.65 | A | 1.01 | A | 1.01 | A |
| Average $I_{in}$ = $I_{LP}$ | 0.07 | A | 0.34 | A | 0.6 | A | 0.6 | A |
| Operating D' | 0.6708 | | 0.5693 | | 0.4743 | | 0.3162 | |
| Max $V_{Ds}$ | 25 | V | 32.5 | V | 40 | V | 50 | V |
| Peak $I_D$ | 0.89 | A | 1.9 | A | 2.5296 | A | 2.53 | A |
| RMS $I_D$ | 0.42 | A | 0.83 | A | 1.01 | A | 0.82 | A |
| Average $I_D$ = $I_{out}$ | 0.3 | A | 0.54 | A | 0.6 | A | 0.4 | A |
| Vout Ripple | 0.034 | V | 0.0709 | V | 0.0895 | V | 0.0727 | V |

# Design Validation (Open Loop)

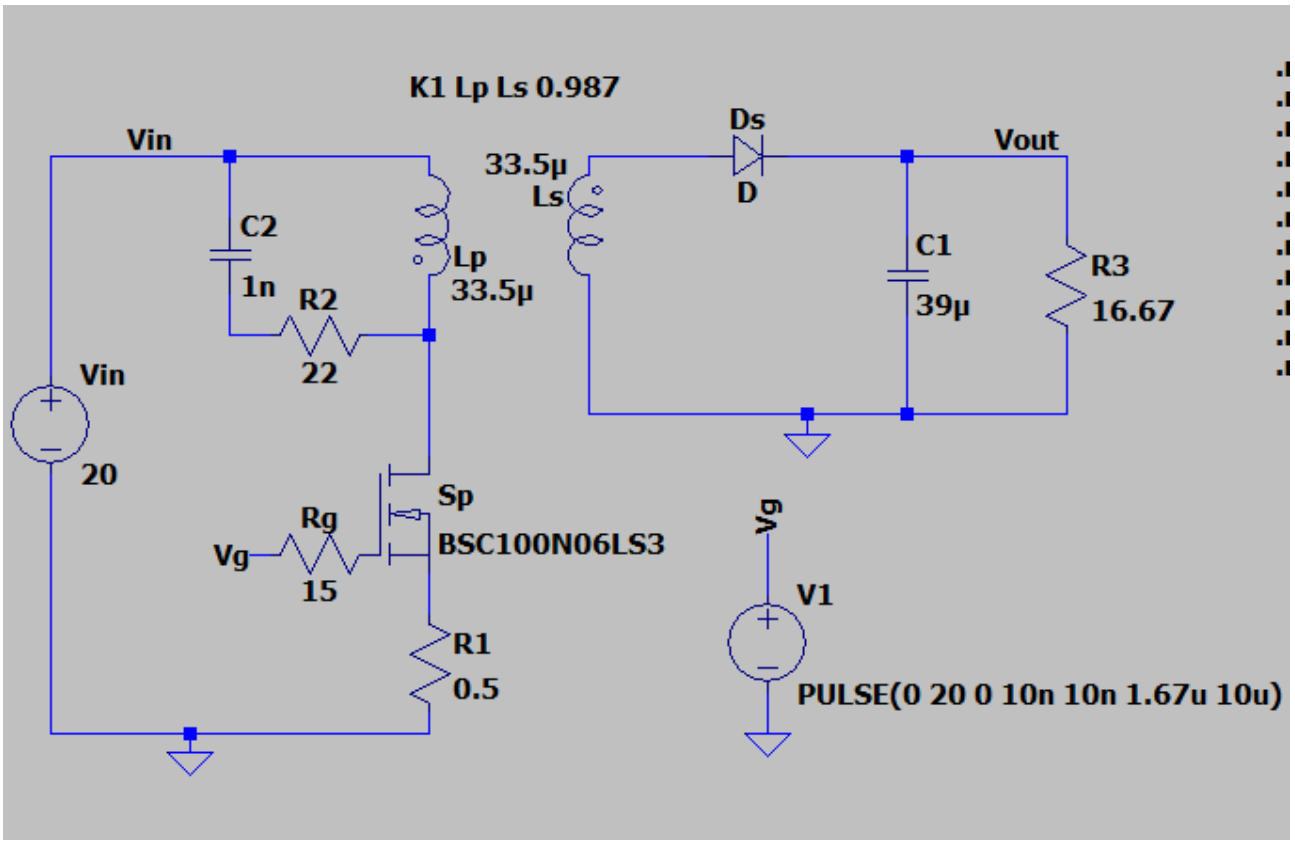



Figure 2: LTspice simulation of open-loop conditions

To validate the open-loop design and the functionality of the circuit LTspice was used to simulate the system under different loads and duty cycles corresponding to the rated power output at each rated load.

C2 and R2 represent a snubber circuit placed to minimise loss and ringing caused by leakage inductance from the non ideal transformer with K1 value of 0.987 (coupling factor) and the parasitic capacitance of the MOSFET at the switching instant (on to off).

This report finds that the LTSpice simulations closely follow that of the calculated values for theoretical open-loop values with the differences mainly from the voltages experienced by the MOSFET and the output diode being higher than that of the theoretical calculations.

Table 3:LTspice results of open-loop performance.

| Parameter | Value | Unit (eq) | Value | Unit (eq) | Value | Unit (eq) | Value | Unit (eq) |
|---|---|---|---|---|---|---|---|---|
| RLoad | 16.67 | Ohms | 23.15 | Ohms | 33.33 | Ohms | 75.00 | Ohms |
| Operating D | 0.17 | | 0.36 | | 0.47 | | 0.47 | |
| Vout | 4.81 | V | 12.50 | V | 20.00 | V | 31.01 | V |
| Pout | 1.39 | W | 6.74 | W | 10.95 | W | 12.82 | W |
| DCM Achieved | YES | | Yes | | Yes | | Yes | |
| Max VSp | 25.60 | V | 43.56 | V | 52.91 | V | 64.27 | V |
| Peak Iin = ILp | 0.94 | A | 1.98 | A | 2.48 | A | 2.67 | A |
| RMS Iin = ILp | 0.23 | A | 0.70 | A | 0.98 | A | 1.10 | A |
| Average Iin = ILp | 0.08 | A | 0.37 | A | 0.58 | A | 0.67 | A |
| Operating D' | 0.62 | | 0.57 | | 0.44 | | 0.31 | |
| Max VDs | 4.82 | V | 32.52 | V | 39.10 | V | 51.67 | V |
| Peak ILs | 1.00 | A | 2.13 | A | 2.66 | A | 2.70 | A |
| RMS ILs | 0.42 | A | 0.84 | A | 0.97 | A | 0.85 | A |
| Average ILs = Iout | 0.29 | A | 0.54 | A | 0.57 | A | 0.41 | A |
| Vo Ripple | 0.04 | V | 0.09 | V | 0.13 | V | 0.11 | V |

# Closed Loop Controller Design

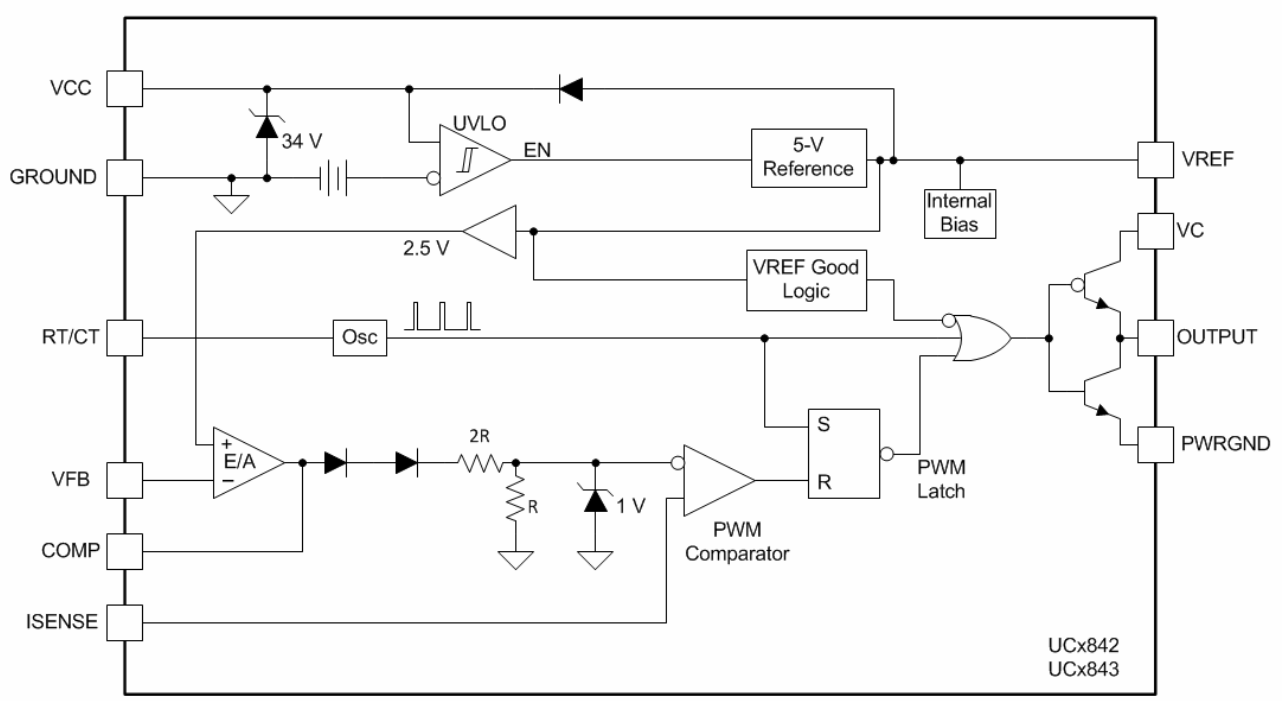



Figure 3:Internal circuit diagram of UC3843

To implement closed loop control, the UC3843 IC and the ATMega328P microcontroller will be used to generate a square wave with an appropriate duty cycle that controls the MOSFET and thus the output voltage that is feedback. The UC3843 IC is an essential component tool as it is a suitable controller that can provide a high drive current/voltage to the MOSFET gate. In the design this IC is used to control the duty cycle of the gate driver PWM by using feedback. To describe the operation of the internal circuitry, sections of it will be divided and analyzed.

Input power to the IC and internal circuitry: The UC3843 has a minimum operating voltage of 8.4V[2] needed to overcome the restriction set by the Under voltage lockout (UVLO) before the IC becomes active. Upon reaching the active state, Internal reference voltages will be generated to control the logic gates. In addition, a 34V zener diode is applied at the input in order to protect the circuitry from damage. With regards to the specifications and design of the flyback transformer, the power supply will be derived from the 20 Vdc supply.

Oscillator: To generate a 100 Khz square wave, the component values for Rt and Ct suitable for this can be extracted from the datasheet. In this case Ct should be 1nF for minimum the charge time and Rt is $18k\Omega$.

However upon testing the circuit, it was observed that when using $18k\Omega$ the generated wave falls below 100 Khz (~93Khz) therefore a lower resistance of $15k\Omega$ was used to generate a 103 Khz sawtooth waveform.

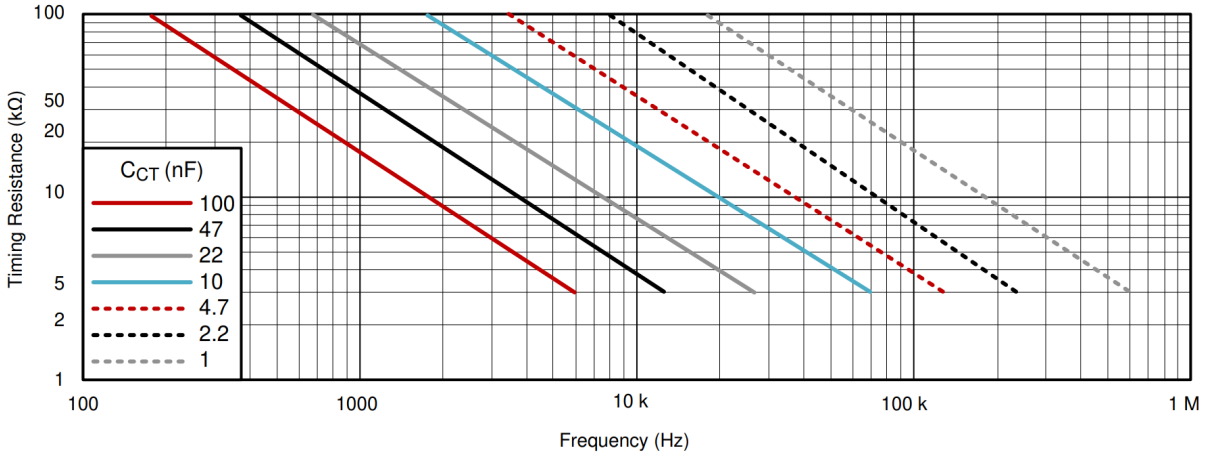



Figure 4: Sawtooth frequency as a function of Rt and Ct [2].

Current feedback: Due to the noisy current signal going through $I_{fb}$ ,a low pass filter at a cutoff frequency of 100 times that of the switching frequency is implemented so that it does not filter any part of the current signal itself, the values of $R_{if}$ and $C_{if}$ were calculated to be 100Ω and 150pF.

In addition, the shunt resistor used in the circuit must meet the comparator's input value constraints of a maximum of 1V. The following equation can be used to determine the value of the shunt resistor:

$$R_s = \frac{1}{I_{LP(pk)}}$$

From the calculations, the maximum $I_{Lp(pk)}$ was calculated to be 2.53A from which a Resistor value of 0.4Ω was derived. In the implementation this was changed to 0.5Ω due to a lack of components.

Voltage feedback: The ATmega328P has a maximum input and output voltage of 5V, therefore a voltage divider was designed such that maximum output voltage is scaled down to around 5V. In the implementation, this was calculated to be $R_a$ = 33kΩ and $R_b$ = 5.6kΩ.

The ADC (Analogue-digital converter) of the ATMega328P, is set to a sampling frequency of 13.33Khz (clock frequency of 250 Khz) as running the ADC on a much higher clock cycle results in lower resolution and therefore lower accuracy. Due to this sampling frequency, a low pass filter must be applied to the output of the voltage divider to ensure that the sampled signal is at a frequency of at least 2 times lower than the sampling frequency to prevent aliasing. The value of the cutoff frequency can be calculated by the following equation:

$$f_{cutoff} = \frac{1}{2*\pi*R*C}$$

Equation 1: cutoff frequency

From the equation a cutoff frequency of around 2 Khz was chosen and with the chosen $R_a$ and $R_b$ values, which is in parallel with the usage of thevenin equivalent and a capacitor value of 18nF was determined.
The control loop and the UC3843 controller: The ATMega328P will process the output voltage and compare it with the user's desired output voltage, if lower/higher then increase/decrease the duty cycle of the output PWM from the Microcontroller. This PWM is then transmitted to the primary/input side of the circuit via a digital isolator which outputs high above 3V and low below.

As VFb in this case is a PWM, a signal conditioning circuit is needed to convert this value to a DC value and this is done by a low pass filter with a cutoff frequency of around 10 times less than that of the PWM frequency. Thus resulting in $R_{10}$ and $C_{11}$ values of 150Ω and 100nF.

The DC value of VFb is then passed through an amplification stage set by the values of $Rop_1$and $Rop_2$
The output of which can be determined by the following equation :

$$V_{pi\ out} = 2.5 + (2.5 - V_{pi\ in})\frac{R_{op2}}{R_{op1}}$$

Equation 2: Output of the UC3843's internal inverting amplifier

In this case, $Rop_1$and $Rop_2$ were set to be 4.7kΩ and 10kΩ. In this configuration, when the DC value of Vpi_in changes from 4 to 1V the output voltage is expected to change from roughly 0 to 5V. After the amplification stage the output voltage loses 1.4V through the two diodes and is divided by 3 and lastly clamped at 1V with an internal zener for the comparator[3]. This clamped voltage ranging from 0 to 1V is called the $I_{lp(pk-REF)}$. The closed loop controllers's functionality, and therefore the duty cycle of the gate driver PWM, is dependent on the relationship between the voltage at $I_{sense}$ and $I_{lp(pk-REF)}$.
The behaviour is as follow: If the voltage at $I_{sense}$ is higher than that of $I_{lp(pk-REF)}$, the reset bit is set to high, causing the output voltage to drop and hence creating a PWM with a duty cycle. The output voltage is setback in accordance with the oscillator frequency.

With regards to the OVP (over voltage protection) a circuit was made so that, upon reaching 32V the UC3843 would shut down due to Vpi_in being set to 5V and thus $I_{lp(pk-REF)}$ to 0V .

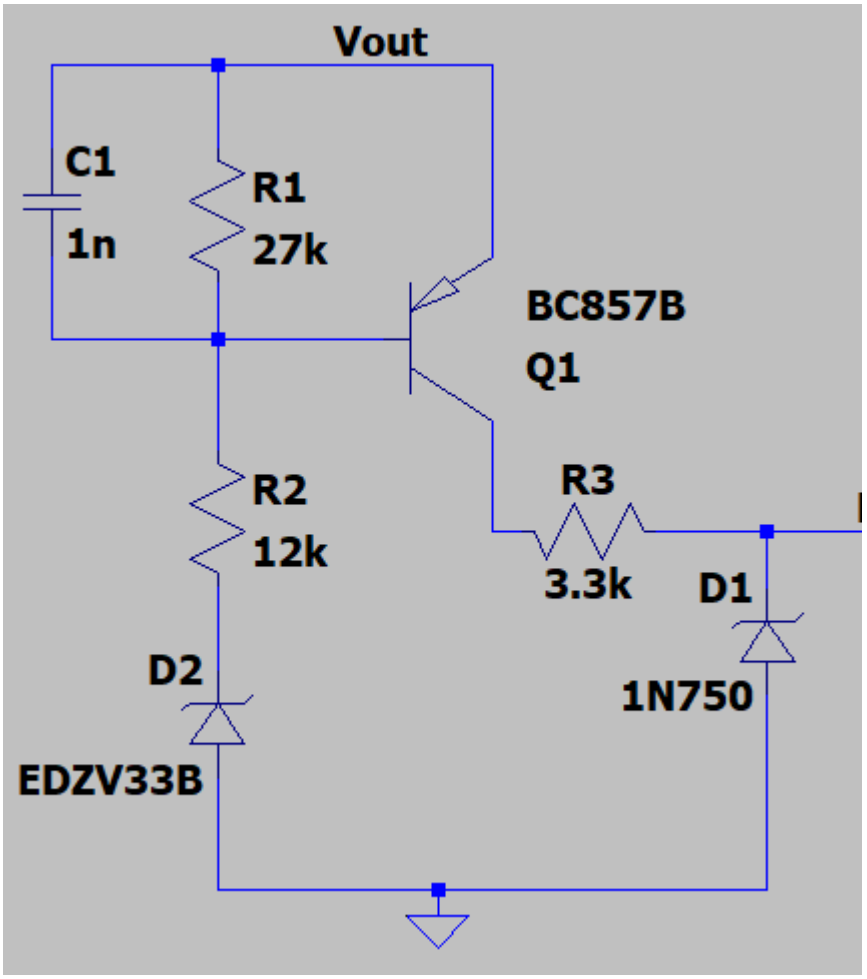



Figure 5: OVP circuit simulation

The reasoning behind the component value selection are as follows: For the BJT to conduct, $V_{BE}$ must be 0.7V or higher for this to happen when Vout = 32V with a Zener diode (D2) clamping at 31V. The voltage divider is calculated so that R1 reaches $V_{BE} = 0.7$. Upon conduction, the emitter and collector voltage will be around 1V, with around 30V at the output. Since the chosen Zener diode (1N750) has a reverse bias current limit of around 75mA a $3.3k\Omega$ resistor was implemented. On conduction this Zener diode clamps the voltage to 5V, shutting down the UC3843. However, due to component shortages of the diode model of D2 (EDZV33B) a substitute zener diode which regulates at 34V was chosen.

For any of the ICs and circuitry needing a reference/supply voltage of 5V, a linear regulator was used to derive 5V from the input voltage of 20V.

A digital isolator (ADUM131D0BRZ) and a 5V isolator (RFM-0505S) was used to supply 5V to the circuitry at the output side and also allow for isolated transmission of VFb PWM from the microcontroller to the UC3843 for control. The Template PCB provided also has isolation through conductive trace gaps separating the output side and the input side of the flyback converter

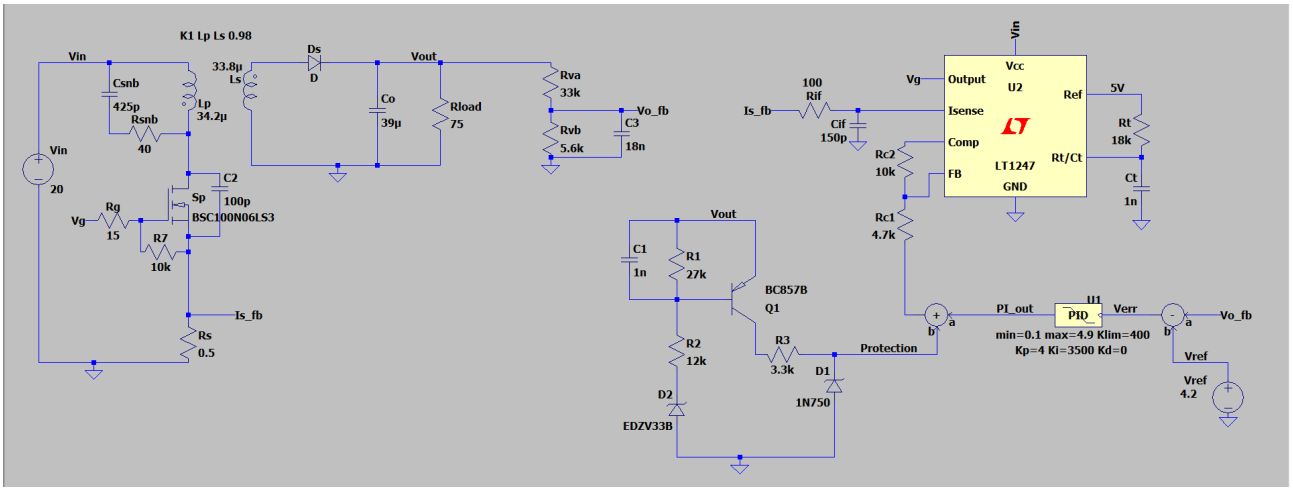



Figure 6: LTspice schematic of closed loop circuit with variable Ki and Kp.

Ki and Kp represent the gain applied to the error voltage, from simulations a larger/smaller Kp results in larger/smaller steady state error. The implications of a smaller Kp value is a longer settling time, a larger Kp value can reduce the settling time but cause ringing and amplification of noise. The integral gain ideally allows for zero steady state. A small Ki will similarly cause a long settling time, a larger Ki will improve this however worsen overshoots. The combination of the two will allow for fast settling time, low ringing, small overshoots and trivial steady state error. From experimentation, it was found that the values of Kp = 1 and Ki = 3000 resulted in the best results.

Table 4: Simulated output voltage steady state voltage of PI controller

| Parameter | Value | Unit | Value | Unit | Value | Unit | Value | Unit |
|---|---|---|---|---|---|---|---|---|
| $R_{load}$ | 16.67 | Ω | 23.15 | Ω | 33.33 | Ω | 75 | Ω |
| $V_{ref}$ | 0.7 | V | 1.75 | V | 2.8 | V | 4.2 | V |
| Steady State $V_{out}$ | 4.81 | V | 12.05 | V | 19.32 | V | 28.92 | V |
| Settling Time (+/- 5%) | 4 | ms | 5 | ms | 5 | ms | 5 | ms |

# The Schematic and PCB

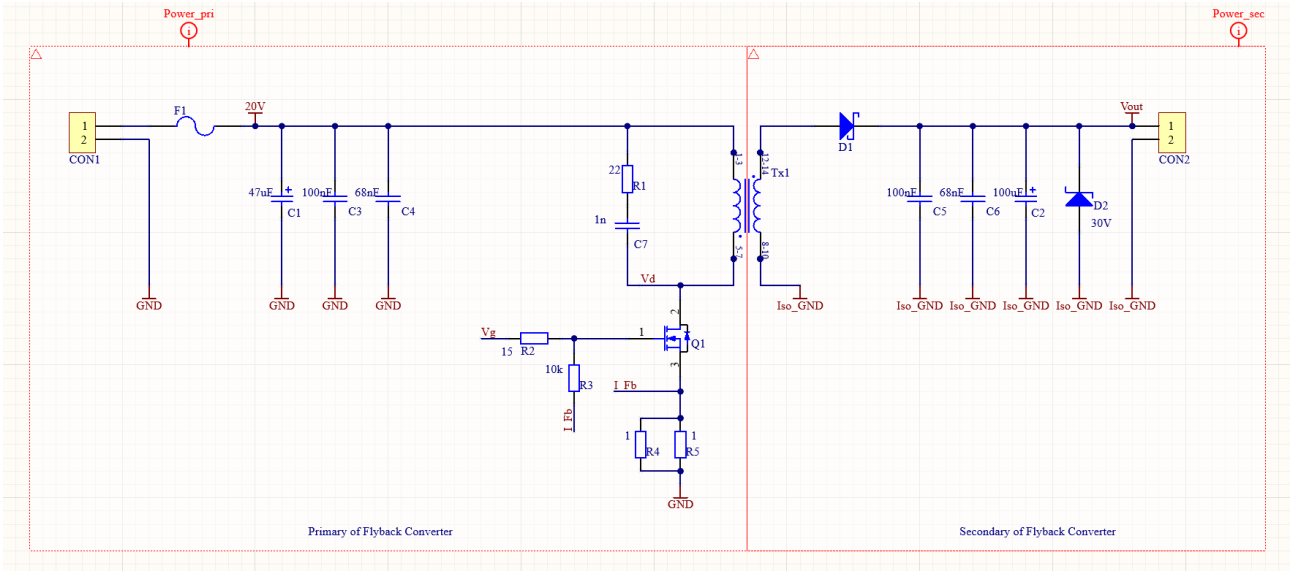



Figure 7: Schematic of Flyback transformer

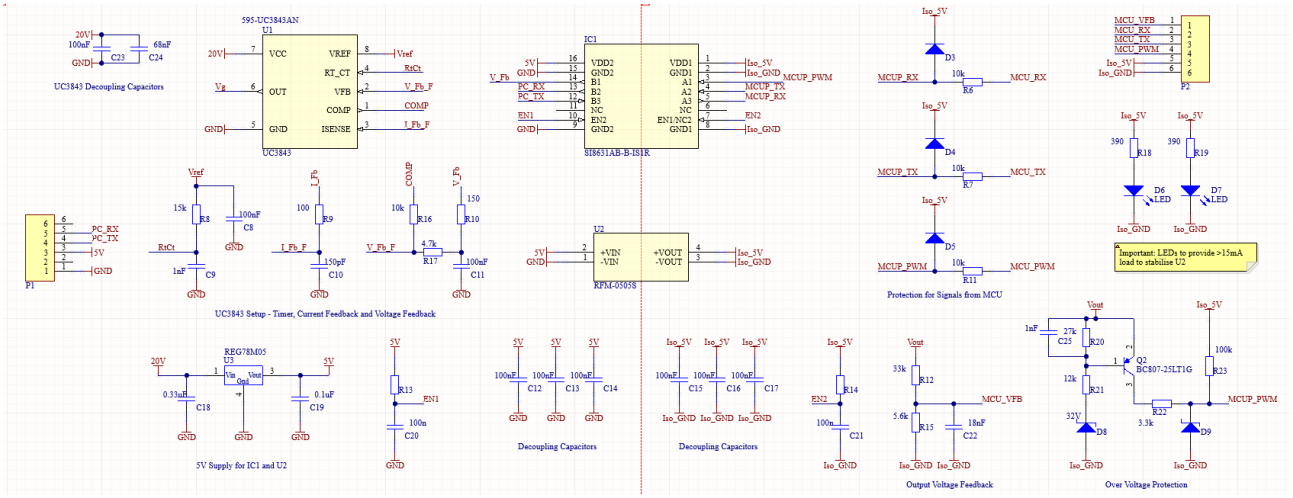



Figure 8: Schematic of the components populating the ICs and signal conditioning CCTs.

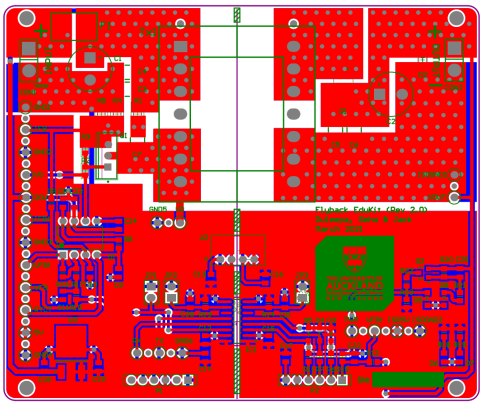


Figure 9: PCB schematic

# The Magnetic Design

## Design Calculations

The core used in the flyback transformer is the ETD34/N87, a ferrite core with an ungapped permeability of 1670 H/m. This core was chosen for its high permeability which maximises magnetic flux density, and its low electrical conductivity, minimising eddy current losses as a result of the material.

$$n \geq \frac{V_{in} D}{V_{out} D'}$$

To ensure discontinuous mode operation of the flyback converter and simplify the mathematics, the turns ratio between the primary and secondary was chosen to be 1.

$$n = \frac{N_p}{N_s}$$

$$N_p = N_s = \sqrt{\frac{L l_e}{u_0 u_r A}}$$

Np and Ns were calculated theoretically using the formulae above to achieve the target inductance of 37.5µH for both the primary and secondary windings. This produced an estimate of 7 turns per winding. The maximum magnetic field strength is given by:

$$H = \frac{N_p I_{LP(pk)}}{l_e} = \frac{7 \cdot 2.53}{0.0786} = 257\ A/m$$

The magnetic flux density is therefore

$$B = u_0 u_r H = 4\pi \cdot 10^{-7} \cdot 1670 \cdot 257 = 470mT$$

which exceeds the maximum magnetic flux density the core is specified to saturate at. Therefore, an air gap of 0.1mm is introduced to greatly decrease the effective permeability of the core and increase the current that can be transferred through the core before it saturates. The air gap reduces the effective permeability to 534.45 H/m, and a new magnetic flux density of 151mT.

Table 5: Simulated magnetic properties of core and selected windings

| Parameter | Value | Unit |
|---|---|---|
| Selected Lp | 37.5 | µH |
| Selected n | 1 | - |
| Max Bmax | 250 | mT |
| Air gap length | 0.1 | mm |
| Effective length | 78.7 | mm |
| Effective permeability | 534.45 | H/m |
| Np | 8 | - |
| Ns | 8 | - |
| Bmax | 151 | mT |
| Lp copper loss | 0.02 | W |
| Ls copper loss | 0.02 | W |

## Design Validation

The Ansys Maxwell model of the transformer uses two instances of a CAD model of the ETD34 to create the core structure. The copper windings are modelled by a hollow cylinder with a thickness of 2x the copper wire with an insulating layer between them to separate the two windings. The transformer is simulated in a vacuum. Figure 11 shows the complete transformer model and figure 10 shows the B field in the core.

In reality, it was very difficult to achieve an ideal coupling factor and the target inductance of 37.5µH. The nature of winding strands of copper wire around a cylinder does not lend itself to precise outcomes, given the limitation of a discrete number of turns and human error in the winding process itself. Multiple different winding techniques were attempted in order to increase the coupling but in the end, the technique used was to wind the primary winding and wind the secondary winding directly on top, with a layer of Kapton tape in between the two layers. Although the copper wires have an insulating outer coating on them, the Kapton tape was used to ensure when the layer disintegrates over time, the primary and secondary windings will still be electrically isolated from one another.

The final iteration of the physical transformer has a primary inductance of 33.1µH and a secondary inductance of 32.97µH with 8 turns on each winding and a coupling factor of 98.77%.

| | Freq [kHz] | Matrix1.L(Winding1,Winding1) [uH] Setup1 : LastAdaptive | M |
|---|---|---|---|
| 1 | 100.000000 | 37.045425 | |

Figure 10: Simulation results of the transformer

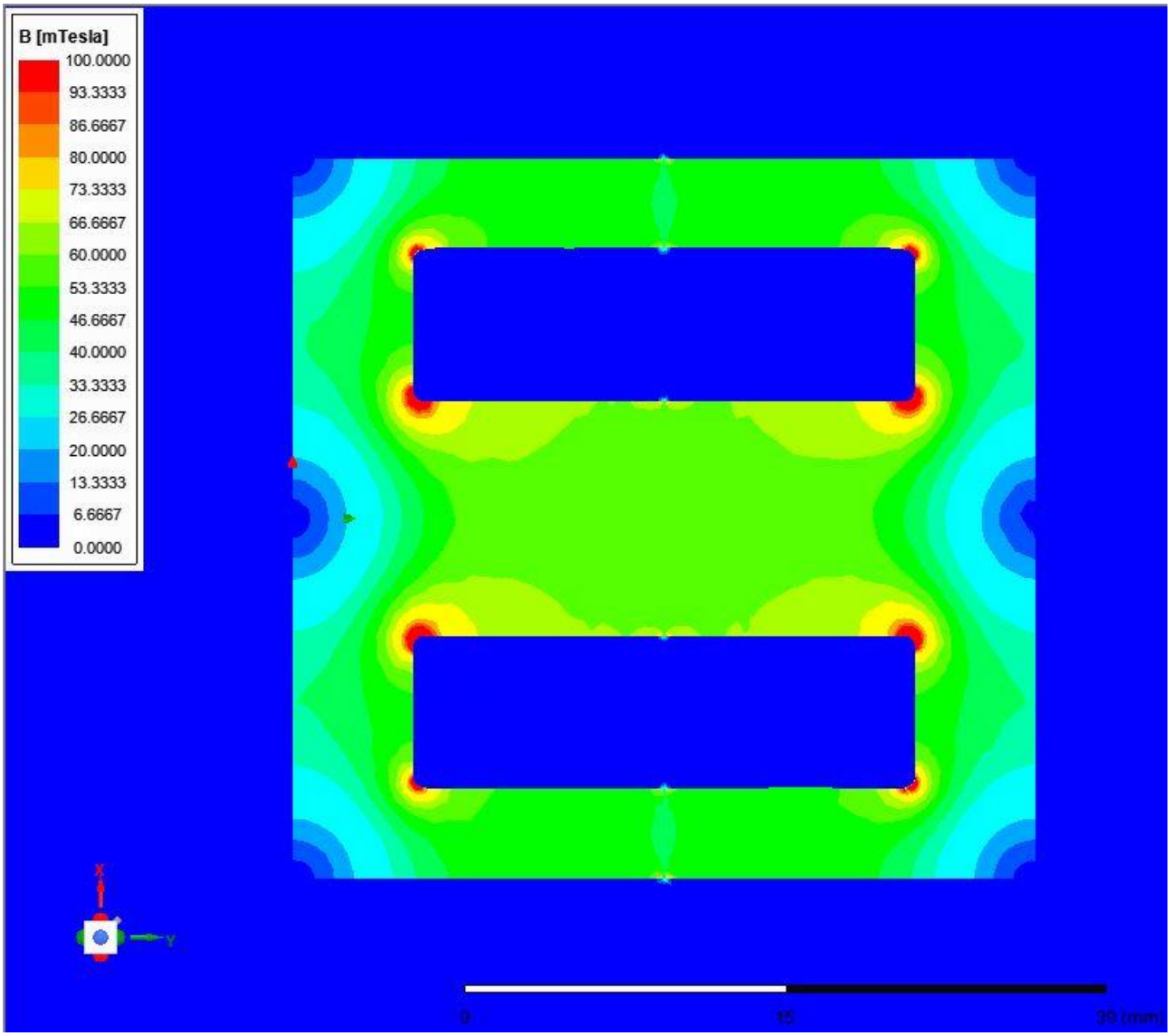



Figure 11: B field inside the core

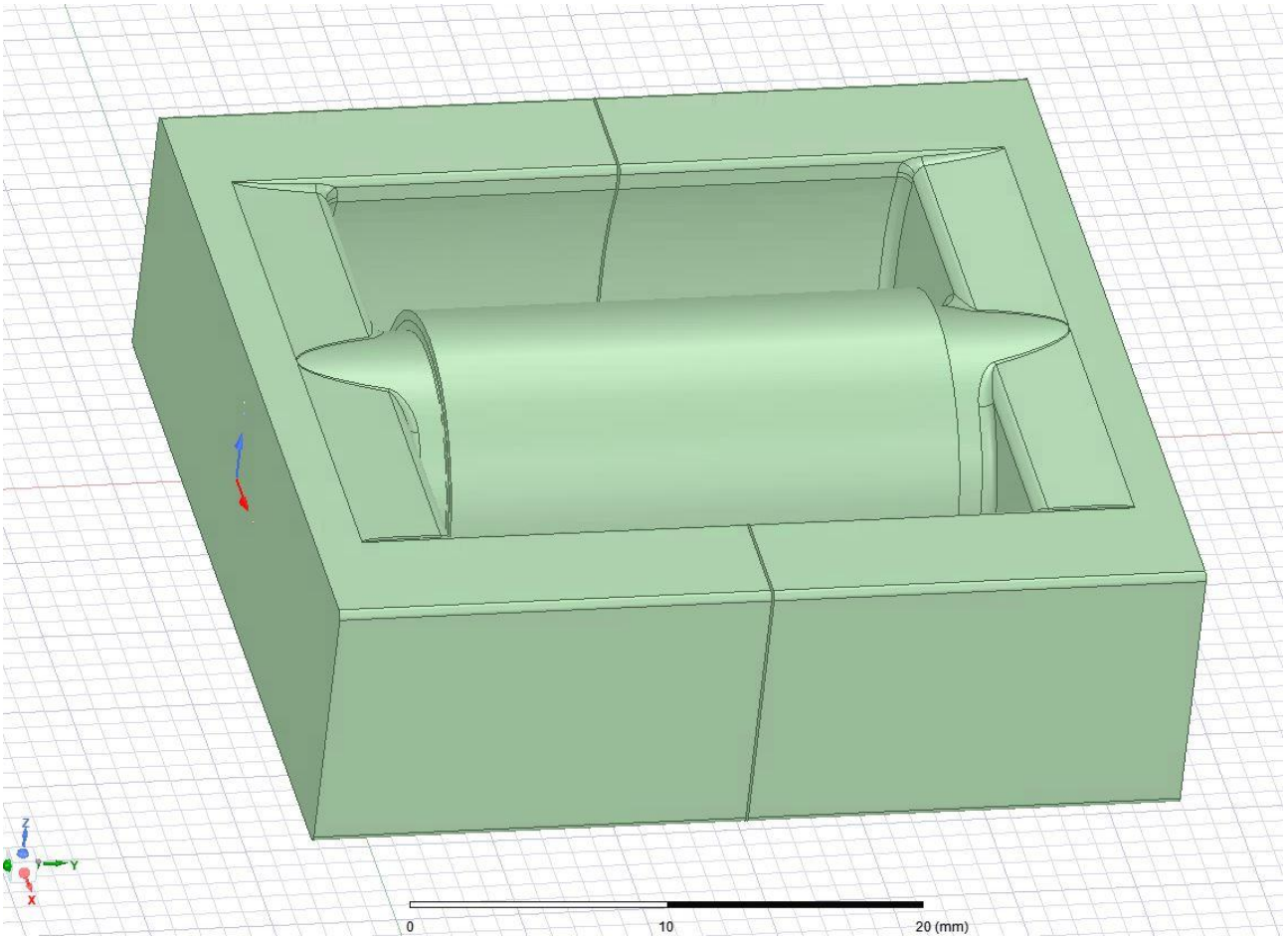
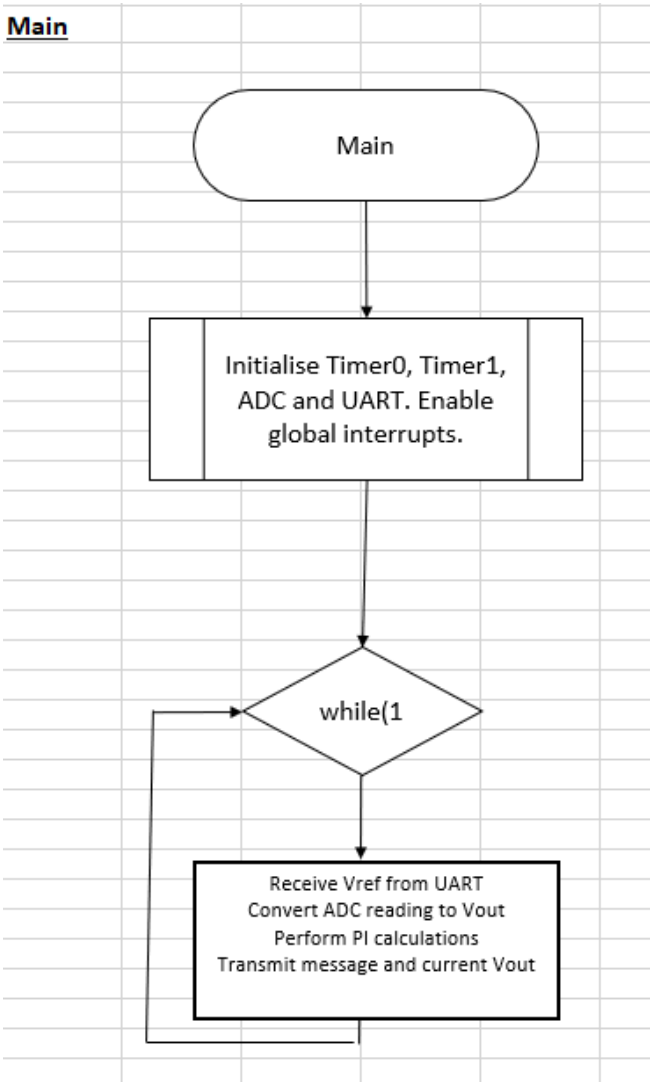


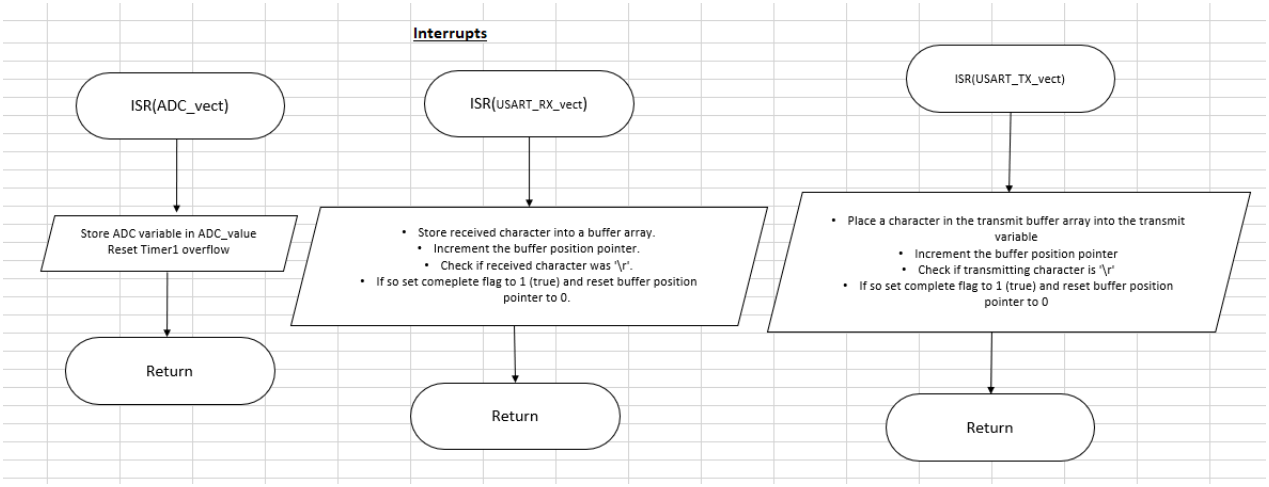

Figure 12: Maxwell model of the transformer

# The Firmware Design

## Flowchart




The main functionality of the firmware is to calculate and output a PWM signal representing the reference voltage for $I_{LP(pk)}$ in the UC3843. This is achieved with deliberately simple calculations, and thus, the code in its entirety is minimal. The main code first initializes all peripherals by calling their corresponding functions, enables global interrupts and then the main while loop is executed. This places the latest user voltage setpoint into the Vref variable and calls the PI calculation function with the current Vout. Additionally, the code transmits the calculated Vout via UART every one second by using a simple counter incrementing by 1 each time the code executes, approximately every 40uS. The code was designed to be as fast as possible to minimise the response time of the whole system and to make full use of the maximum ADC sampling rate.

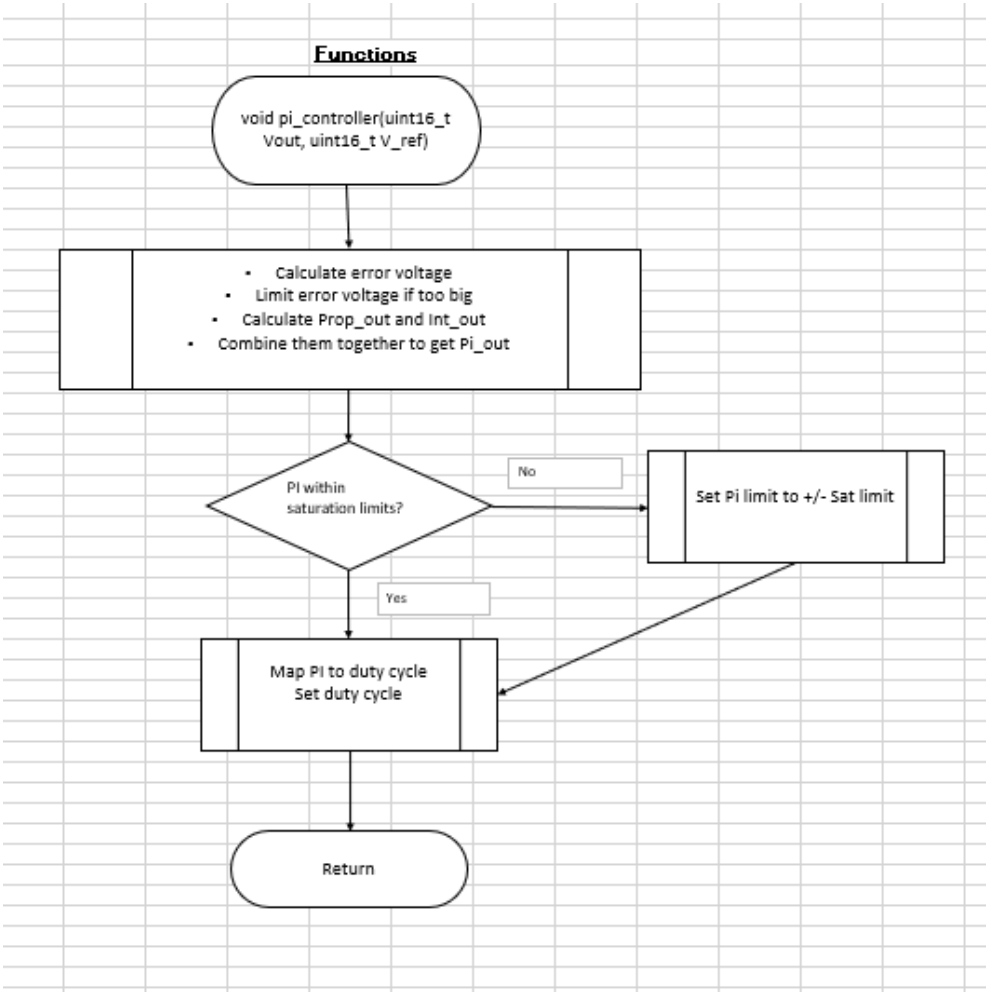



3 interrupts are used in the code, for ADC readings, UART receive and UART transmit.

The ATMega328P has a 10bit ADC peripheral to sample voltages between 0 and 5V. In this design the voltage output ranges from 5 to 30V therefore a voltage divider is implemented to step down the output voltage to an acceptable level for the ADC. A capacitor is used in parallel to this voltage divider, since the ADC peripheral has a limited sampling rate and the Nyquist–Shannon sampling theorem states that the sampling frequency must be at least twice the signal frequency of which it is sampling therefore to ensure this the capacitor and voltage divider resistor form a low pass filter. The ADC peripheral compares the voltage fed in with its internal reference and maps it to a 10 bit variable (0 to 1023). The code uses a timed interrupt for the ADC as the ADC has a minimum acquisition and conversion time and to ensure no time is wasted the interrupt is triggered when timer1 overflows which has been calculated to the minimum sampling period.

The UART receive interrupt is triggered whenever the designated register UDR0 is filled with a character. This functionality must be done as an interrupt as it is uncertain when the user inputs a value and the code must continue to run for the microcontroller to output an accurate and constant voltage reference.

The UART transmit interrupt is not necessarily needed however is convenient to use as the transmitting of characters takes time and the time in between can be used to continue calculating the next voltage reference.




The code has few functions most of which are for initialising the peripherals. The most important function is the pi_controller function which performs the PI calculations. The inputs to the PI controller are the output voltage (calculated from the ADC reading) and user voltage setpoint. The reference voltage is subtracted from the output voltage to find the error, which is the inverse of what is normally performed to account for an inversion done by the UC3843. The voltage error is then checked whether it exceeds the error voltage limit and is clamped if it does. Rate limiting is necessary so that the circuit does not undergo extreme transitions for example from 5 to 30V quickly as that can cause large overshoots at the output. The proportional component of the controller is calculated by multiplying the error voltage with a constant $K_p$. The code can not perform a standard integration since everything is in discrete time. Instead, Int_out is declared as a static variable that accumulates error everytime the PI calculations are performed. For a single execution of the PI controller function, the Int_out area is calculated by multiplying $K_I$ and $T_{sample}$ with the error voltage. $T_{sample}$ was determined by timing the code in Proteus. The proportional and integral components are then summed to find the PI output. Both the integral and PI outputs are run through a limit function as an anti-windup that prevents error accumulation when overshoots occur. The PI output is then mapped to a value between 0-159 to set the duty cycle of the PWM waveform fed to the UC3843. The mathematical operations inside the PI controller function were optimised using bit shifts in order to reduce the number of

instructions the processor has to execute to perform divisions and multiplications and therefore make the code as fast as possible.

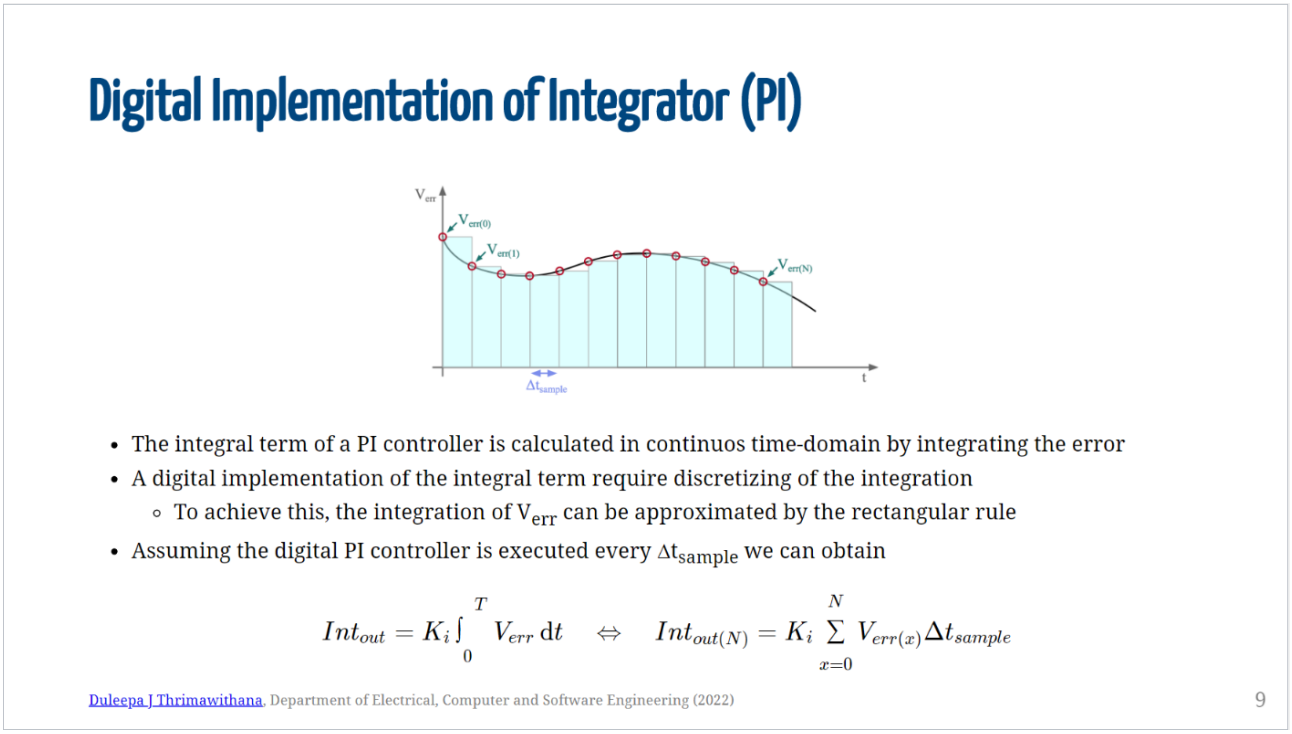



Figure 13: Digital implementation of PI controller [4]

## Peripheral Configurations

Table 6: UART configuration

| Parameter | Configuration |
|---|---|
| Number of data bits | 8 |
| Number of stop bits | 1 |
| Baud rate | 9600 |
| Parity mode | None |
| Transmission mode | Full Duplex |
| Transmit mode | Interrupts (Transmit/Receive Complete) |
| Transmit voltage | 5 V |

Table 7: Timer0 configuration

| Parameter | Configuration |
|---|---|
| Compare Output Mode | Fast PWM Mode & Clear on Compare match with OCCR0B |
| Pre-Scaler | 1 |
| OCR0A | 159 |
| Output Pin | D5 |
| OCR0B | Changes depending on Duty Cycle |

The PWM generated using timer0 is used for ATMega328P output representing the voltage reference. A top value of 159 creates a 100kHz signal and OCR0B is used to control the duty cycle and achieve pulse width modulation.  Prescaler of 1 is used to maximise the step resolution.

Table 8: Timer1 configuration

| Parameter | Configuration |
|---|---|
| Waveform Generation Mode | Fast PWM |
| Pre-Scaler | 8 |
| OCR0A | 149 |

Timer1 is used for the ADC readings. OCR0A is calculated to overflow every 75uS which is the minimum time the ADC takes to sample.

Table 9: ADC configuration

| Parameter | Configuration |
|---|---|
| ADC Input | Mux0 |
| Pre-Scaler | 64 |
| Voltage Reference Selection | AVcc with external capacitor at AREF pin |
| External Interrupt | Enabled |
| ADC Auto trigger source | Timer/Counter1 overflow |
| ADC Auto Trigger | Enabled |
| ADC Buffer | Disabled |

Table 10: I/O configuration

| Parameter | Configuration |
|---|---|
| PWM Output | PIND5 (Output) |
| ADC PIN Monitoring Output | PINC0 (Input) |

# Design Validation

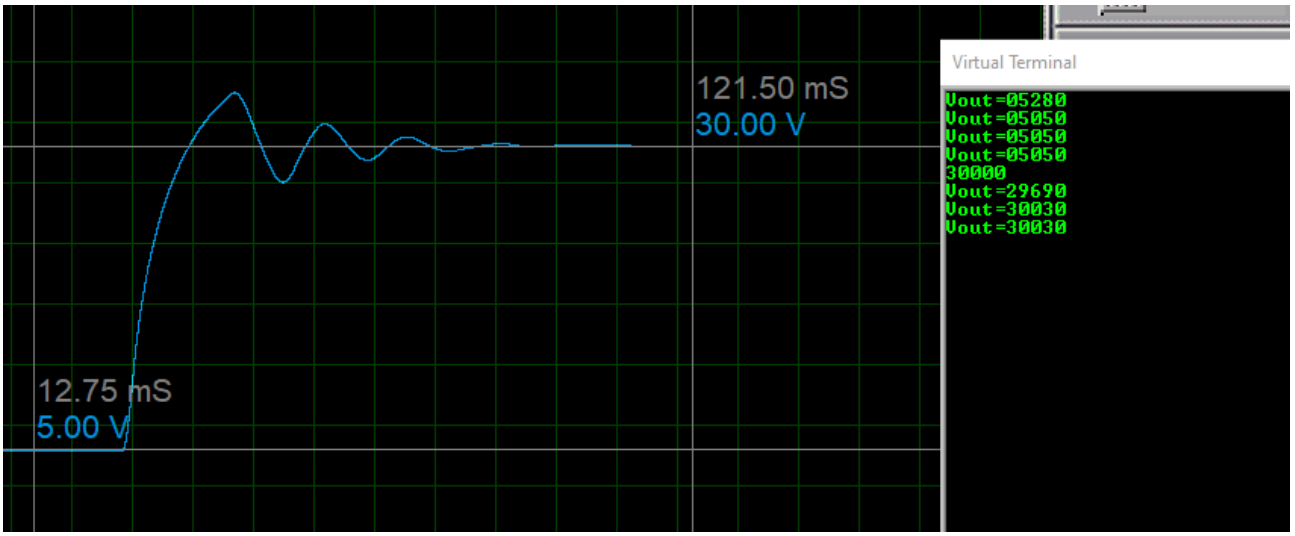



Figure 14: Step response 5- 30V

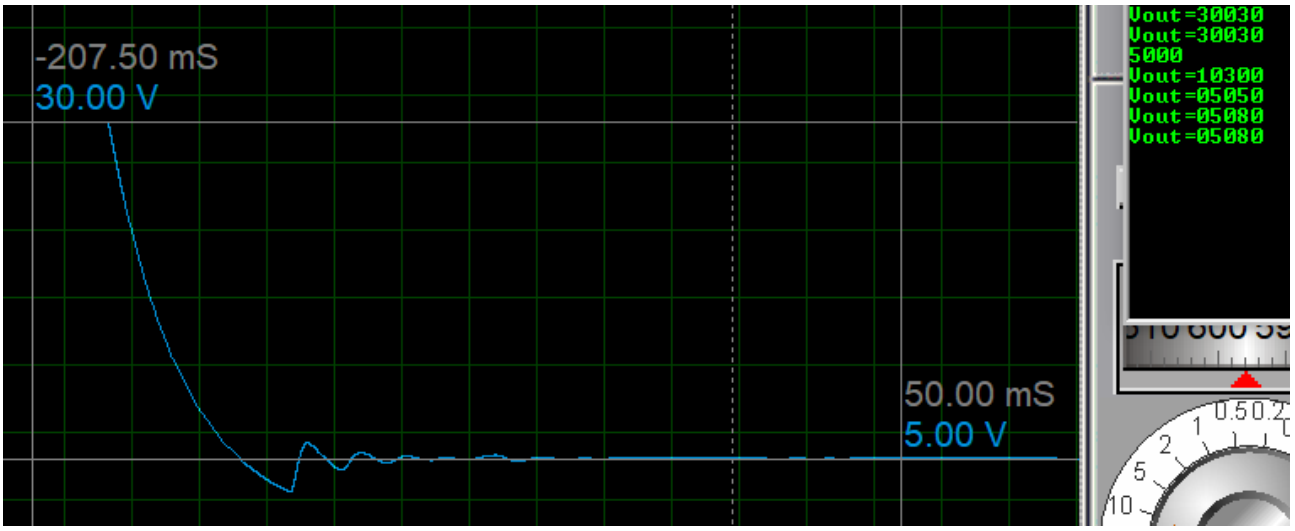



Figure 15: Step response 30 - 5V

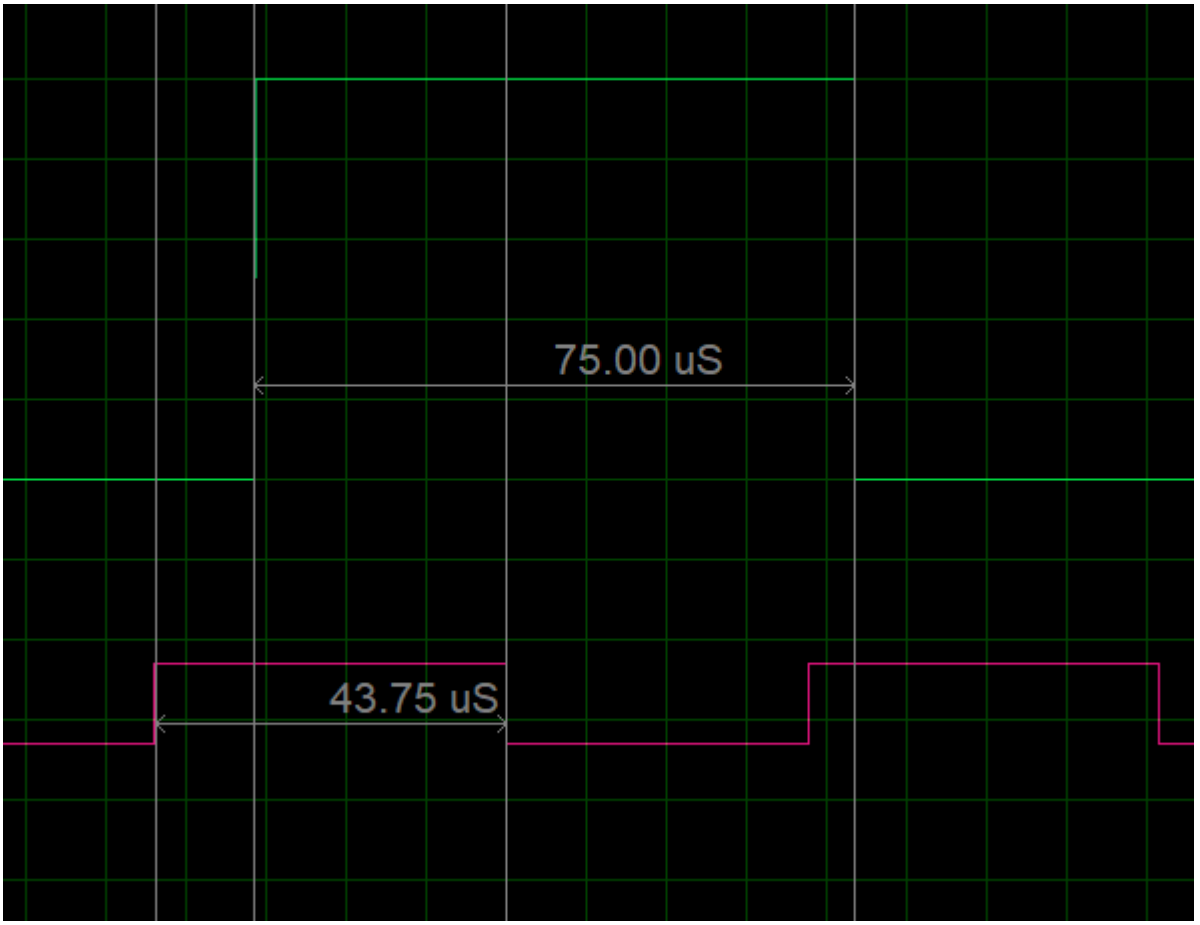



Figure 16: ADC and PI timing

Figure 15 demonstrates the speed of the code. The ADC sampling time is represented by the green waveform and the pink waveform shows the PI controller execution.

# Performance of the Power Supply

## Design Validation


Figure 17: Vout Ripple at 5V, rated load


Figure 18: Vout ripple at 12.5V, rated load


Figure 19: Vout ripple at 20V, rated load


Figure 20: Vout ripple at 30V, rated load


Figure 21: Vout ripple at large load (300 ohms)

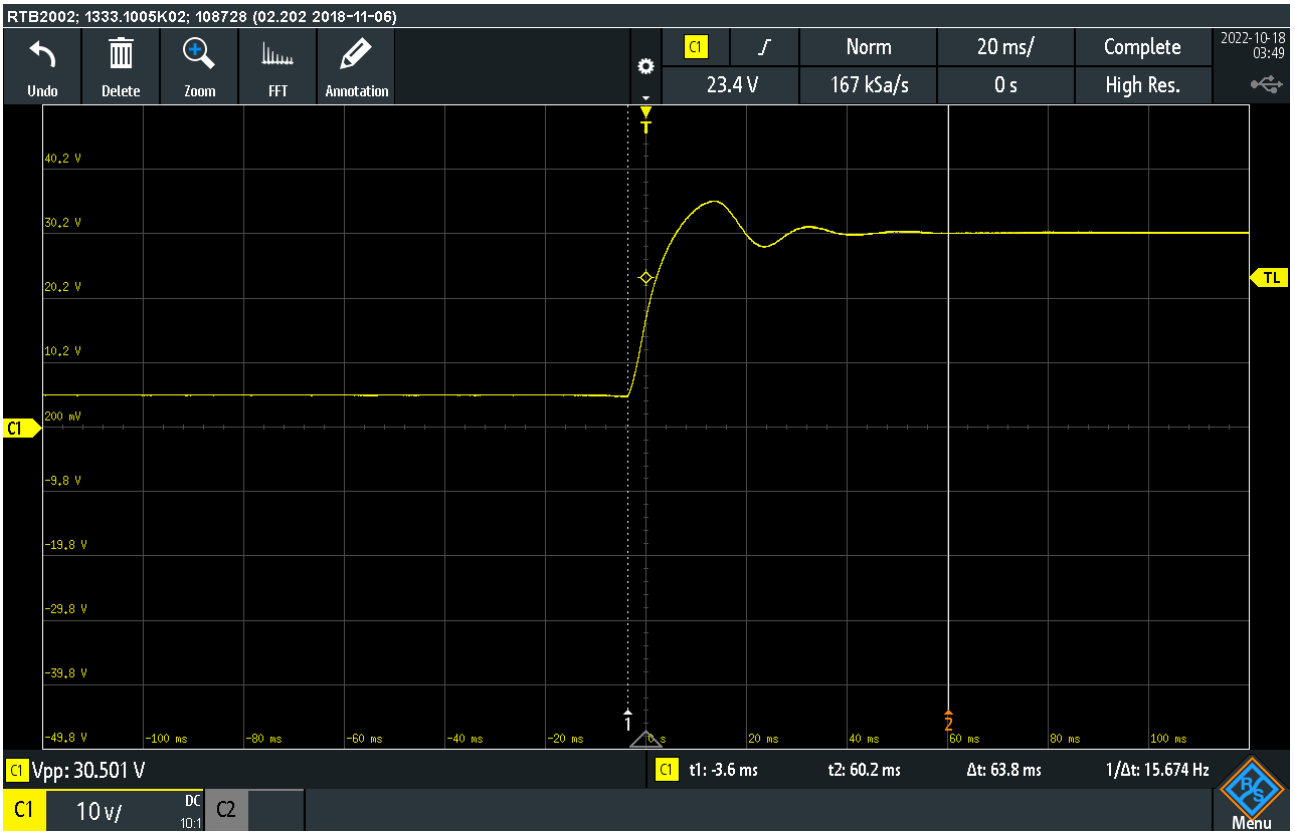



Figure 22: Step response showing timing from 5 - 30 V

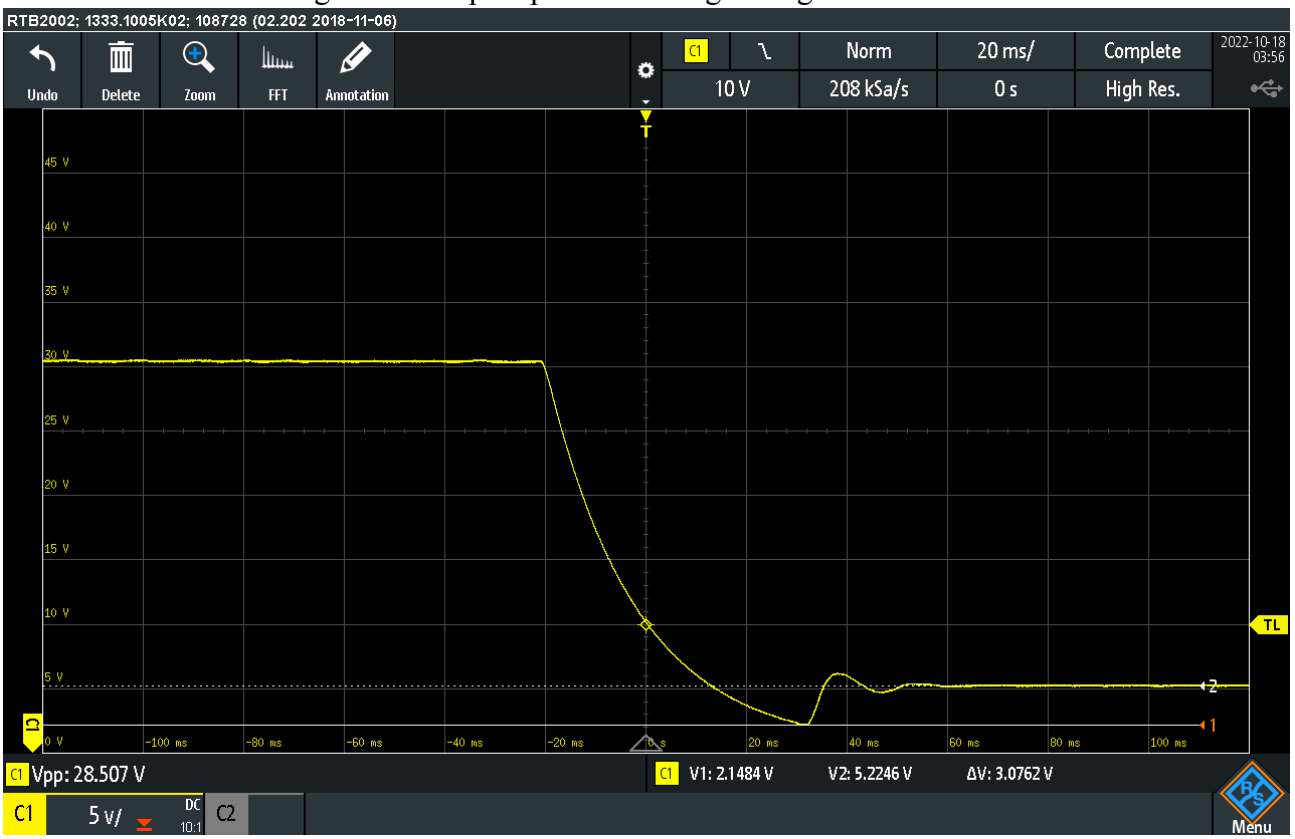



Figure 23: step response showing timing from 30 - 5 V

Table 11: DC output conditions

| User setpoint | Rated Load | DC output at Rated load | DC output at large load (300Ω) |
|---|---|---|---|
| 5V | 16.67Ω | 5.1V | 5.01V |
| 12.5V | 23.15Ω | 11.53V | 12.5V |
| 20V | 33.33Ω | 16.17V | 20.2V |
| 30V | 75Ω | 25.64V | 30.12V |

## The Performance

The flyback at rated loads has varying steady state error. The worst case scenario being at 20V for rated load of 33.33 ohms. The output voltage produced at this load has an error of 19.15%. At large loads, 300 ohms, the steady state error is significantly improved with the worst case scenario only having an error of 1% at 20v.

The step response time of the design is favourable, with a step from 5 to 30V taking approximately 63.8ms, and a step down from 30 - 5V taking 80ms.

The output voltage ripple present at rated loads is not desirable and does not meet the specifications. This is due to the value of the output capacitor being too low, and discharging too quickly.

# Improvements

With more time to improve and validate the design in order to increase performance the team would make the following changes:

- Decrease the current sense resistors

As mentioned, at rated load there is some steady state error which increases as the user increases the voltage setpoint, eg: Vout is 25V when the setpoint is 30V. This occurs because the maximum value of Ilp(peak) (ref) internally inside the UC3843 is 1V, but because the current sense resistors are 0.5 Ohms and the maximum value of Ilp(peak) is 2.53A, the voltage across these resistors can exceed 1V. As a result, when operating near maximum duty cycle, the UC3843 is switching the MOSFET off too quickly during one switching cycle, leading to not enough energy being stored in the transformer and therefore the output voltage having steady state error. A new parallel combination of $\leq 0.4$ Ohms for the current sense resistors would limit the voltage across these to less than 1V.

- Improve snubber

The current snubber resistor and capacitor values achieve the goal of reducing ringing on the switching edge, however these values could be further optimised. Doing so would decrease power

consumption in the snubber resistor, allowing more power to transfer to the output and also further reduce voltage stress across the MOSFET.

- Larger output capacitor

At present, there is a noticeable voltage ripple across the output with the capacitor value of 100µF. Increasing this value to somewhere in the range of 330-470µF would significantly improve this, at the expense of response time, so a balance would need to be found between these attributes.

- Use a 16 bit timer

As mentioned earlier, 8 bit Timer0 is used to set the reference voltage for the UC3843 by outputting a PWM with a particular duty cycle. This configuration uses a top value of 159, meaning there are only 158 discrete voltage levels for the UC3843 reference. Changing this peripheral to 16 bit Timer1 would allow for more discrete voltage setpoints and therefore more accuracy in the duty cycle setpoint.

- Adjust PI calculation constants

Kp, Ki, PI_limit, Error_limit and T_sample values were chosen using responses from simulation softwares. Further testing of the physical hardware and adjusting of constants would likely improve settling time, steady state error, ripple and overshoots.

- Better user terminal

The current implementation of the code prints the message ‘Vout =’ followed by the current Vout value. When the user inputs a value nothing is displayed additionally. These compromises were made to minimise delays in the code since both printing and receiving characters takes a significant amount of time that could otherwise be used to perform the next PI calculation. Better utilisation of interrupts could possibly allow for a more user friendly terminal without sacrificing accurate PI calculation.

# Conclusions

To conclude, this report finds that the design meets most of the requirements outlined by the brief however there are some problems with output quality. At high loads the flyback transformer is quite accurate with the worst case scenario only having 1% error. At rated loads the transformer performs worse with a worst case scenario error of 19.15%. The design also has quite large problems with output ripple which does not meet the design specifications.

The Flyback converter can still be improved through fine tuning and more testing of different component values. Also rewinding the transformer to have a better coupling factor would also increase the accuracy of the converter output. Due to the limited availability of components not all of the circuitry was composed of ideal component values, for example the current sense resistor. To improve output ripple a larger capacitor could be used at the cost of settling time. All of these could be improved on to make a better flyback converter.

# References

[1] D. J. Thrimawithana, Class Lecture, Topic: "Electronics Systems Design: An Introduction to ELECTENG 311", Department of Electrical, Computer, and Software Engineering, The University of Auckland, Auckland, April 2021.

[2] Texas Instruments,n.d.,UCx84x Current-Mode PWM Controllers.https://www.ti.com/lit/ds/symlink/uc3843.pdf?ts=1666590572619&ref_url=https%253A%252F%252Fwww.ti.com.cn%252Fproduct%252Fcn%252FUC3843

[3] D. J. Thrimawithana, Class Lecture, Topic: "Closed Loop Controller Design", Department of Electrical, Computer, and Software Engineering, The University of Auckland, Auckland, April 2021.

[4] D. J. Thrimawithana, Class Lecture, Topic: "Controller Implementation", Department of Electrical, Computer, and Software Engineering, The University of Auckland, Auckland, April 2021.


**Dep. of Electrical, Computer, & Software Engineering**
The University of Auckland
20, Symonds Street
Auckland, New Zealand
**T** +64 9 373 7599
**W** auckland.ac.nz