Computer Organization Quiz 1 – chap 1.
3/31 13:20 ~ 14:00

True or False (10 pts / problem)

1. (x) In 1998, mini-computers are gradually eliminated because supercomputers arise and their super powerful computing capability makes mini-computers useless and not cost-effective.
2. (o) Two representative design techniques to show the technical level of a country in the semiconductor area are the techniques of CPU design and memory design.
3. (o) Consider the CMOS technology in IC design, the power consumption of an IC increases as its working frequency increases under keeping the other factors unchanged. And this is also the main reason why the CPU design goes towards the multi-core design rather than running on higher clock frequency.
4. (o) Two designs of the same functionality have different die sizes. The chip with larger die size has lower yield and then the higher cost for manufacturing to produce the same number of chips for sale.
5. (x) Alice used to run several programs or use several tools at a time. For this kind of use model, a new computer running at higher clock rate instead of having more CPU cores running at the same clock rate is better for Alice's use model in terms of response time.
6. (x) Elapse time is the time spent in processing a job, not including the time for IO and OS overhead and

idle time.

7. (o) For an instruction set of a CPU with variant purposes, it is hard to have identical execution time for each instruction. It would be best that the longer execution time is a multiple of the minimum execution time.
8. (x) When a CPU runs with 100% loading, its power consumption is also the highest. On the contrary, as a CPU keeps idle with 0% loading, it has no power consumption.
9. (o) If a 50% CPU performance improvement in a year always comes true, the performance of a new CPU designed and released two years later is higher by 2.25 times than that of current CPU.
10. (o) If we use clock rate and CPI to compare the performances of two CPUs, the potential issue is we ignore the differences between two ISAs and their instruction complexity.