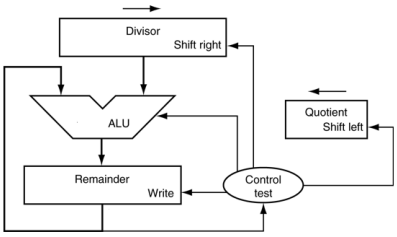
Computer Organization: Quiz 3 **Student ID:** **;Name:**

(TRUE or FALSE) (100 pts)

1. (O) Consider a ripple carry adder, the delay of a ripple carry adder is the sum of the following three delays: (1) the delay of generate and propagate circuit, (2) the delay of carry ripple from lsb to msb, and (3) the delay of sum circuit in msb.
2. (x) We can use bit-level *generate* and *propagate* to assemble a carry lookahead adder of any bit size without inducing any penalty.
3. (O) Consider the Booth multiplication algorithm; we use b_0b_{-1} to determine which operation should be performed during scanning the multiplier from lsb to msb. If b_0b_{-1} = 01, we should perform an addition.
4. (O) Consider the bit sequence 0101111011001 as a multiplier; the required number of additions and subtractions using the Booth algorithm is 8.
5. (o) The operation of subtracting one very large positive number from one very small negative number may produce an overflow.
6. (x) The use of sticky bit can count how many 1s appear in the already rounded bits.



7. (x) The above figure shows a division hardware for 32-bit MIPS CPU design. The divisor register and ALU are both 32-bit long.
8. (O) In IEEE standard 754 for floating point number representation, we only store the fraction part of the normalized significand since the integer part is always 1.
9. (x) When we add two floating point numbers in IEEE 754 format, we do not need to shift the exponent because two significands are already normalized and we need to keep significand normalized after addition.
10. (x) In IEEE standard 754, only normalized floating point numbers can be represented and denormalized numbers cannot be represented in IEEE 754 format.