國立交通大學 資訊工程系 計算機組織 第二次考試 (2022/6/9 1:20PM~3:20PM)

請注意：1. 不可看書及任何參考資料(Close book)。 2. 請詳述設計或計算過程(detail your design or computation process)。 3. 請依題號作答，否則高題號答案出現後，之後的低題號答案將不予計分(answer each problem in problem sequence. The answers of small ID problems that appear behind the answers of large ID problems will be ignored)。

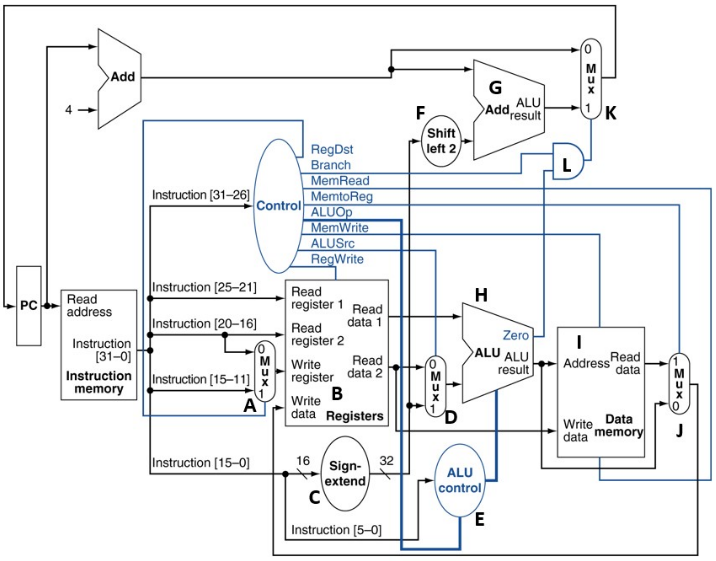


Fig. 1

	Signal name	R-fmt	lw	sw	beq
In	Op5	0	1	1	0
	Op4	0	0	0	0
	Op3	0	0	1	0
	Op2	0	0	0	1
	Op1	0	1	1	0
	Op0	0	1	1	0
Out	RegDst	?	0	X	X
	ALUSrc	0	?	1	0
	MemtoReg	0	1	X	?
	RegWrite	1	?	0	0
	MemRead	0	1	0	?
	MemWrite	?	0	1	0
	Branch	0	0	?	1
	ALUOp1	1	0	?	0
	ALUOp2	0	0	0	?

Fig. 2

ALUOp		Funct field						Operation
ALUOp1	ALUOp0	F5	F4	F3	F2	F1	F0	$C_3\,C_2\,C_1\,C_0$
0	0	X	X	X	X	X	X	0010 (lw/sw)
X	1	X	X	X	X	X	X	0110 (beq)
1	X	X	X	0	0	0	0	0010 (add)
1	X	X	X	0	0	1	0	0110 (sub)
1	X	X	X	0	1	0	0	0000 (AND)
1	X	X	X	0	1	0	1	0001 (OR)
1	X	X	X	1	0	1	0	0111 (slt)

ALUOp1	ALUOp0	F5	F4	F3	F2	F1	F0
1	X	X	X	X	X	X	1

Fig. 3

1. Single-cycle CPU (21 pts)

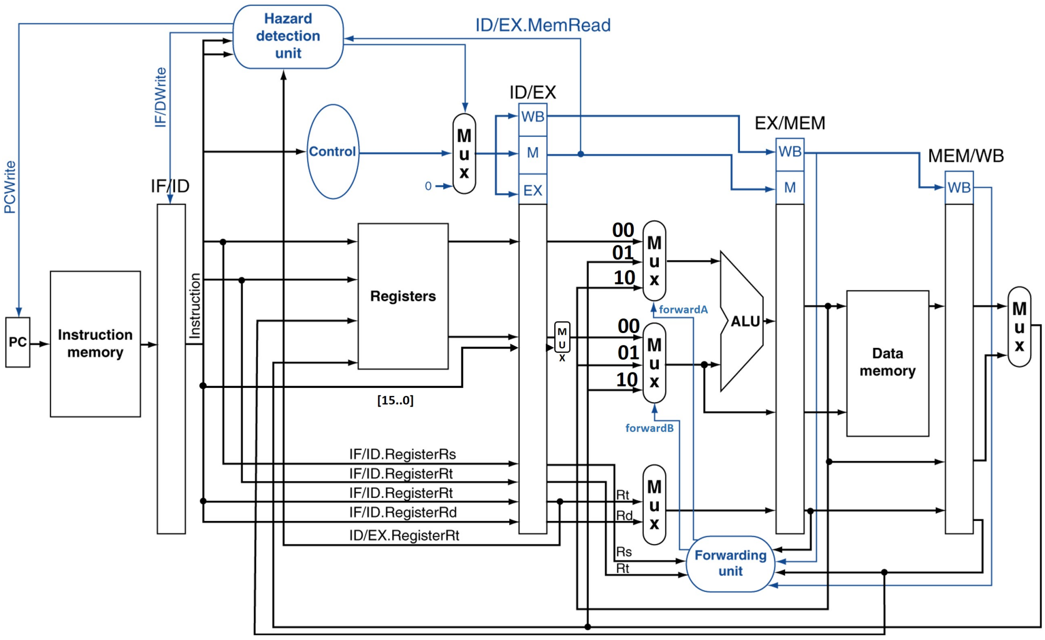
Fig. 1 shows a MIPS single-cycle CPU design. Components *A* to *L* are highlighted in the figure.

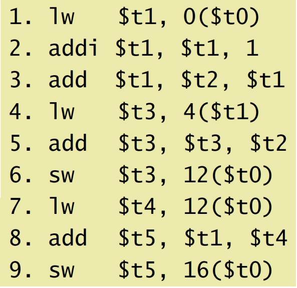
(a) (4 pts) Which components are not required by *store* instructions? (note that “are not required” means that the execution of store instruction is not affected by the result of the component)

(b) (4 pts) Which components are not required by *beq* instructions?

(c) (5 pts) Fig. 2 shows the truth table of the first-level control unit for the single-cycle CPU design. Complete the truth table for each question mark in the table.

(d) (8 pts) Fig. 3 shows the truth table of the second-level control unit for the single-cycle CPU design and the incomplete output function for output signal c_0. Complete this table.





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1. lw    $t1, 0($t0)
2. addi  $t1, $t1, 1
3. add   $t1, $t2, $t1
4. lw    $t3, 4($t1)
5. add   $t3, $t3, $t2
6. sw    $t3, 12($t0)
7. lw    $t4, 12($t0)
8. add   $t5, $t1, $t4
9. sw    $t5, 16($t0)
```

Fig. 4 Fig. 5

2. **Pipelined CPU (31 pts)**

The above figures show a code sequence of 9 instructions performed on a MIPS 5-stage pipelined CPU with forwarding unit and hazard detection unit.

(a) (11 pts) For the execution of the above code sequence, which instructions need the forwarding scheme to diminish the required clock cycles (Notably, you only need to count the instructions that consume data, not including the instructions producing data) (8 pts)? How many clock cycles does the CPU with forwarding scheme need to complete the execution of the code sequence (3 pts)?

(b) (6 pts) For all forwarding operations used in performing the code sequence, list the values of one *forwardA* and one *forwardB* for the multiplexers of the ALU's input sources. You can choose any two forwarding cases as your answer. You need to specify the instructions you use. Besides, one instruction must be the case referring to the first input source and the other to the second input source.

(c) (5 pts) Use any instructions in the code sequence to explain how the hazard detection unit works, including the conditions to make a hazard happen and the schemes to make things go well.

(d) (9 pts) We can re-order the instructions to diminish the required clock cycles further. Please list the new code sequence after re-ordering to obtain the least required clock cycles (6 pts). How many clock cycles does the CPU need to complete the execution of the re-order code sequence (3 pts)?

3. **Superscalar CPU (6 pts)** Explain how a superscalar CPU works.

4. **Memory hierarchy (36 pts)** Consider a 32-bit byte addressing memory and a cache with data size of 256K bytes for the following problems. Each cache block is 256-byte.

(a) (8 pts) Explain the spatial locality and temporal locality (4 pts). For each kind of locality, list one example and illustrate why it goes into that category. (4 pts)

(b) (6 pts) For a direct-mapped cache, what is the address format (the number of bits for tag, index and offset)?

(c) (6 pts) For a 4-way set associative cache, what is the address format?

(d) (8 pts) Consider the following memory accesses in physical address: 0X11A9 83E2, 0X11A9 8200, 0X11A9 8311, 0X11BF 8311. For the 4-way set associative cache, explain why each access in cache is hit or miss. Assume before these accesses, two blocks of each set in the cache has been used to store the data block of earlier memory accesses, and the data block now in the cache do not contain any data of these five memory accesses.

(e) (8 pts) On a virtually addressed memory system, given a virtual address, we need to translate the virtual address to a physical address first before accessing the cache. Describe the schemes before accessing the cache for the following two conditions. You need to describe the operations on TLB, page table, and hard disk. (i) the data is not in the cache and memory and is in the hard disk; (ii) the data is in the memory but the page information is not in the TLB.

5. **Data coherence and consistency (9 pts)**

(a) (6 pts) Use the following example to explain the snooping cache coherence protocol. CPU *A* reads *X*, then CPU *B* reads *X*. CPU *A* writes a new value in *X*, and finally CPU *B* reads *X*.

(b) (3 pts) As processor *P*1 writes *X*, and then writes *Y*. Complete the description to guarantee the memory consistency. "All processors that see new *Y*…".