Computer Organization: Quiz 1 **Student ID:** **;Name:**

(TRUE or FALSE) (100 pts)

1. (o) From the point of view of a web service provider, throughput is a suitable metric to measure the performance of the web-service computers.
2. (x) The required time for performing an array resetting in a program should be categorized as system CPU time.
3. (o) Runtime of a program is determined by clock rate (CR) and required number of clock cycles (CC). For the condition that we cannot reduce the clock period of a CPU, we can reduce the required number of clock cycles for a program to improve computer performance.
4. (x) For the same hardware design, we always can reduce the runtime of a program when we lower the clock cycle time.
5. (o) Million instructions Per Second (MIPS) metric favors the RISC architecture since it only counts the number of executed instructions per second without considering the complexity of executed instructions.
6. (o) Instruction set architecture (ISA) provides an interface for hardware and software design, and makes portable binary program feasible.
7. (x) Even with the aids of ISA, compute system software developers cannot start their system software development until the new CPU has been made.
8. (x) Designing new CPUs operating on higher clock rate has become much more challenging due to the fact that semiconductor technology can not shrink devices any more.
9. (x) The consumed power of a computer under full loading is much bigger than that under zero loading because the consumed power under zero loading is zero or very close to zero.
10. (x) A computer needs 10 seconds to run a program, where addition and division both occupy half runtime of the program. It is possible to design a new adder for the computer such that the new computer only needs 5 seconds to run the program.
11. (x) The only reason why mini-computers disappear in the market is that the price of personal computers becomes lower gradually.
12. (o) Algorithms affects the number of instruction count and possibly CPI (number of cycles per instruction).
13. (o) The access time required for huge amount of memory accesses is one of the main challenges for designing AI accelerators.