Computer Organization: Quiz 5 **Student ID: ;Name:**

(TRUE or FALSE) (104 pts)

1. Temporal locality describes the phenomena that the items accessed recently are likely to be accessed again soon. (o)
2. With the locality phenomenon, a memory hierarchy system that is designed to use a small size of cache can has very high performance to reduce the totally required access time at lower memory level significantly, such as the levels in the main memory and hard disk. (o)
3. For a 32-bit byte addressing memory and a direct mapped cache with 256 16-word blocks, the offset field needs 6 bits, the index field needs 8 bits, and the tag field is 18-bit wide. (o)
4. If the cache in problem 3 is replaced with a fully associate cache, the offset field needs 6 bits, the index field is 1-bit wide, and the tag field is 25-bit wide. (x)
5. If the cache in problem 3 is replaced with a 2-way associate cache with 256 sets where each set contains 2 16-word blocks, the offset field needs 6 bits, the index field is 7-bit wide, and the tag field is 19-bit wide. (x)
6. For a 2-level cache, the main objective of the 1-level cache is to minimize the hit time while that of the 2-level cache is to minimize the miss rate (o).
7. For cache design, larger block size can reduce miss rate. However, increasing block size also increases the possibility of pollution, which might increase miss rate. (o)
8. Write through policy is to write the new data to cache as well as memory simultaneously. (o)
9. Write no allocate policy is, as a write miss occurs, to write data to memory only without loading data into cache. (o)
10. 4-bank interleaved memory can access 4-word data from memory concurrently and 4-word data must be sent to cache in a data transfer. (x)
11. Virtual memory must has larger capacity than physical memory. (x)
12. Virtually memory has flexible mapping scheme and allows to map different virtual pages to the same physical page. That is, two virtual pages of a process can be mapped to the same physical page. (x)
13. The page table of a process is created by OS and stored in the main memory. As a page is already moved to the main memory, an access to this page needs two memory accesses, where the first access is for the translation from virtual address to physical address and the second access is for data access in the main memory. (o)