國立交通大學 資訊工程系 計算機組織 第二次考試 (2023/6/1 1:20PM~3:20PM)

請注意：1. 不可看書及任何參考資料(Close book)。 2. 請詳述設計或計算過程(detail your design or computation process)。 3. 請依題號作答，否則高題號答案出現後，之後的低題號答案將不予計分 (answer each problem in problem sequence. The answers of small ID problems that appear behind the answers of large ID problems will be ignored)。

1. **CPU control (24 pts)**

   (a). (15 pts) Consider the MIPS CPU in Fig. 1. Please complete Table 1 that describes the CPU control signals.

   (b). (9 pts) Assume the CPU control signals are described in Table 2. The opcodes of *R-format* instructions, *lw*, *sw*, and *beq* are: (op_5, op_4, op_3, op_2, op_1, op_0)=(0, 0, 0, 0, 0, 0), (1, 0, 0, 0, 1, 1), (1, 0, 1, 0, 1, 1), and (0, 0, 0, 1, 0, 0). Please write the Boolean function for each control signal.

2. **Pipelined CPU (20 pts)**

   Fig. 2 shows a pipelined CPU, fundamental forwarding conditions, and a code sequence. Assume *lw* enters the pipelined CPU at clock cycle 1.

   (a). (6 pts) Which condition should be applied as the second and third instructions are at the execution stage, respectively? Your answer should look like 1a.

   (b). (3 pts) What are the complete forwarding conditions that can detect the need of forwarding for the third instruction? Your answer should look like if (…..) forwardX=number.

   (c). (11 pts) At clock cycle 3, What stages are the first three instructions in (3 pts)? At clock cycle 4, what stages are the second and third instructions in (2 pts)? What cycle is the first bubble for stalling generated (1 pts)? In which stage (1 pts)? As the bubble is generated, what values of *IF/DWrite* and *PCWrite* are set (2 pts)? What are their functions at this time (2 pts)?

3. **Dynamic branch predictor** (6 pts) Figure 3 depicts two types of dynamic 2-bit branch predictors. Consider the following codes. Assume that initially the predictor stays at state 0. If inner loop bypasses (not taken) two times and then repeats (taken) four times, please list whether each prediction result is correct for two predictors.

```
outer: …
       …
inner: …
       …
       beq …, …, inner
       …
       beq …, …, outer
```

4. **Superscalar** (5 pts) Describe the operations of a superscalar CPU.

5. **Memory Addressing for Hierarchical memory** (45 pts)

   Consider a 16-bit computer with a hierarchical memory system consisting of a disk, a 2^{16}-byte main memory using byte-addressing on PCB, and a two-level cache with primary cache of 2^9-byte data inside CPU. The OS adopts a 18-bit virtual address with a page size of 512B. Notably a word of the computer consists of 2 bytes.

   (a). (6 pts) How many pages are there in this virtual memory (2 pts)? How many bits are used for the fields of page offset and virtual page number, respectively (4 pts)?

   (b). (6 pts) The primary cache is designed as follows. It is a 2-way set associated cache. Each block is 8-

word long and the replacement policy is LRU. How many bits are used for the fields of tag, set, and offset (including byte and word offset)?

(c). (7 pts) What are the disadvantages of using virtually address to access cache (2 pts)? What are the advantages of the physically tagged and virtually indexed cache (2 pts)? Is the physically tagged and virtually indexed cache suited to this hierarchical memory system? why (3 pts)?

(d). (10 pts) Assume the disadvantage of virtually addressed cache has been resolved, we apply virtually addressed cache in this computer. What are the results of using the following virtually address accesses to access cache if the cache initially contains the blocks, 0x23A6, 0x5080, and 0xA640? 0x13A8, 0x23A8, 0x138A, 0x5184, and 0xA088. You need to write the values of tag, set, and offset to show why an access is hit or miss to get full credit. If a block replacement occurs, you need to list the block to be replaced. No credit is given if you do not list these detailed information.

(e). (10 pts) Table 3 shows the possible combinations of events in the TLB, virtual memory system, and physically indexed (tagged) cache. Determine whether each event is possible and explain the circumstance of each event such as whether it is in memory and cache.

(f). (6 pts) Consider the design change: increase cache size, increase associativity, and increase block size. What type of misses, including compulsory, capacity, and conflict, can be reduced by each design change? Why?

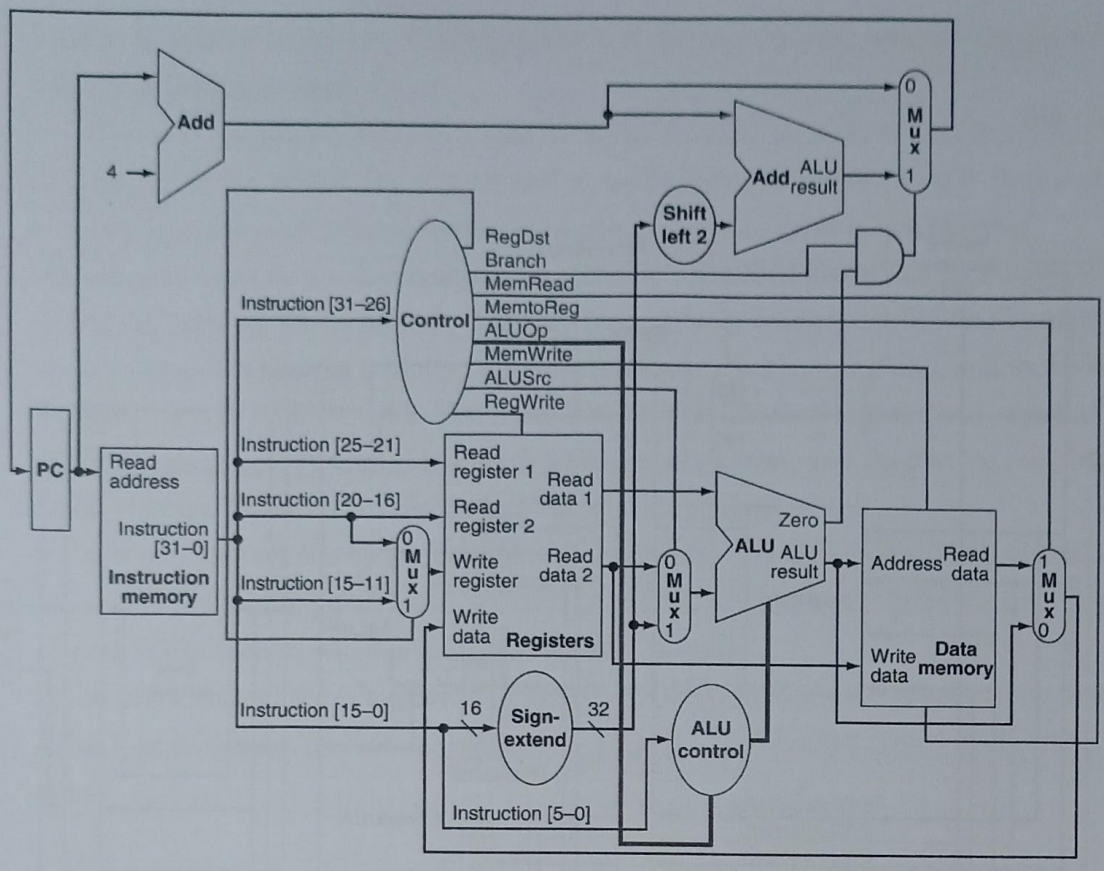

Figure 1

Table 1

Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	1	0	0	1	0	0	0	1	0
lw	0	1	1	1	1	0	0	0	0
sw	X	1	X	0	0	1	0	0	0
beq	X	0	X	0	0	0	1	0	1

Table 2.

Op_2 $\sim(Op_5 \vee Op_2)$ | Op_3 $Op_5 \wedge (\sim Op_3)$ | $\sim(Op_5 \vee Op_2)$ $\sim(Op_5 \vee Op_2)$ Op_2

Instruction	RegDst	ALUSrc	Memto-Reg	Reg Write	Mem Read	Mem Write	Branch	ALUOp1	ALUp0
R-format	0	1	1	0	x	x	1	1	0
lw	x	0	1	0	1	1	x	0	0
sw	0	x	X	1	0	1	0	0	0
beq	1	0	1	x	0	x	0	0	1

Table 3.

TLB	Page table	Cache	Possible ? If so, under what circumstance ?
Hit	Hit	Miss	
Miss	Hit	Hit	
Miss	Hit	Miss	

Hit	Miss	Miss
Miss	Miss	Hit

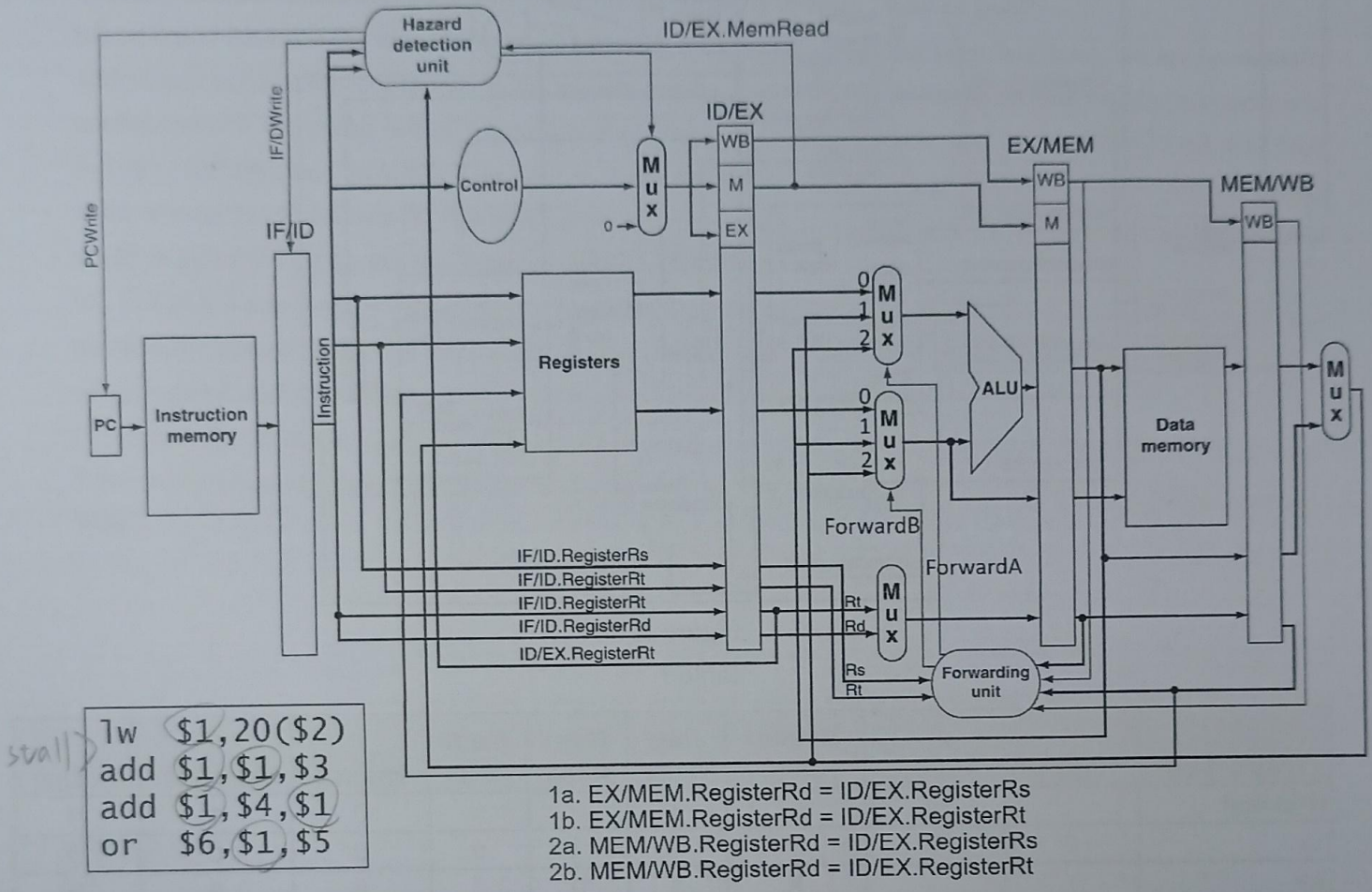

Figure 2

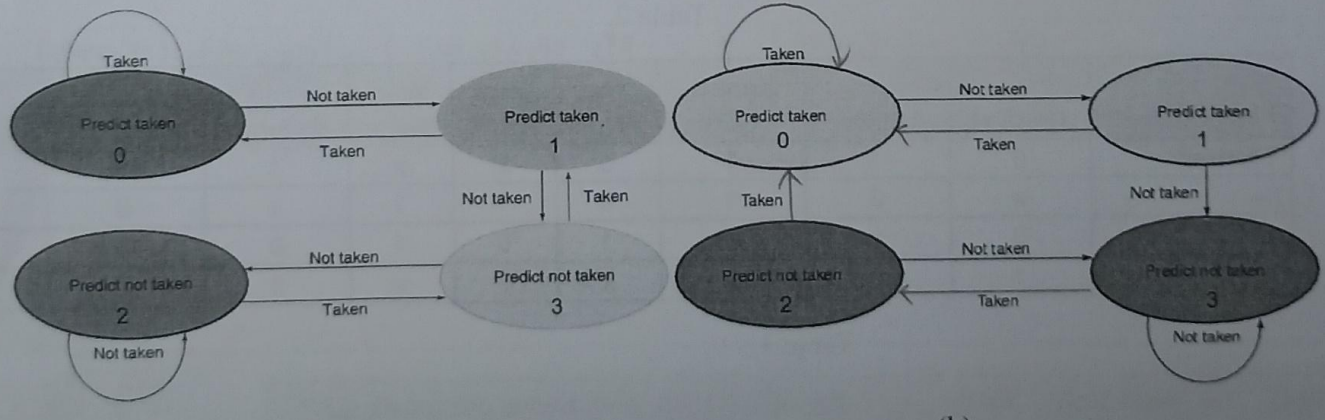

Figure 3(a) (b)