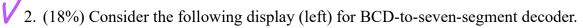
## Department of Computer Science National Chiao Tung University

## **Digital System Design**

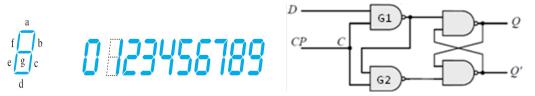
Second Midterm Exam

12/06/2012

1. (10%) Derive the optimal (simplified) two-level NOR-OR implementation of f(x,y,z) = x'y'z' + x'z + y'z.



- (a) Implement *a*, *b*, *c*, *d* using a decoder and external gates (with least wires).
- (b) Implement *e* with an 8x1 multiplexer and an inverter.



(10%) Consider the above circuit (right). Obtain the output values of G1 and G2 for different values of *CP* and *D* inputs to show that it is a *D*-latch.

1. (10%) Implement a four-bit (even) parity generator using a 4x1 multiplexer and minimum number of logic gates.

5. (10%) Design a code converter that converts a decimal digit from the 2421 code to BCD, with  $d(w,x,y,z) = \sum (5,6,7,8,9,10)$ .

(16%) Consider a sequential circuit with a D flip-flop A, a JK flip-flop B, an input x, and an output z, with the following input/output equations

$$D_A = Ax'$$
,  $J_B = x$ ,  $K_B = Ax + B$ ,  $z = Bx'$ 

Derive the state table of the circuit.

(18%) Derive the state table and state diagram of a sequential circuit with three T flip-flops (A, B, and C), as described by the three input equations:

$$T_A = BC$$
,  $T_B = C$ ,  $T_c = 1$ .

Assume that each flip-flop has a propagation delay of 15ns, a setup time of 10ns, a hold time of 5ns, and the AND gate has a propagation delay of 5ns. Obtain the maximum clock frequency that the circuit can operate correctly (according to the state diagram).

(8%) Explain the purpose of the *carry lookahead* logic for a binary adder. Give the carry output of the second stage of a 4-bit adder as a function of input carry  $C_0$  and carry generate/propagate signals.

