Homework #7

5.1 The D latch of Fig. 5.6 is constructed with four NAND gates and an inverter. Consider the following three other ways for obtaining a D latch. In each case, draw the logic diagram and verify the characteristic table for each.

(b) Use only NOR gates.

5-11

5.2 Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter.

5-23

5.6 A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is specified by the following next-state and output equations (HDL—see Problem 5.35):

$$A(t+1) = xy' + xB$$
$$B(t+1) = xA + xB'$$
$$z = A$$

(a) Draw the logic diagram of the circuit.
(b) List the state table for the sequential circuit.
(c) Draw the corresponding state diagram.

5.8* Derive the state table and the state diagram of the sequential circuit shown in Fig. P5.8. Explain the function that the circuit performs.

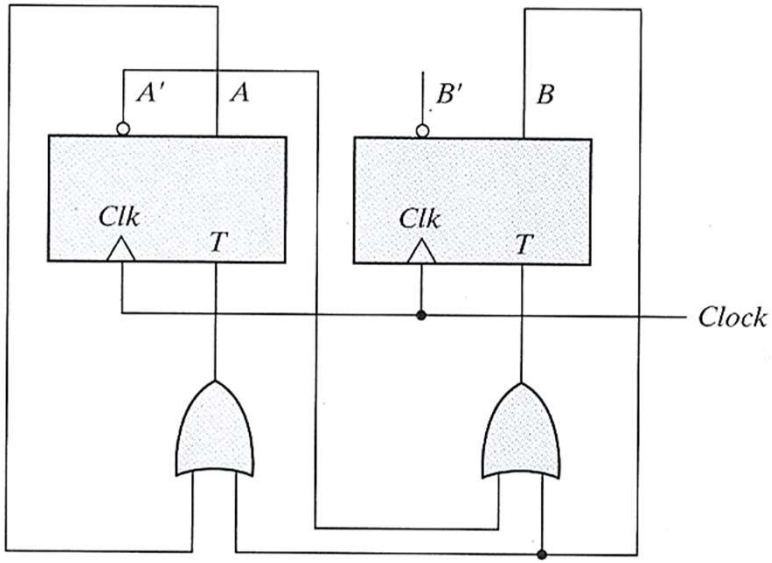


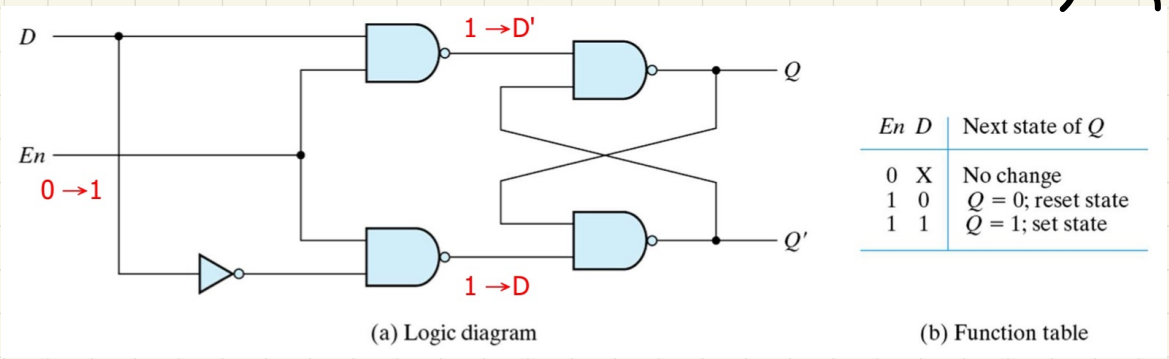
FIGURE P5.8

5.10 A sequential circuit has two *JK* flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are

$$J_A = Bx + B'y' \qquad K_A = B'x + y$$
$$J_B = A'x \qquad K_B = A + xy'$$
$$z = (A + B)\,x'y'$$

(a) Draw the logic diagram of the circuit.
(b) Tabulate the state table.

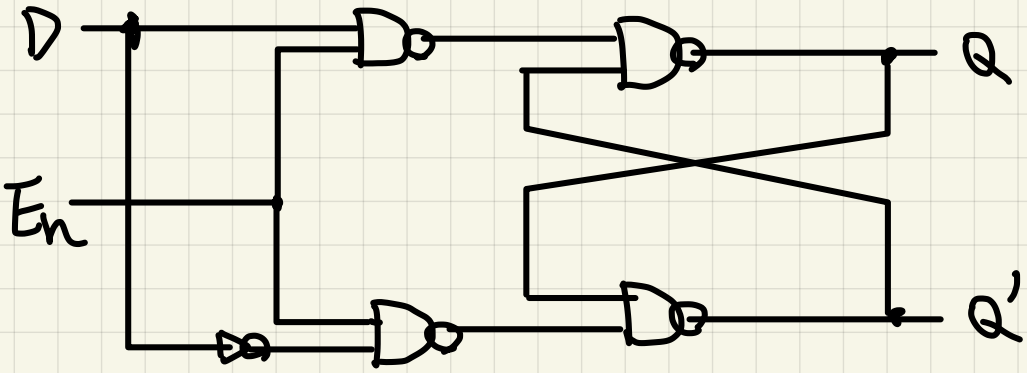
5-1

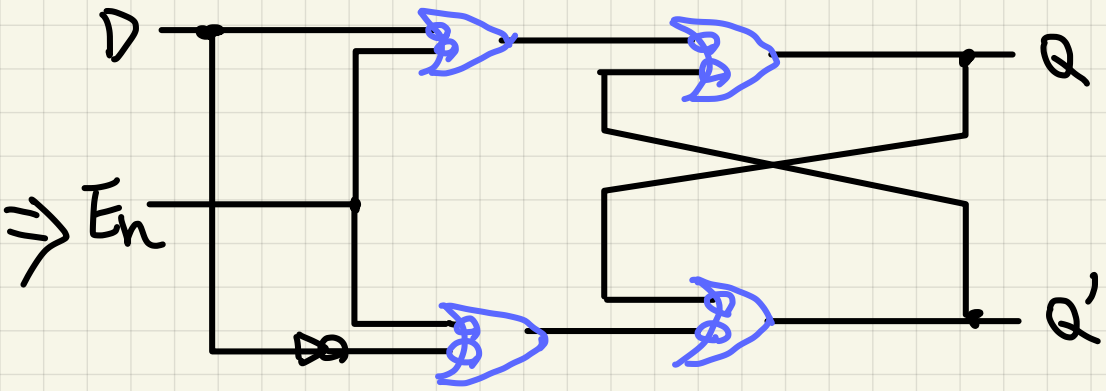


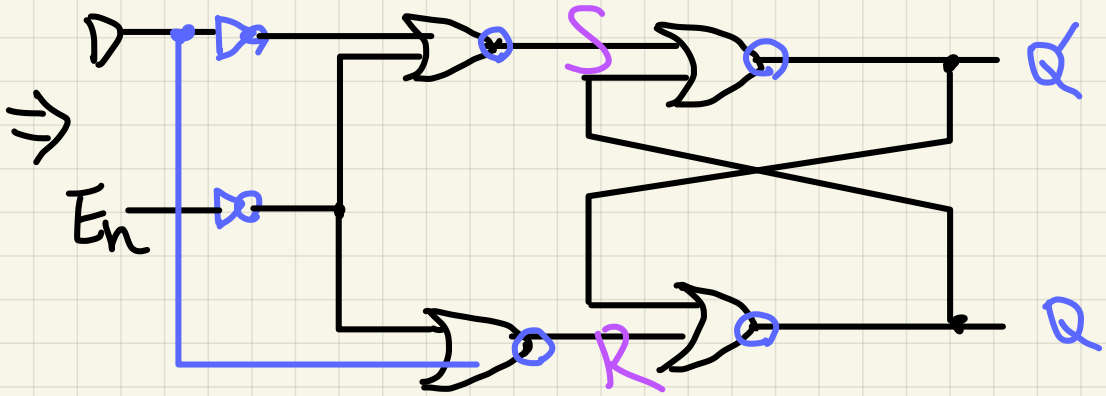
(a) Logic diagram

En	D	Next state of Q
0	X	No change
1	0	Q = 0; reset state
1	1	Q = 1; set state

(b) Function table



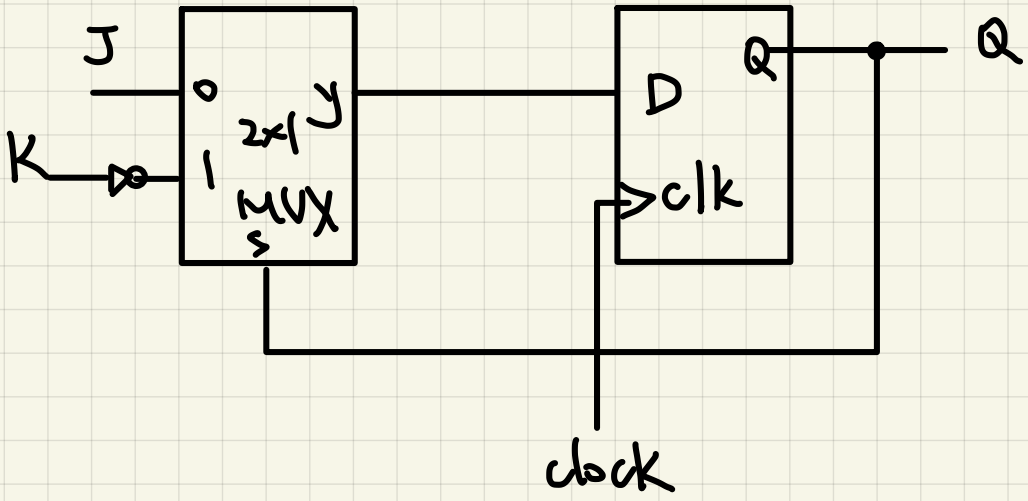




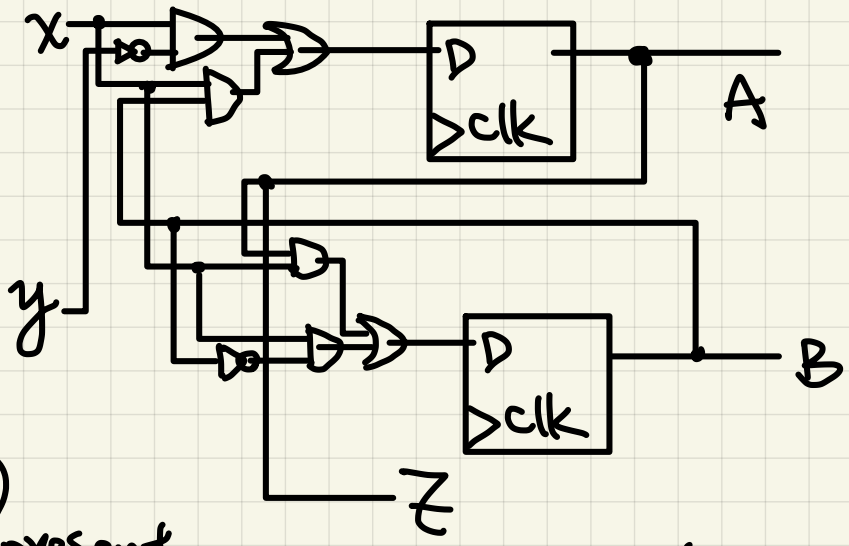
state table

En	D	S	R	next Q
0	X	0	0	no change
1	0	0	1	Q=0 (reset)
1	1	1	0	Q=1 (set)

5.2



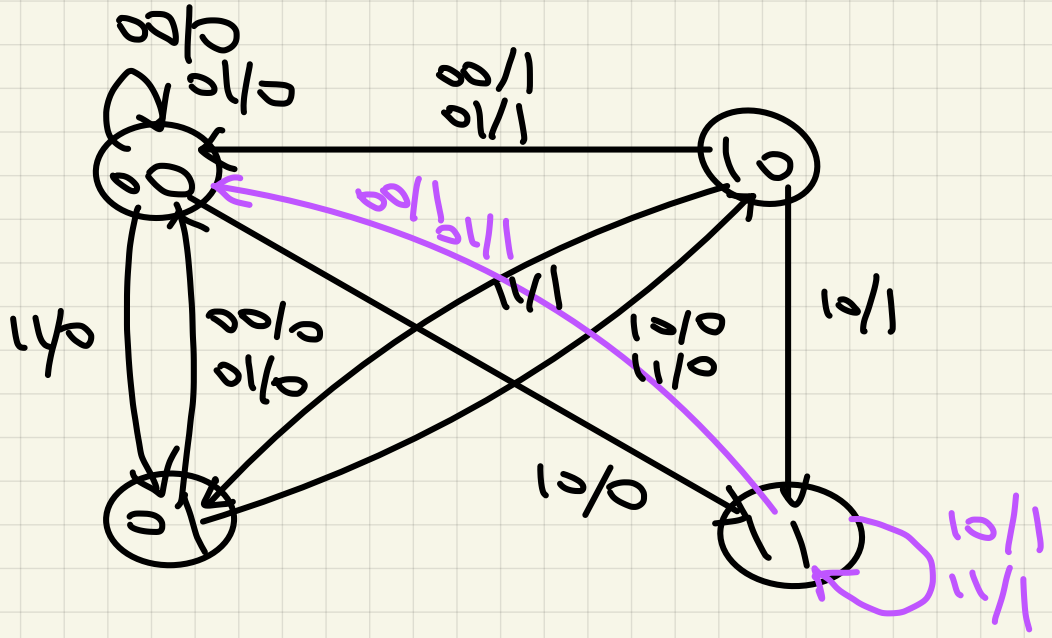
5.6 (a)



(b)

present				next		
A	B	x	y	A	B	Z
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	0	0
1	1	0	1	0	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

(c)



5.8 $T_A = \cancel{AB}$ A+B

$T_B = \cancel{A'B}$ A'+B

$A(t+1) = A(t) \oplus T_A$

$B(t+1) = B(t) \oplus T_B$

present A	present B	T_A	T_B	next A	next B
0	0	0	1 → 0	0	0
0	1	0 → 1	0	0	1
1	0	1	1 → 0	0	0
1	1	1	0	1	1

no change

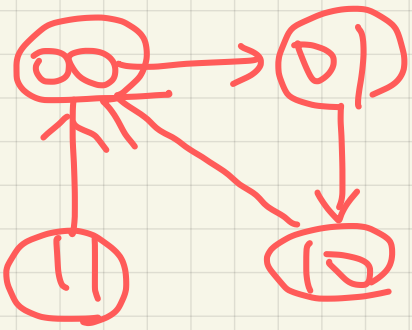
reset

set

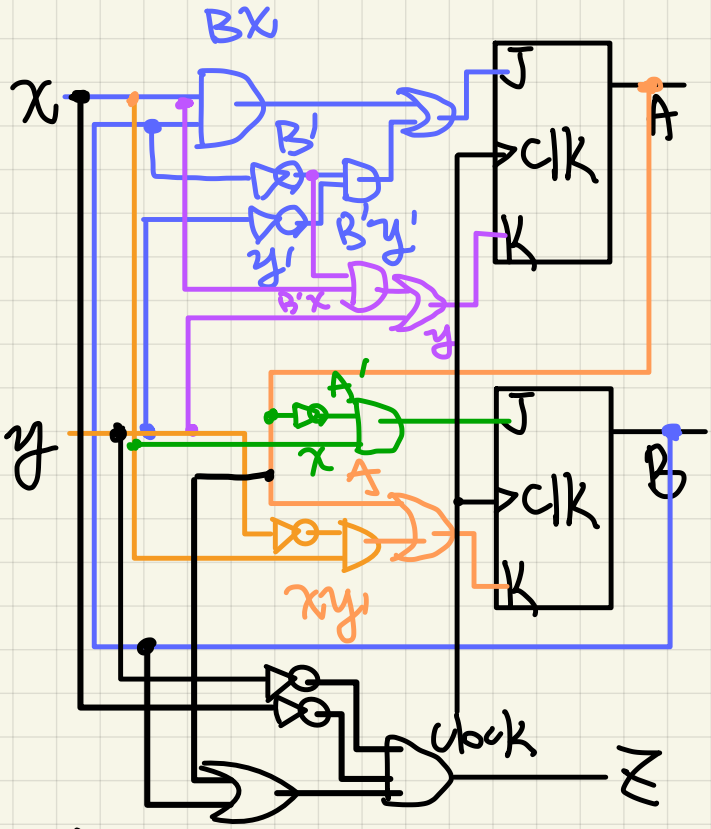
reset

set

0 → 01 → 10 → 00



5.10(a)



5.10(b)

present				next			J_A	K_A	J_B	K_B
A	B	x	y	A	B	Z				
0	0	0	0	0	1	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	1
0	0	1	0	0	1	0	0	0	1	0
0	0	1	1	1	0	0	1	1	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	1	0	0	0	0	0	0	1
0	1	1	0	1	1	0	1	1	1	0
0	1	1	1	1	0	0	1	1	0	1
1	0	0	0	1	1	0	1	0	1	0
1	0	0	1	1	0	0	1	0	0	1
1	0	1	0	1	1	0	1	0	1	0
1	0	1	1	0	0	1	0	1	0	1
1	1	0	0	1	1	0	1	0	1	0
1	1	0	1	1	0	0	1	0	0	1
1	1	1	0	1	1	0	1	0	1	0
1	1	1	1	0	0	1	0	1	0	1