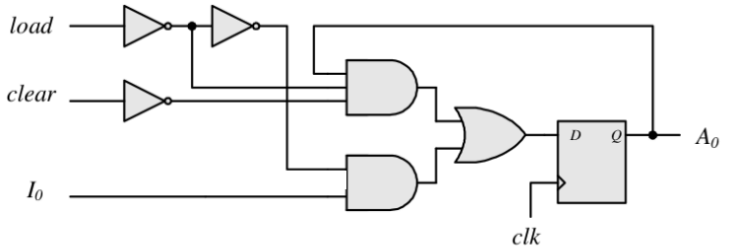
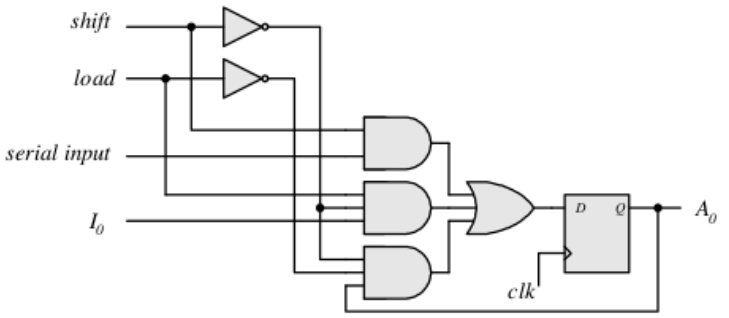
**6.2** Modify Fig. 6.2, with each stage replicating the first stage shown below:




| *Load* | *Clear* | *D* | *Operation* |
|---|---|---|---|
| *0* | *0* | $A_0$ | *No change* |
| *0* | *1* | *0* | *Clear to 0* |
| *1* | *x* | $I_0$ | *Load input* |

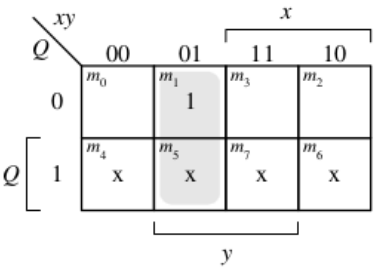
**6.6** First stage of register:



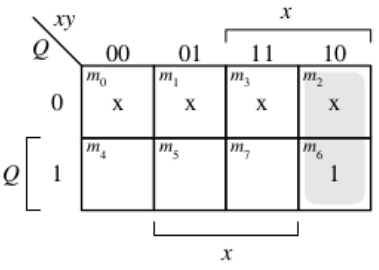
**6.9**

**(b)**

| Present state Q | Inputs x | y | Next state Q | Output D | FF inputs $J_Q$ | $K_Q$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | x |
| 0 | 0 | 1 | 1 | 1 | 1 | x |
| 0 | 1 | 0 | 0 | 1 | 0 | x |
| 0 | 1 | 1 | 0 | 0 | 0 | x |
| 1 | 0 | 0 | 1 | 1 | x | 0 |
| 1 | 0 | 1 | 1 | 0 | x | 0 |
| 1 | 1 | 0 | 0 | 0 | x | 1 |
| 1 | 1 | 1 | 1 | 1 | x | 0 |

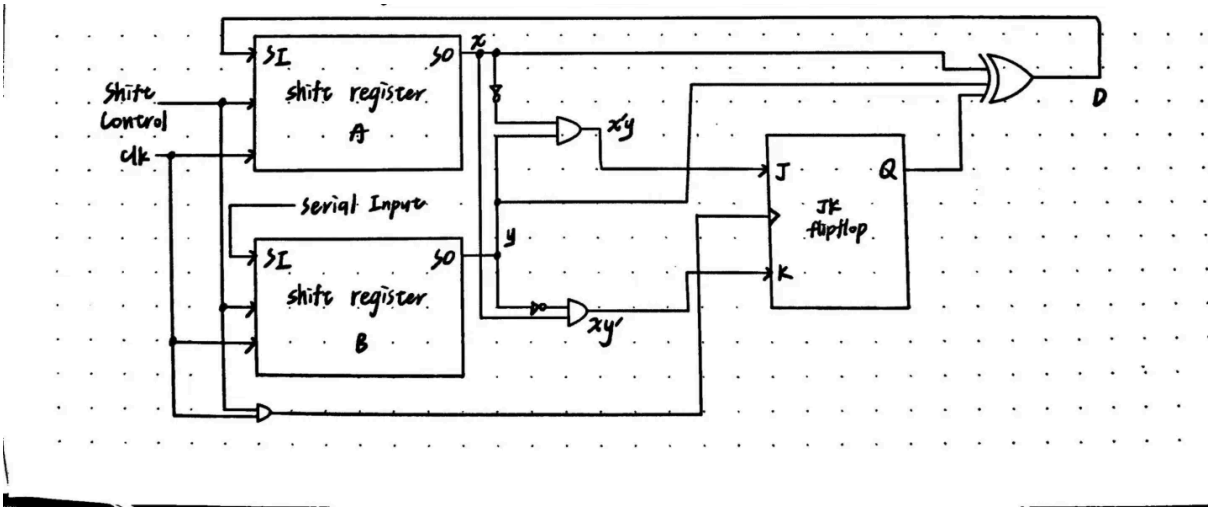



$J_Q = x'y$




$K_Q = xy'$

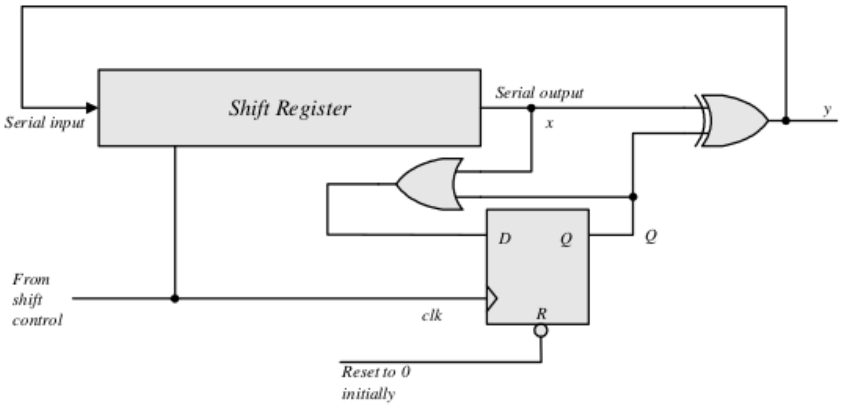
$D = Q \oplus x \oplus y$



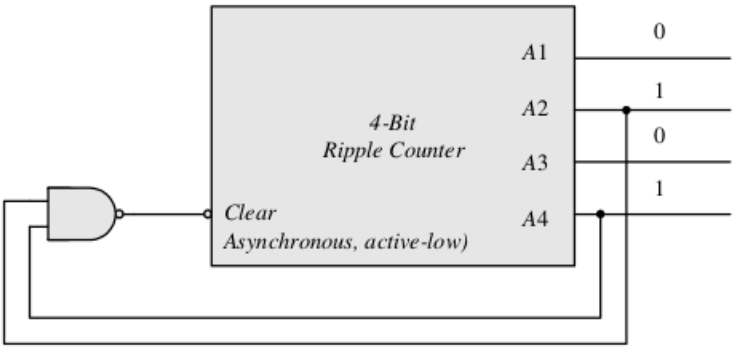
**6.10** See solution to Problem 5.7.

Note that y = x if Q = 0, and y = x' if Q = 1. Q is set on the first 1 from x.

Note that x ⊕ 0 = x, and x ⊕ 1 = x'.



**6.13**


A1
A2
A3
A4
4-Bit
Ripple Counter
Clear
Asynchronous, active-low)
0
1
0
1