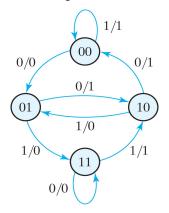
## Department of Computer Science National Chiao Tung University

## **Digital System Design**

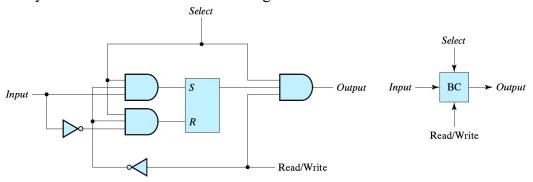
Final Exam

1/17/2013

- 1. (10%) Design a JK flip-flop with a T flip-flop.
- 2. (10%) Derive the state diagram of a circuit that will generate a Gray code sequence for an input binary sequence. The circuit can be reset asynchronously to start and end the operation. (Note that for an m-bit binary sequence,  $a_{m-1}$ ,  $\cdots$   $a_0$ , its Gray code representation,  $g_{m-1}$ ,  $\cdots$   $g_0$ , can be determined by:  $g_{m-1} = a_{m-1}$  and  $g_i = a_i \oplus a_{i+1}$  for  $i \le m-2$ .)
- 3. (12%) Consider the state diagram shown below. Design a sequential circuit with D flip-flops A and B, with one input x and one output y.



4. (10%) Consider the SRAM memory cell shown below. Show that we can connect four such cells to form a 4-bit shift register and describe how a 4-bit binary number can be store in such a register.



- 5. (8%) Include a clear input to the shift register discussed above.
- 6. (8%) Briefly explain advantages (and disadvantages) of using a ripple counter, versus a synchronous counter, as a binary counter.
- 7. (8%) Construct a mod-14 counter with a four-bit binary synchronous counter with parallel load, and a logic gate.

- 8. (8%) Briefly describe how 64K×8 RAM chips should be connected to provide a memory capacity of 256K bytes. You may use a block diagram to explain.
- 9. (8%) Derive the Hamming code word for the 12-bit data: 001110011011.
- 10. (10%) Find different ways of using a PLA to implement the following functions if only four product terms (AND gates) are allowed. (There is no need to provide the PLA programming table.)

$$F_1(A,B,C) = \sum (0,2,3,6),$$
  
 $F_2(A,B,C) = \sum (2,4,5,7)$ 

- 11. (8%) Specify the minimum size of a ROM that will accommodate the truth table for each of the following combinational circuit components. You may use an additional gate to reduce the ROM size.
  - (a) a code converter that converts a decimal digit from the 2421 code to the Excess-3 code, with  $d(w,x,y,z) = \sum (5,6,7,8,9,10)$ .
  - (b) a binary multiplier that multiplies two 8-bit binary words.