Homework #9

6.2 Include a synchronous clear input to the register of Fig. 6.2. The modified register will have a parallel load capability and a synchronous clear capability. The register is cleared synchronously when the clock goes through a positive transition and the clear input is equal to 1.

6.6 Design a four-bit shift register with parallel load using *D* flip-flops. There are two control inputs: *shift* and *load*. When *shift* = 1, the content of the register is shifted by one position. New data are transferred into the register when *load* = 1 and *shift* = 0. If both control inputs are equal to 0, the content of the register does not change.

6.9 Two ways for implementing a serial adder $(A + B)$ is shown in Section 6.2. It is necessary to modify the circuits to convert them to serial subtractors $(A - B)$.

(b) *Using the circuit of Fig. 6.6, show the changes needed by modifying Table 6.2 from an adder to a subtractor circuit.

6.10 Design a serial 2's complementer with a shift register and a flip-flop. The binary number is shifted out from one side and it's 2's complement shifted into the other side of the shift register.

6.13 Show that a BCD ripple counter can be constructed using a four-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010.