數位邏輯設計

6.1 Registers

主講者：吳順德

國立臺灣師範大學機電工程系 副教授

Registers & Counters

- Clocked sequential circuits

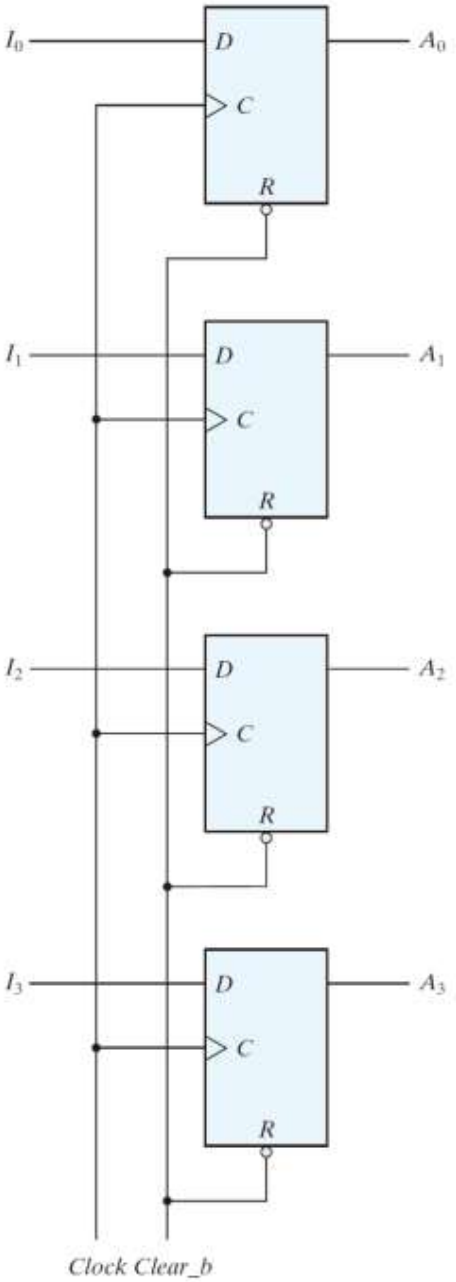
  Flip-flops + Combinational gates

  (essential) (optional)

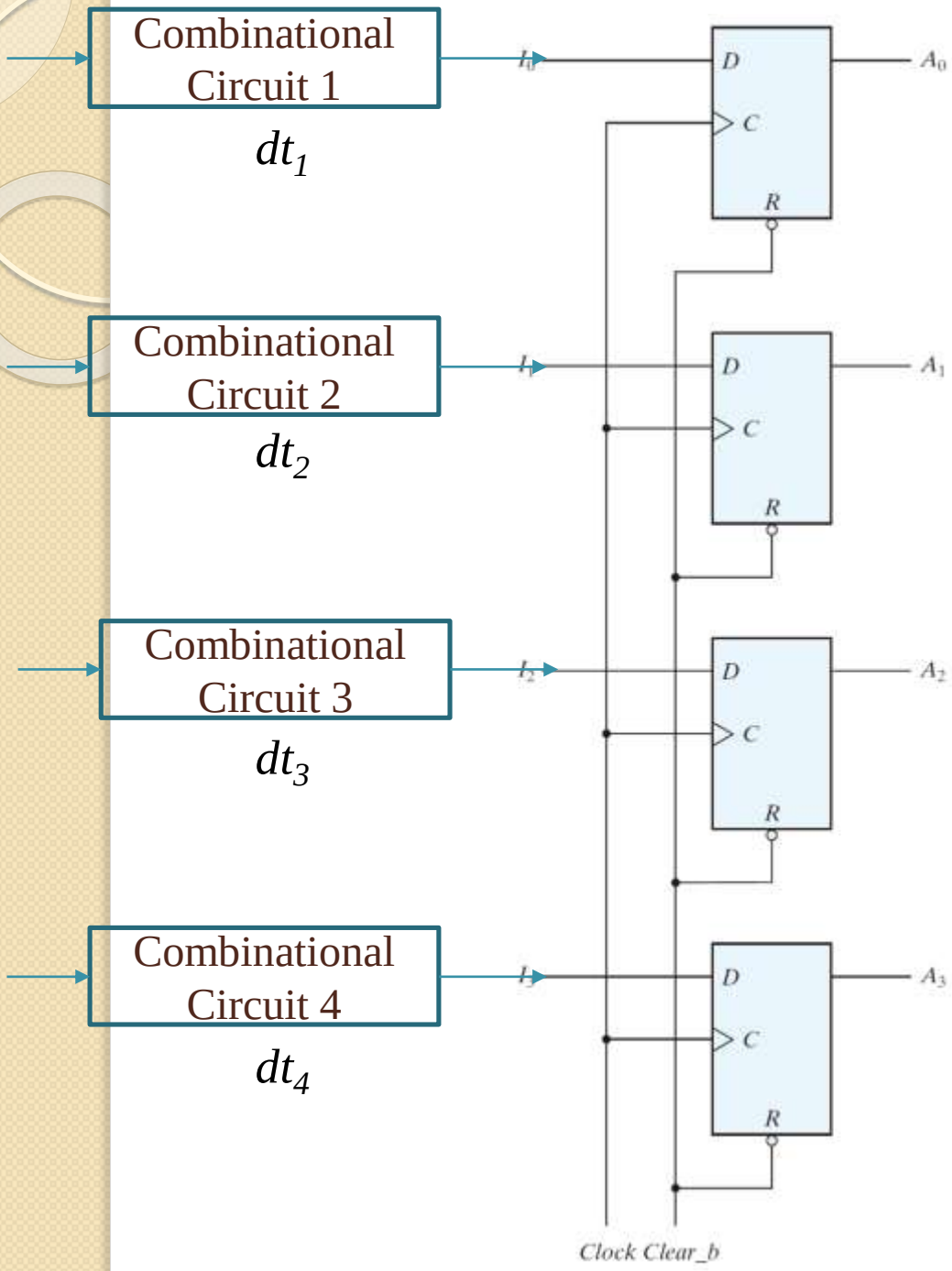
- Register:
  - a group of flip-flops that holds the binary information.
- Counter:
  - a register that goes through a predetermined sequence of states

n bits Register

- *Clear_b:*
  - reset all four flip flops.
- Clock:
  - Control data Trasfer

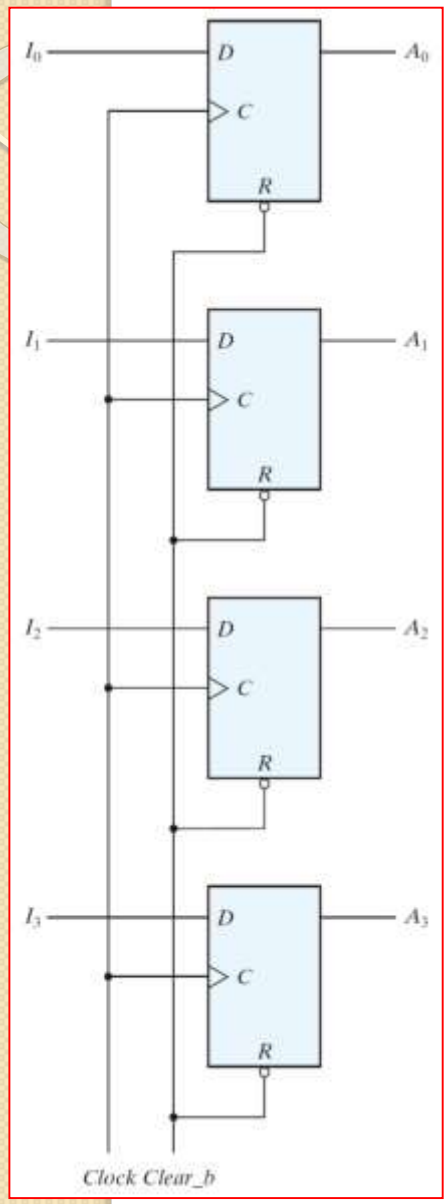


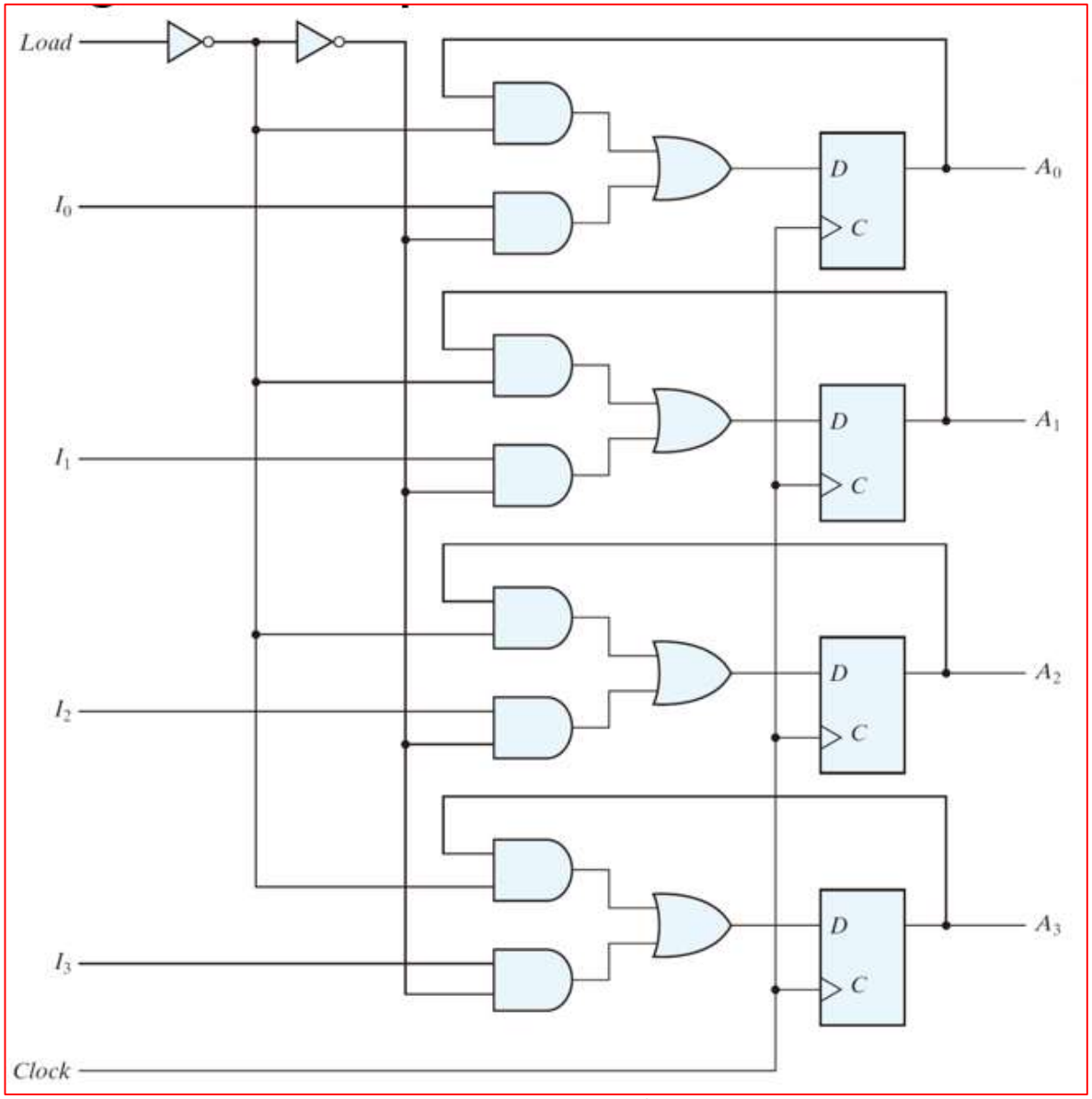
- *Clear_b:*
  - reset all four flip flops.
- Clock:
  - Control data Trasfer

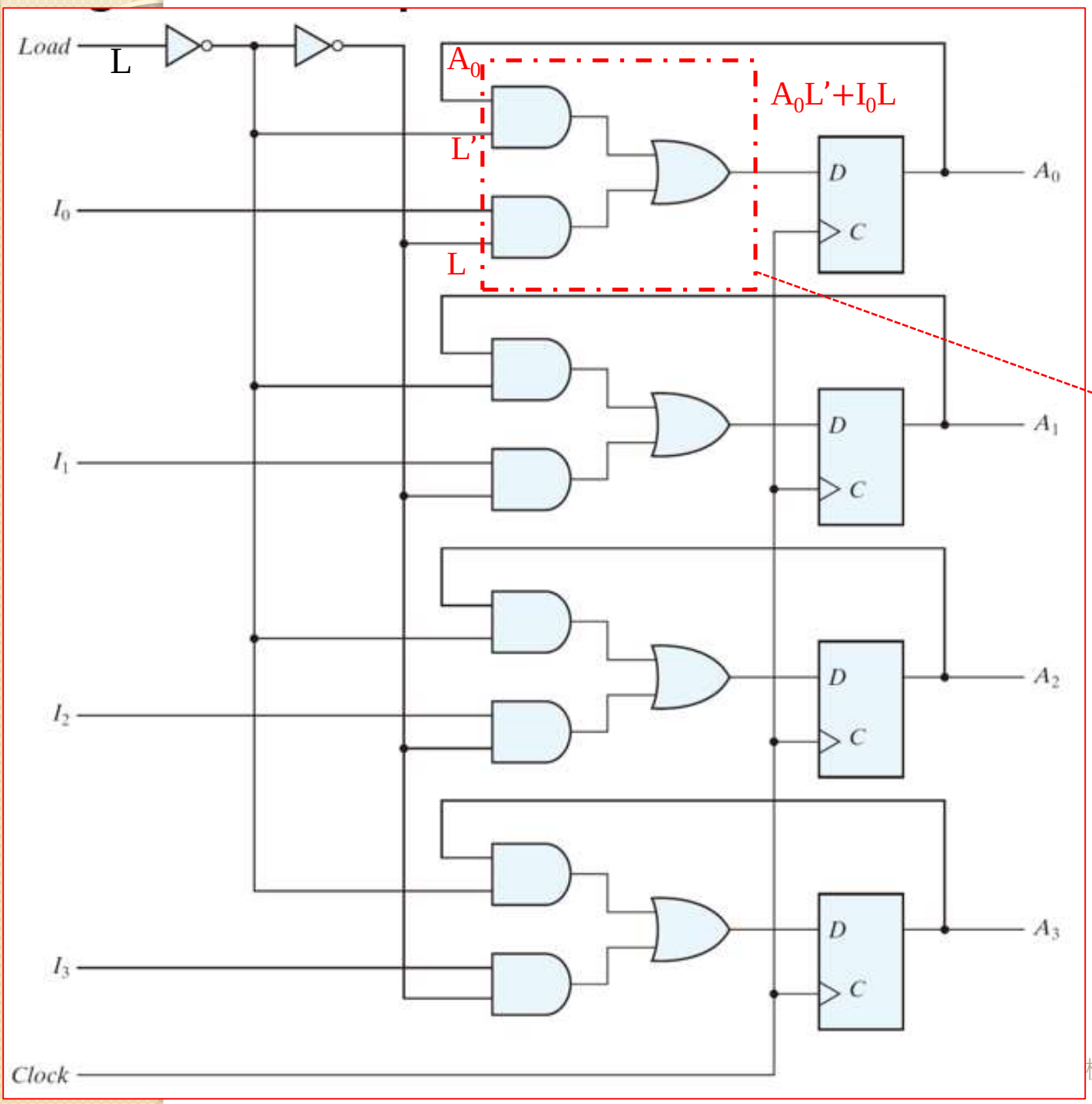


- Different delay time.
- Encountering problem when delay time large than the period of Clock signal.

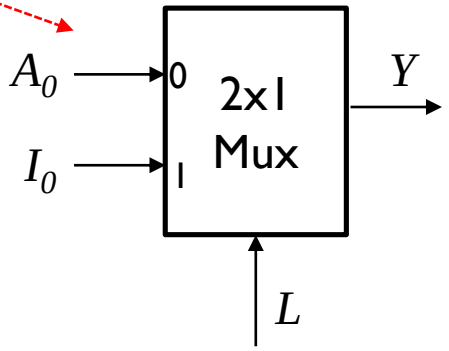
Register with Parallel Load





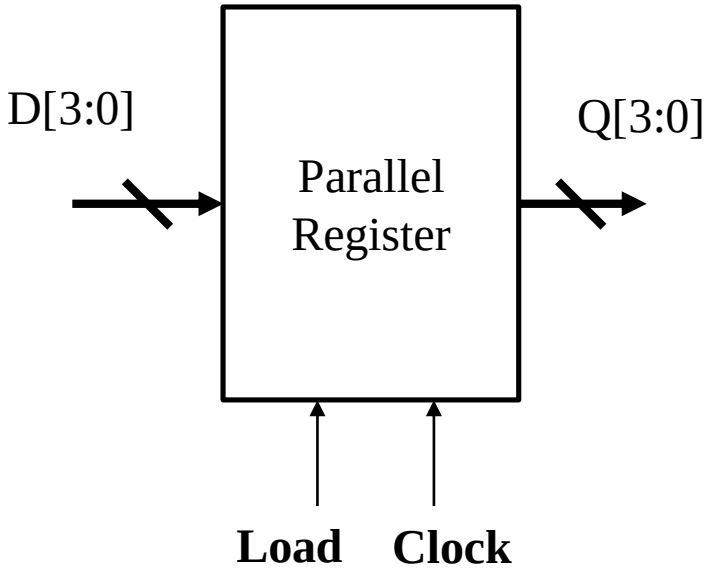


L	D	Q
0	A_0	A_0
1	I_0	I_0



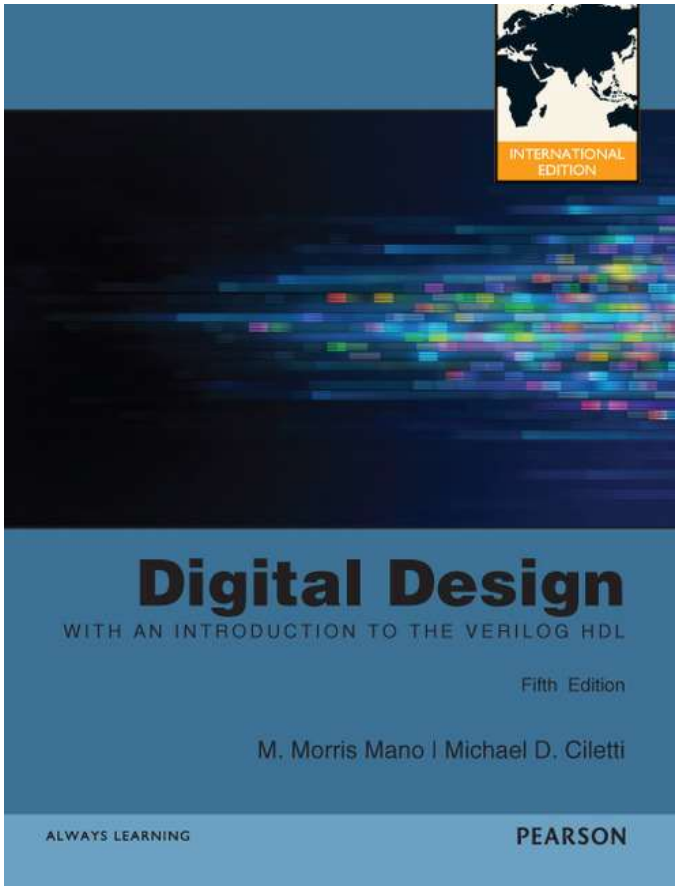
Outputs are controlled by both Clock and Load signals.

Symbol



Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



數位邏輯設計

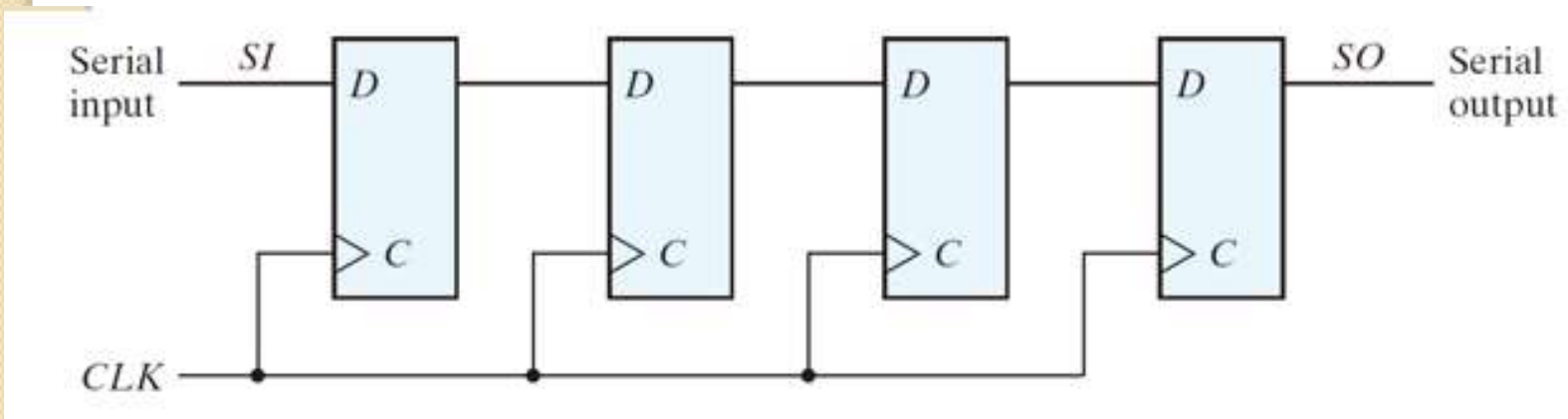
6.2.1 Shift Registers

主講者：吳順德

國立臺灣師範大學機電工程系 副教授

Shift Register

- Shift register
  - a register capable of shifting its binary information in one or both directions

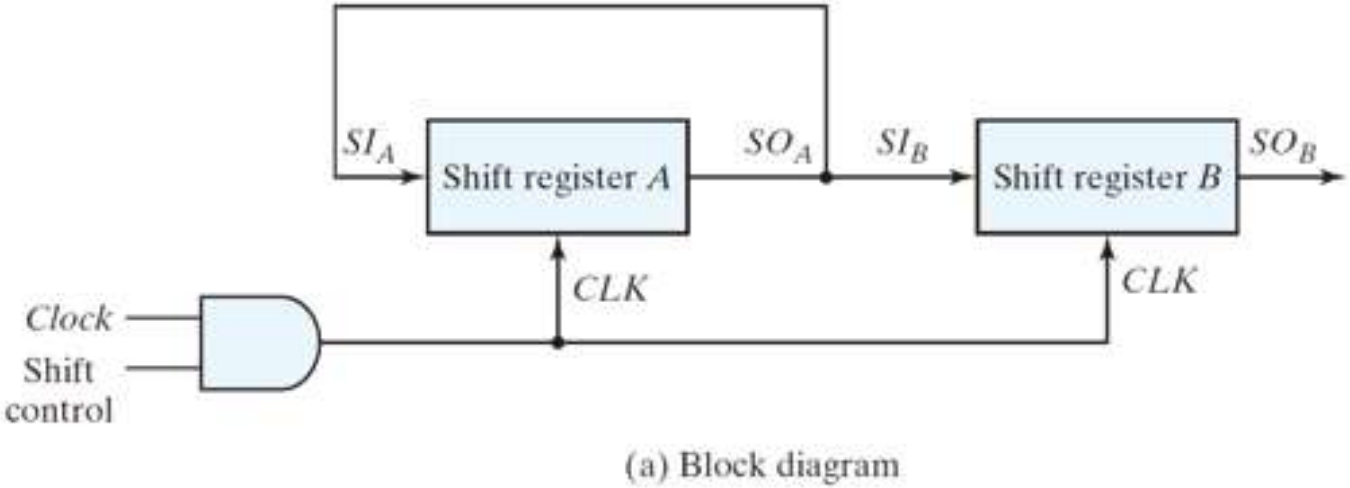


initial	1	0	1	1	0
CLK↑	1	1	0	1	1
CLK↑	1	1	1	0	1
CLK↑	1	1	1	1	0

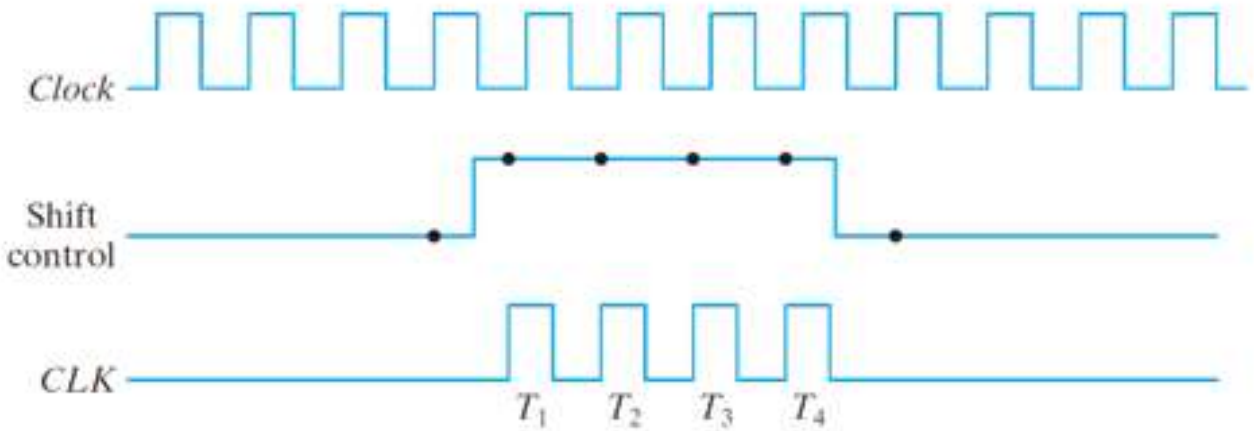
Serial Transfer vs. Parallel Transfer

- Serial transfer
  - Information is transferred one bit at a time
  - shifts the bits out of the source register into the destination register
- Parallel transfer:
  - All the bits of the register are transferred at the same time

Serial Transfer

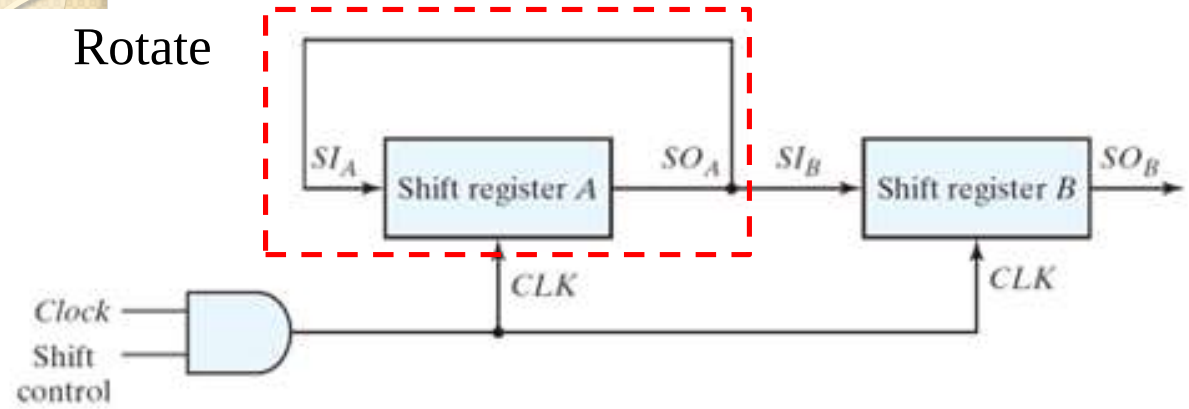


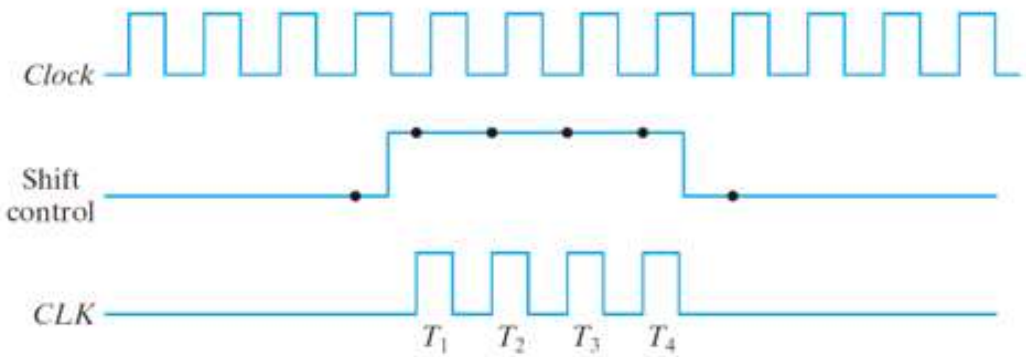
(a) Block diagram



(b) Timing diagram

Rotate



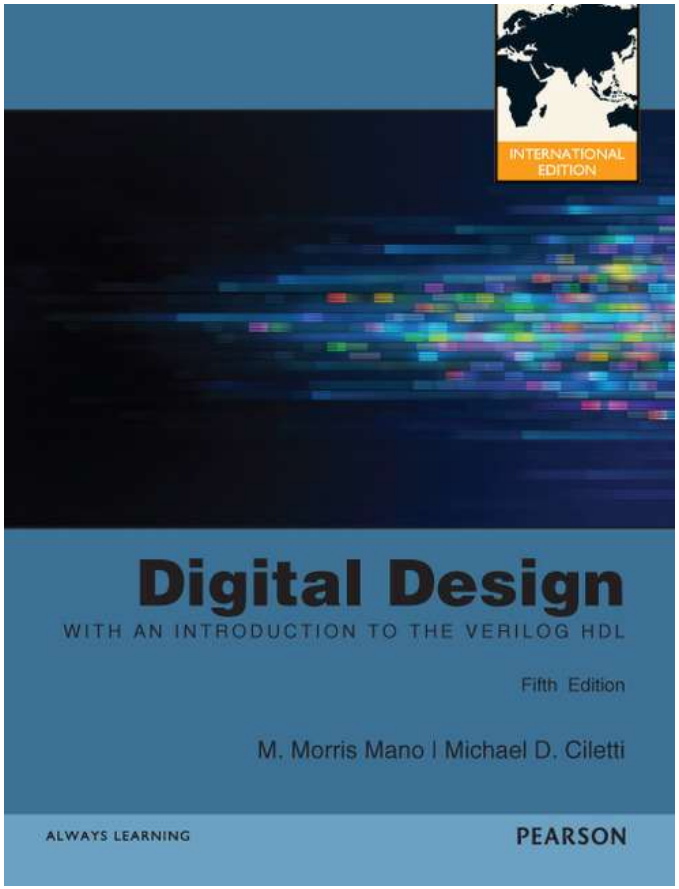


- The content of Register A are restored.
- The content of Register A are copy into Register B.

Timing Pulse	Shift Register *A*				Shift Register *B*			
Initial value	1	0	1	1	0	0	1	0
After T_1	1	1	0	1	1	0	0	1
After T_2	1	1	1	0	1	1	0	0
After T_3	0	1	1	1	0	1	1	0
After T_4	1	0	1	1	1	0	1	1

Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



數位邏輯設計

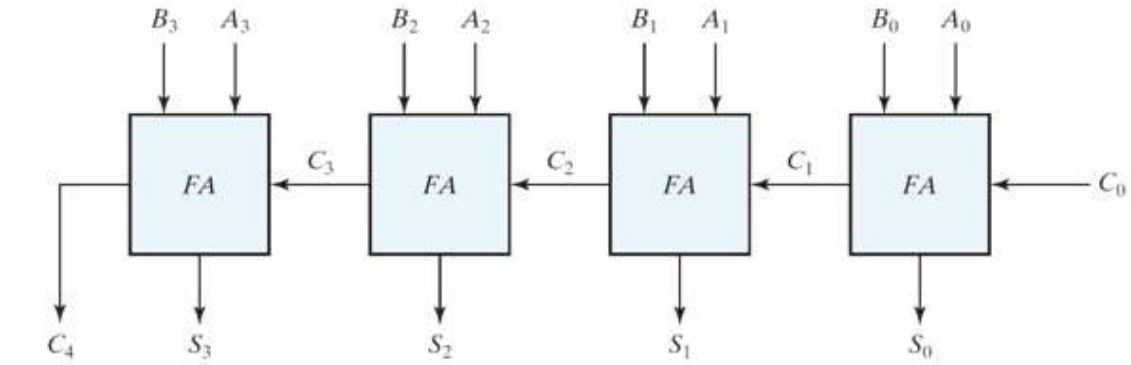
6.2.2 Shift Addition

主講者：吳順德

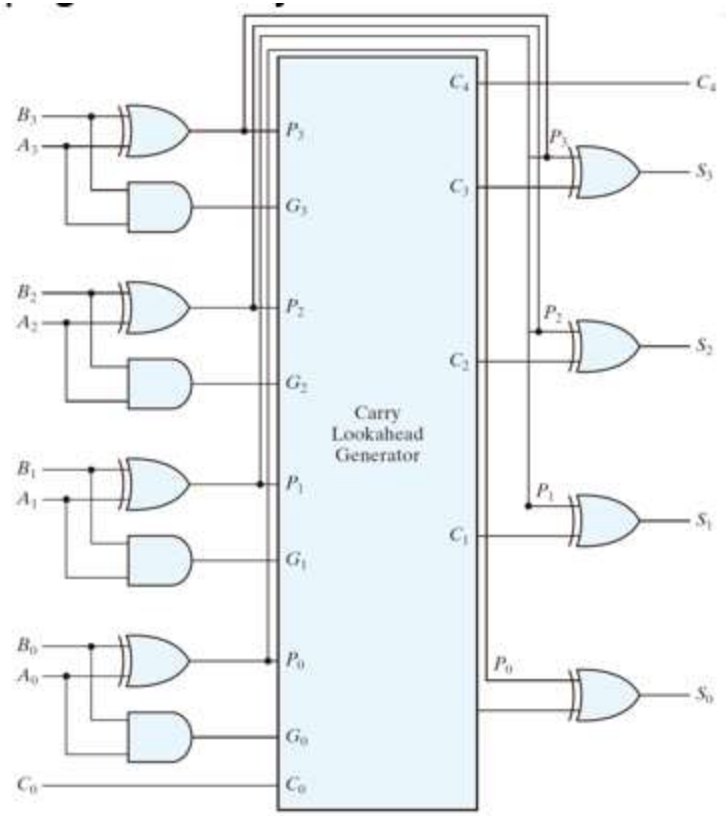
國立臺灣師範大學機電工程系 副教授

Recall: Parallel Addition

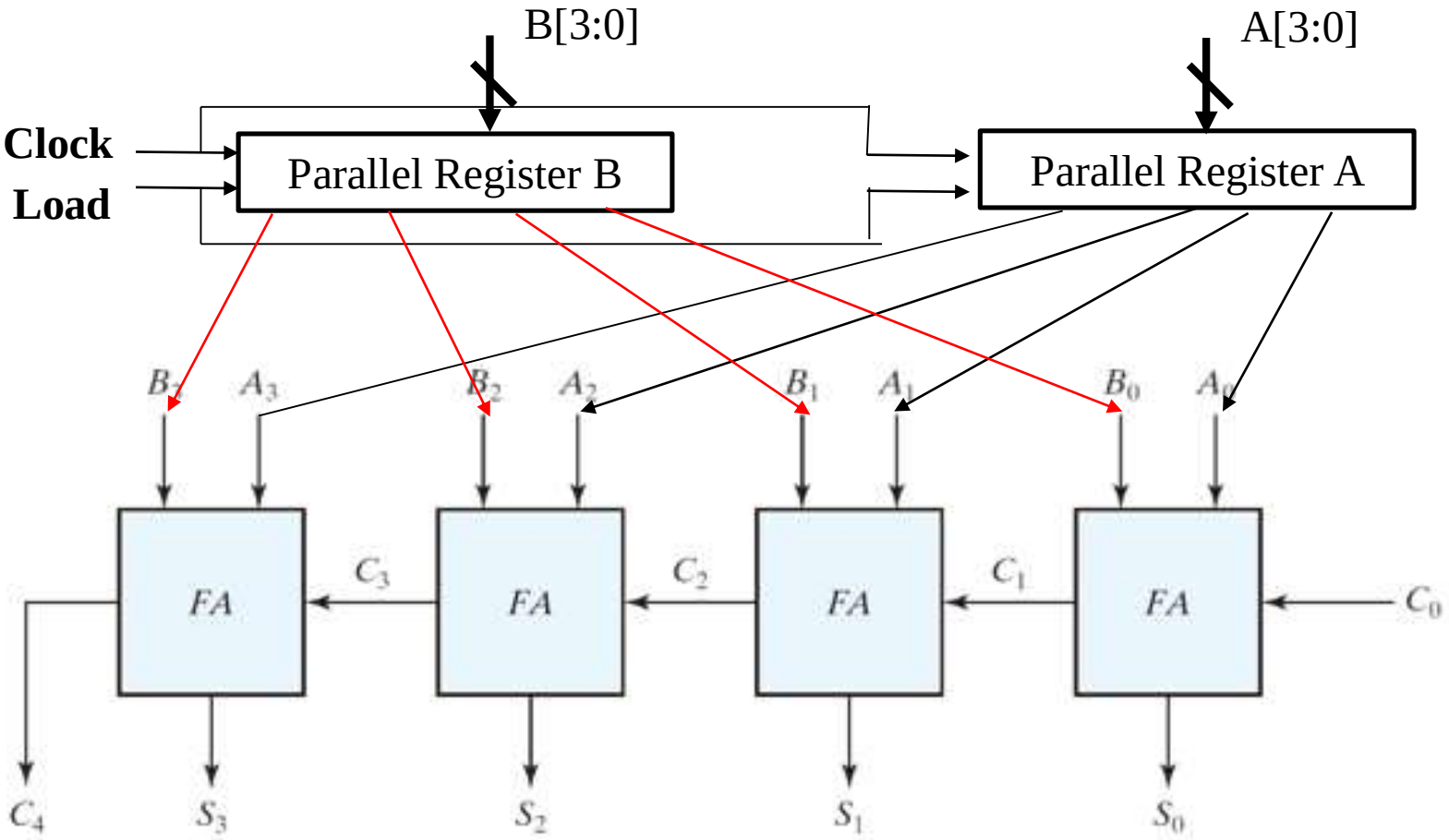
Ripple Carry Adder



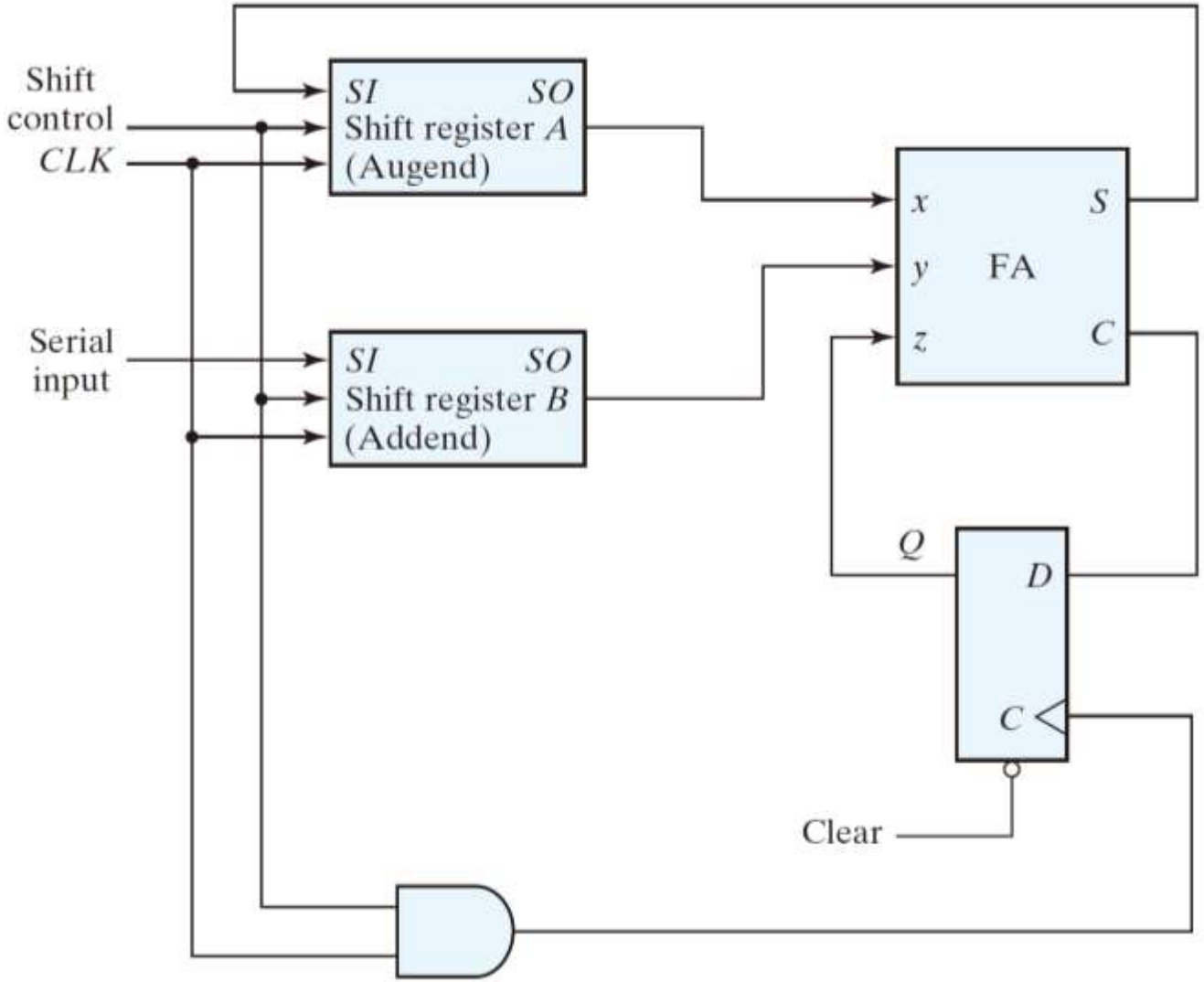
Carry Look Ahead Adder



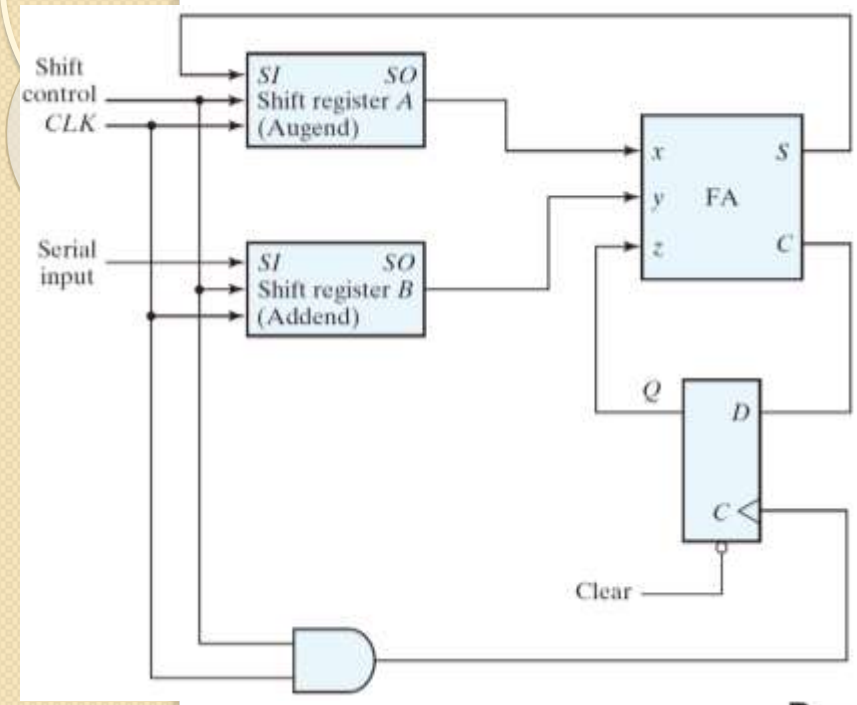
Recall: Parallel Addition



Serial Addition using D flip Flop



State Table For Serial Addition



$S = x \oplus y \oplus Q$

Present State		Inputs		Next State	Output
Q	Carry	x	y	Q	S
0		0	0	0	0
0		0	1	0	1
0		1	0	0	1
0		1	1	1	0
1		0	0	0	1
1		0	1	1	0
1		1	0	1	0
1		1	1	1	1

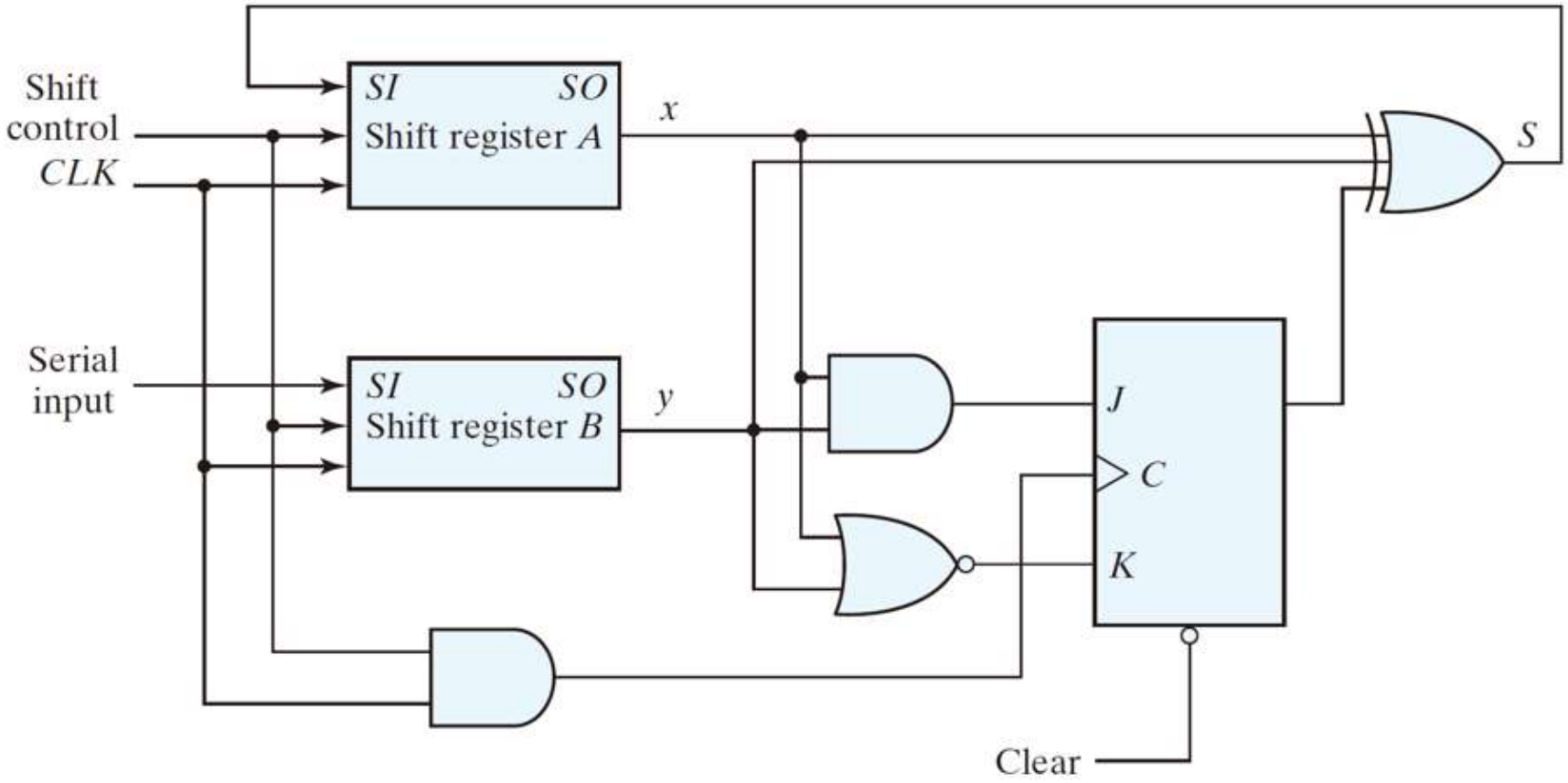
Serial Addition Using JK Flip Flop

Present State	Inputs		Next State	Output	Flip-Flop Inputs	
Q	x	y	Q	S	J_Q	K_Q
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

$$J_Q = x\,y$$
$$K_Q = x'\,y' = (x + y)'$$
$$S = x \oplus y \oplus Q$$

$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

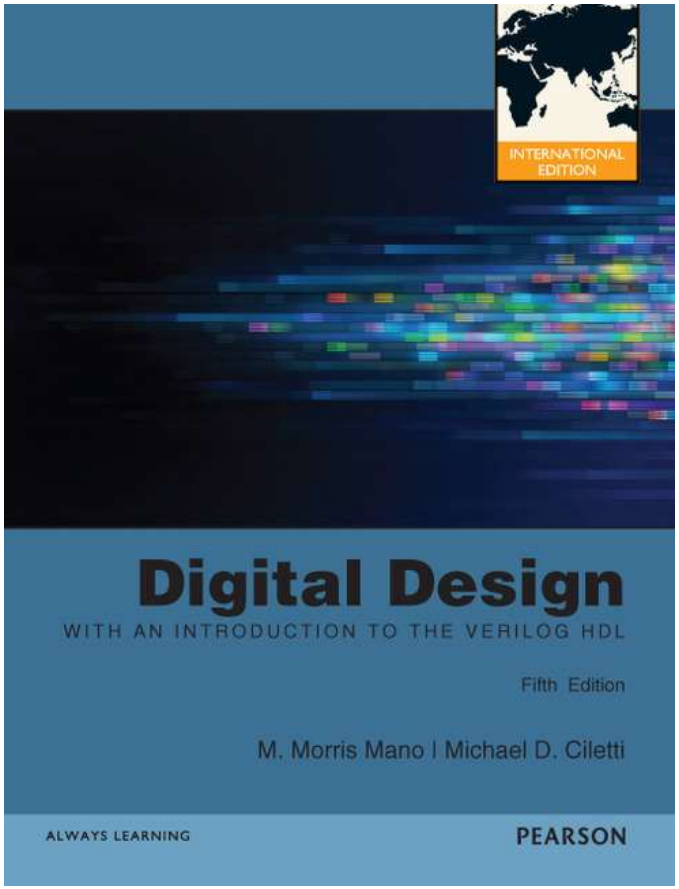
$$J_Q = x\,y$$
$$K_Q = x'\,y' = (x + y)'$$
$$S = x \oplus y \oplus Q$$



Reset Register A

Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



數位邏輯設計

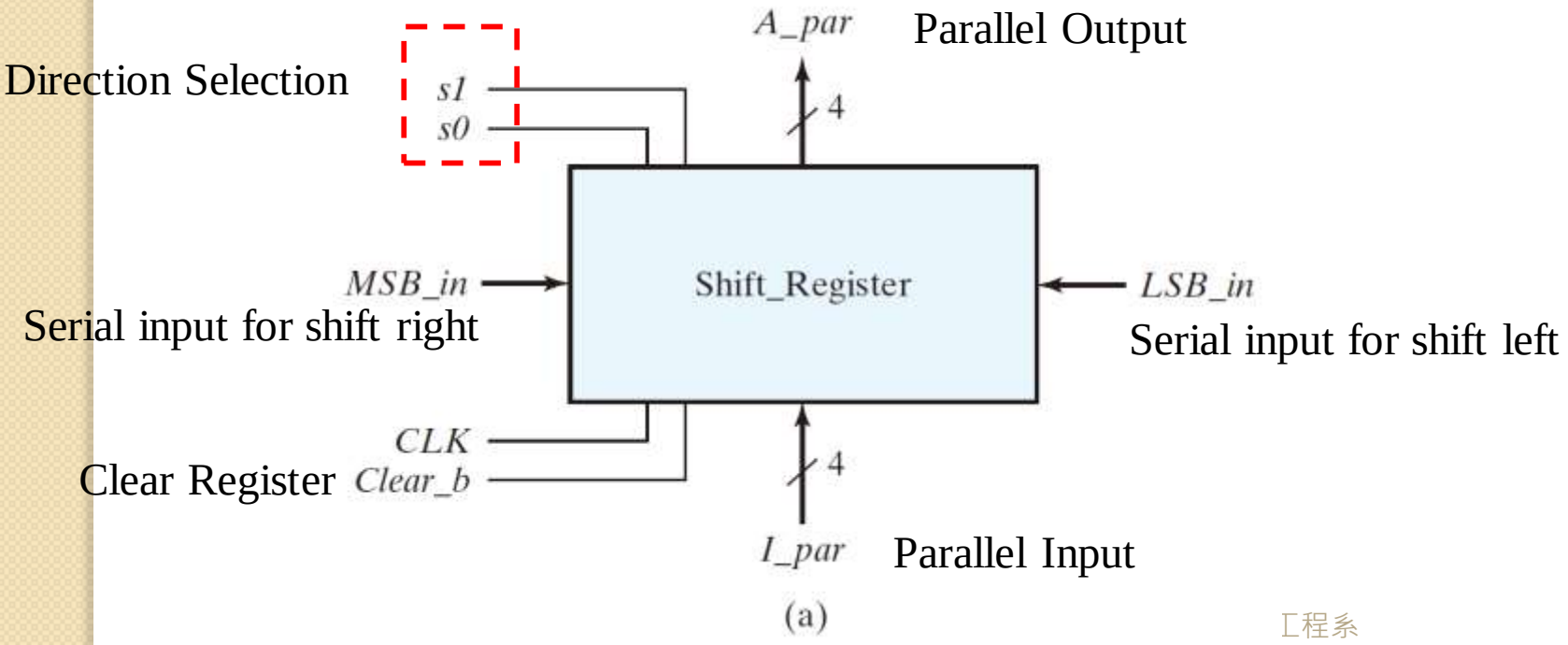
6.2.3 Universal Shift Register

主講者：吳順德

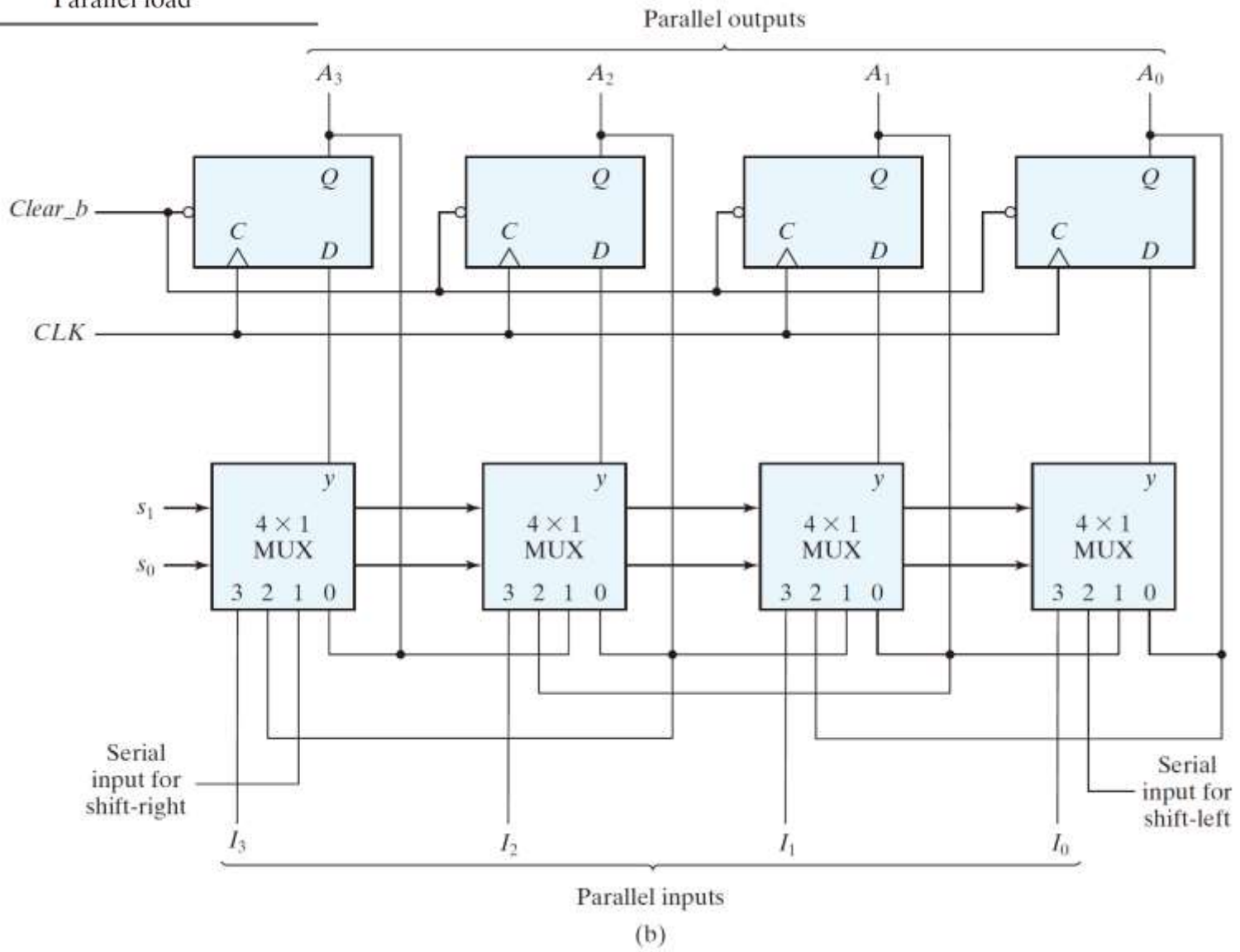
國立臺灣師範大學機電工程系 副教授

Universal Shift Register

- Universal shift register:
  - both direction shifts
  - parallel load/out capabilities
  - A clear control to clear the register to 0.



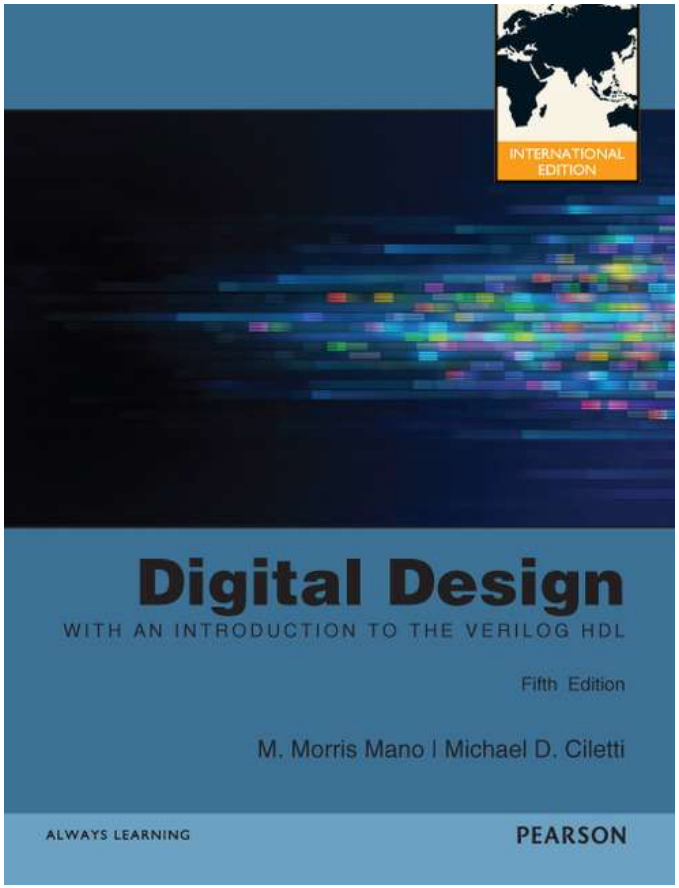
Mode Control		
s_1	s_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load



(b)

Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



數位邏輯設計

6.3.1 Counter

主講者：吳順德

國立臺灣師範大學機電工程系 副教授

Counter

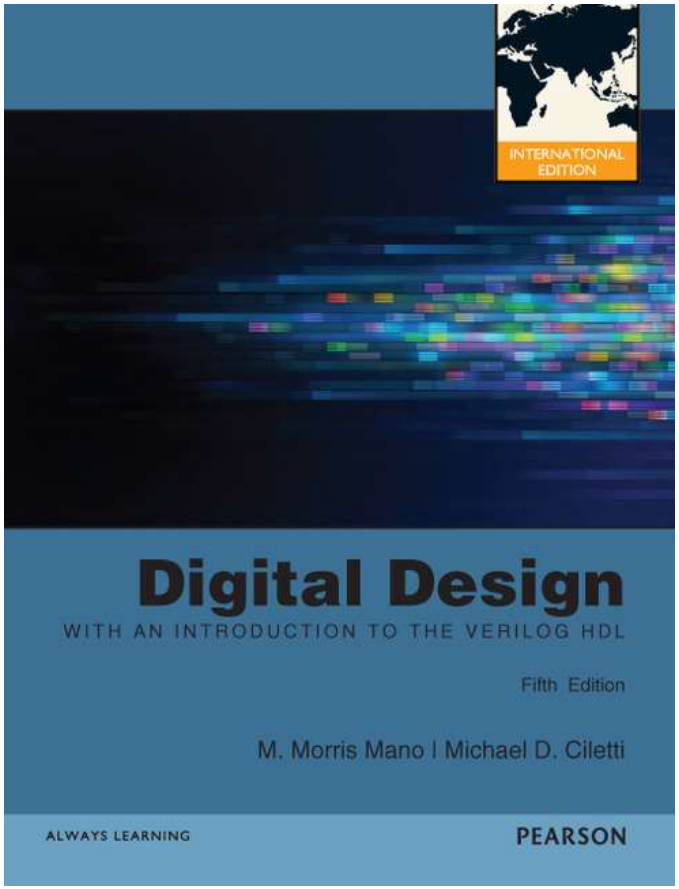
- Counter is a register that goes through a prescribed sequence of states upon the application of input pulses
- Input pulses:
  - may be clock pulses or originate from some external source
- The sequence of states:
  - follow the binary number sequence (Binary counter)
  - any other sequence of states

Categories of counters

- Ripple counters
  - The flip-flop output transition serves as a source for triggering other flip-flops.
  - no common clock pulse (not synchronous)
- Synchronous counters:
  - The CLK inputs of all flip-flops receive a common clock.

Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



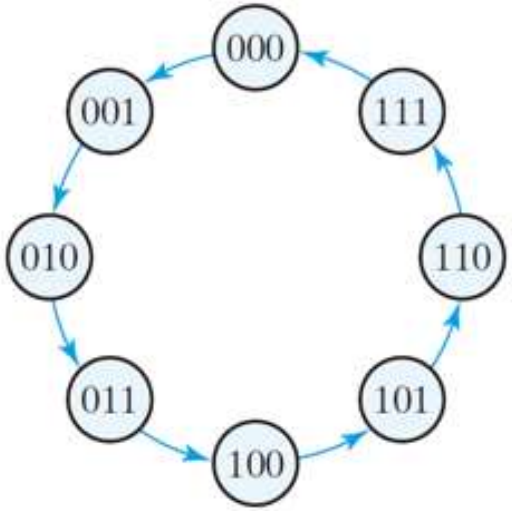
數位邏輯設計

6.3.2 Binary Ripple Counter

主講者：吳順德

國立臺灣師範大學機電工程系 副教授

Recall: 3 bits Binary Counter

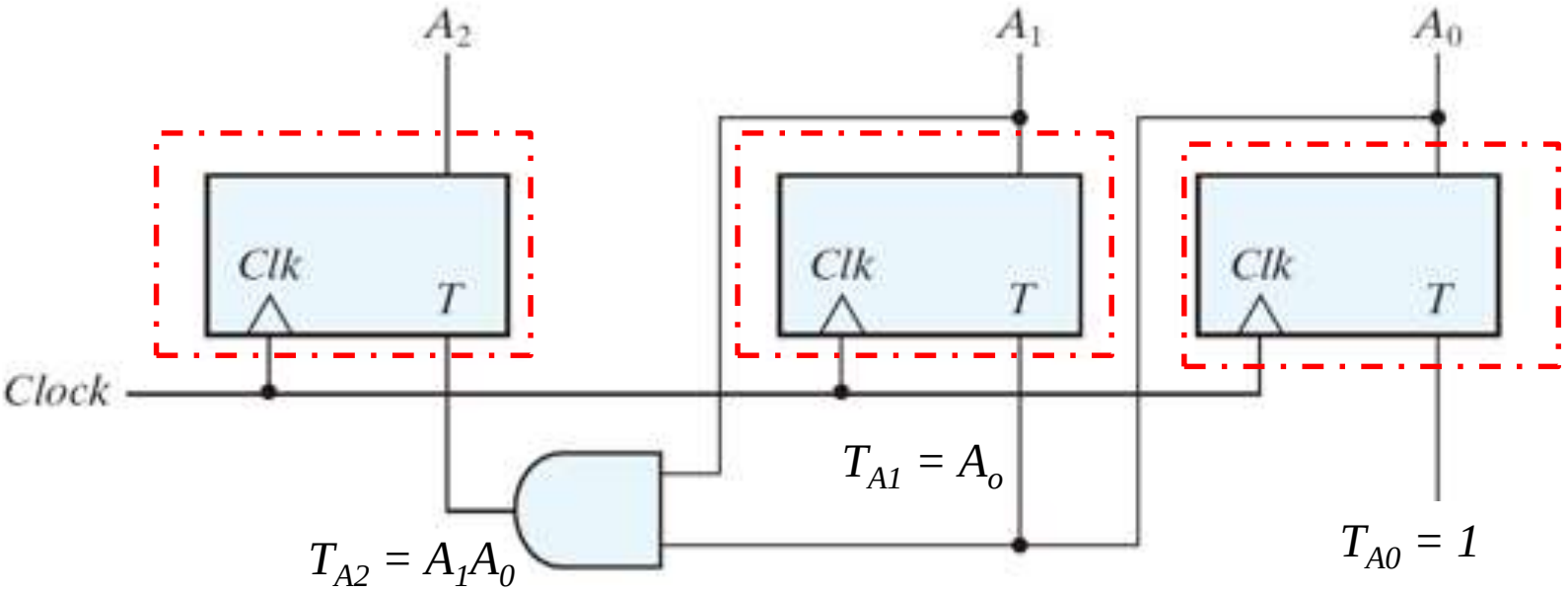


Present State			Next State		
A_2	A_1	A_0	A_2	A_1	A_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

$Q(t)$	$Q(t+1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

Present State			Next State			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	1	1
1	1	1	0	0	0	1	1	1

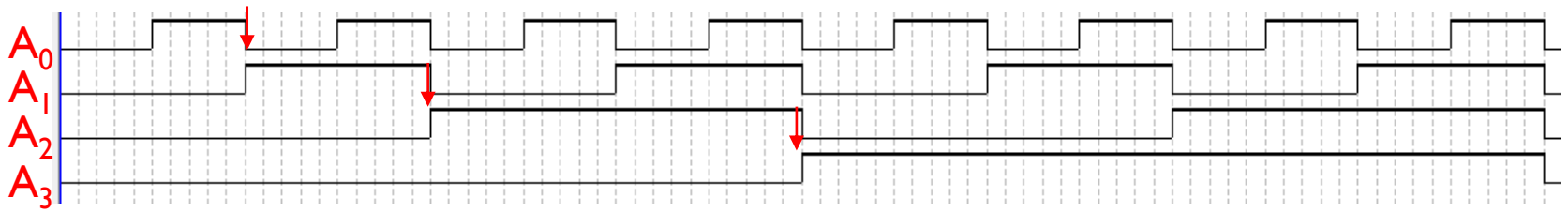
Recall: 3 bits Binary Counter



General Binary Ripple Counter

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0

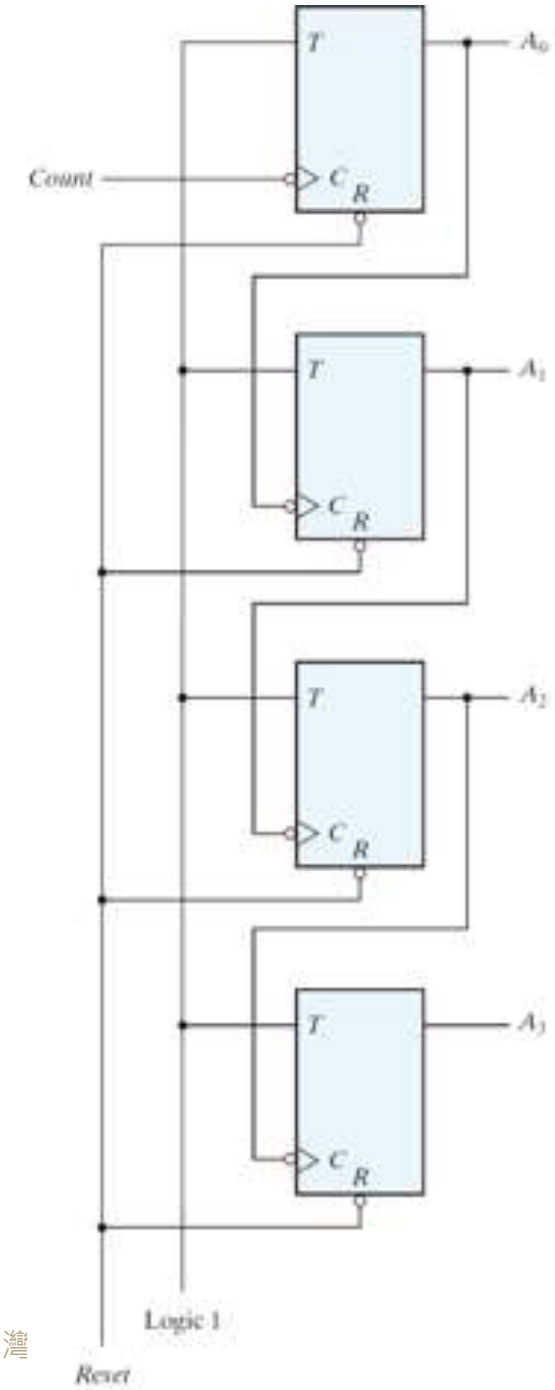
- Count: system clock.
- A_0 is complements with each Count pulse.
- A_1 is complements with each A_0 pulse.
- A_2 is complements with each A_1 pulse.
- A_3 is complements with each A_2 pulse.



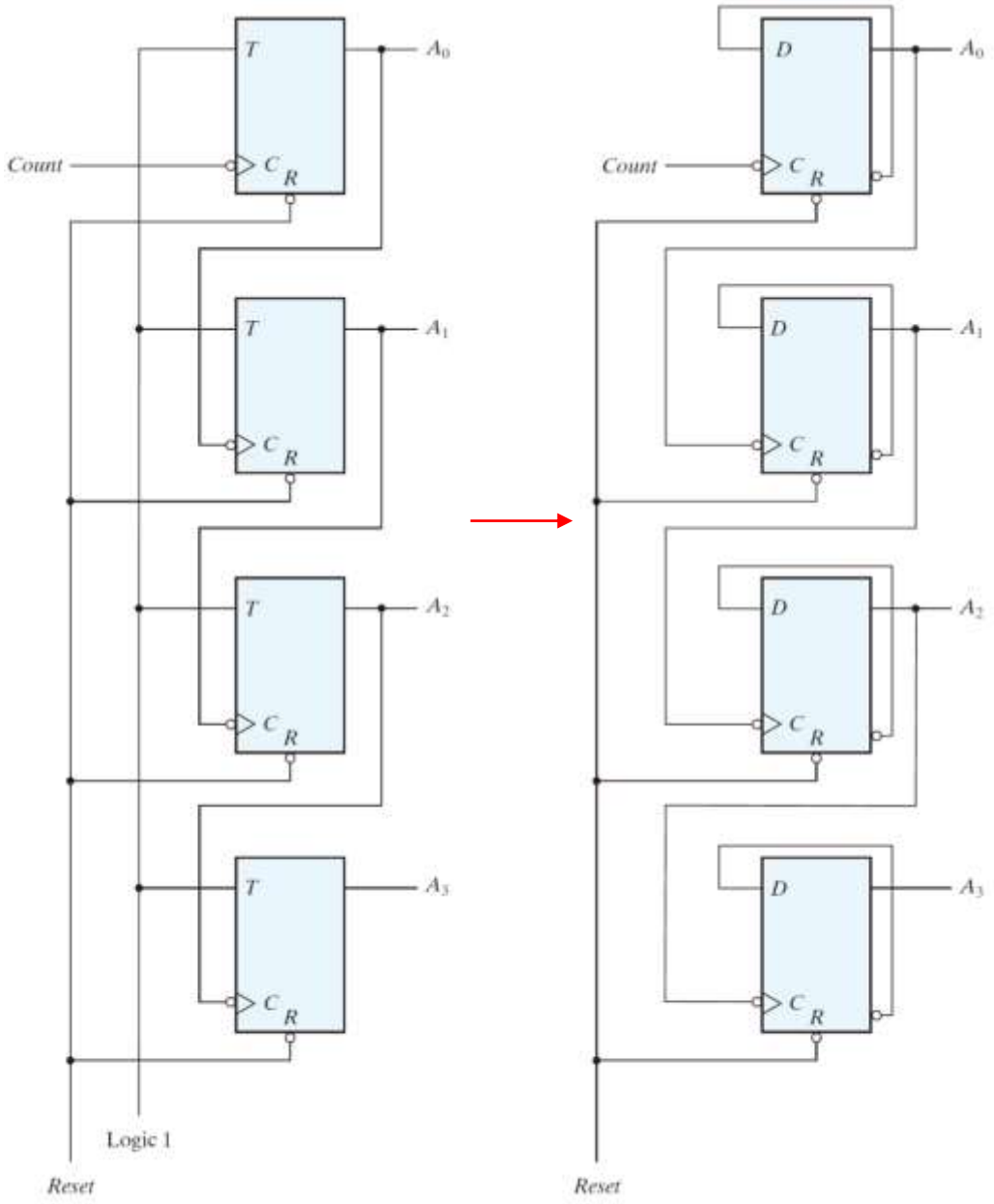
Negative edge triggered!

Binary Ripple Counter (T Flip Flop)

- Count: system clock.
- A_0 is complements with each Count pulse.
- A_1 is complements with each A_0 pulse.
- A_2 is complements with each A_1 pulse.
- A_3 is complements with each A_2 pulse.



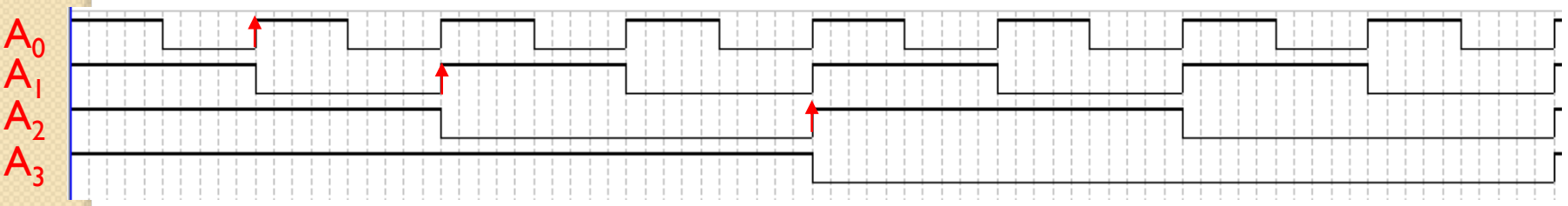
Binary Ripple Counter (D Flip Flop)



(a) With *T* flip-flops (b) With *D* flip-flops

Binary Countdown Counter

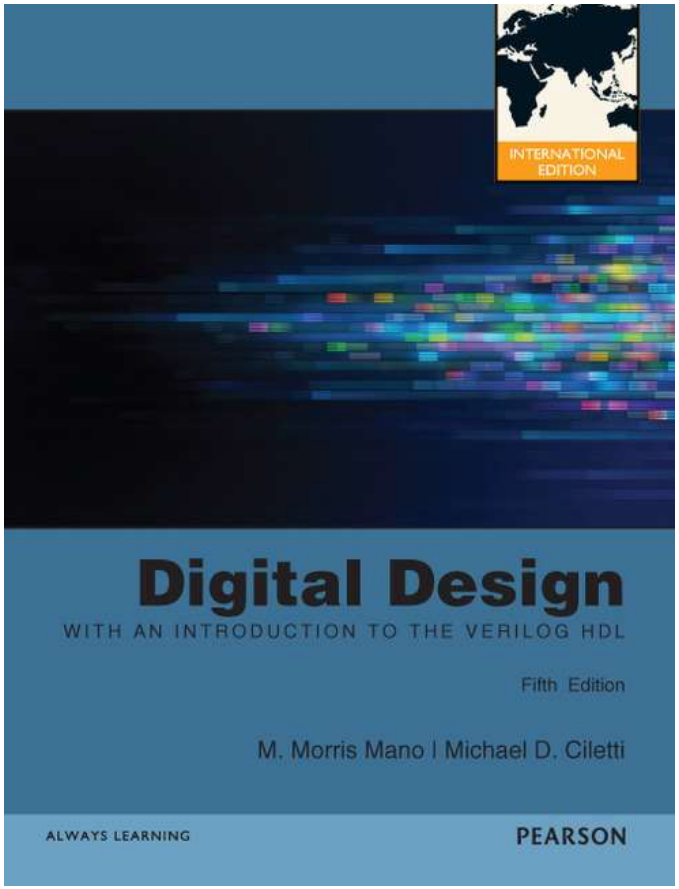
1 1 1 1
1 1 1 0
1 1 0 1
1 1 0 0
1 0 1 1
1 0 1 0
1 0 0 1
1 0 0 0



Positive edge triggered!

Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



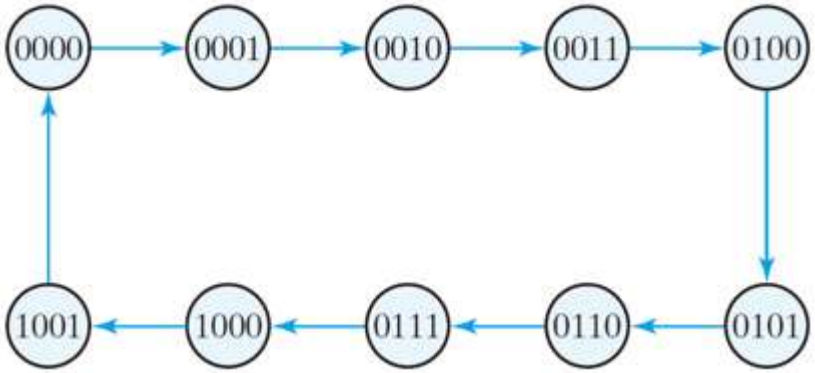
數位邏輯設計

6.3.3 BCD Ripple Counter

主講者：吳順德

國立臺灣師範大學機電工程系 副教授

BCD Ripple Counter

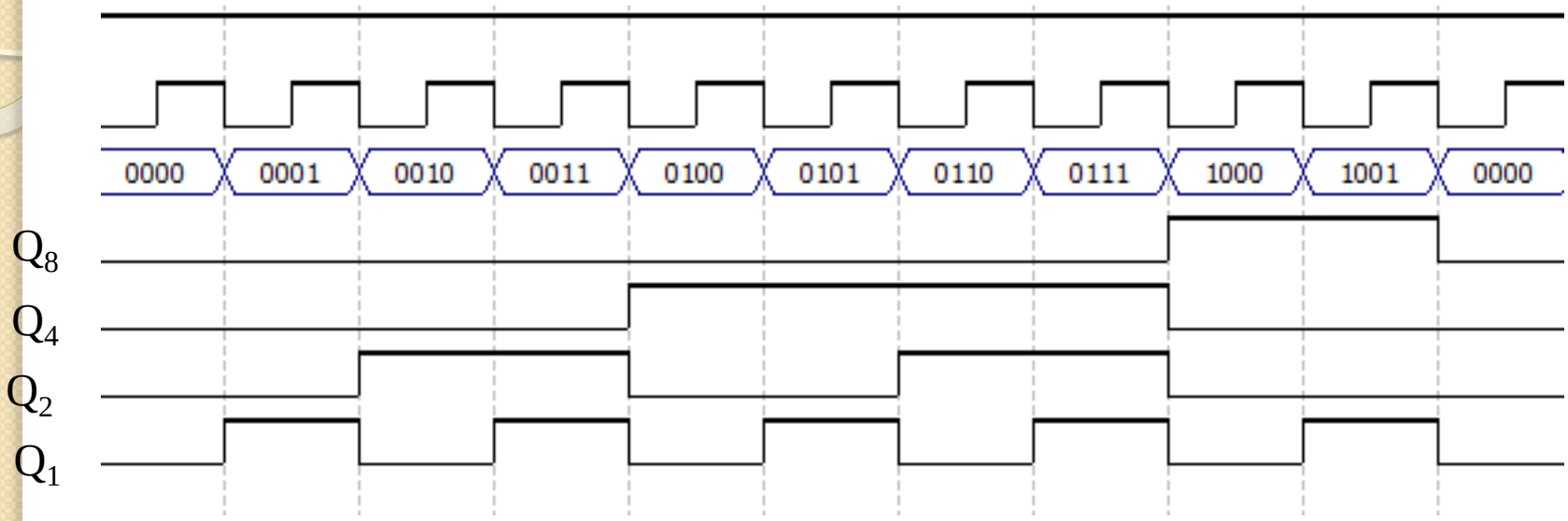


Binary Ripple Counter

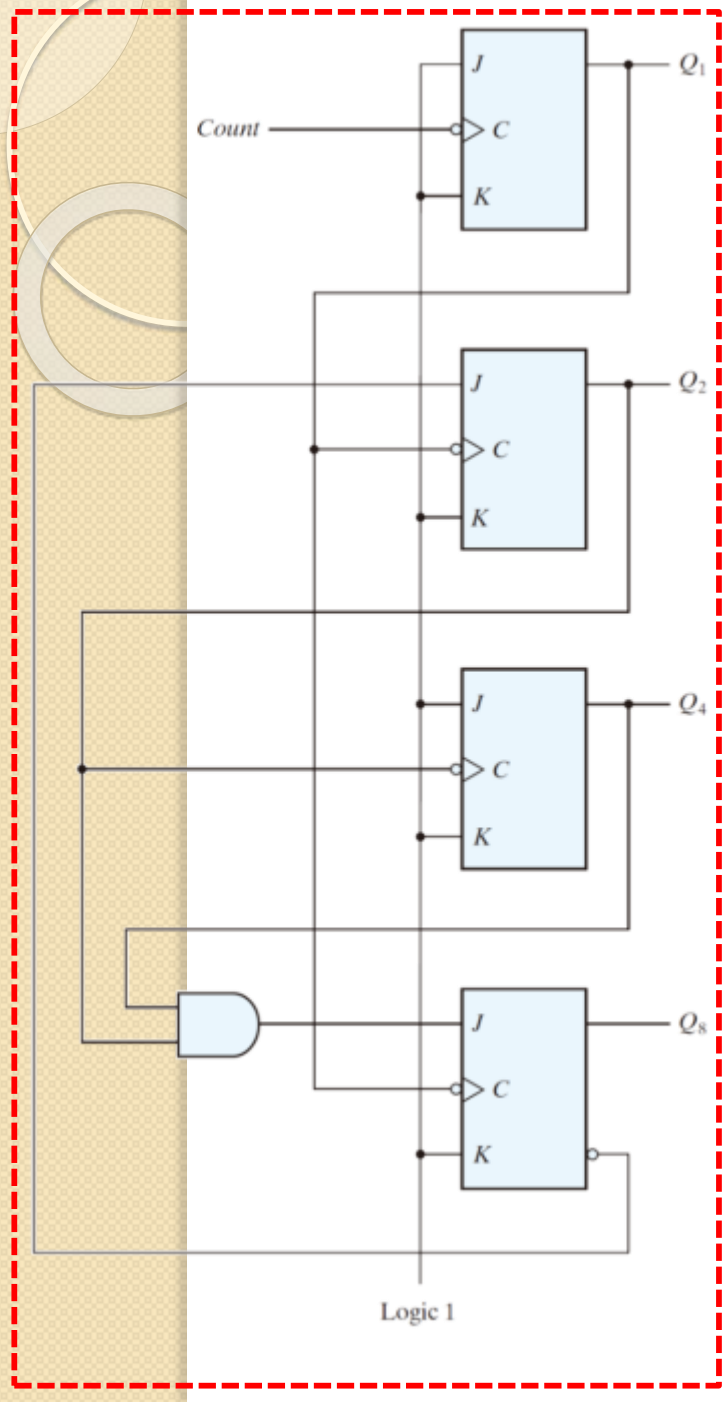
Q_8	Q_4	Q_2	Q_1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
0	0	0	0

- Q8:
  - When Q_2Q_4=1,Q_8 is complemented with Q_1 pulse.
  - Q_8 is reset when Q_2Q_4 is 0
- Q2:
  - When Q_8=0, Q_2 is complemented with Q_1 pulse.
  - When Q_8=1, Q_2 =0.

BCD Ripple Counter



- Q8:
  - When Q_2Q_4=1,Q_8 is complemented with Q_1 pulse.
  - Q_8 is reset when Q_2Q_4 is 0
- Q2:
  - When Q_8=0, Q_2 is complemented with Q_1 pulse.
  - When Q_8=1, Q_2 =0.

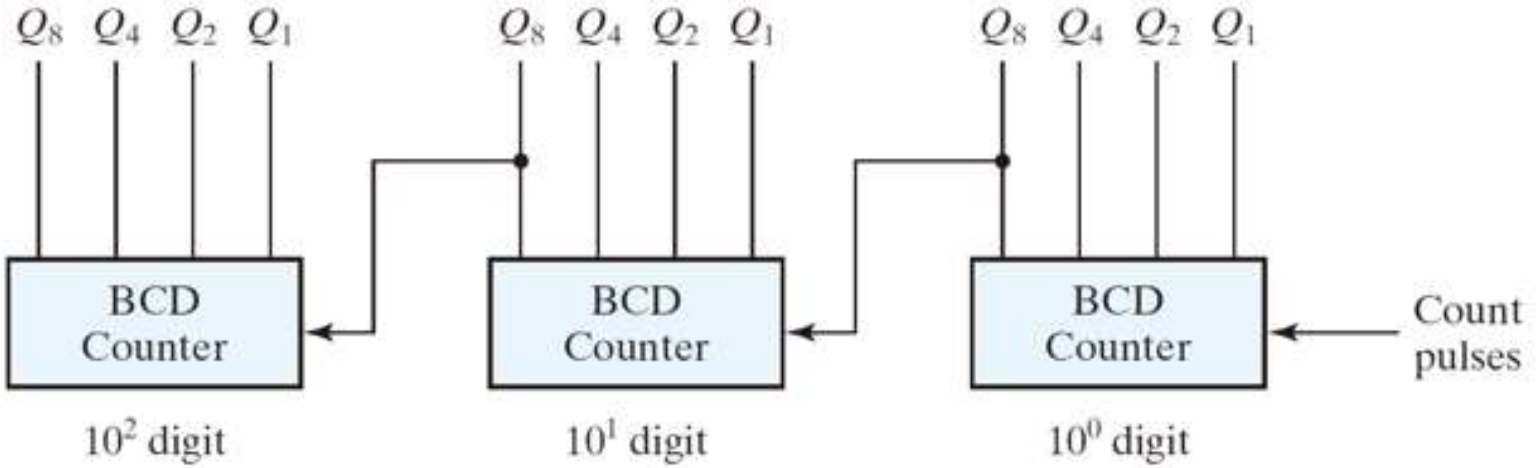


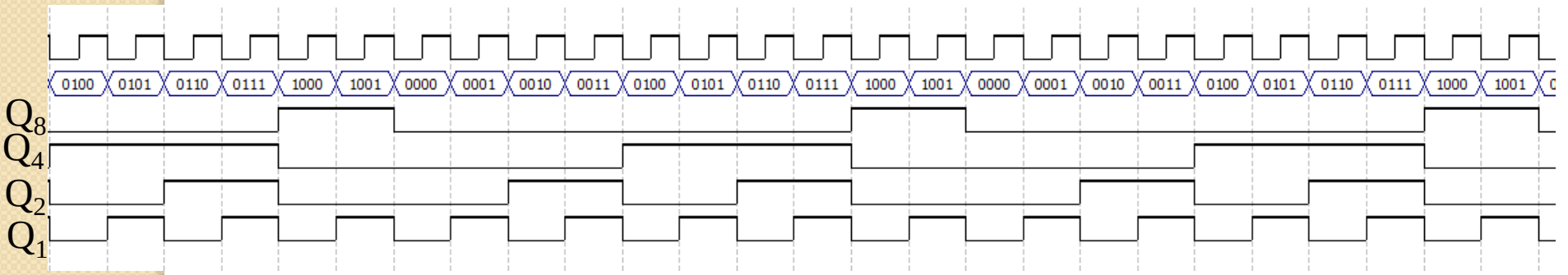
- Q8:
  - When Q_2Q_4=1,Q_8 is complemented with Q_1 pulse.
  - Q_8 is reset when Q_2Q_4 is 0
- Q2:
  - When Q_8=0, Q_2 is complemented with Q_1 pulse.
  - When Q_8=1, Q_2 =0.

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

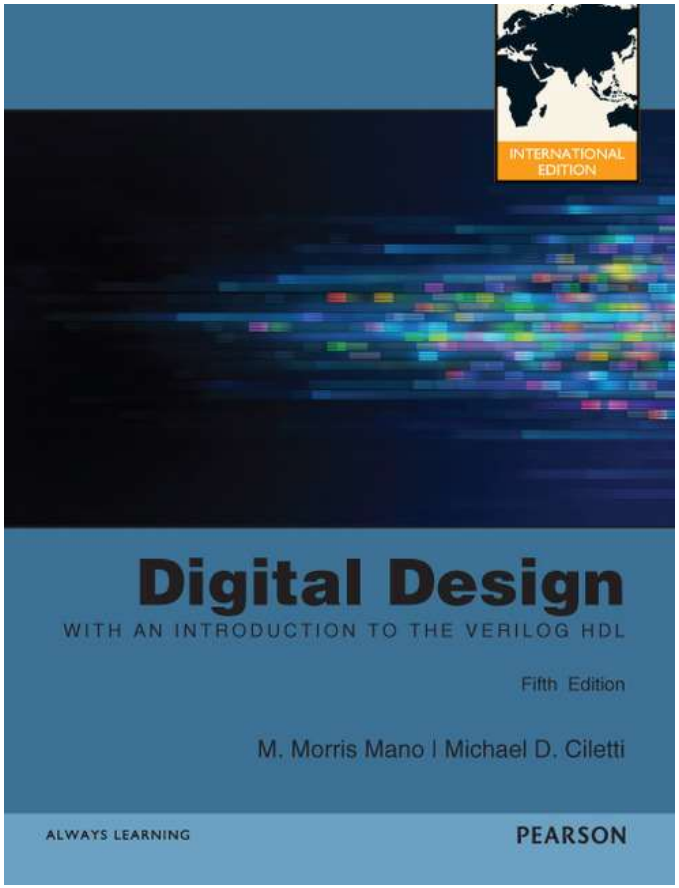
Three-Decade Digits BCD counter





Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



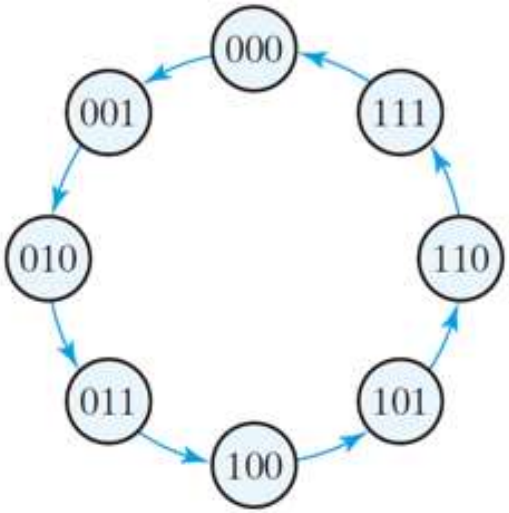
數位邏輯設計

6.4.1 Synchronous Binary Counter

主講者：吳順德

國立臺灣師範大學機電工程系 副教授

Recall: 3 bits Binary Counter

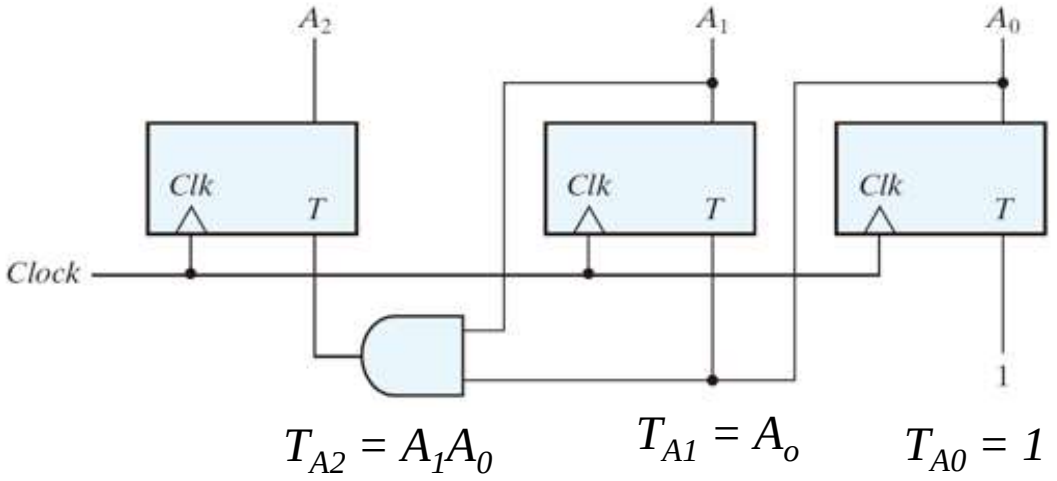


Present State			Next State		
A_2	A_1	A_0	A_2	A_1	A_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

- Rules:
  - A_0 is complemented for every clock pulse.
  - A_1 is complemented A_0 =1.
  - A_2 is complemented A_1A_0 =1.

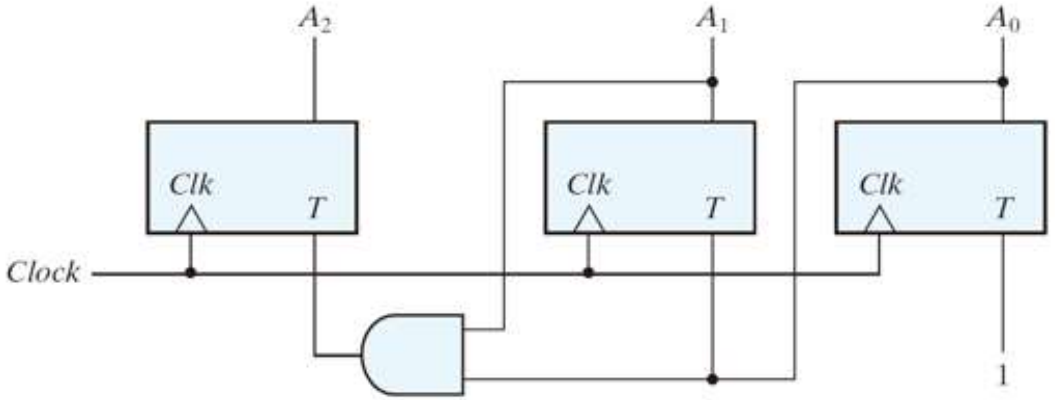
Recall: 3 bits Binary Counter

- Rules:
  - A_0 is complemented for every clock pulse.
  - A_1 is complemented A_0 =1.
  - A_2 is complemented A_1A_0 =1.



n Bits Synchronous Binary Counter (T Flip Flop)

- Rules:
  - A_n is complemented when $A_{n-1}\ldots\ldots A_1A_0$ =1.
  - A_n is no change when $A_{n-1}\ldots\ldots A_1A_0$ =0.

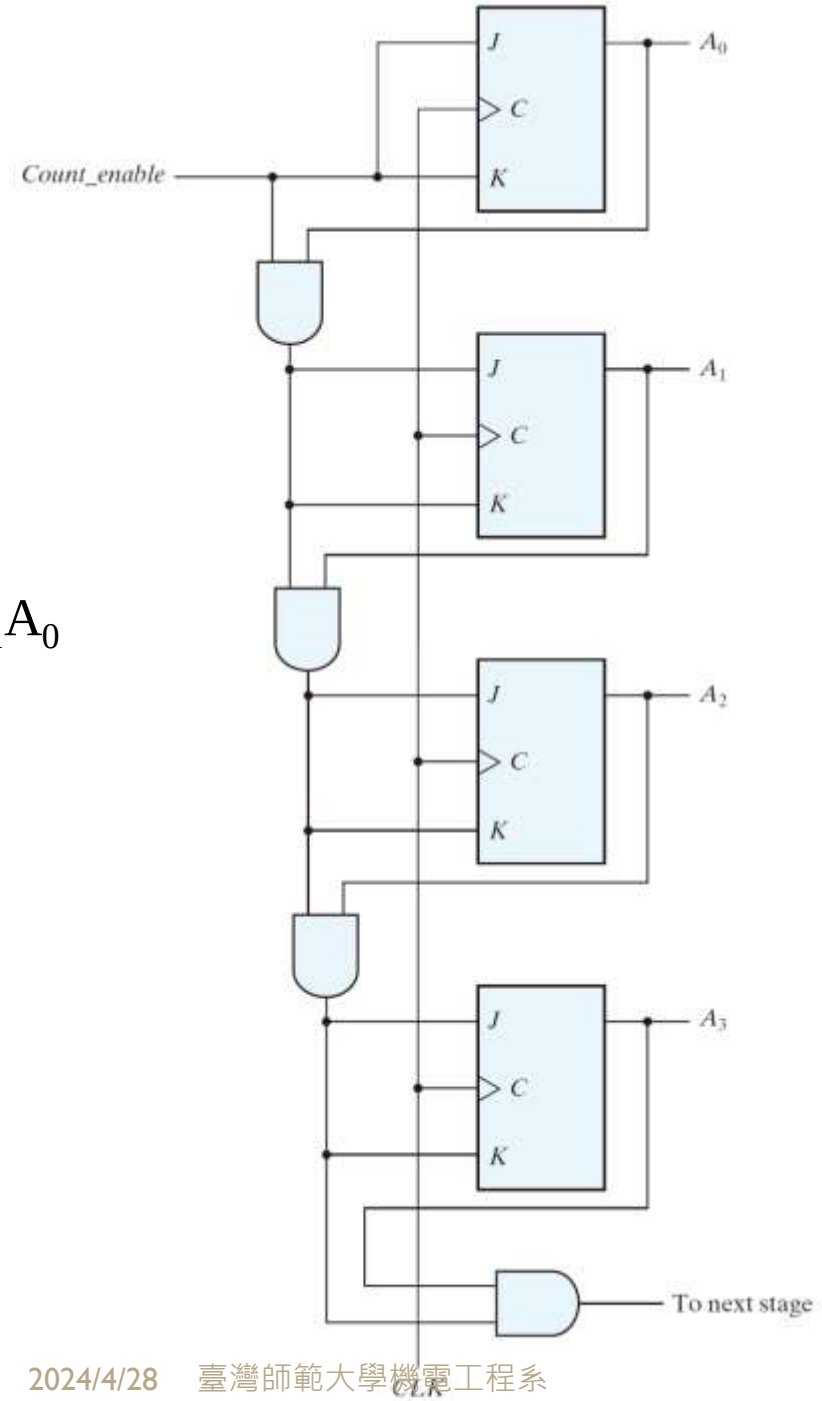


- Synchronous:
  - All flip flops are controlled by the same clock signal.

Binary Counter (JK Flip Flop)

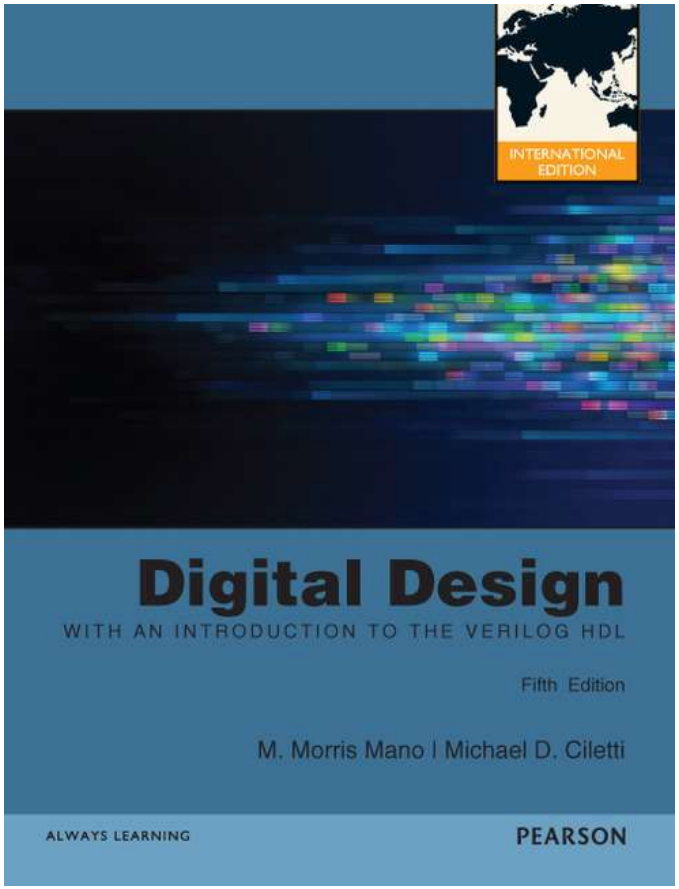
- Count_enable (Ce)
  - Ce= 0 : J =K =0

    A no change
  - Ce =1 : J = K = $A_{n-1}\ldots\ldots A_1A_0$



Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



數位邏輯設計

6.4.2 Synchronous Up/Down Binary Counter

主講者：吳順德

國立臺灣師範大學機電工程系 副教授

Binary Counter

- Binary **Ripple** Counter
  - Up Count: Negative Triggered.
  - Down Count: Positive Triggered
- **Synchronous** Binary Counter
  - Same function for negative and positive trigger.
  - Need combinational circuits to implement Up/Down Count,

Down Counter

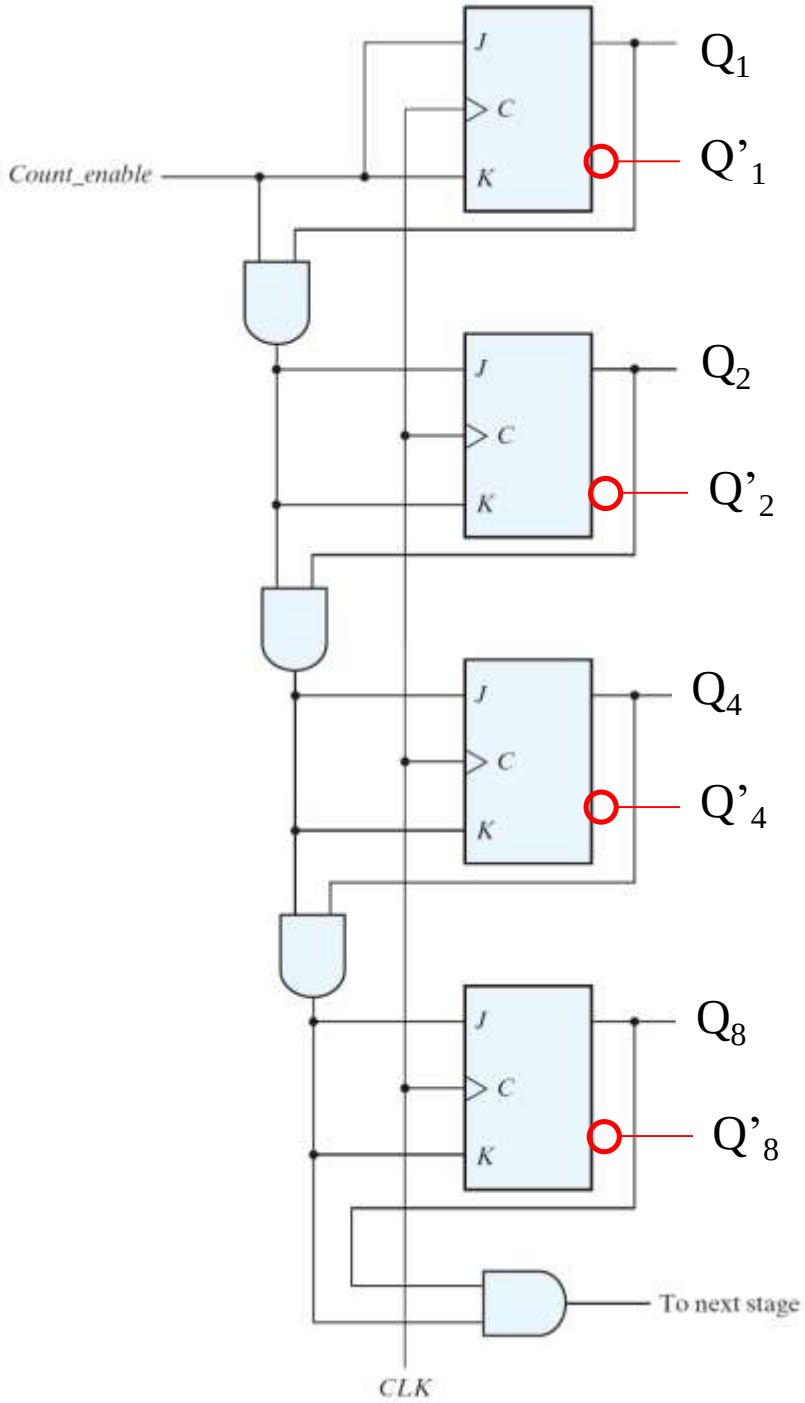
Up

Q_8	Q_4	Q_2	Q_1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1

Down

Q_8	Q_4	Q_2	Q_1
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0

All of Q_8 Q_4 Q_2 Q_1 take Complements.



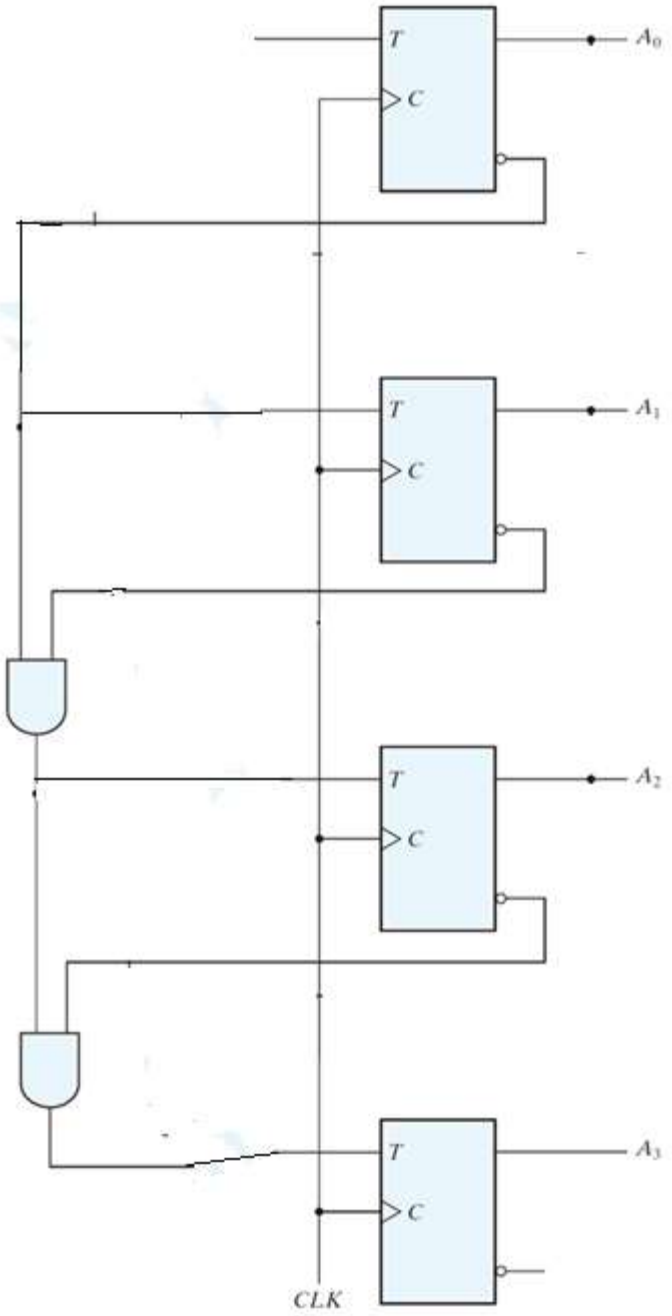
Down Counter

Up

Q_8	Q_4	Q_2	Q_1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1

Down

Q_8	Q_4	Q_2	Q_1
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0

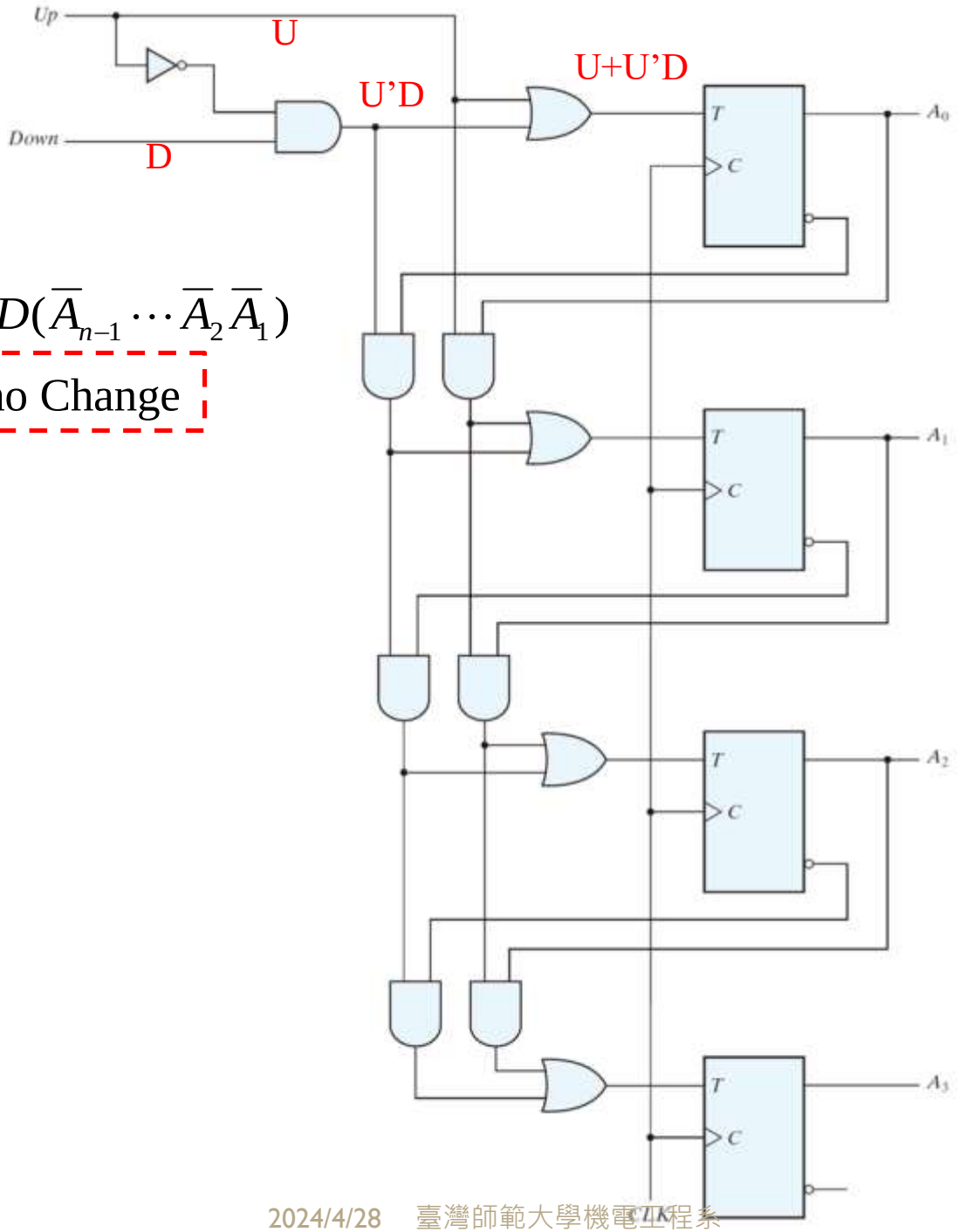


- Rules:
  - A_n is complemented when $\overline{A}_{n-1} \cdots \overline{A}_2 \overline{A}_1 = 1$
  - A_n is no change when $\overline{A}_{n-1} \cdots \overline{A}_2 \overline{A}_1 = 0$

Up/Down Counter

$$T_{An} = U(A_{n-1} \cdots A_2 A_1) + U'D(\overline{A}_{n-1} \cdots \overline{A}_2 \overline{A}_1)$$

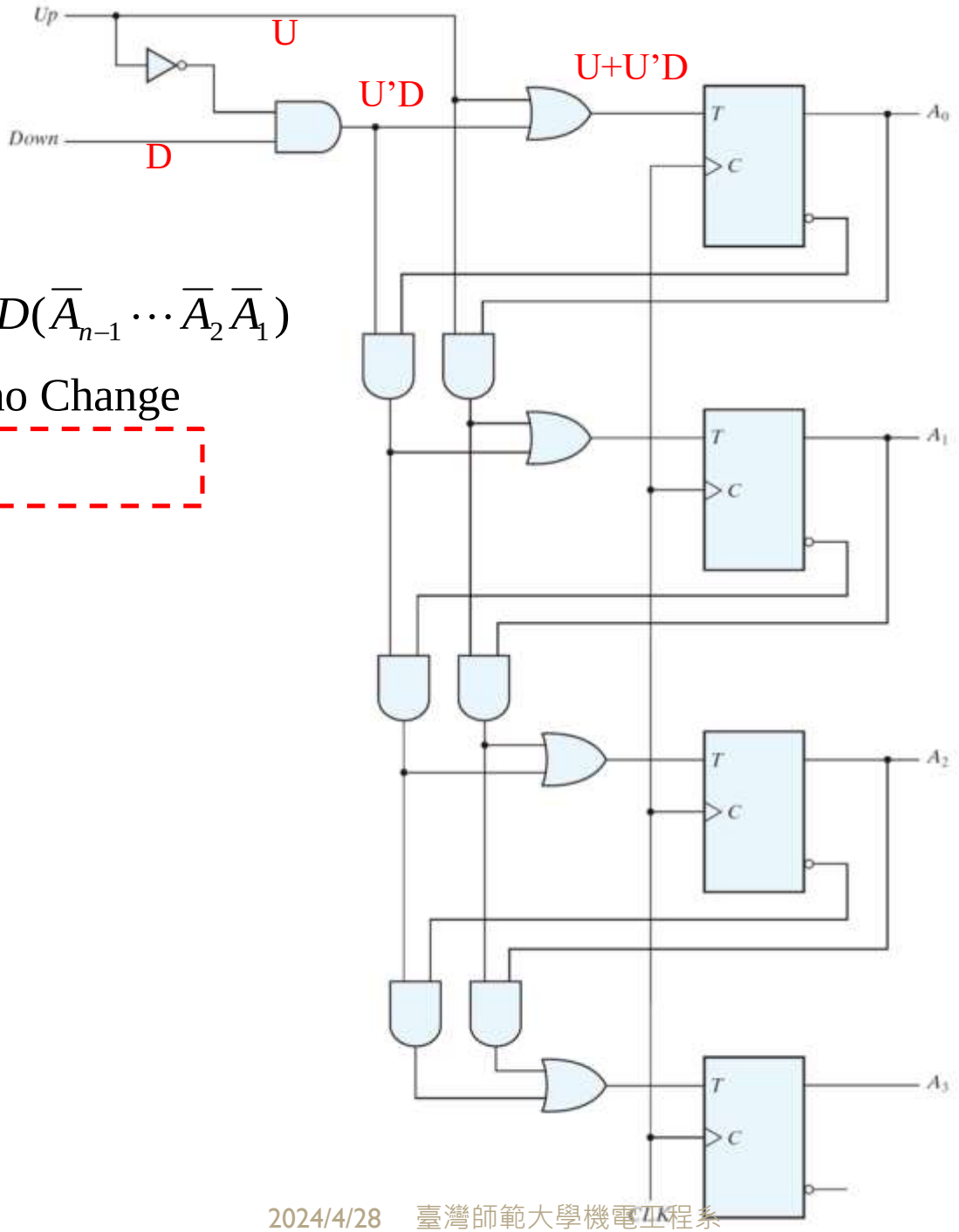
- U=0, D=0 ➔ T=0 ➔ no Change
- U=0, D=1 ➔ Down
- U=1, D=0 ➔ Up
- U=1, D=1 ➔



Up/Down Counter

$$T_{An} = U(A_{n-1} \cdots A_2 A_1) + U'D(\overline{A}_{n-1} \cdots \overline{A}_2 \overline{A}_1)$$

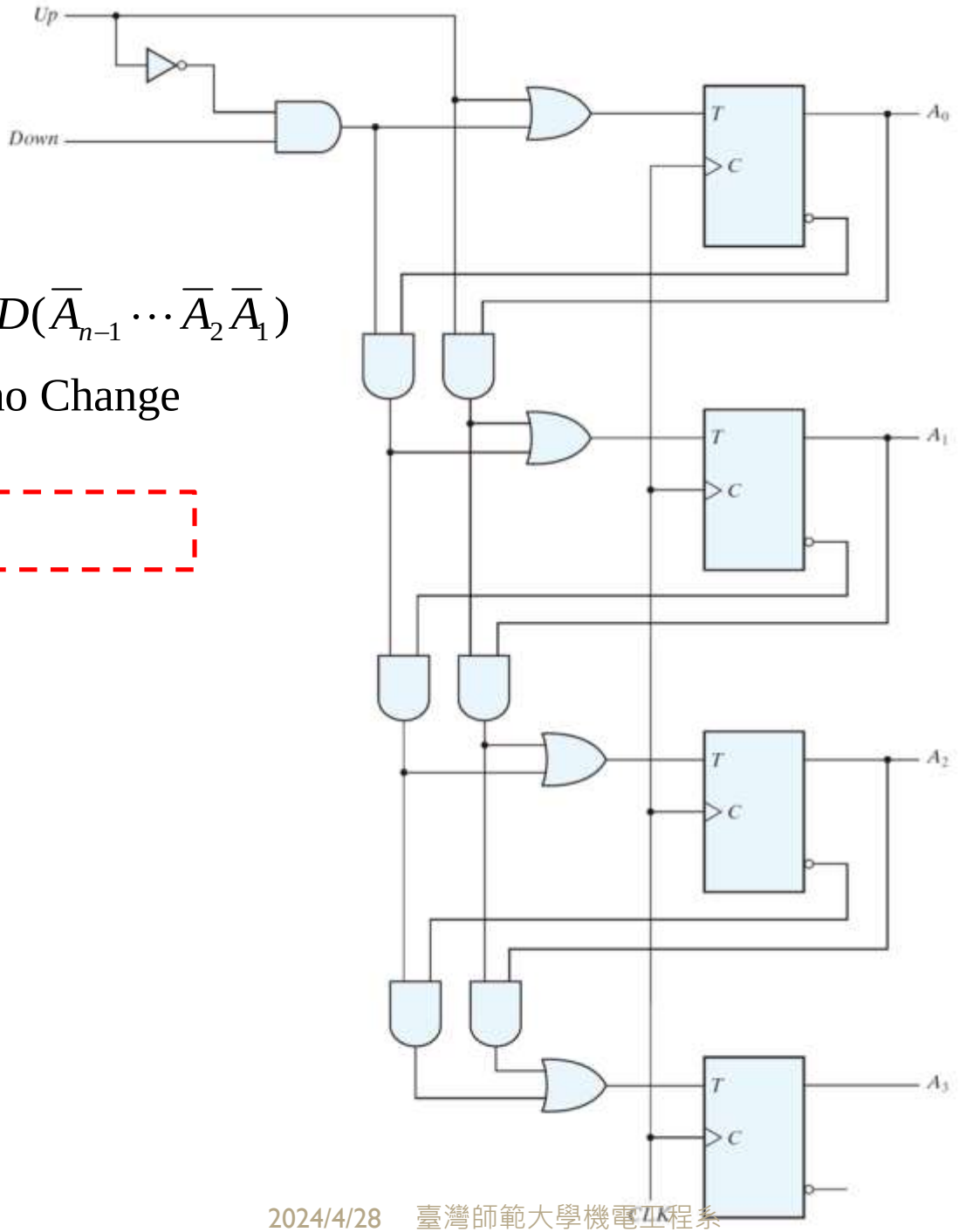
- U=0, D=0 ➔ T=0 ➔ no Change
- U=0, D=1 ➔ Down
- U=1, D=0 ➔ Up
- U=1, D=1 ➔



Up/Down Counter

$$T_{An} = U(A_{n-1} \cdots A_2 A_1) + U'D(\overline{A}_{n-1} \cdots \overline{A}_2 \overline{A}_1)$$

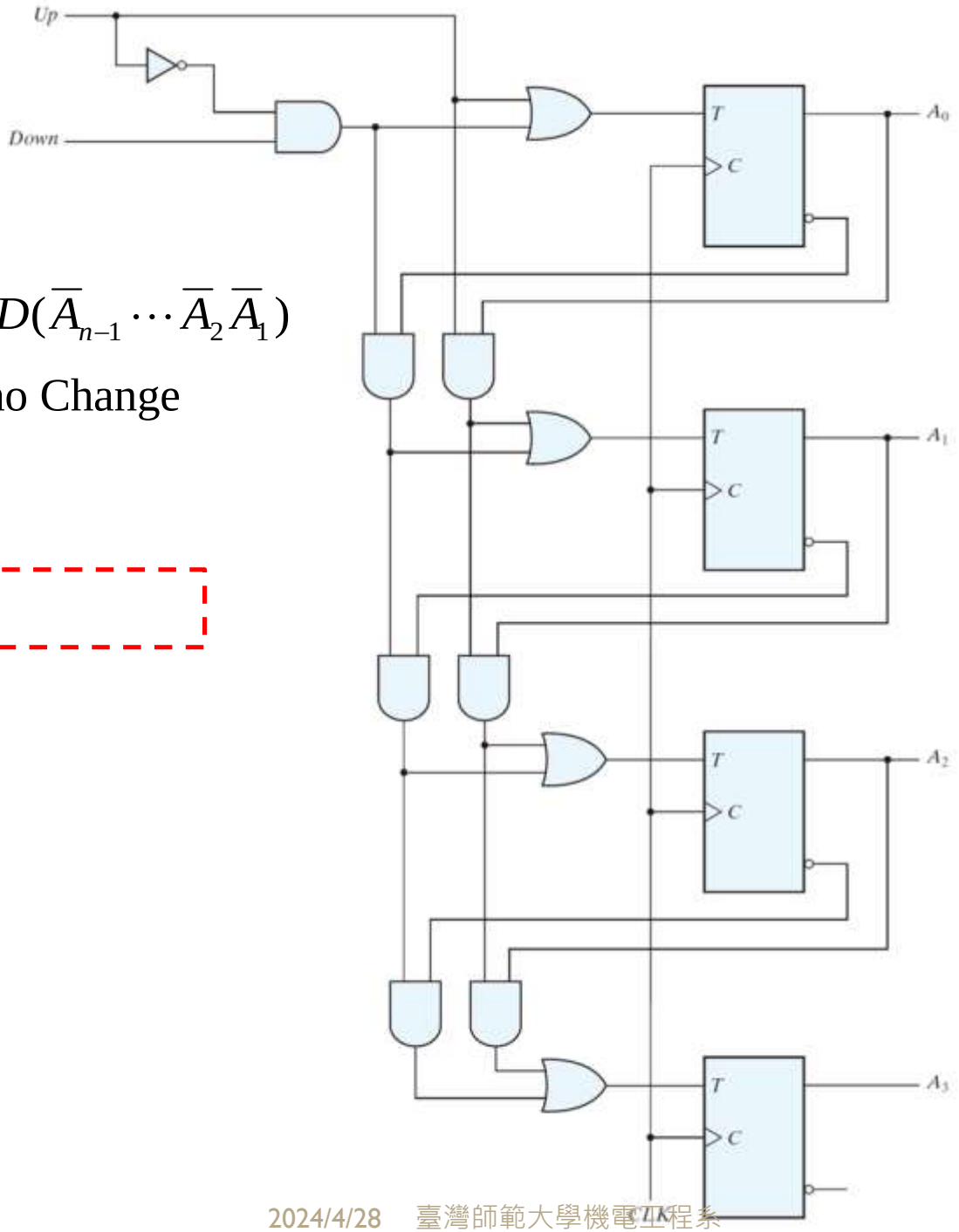
- U=0, D=0 ➔ T=0 ➔ no Change
- U=0, D=1 ➔ Down
- U=1, D=0 ➔ Up
- U=1, D=1 ➔ Up



Up/Down Counter

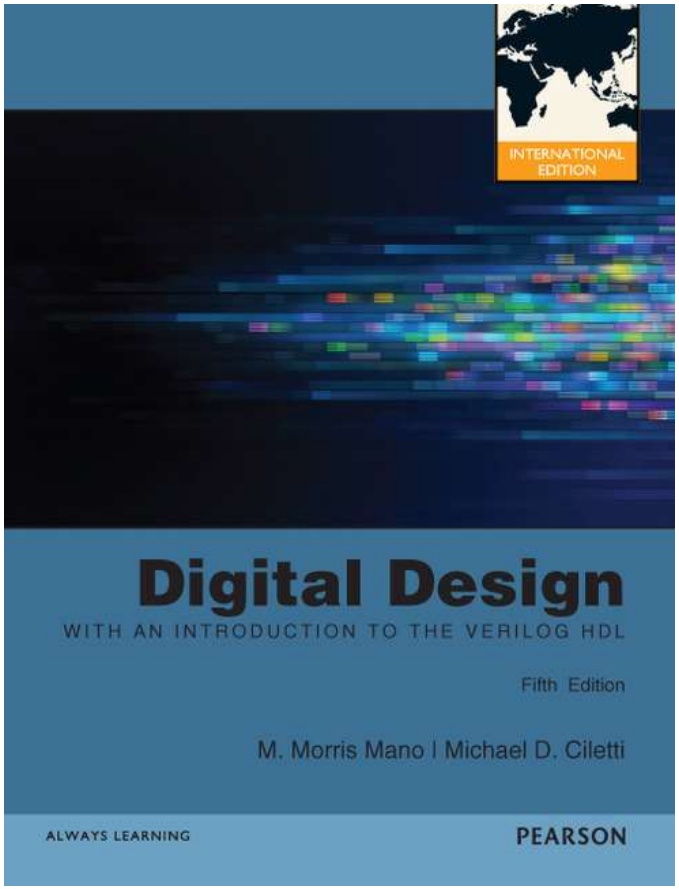
$$T_{An} = U(A_{n-1} \cdots A_2 A_1) + U'D(\overline{A}_{n-1} \cdots \overline{A}_2 \overline{A}_1)$$

- U=0, D=0 ➔ T=0 ➔ no Change
- U=0, D=1 ➔ Down
- U=1, D=0 ➔ Up
- U=1, D=1 ➔ Up



Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



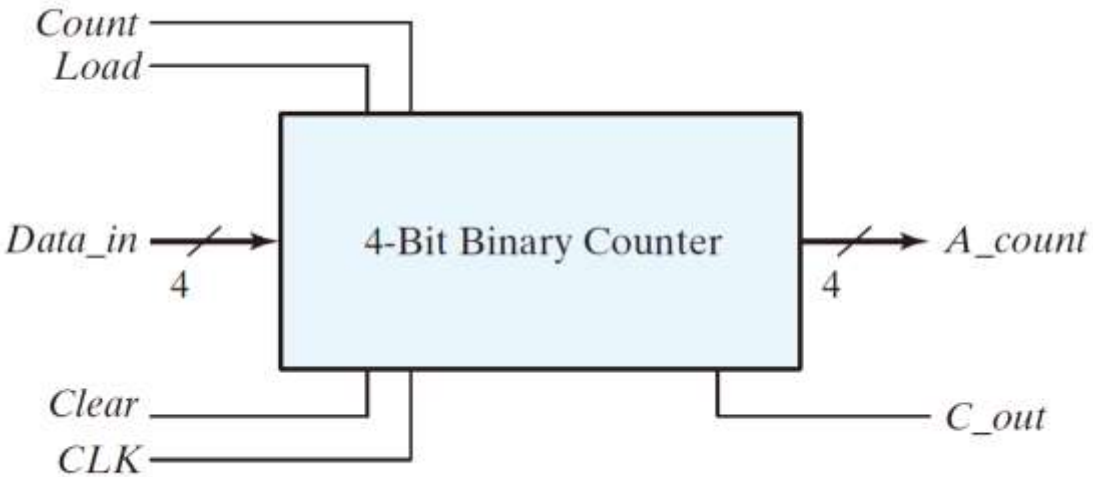
數位邏輯設計

6.4.3 Synchronous Binary Counter With Parallel Load

主講者：吳順德

國立臺灣師範大學機電工程系 副教授

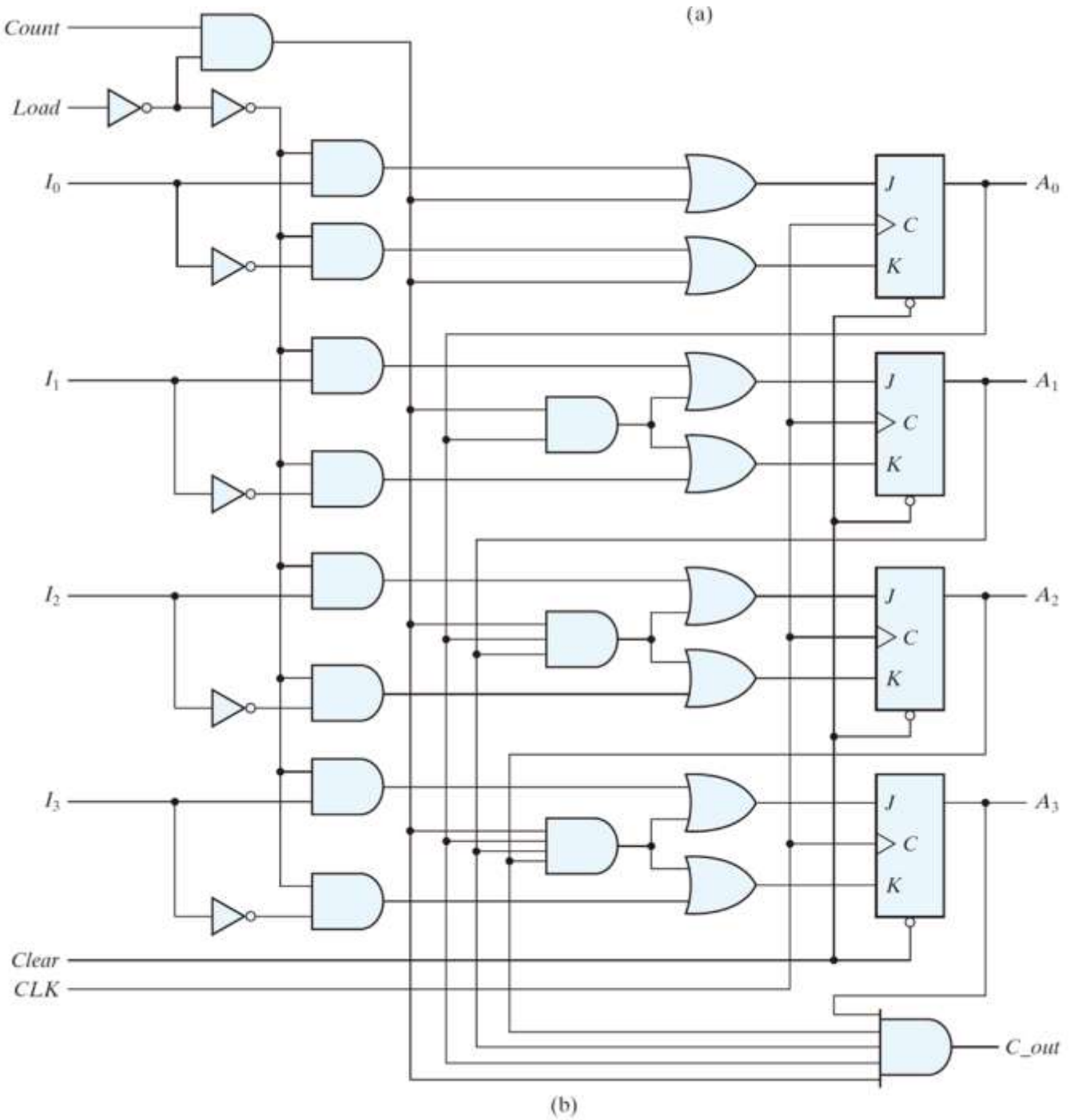
4-bit binary counter with parallel load



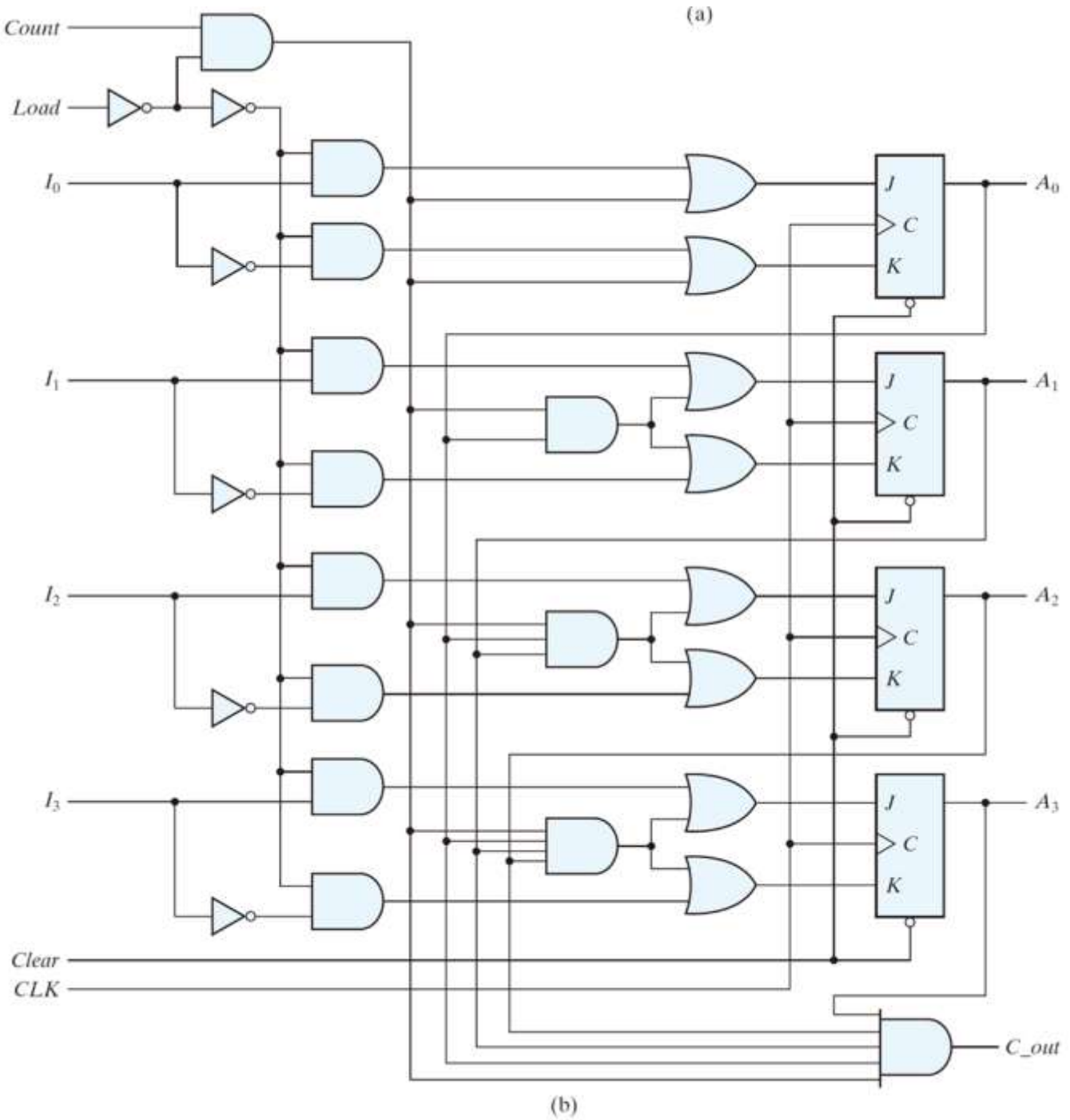
(a)

Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

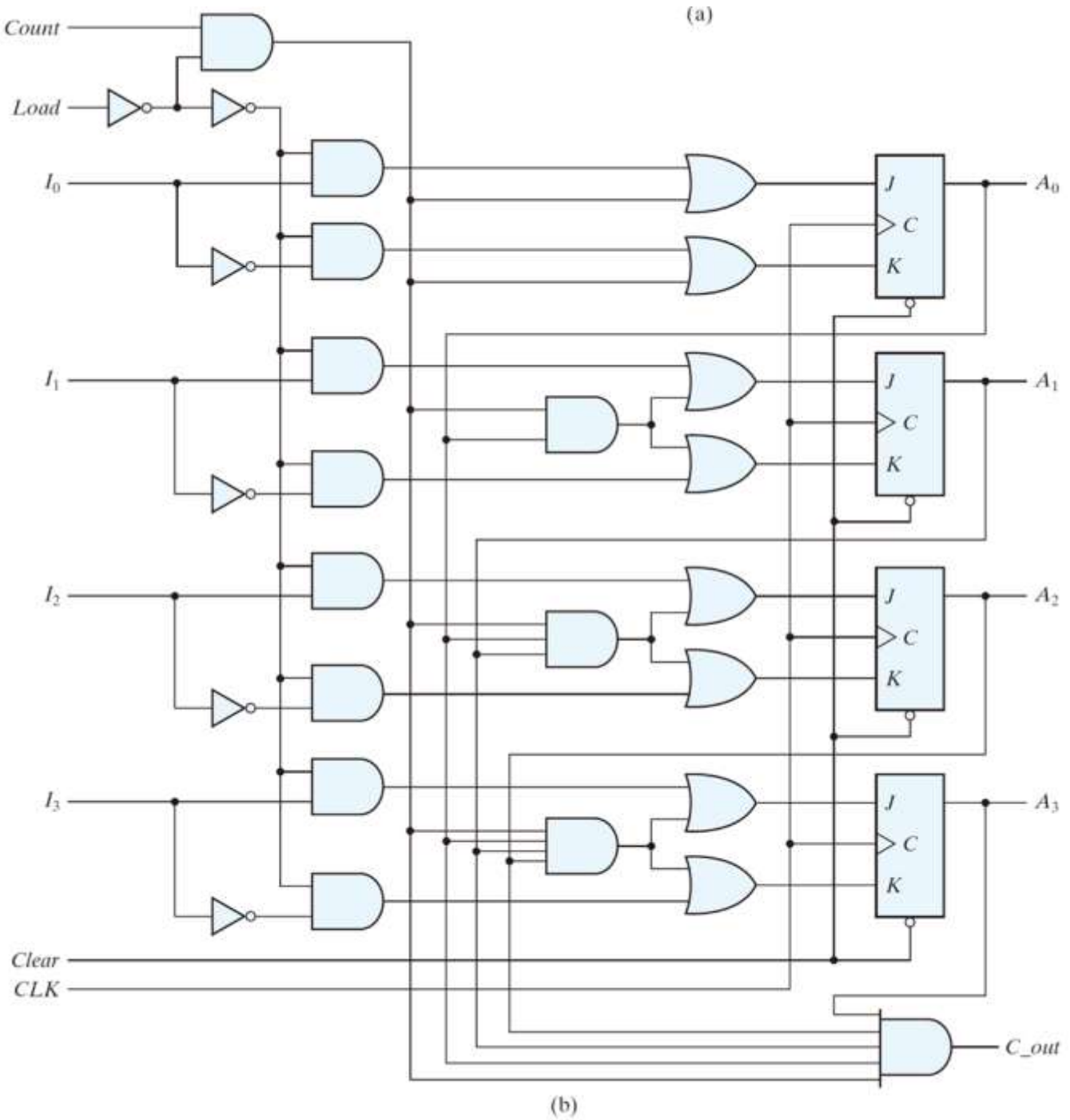
Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change



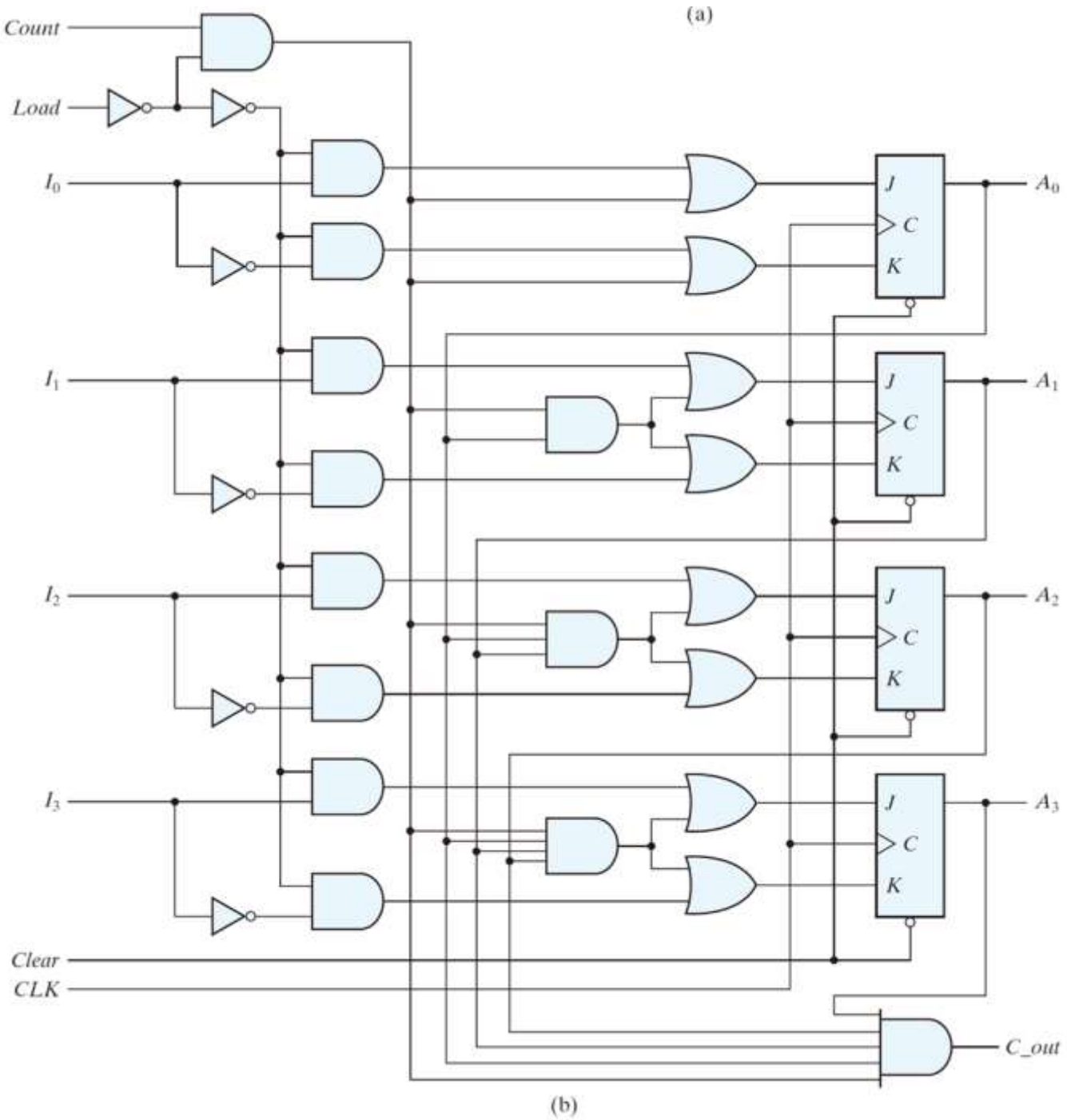
Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change



Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

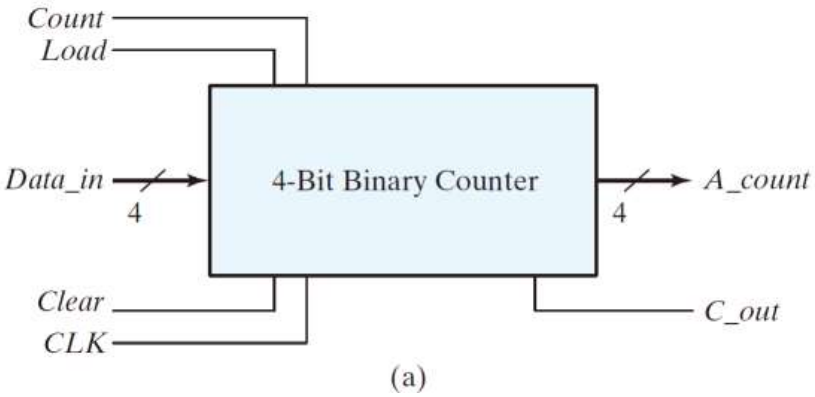


Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change



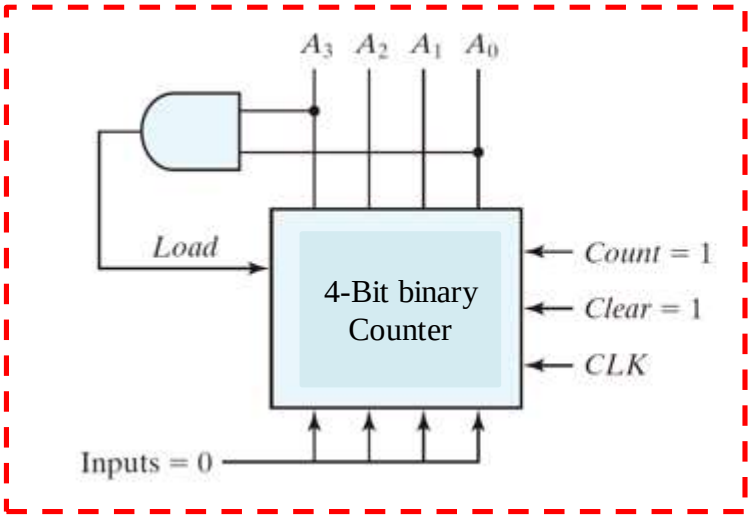
BCD Counter Implemented by Binary Counter

Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

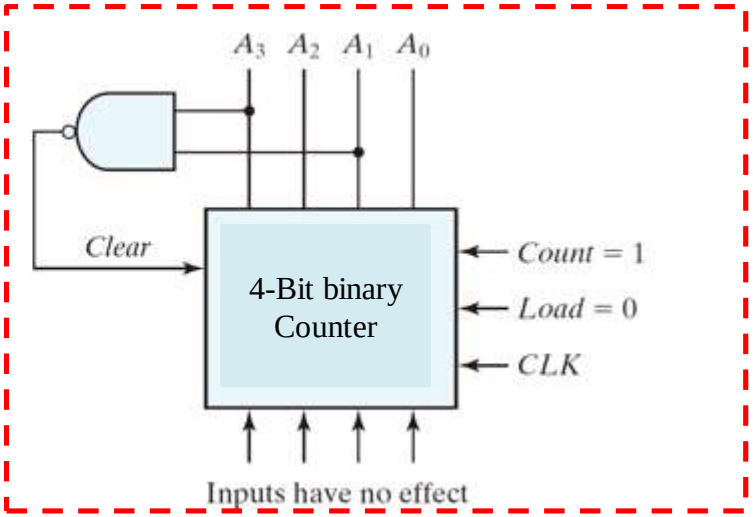


(a)

Method 1

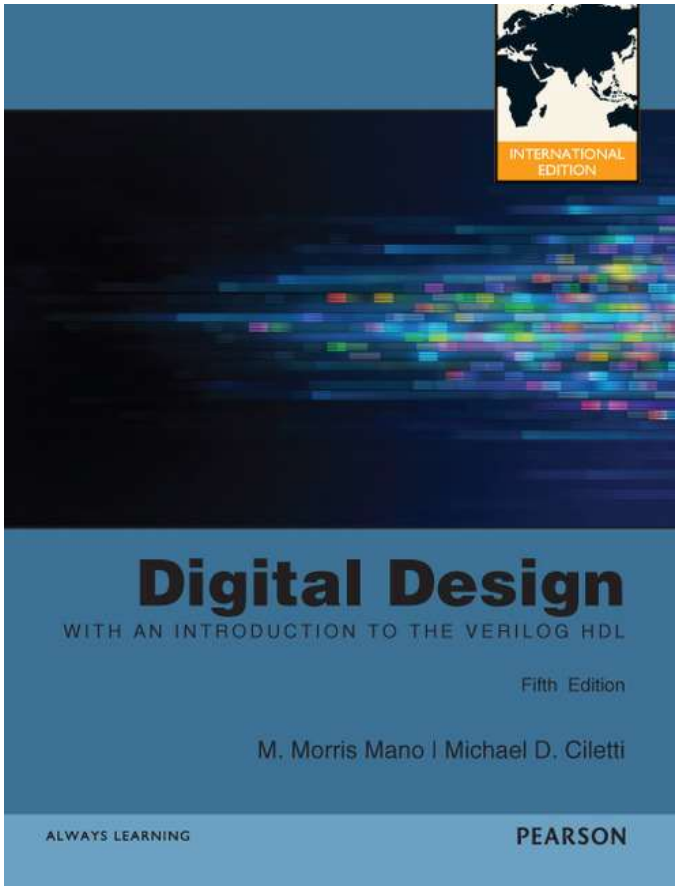


Method 2



Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



數位邏輯設計

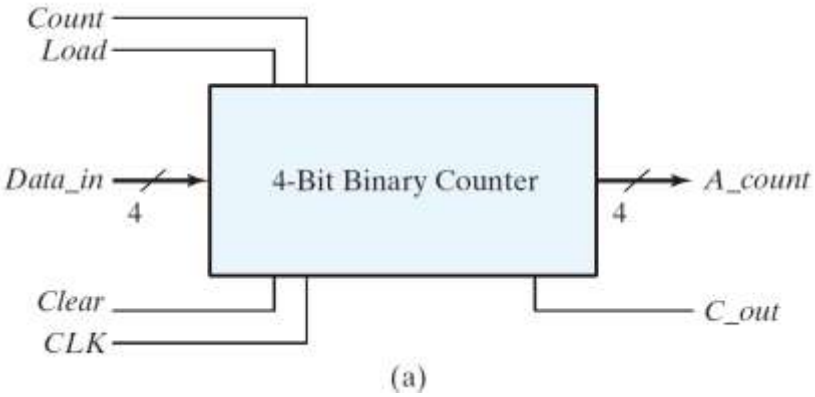
6.4.4 Synchronous BCD Counter

主講者：吳順德

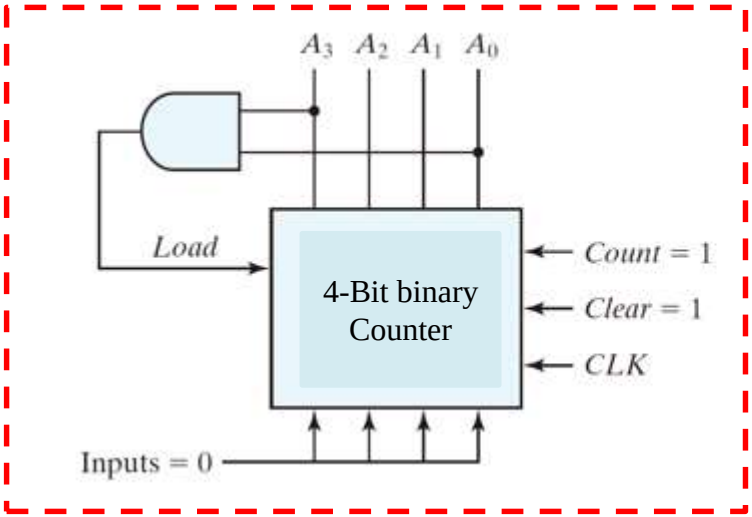
國立臺灣師範大學機電工程系 副教授

BCD Counter Implemented by Binary Counter

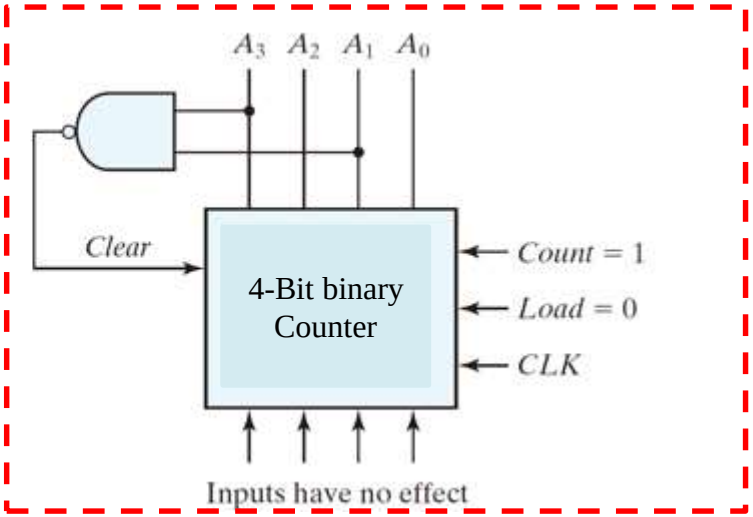
Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change



Method 1



Method 2



Synchronous BCD Counter

Present State				Next State				Output
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y
0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	1	0	0
0	0	1	0	0	0	1	1	0
0	0	1	1	0	1	0	0	0
0	1	0	0	0	1	0	1	0
0	1	0	1	0	1	1	0	0
0	1	1	0	0	1	1	1	0
0	1	1	1	1	0	0	0	0
1	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	0	1

+

$Q(t)$	$Q(t = 1)$	T
0	0	0
0	1	1
1	0	1
1	1	0

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	TQ_8	TQ_4	TQ_2	TQ_1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	TQ_8	TQ_4	TQ_2	TQ_1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

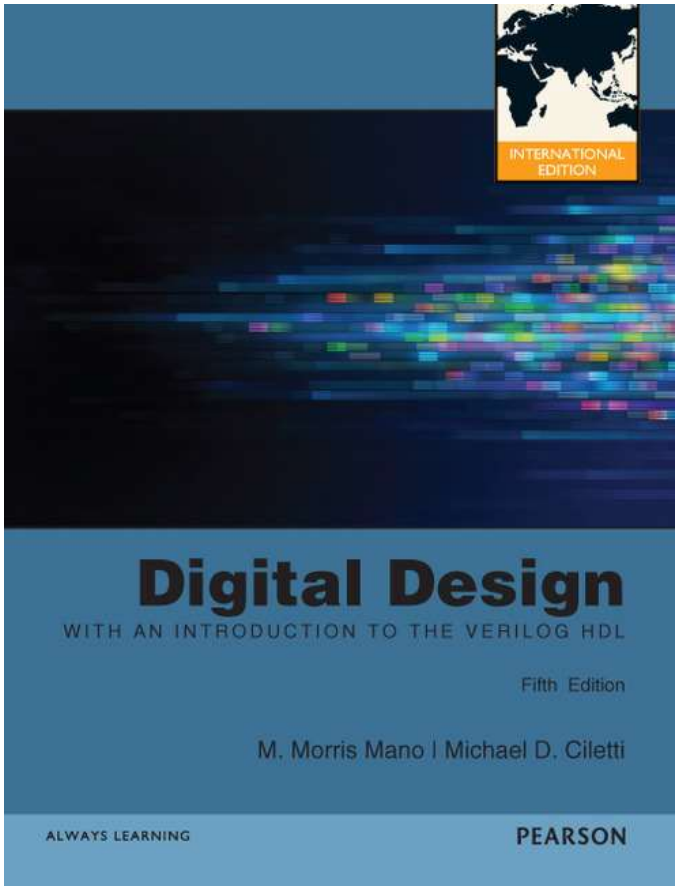
Simplified by K-Map

$$T_{Q1} = 1$$
$$T_{Q2} = Q'_8 Q_1$$
$$T_{Q4} = Q_2 Q_1$$
$$T_{Q8} = Q_8 Q_1 + Q_4 Q_2 Q_1$$
$$y = Q_8 Q_1$$

$$T_{Q1} = 1$$
$$T_{Q2} = Q'_8 Q_1$$
$$T_{Q4} = Q_2 Q_1$$
$$T_{Q8} = Q_8 Q_1 + Q_4 Q_2 Q_1$$
$$y = Q_8 Q_1$$

Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



數位邏輯設計

6.5.1 Counter with Unused States

主講者：吳順德

國立臺灣師範大學機電工程系 副教授

Counters

- Counter can be designed to generate any desired sequence of states
- Modulo-N counter (Divide-by-N counter)
  - a counter that goes through a repeated sequence of N states
- n flip-flops $\Rightarrow 2^n$ binary states
- Unused states
  - states that are not used in specifying the FSM and are **not listed in the state table.**
  - may be treated as don't-care conditions or may be assigned specific next states.

Modulo-6 counter

Present State			Next State			Flip-Flop Inputs					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

Q(t)	Q(t = 1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Two unused states: 011 & 111 (not listed in the state table)

The simplified flip-flop input eqs.

$J_A = B,\ K_A = B$

$J_B = C,\ K_B = 1$

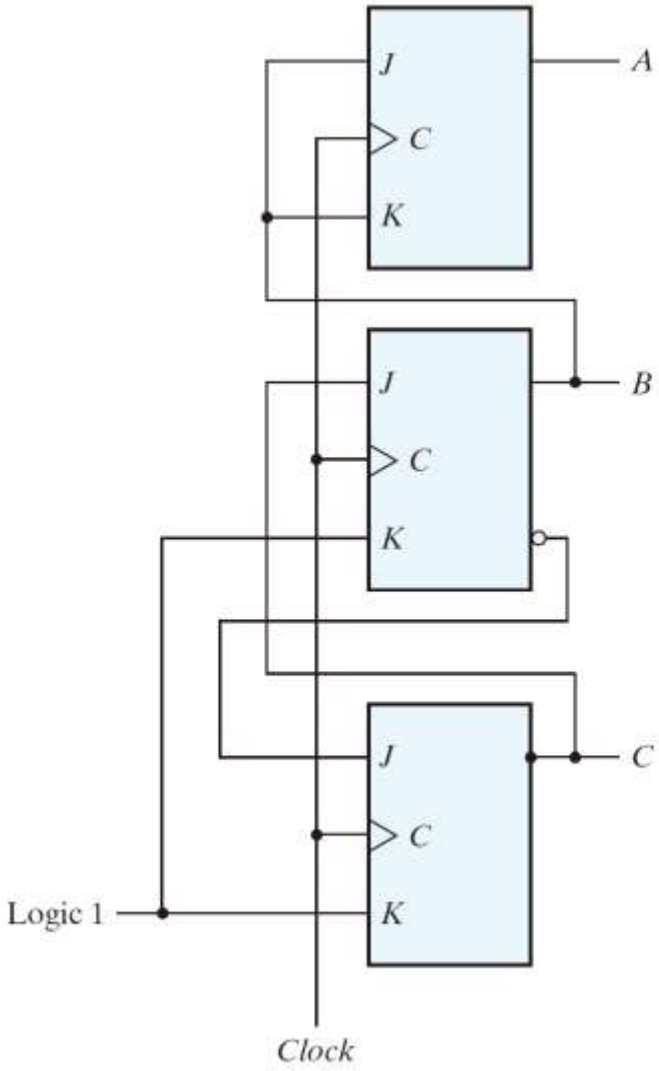
$J_C = B',\ K_C = 1$

Modulo-6 counter

$J_A = B,\ K_A = B$

$J_B = C,\ K_B = 1$

$J_C = B',\ K_C = 1$



(a) Logic circuit diagram

Self Correcting

$J_A = B,\ K_A = B$

$J_B = C,\ K_B = 1$

$J_C = B',\ K_C = 1$

ABC=111 ➔ ABC=000

$J_A = 1,\ K_A = 1$ ➔A=0

$J_B = 1,\ K_B = 1$ ➔B=0

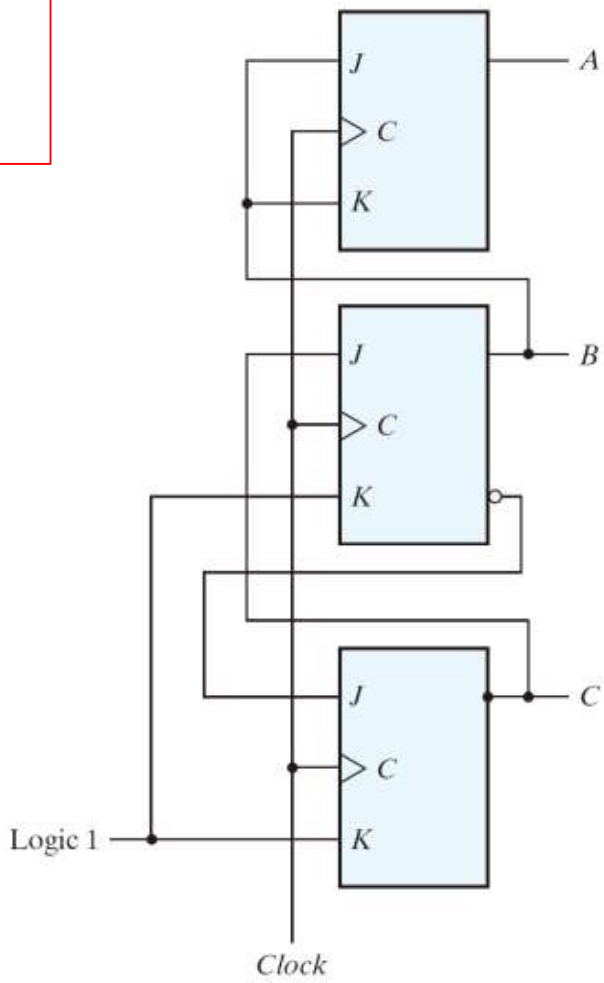
$J_C = 0,\ K_C = 1$ ➔C=0

ABC=011 ➔ ABC=100

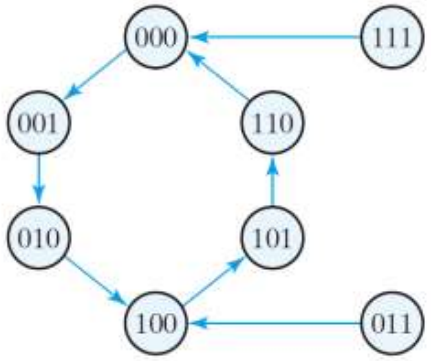
$J_A = 1,\ K_A = 1$ ➔A=1

$J_B = 1,\ K_B = 1$ ➔B=0

$J_C = 0,\ K_C = 1$ ➔C=0



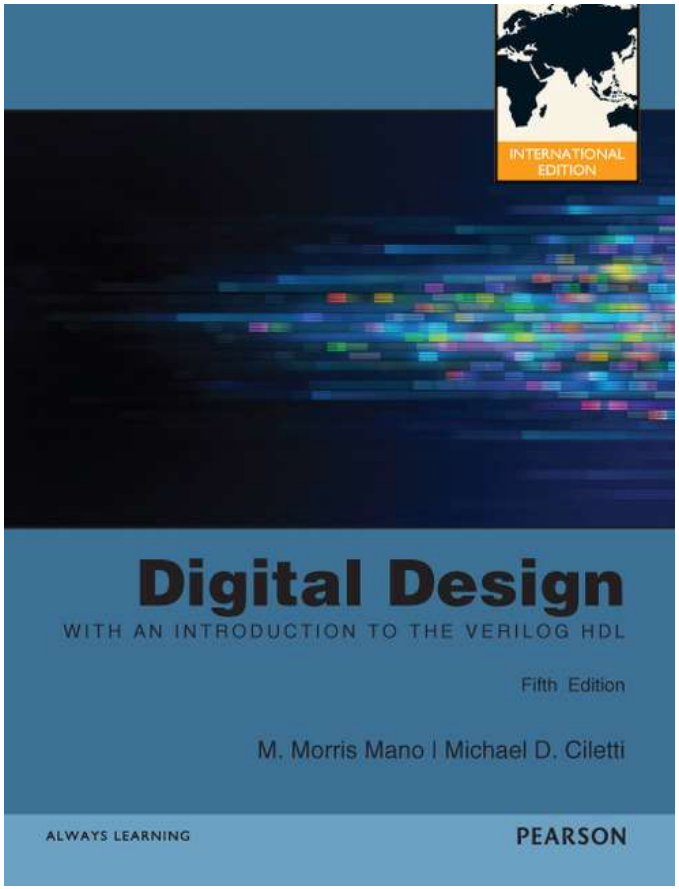
(a) Logic circuit diagram



(b) State transition diagram

Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



數位邏輯設計

6.5.2 Ring Counter

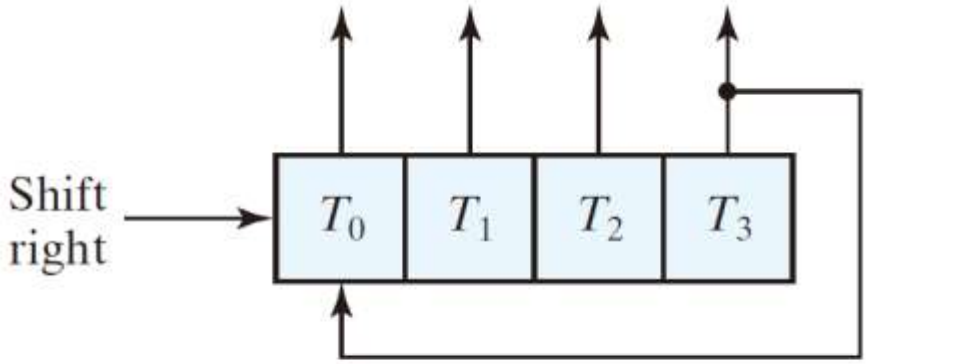
主講者：吳順德

國立臺灣師範大學機電工程系 副教授

Ring Counter

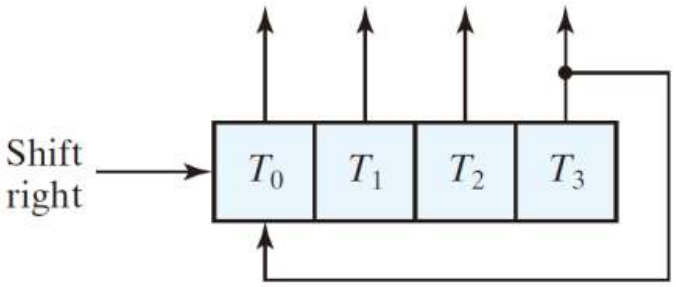
- A ring counter is a circular shift register with only one flip-flop being set at any particular time
  - (initial value = 1 0 0 … 0)

A_2	A_2	A_1	A_0
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1
1	0	0	0

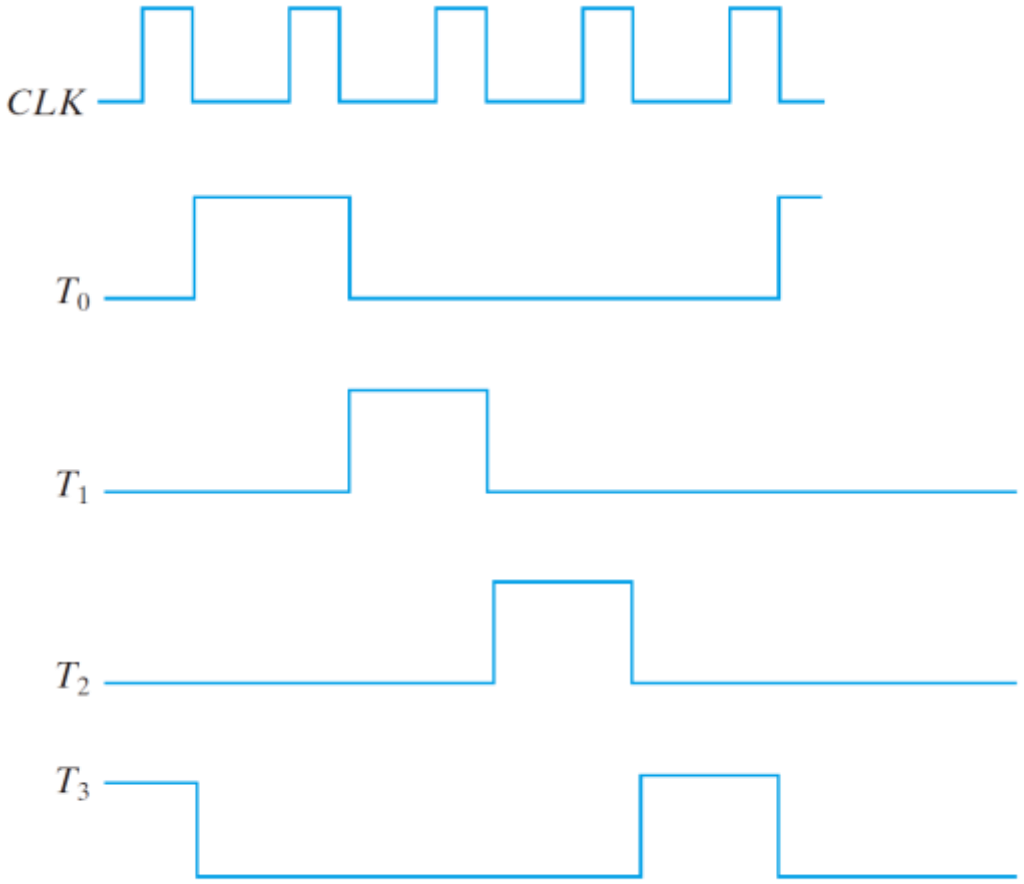


(a) Ring-counter (initial value = 1000)

Timing Diagram for Ring Counter



(a) Ring-counter (initial value = 1000)

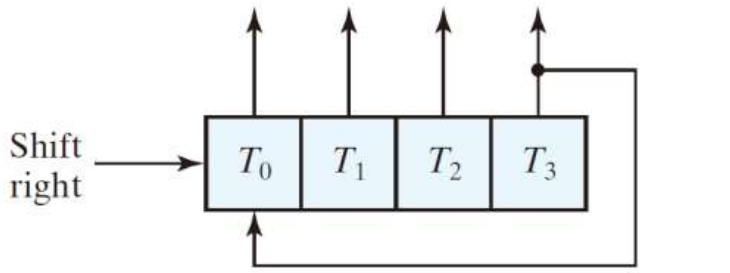


(b) Sequence of four timing signals

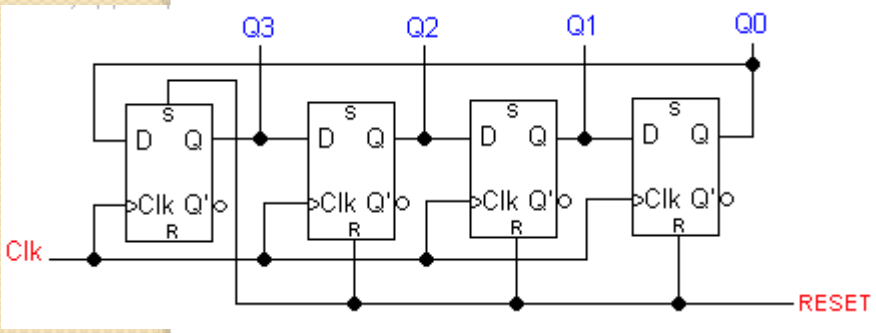
A ring counter is use to generate timing signals that control the sequence of operations.

Reduce the number of Flip Flops

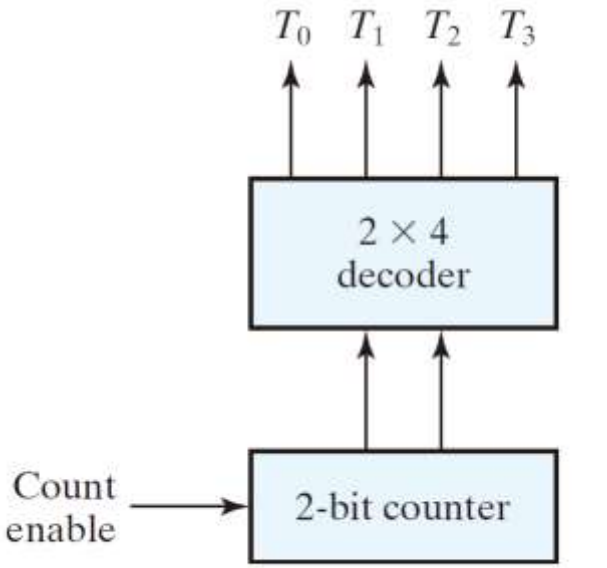
4 Flip Flops



(a) Ring-counter (initial value = 1000)



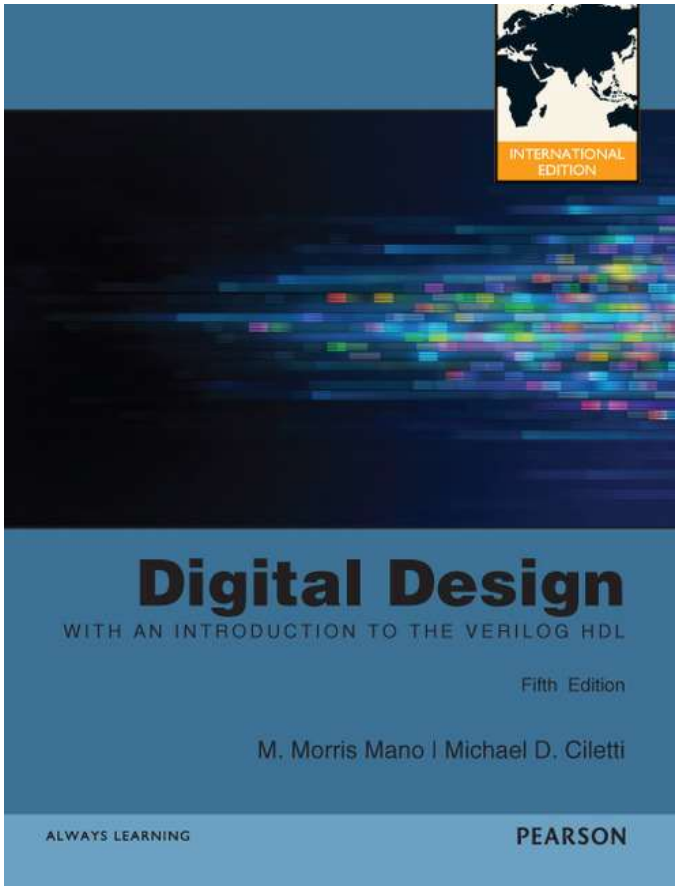
2 Flip Flops



(c) Counter and decoder

Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



數位邏輯設計

6.5.3 Johnson Counter

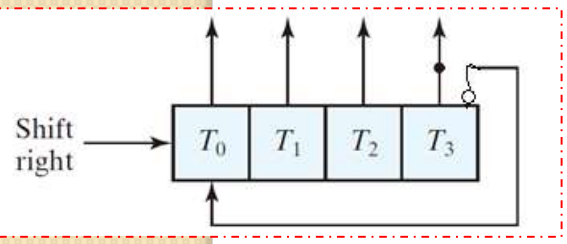
主講者：吳順德

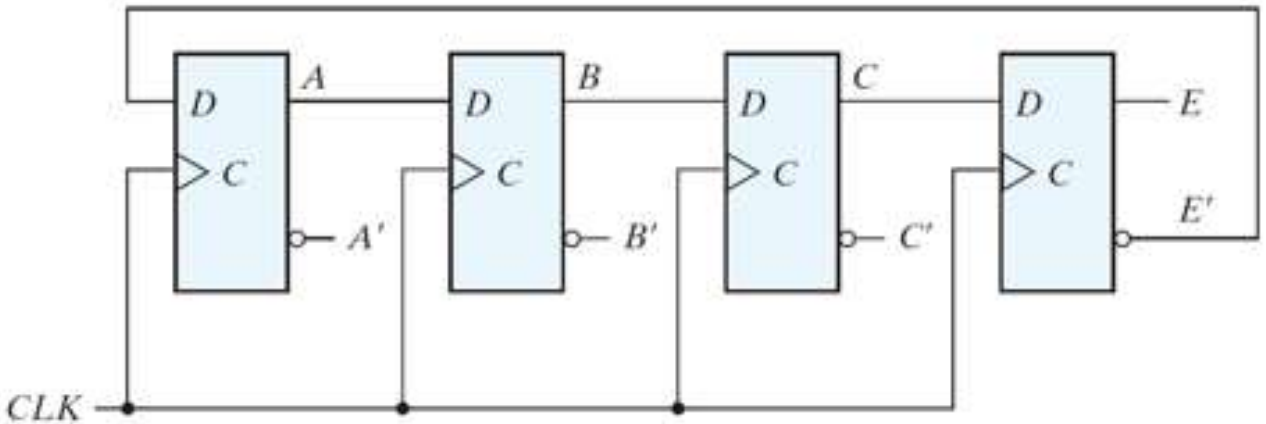
國立臺灣師範大學機電工程系 副教授

Johnson Counter

- A ring counter is used to generate timing signals that control the sequence of operations.
- A Johnson Counter is a k bits switch tail ring counter with $2k$ decoding gates to provide outputs for $2k$ timing signals.

Switch-tail ring counter





(a) Four-stage switch-tail ring counter

Sequence number	Flip-flop outputs				AND gate required for output
	A	B	C	E	
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

(b) Count sequence and required decoding

k flip flops
➔2k states

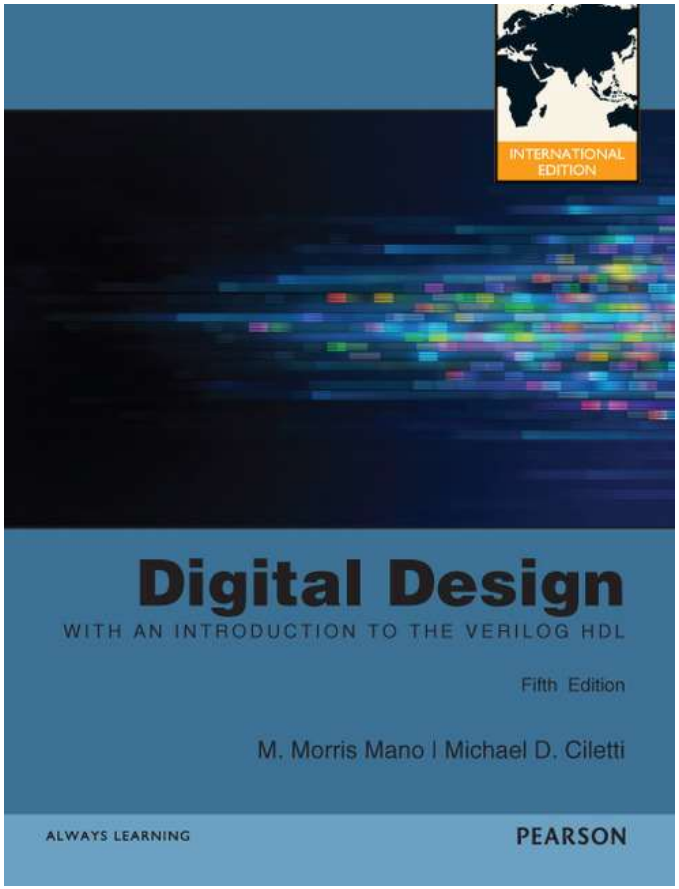
Sequence of Timing Clock

Sequence number	Flip-flop outputs A	B	C	E	AND gate required for output
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

	0000	1000	1100	1110	1111	0111	0011	0001	0000
$A'E'$	1	0	0	0	0	0	0	0	1
AB'	0	1	0	0	0	0	0	0	0
BC'	0	0	1	0	0	0	0	0	0
CE'	0	0	0	1	0	0	0	0	0
AE	0	0	0	0	1	0	0	0	0
$A'B$	0	0	0	0	0	1	0	0	0
$B'C$	0	0	0	0	0	0	1	0	0
$C'E$	0	0	0	0	0	0	0	1	0

Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.



數位邏輯設計

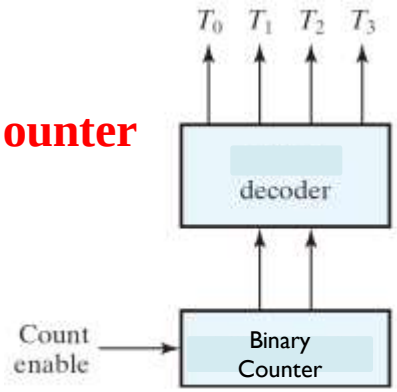
6.5.4 Comparison of Counters

主講者：吳順德

國立臺灣師範大學機電工程系 副教授

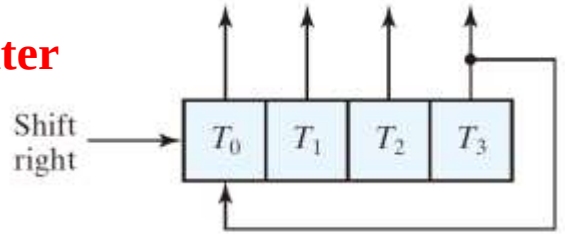
Example: Generating 16 timing signal

Binary Counter



4 flips flops + 4X16 decoder

Ring Counter

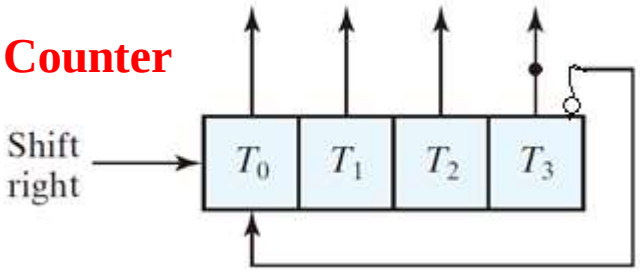


(a) Ring-counter (initial value = 1000)

16 flips flops

decoding circuit is unnecessary!

Johnson Counter



8 flips flops + simple decoding circuit

Reference

- M. M. Mano and M. D. Ciletti, “Digital Design," 5th Ed., Pearson Education Limited, 2013.