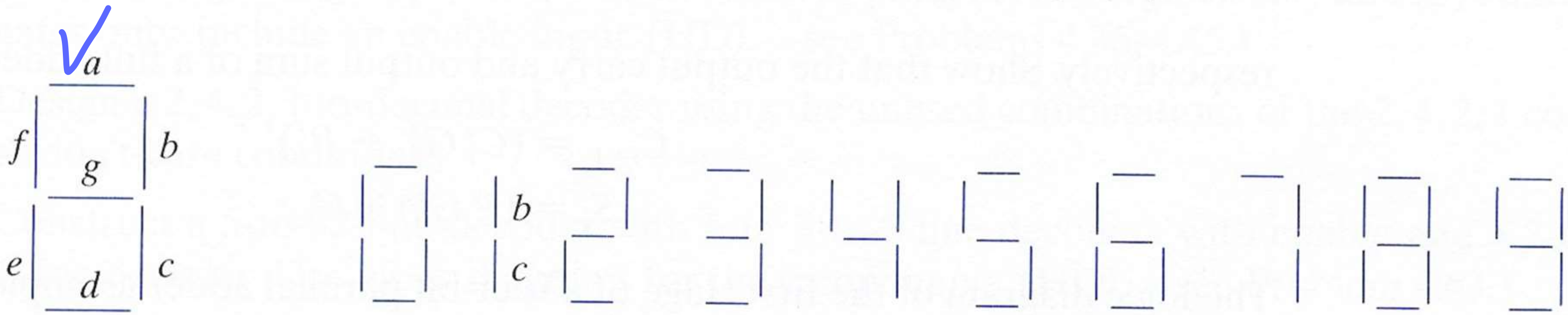
Homework #6

4.6 A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise.

(a)* Design a 3-input majority circuit by finding the circuit's truth table, Boolean equation, and a logic diagram.

4.9 An ABCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder *(a, b, c, d, e, f, g)* select the corresponding segments in the display, as shown in Fig. P4.9(a). The numeric display chosen to represent the decimal digit is shown in Fig. P4.9(b). Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display. (HDL—see Problem 4.51.)



(a) Segment designation

(b) Numerical designation for display

FIGURE P4.9

4.12 Design a half-subtractor circuit with inputs x and y and outputs *Diff* and B_{out}. The circuit subtracts the bits $y - x$ and places the difference in D and the borrow in B_{out}.

(a) Design a full-subtractor circuit with three inputs x, y, B_{in} and two outputs *Diff* and B_{out}. The circuit subtracts $y - x - B_{in}$, where B_{in} is the input borrow, B_{out} is the output borrow, and *Diff* is the difference.

4.28 Using a decoder constructed with NAND gates (similar to Fig. 4.19) and external gates, design the combinational circuit defined by the following three Boolean functions:

(a) $F_1 = xy + xz' + yz'$ 67, 46, 26 = $\Sigma(2,4,6,7) = F_1$

$F_2 = xz + xy + yz$

$F_3 = y'z + x'y'z' + xy$

4.35 Implement the following Boolean function with a 4 × 1 multiplexer and external gates.

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(a)* $F_1(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$

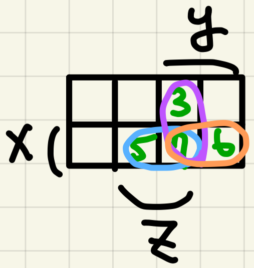
R53

8×1 ?

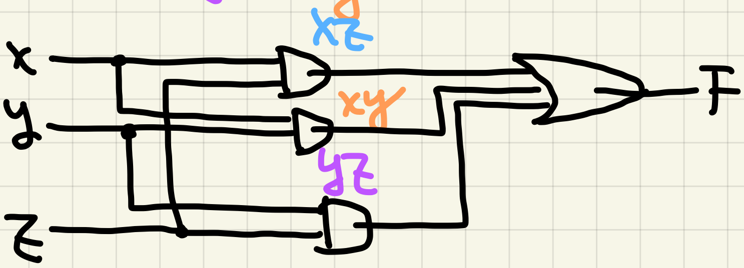
2×1 ?

4.6

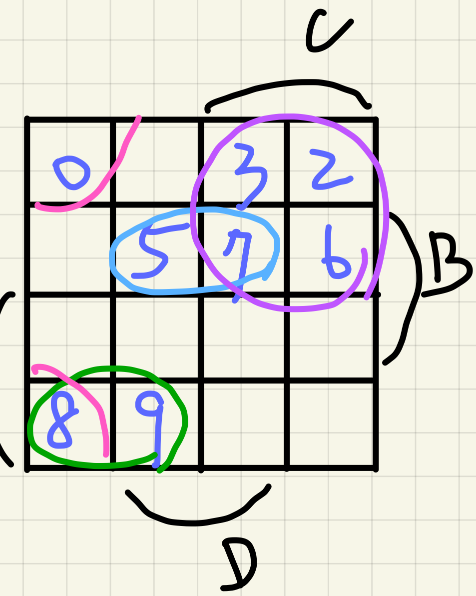
	x	y	z	Output
	0	0	0	0
	0	0	1	0
	0	1	0	0
	1	0	0	0
6	1	1	0	1
5	1	0	1	1
3	0	1	1	1
7	1	1	1	1



$F = xz + yz + xy$



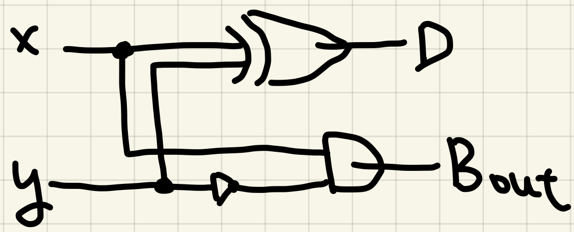
4.9 (a)



$a = AB'C' + A'BD + B'C'D' + A'C$

4.12 ① half-subtractor

x	y	D	B_{out}
0	0	0	0
0	1	1	0
1	0	1	1
1	1	0	0



$\Rightarrow D = x \oplus y = xy' + x'y$

$B_{out} = xy'$

借後的 diff　　借 =

② x	y	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	~~1~~ 0	1
1	1	0	0	0
1	1	1	1	1

4.28 (a)

$F_1 = (m_2 + m_4 + m_6 + m_7)$

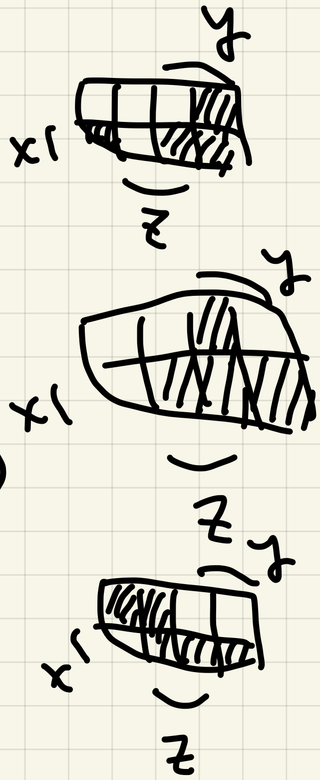
$= (m_2' m_4' m_6' m_7')'$

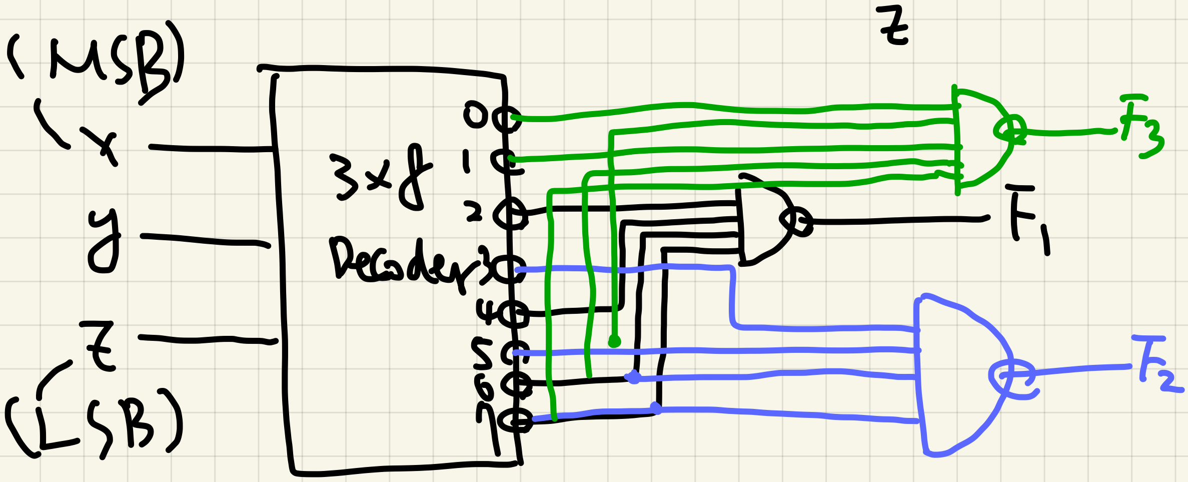
$F_2 = (m_3 + m_5 + m_6 + m_7)$

$= (m_3' m_5' m_6' m_7')'$

$F_3 = (m_0 + m_1 + m_5 + m_6 + m_7)$

$= (m_0' m_1' m_5' m_6' m_7')'$





4.35(a)

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$AB=00$
$F=D$

$AB=01$
$F=C'D'$
$=(C+D)'$

$AB=10$
$F=CD$

$AB=11$
$F=1$