7.8 **(a)** $\frac{512\text{ K}}{64\text{ K}} = 8$ chips

(b) $512\text{ K} = 2^{19} \Rightarrow$ 19-bit address lines.

$64\text{ K} = 2^{16} \Rightarrow$ 16-lines are connected to each chip

and remaining $(19 - 16) = 3$ are for selecting the chips.

(c) $19 - 16 = 3$ lines with 3×8 decoder.

7.12

Bit position	1	2	3	4	5	6	7	8	9	10	11	12	13
	P_1	P_2		P_4				P_8					
(a)	0	1	1	1	0	0	1	0	1	0	1	0	0
(b)			1	1	1	1	0	1	0	1	0	0	1		1	1

9-bit data word = 100110100

9-bit data word = 101000111

7.13 (**a**) 25 bits ⇒ Check bits K = 5 ⇒ 6 parity bits

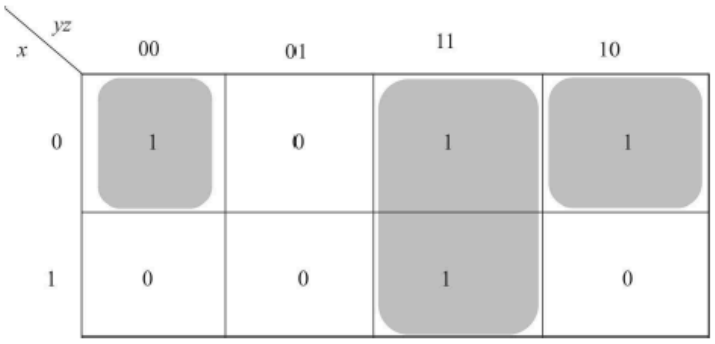
+1 bit

(**b**) 55 bits ⇒ Check bits K = 6 ⇒ 7 parity bits

+1 bit

7.18 **(a)** 5-bit binary multiplier:
Size of ROM = $2^{10} \times 10$ = 1 K × 10 ROM
(b) 5-bit adder-subtractor:
Size of ROM = $2^{11} \times 6$ = 2 K × 6 ROM

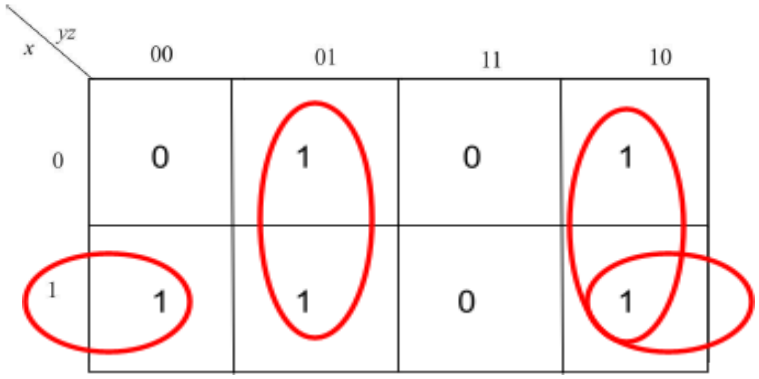
7.19



$A(x, y, z) = \Sigma(0, 2, 3, 7)$

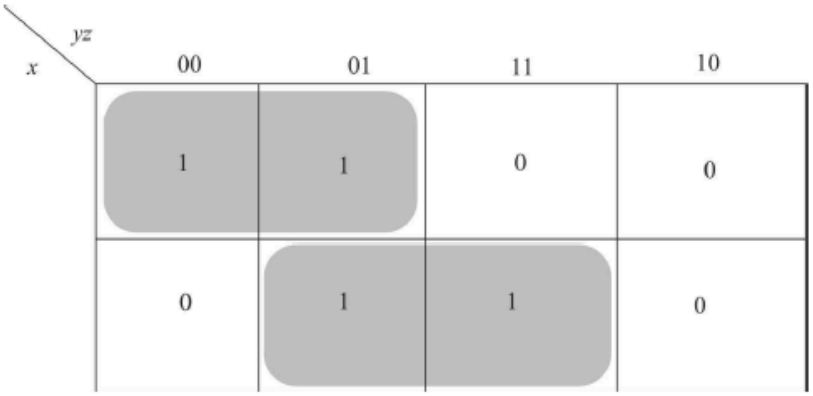
$= x'z' + yz$

A' = $xz' + y'z$



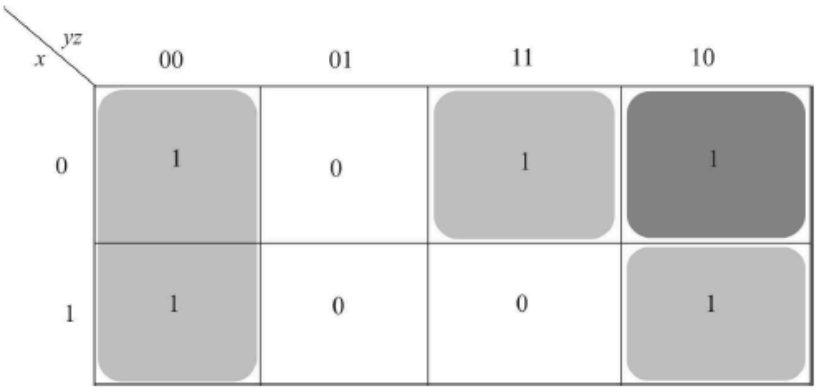
$B(x, y, z) = \Sigma(1, 2, 4, 5, 6)$

B $(x, y, z) = y'z + yz' + xz'$



$C(x, y, z) = \Sigma(0, 1, 5, 7)$

$C(x, y, z) = x'y' + xz$



$D(x, y, z) = \Sigma(0, 2, 3, 4, 6)$
$D(x, y, z) = z' + x'y$
$D' = Z(x + y') = xz + y'z$

PLA programming table:

					Outputs			
		Inputs			(C)	(T)	(T)	(C)
	Product term	x	y	z	A	B	C	D
xz’	1	1	-	0	1	1	-	-
y’z	2	-	0	1	1	1	-	1
yz’	3	-	1	0	-	1	-	-
x’y’	4	0	0	-	-	-	1	-
xz	5	1	-	1	-	-	1	1