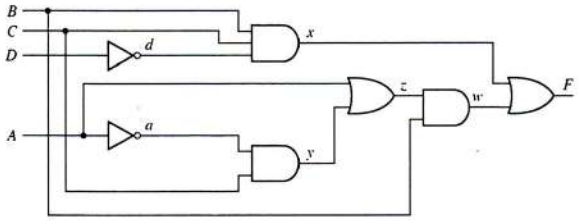
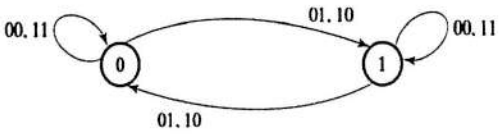
Department of Computer Science
National Chiao Tung University
Digital System Design
Second Midterm Exam 12/03/2010

1. (10%) Obtain the simplified Boolean expressions for output F in terms of the input variables for the circuit shown below (left).





2. (10%) Consider the state diagram shown above (right). Design a sequential circuit with a JK flip-flops A, and two inputs x and y.

3. (12%) Design a code converter that converts a decimal digit from the excess-3 code to BCD.

4. (8%) Implement $F(A,B,C,D) = \sum(3,5,7,8,9,11,15)$ with a multiplexer.

5. (8%) A combinational circuit is specified by the following Boolean functions:

   $$F_1(A,B,C) = \sum(3,5,7), \quad F_2(A,B,C) = \sum(1,2,3,5,6), \quad F_3(A,B,C) = \sum(0,4)$$

   Implement the circuit with a decoder constructed with AND gates, and NOR or OR gates, connected to the decoder output.

6. (20%) Design a JK flip-flop using a T flip-flop. Assume the T flip-flop has a propagation delay of 10ns, a setup time of 8ns, and a hold time of 6ns. (i) What is the setup/hold time for the JK flip-flop? (ii) What is the maximum clock frequency the circuit can operate if both J and K are connected to 1. (Assume all gates have 5ns propagation delay.)

7. (10%) Derive the state diagram of a circuit that can recognize the occurrence of bits 0100 on input x by making output y equal to 1.

8. (10%) Derive the state table of a Moore machine with T three flip-flops inputs T_A, T_B, and T_C connected to F_1, F_2, and F_3, respectively, in Problem 5.

9. (12%) Design a 3-bit magnitude comparator using three 1-bit comparators and some gates. Use block diagrams for the 1-bit comparators. Redo the design using a 4-bit adder-subtractor.