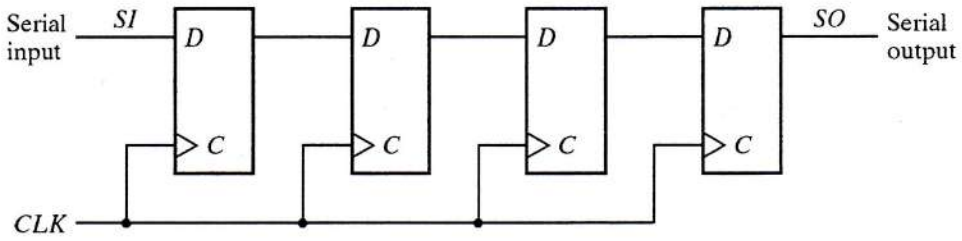
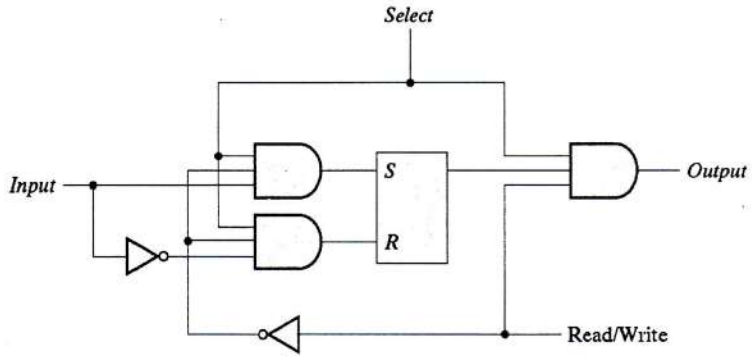
Department of Computer Science
National Chiao Tung University
Digital System Design
Final Exam 1/21/2011

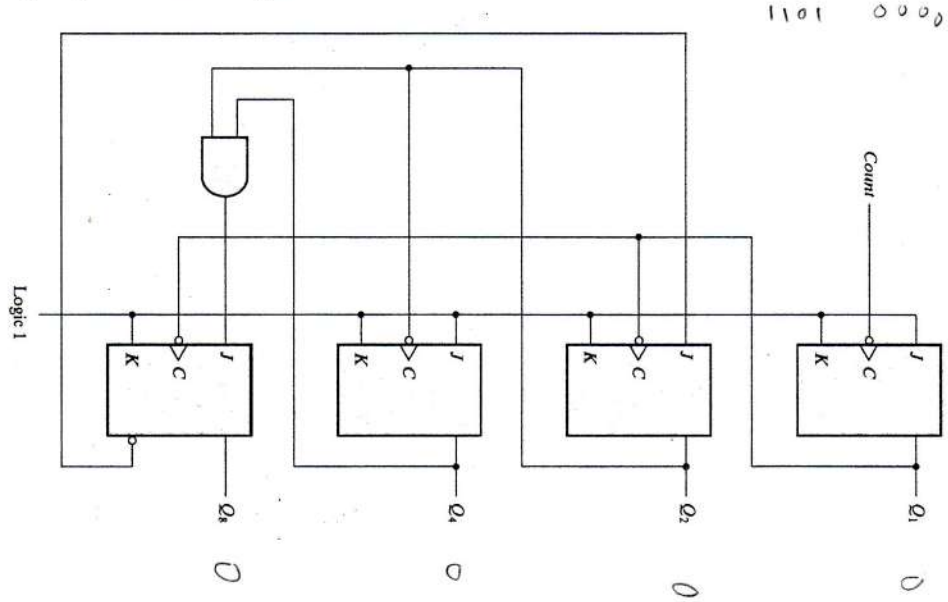
1. (10%) Include a synchronous clear input in the shift register shown below. Briefly explain why we cannot replace the four *D* flip-flops with four *D* latches.



2. (10%) Describe the read/write operations of the SRAM memory cell shown below. Briefly explain why the 1-bit data can be stored with a latch instead of using a flip-flop.



3. (10%) Analyze following BCD ripple counter to determine whether the counter will operate properly if a noise signal sends the circuit to unused states 1100 or 1111.



4. (10%) Draw the logic diagram of a three-bit binary ripple countdown counter, using flip-flops that trigger on the positive edge of the clock. Briefly explain whether we can load the content of an n-bit ripple counter to a register for arbitrarily large n.

5. (15%) Design a counter using D flip-flop for Q_4, T flip-flop for Q_2, and JK flip-flop for Q_1, that goes through the following repeated sequence: 0, 1, 2, 4, 5, 6. Determine whether the counter is self-correcting.

6. (10%) Show that a mod-12 counter can be constructed from a four-bit binary counter (a mod-16 counter) with asynchronous clear and a NAND gate. Briefly explain whether we do this for both ripple counter and synchronous counter.

7. (12%) Use a 16K × 8 RAM to briefly explain:
   (i) *Coincident Decoding,*
   (ii) *Address Multiplexing.*
   What are the advantages of using (i) and (ii) for a memory unit?

8. (10%) A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word what was written into memory if the 12-bit word read out is as follows:
   (a) 111000001010,
   (b) 101101101000.

9. (10%) Tabulate the PLA programming table for the three Boolean functions listed below. Minimize the numbers of product terms.

$$F_1(A,B,C) = \sum(3,5,7),$$

$$F_2(A,B,C) = \sum(1,2,3,5,6),$$

$$F_3(A,B,C) = \sum(0,4)$$

10. (8%) Specify the size of a ROM (number of words and number of bits per word) that will accommodate the truth table for the following combinational circuit components:
    (a) a 4-bit adder-subtractor,
    (b) a BCD-to-excess-3-code convertor (can use an inverter).