Department of Computer and Information Science
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# Digital Systems

Final Exam 06/16/2003

1. Convert a *D* flip-flop into a *JK* flip-flop, using external gates. Please follow the sequential circuit design procedure starting from a state table with *J* and *K* as circuit inputs. (10%)

2. Derive the state diagram of a sequence recognizer using the minimum number of states. The function of the circuit is to recognize the occurrence of bits 0010 on input *X* by making output *Z* equal to 1 only when the previous three inputs to the circuit were 001 and current input is a 0. (10%)

3. Design a counter with the following repeated count sequence: (*A*,*B*,*C*) = 0, 1, 3, 7, 6, 4. Use *JK* flip-flop for *C* and *D* flip-flops for *A* and *B*. Give the count sequence for an initial count equal to 2. (16%)

4. Give an example of *clock gating*. What is the main problem of a digital system which adopts the strategy of *clock gating*? (8%)

5. Consider the 4-bit synchronous binary counter shown below. Give the state change(s) which will require the longest time for the outputs to change? As the frequency of the clock input increased, which state change(s) will go wrong first? (10%)

6. Implement the following two Boolean functions with a PLA: (10%)

$$F_1(W,X,Y) = \sum m(1,2,3,4)$$

$$F_2(W,X,Y) = \sum m(3,5,6,7)$$

7. How many address lines and input-output data lines are needed for a 256K × 64 RAM chip? Assuming that the RAM cell array is square and the chip uses coincident decoding by splitting the internal decoder into row select and column select. What is the size of each decoder? (10%)

8. Briefly explain the following three techniques through which SRAM bits can be used to control a programmable logic device, e.g., in a Xilinx FPGA. (6%)

   (a) Pass transistor control
   (b) Multiplexer control
   (c) Look up table implementation

9. Using an *n*-bit counter with parallel load, an *n*-bit adder, and external gates, draw the logic diagram that implements the following register transfers. (10%)

$$\overline{C_1}\,\overline{C_2}\colon AR \leftarrow AR + BR$$

$$\overline{C_1}\,C_2\colon AR \leftarrow AR - BR$$

$$C_1\colon AR \leftarrow AR + 1$$

10. Inputs $X_i$ and $Y_i$ of each full adder in an arithmetic circuit have digital logic specified by the Boolean functions

$$X_i = A_i \qquad\qquad Y_i = \overline{B_i}S + B_i\overline{C_{in}}$$

where $S$ is a selection variable, $C_{in}$ is the input carry, and $A_i$ and $B_i$ are input data for stage $i$. Derive the function table of the arithmetic circuit. (10%)