CA homework# 4 report

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1

Critical path:

```
ABC: Start-point = pi22 (\o_i_addr_r [3]).  End-point = po65 ($0\o_i_addr_w[63:0] [63]).
ABC: + write_blif <abc-temp-dir>/output.blif
```

Put pipeline registers between two stages so that it can reduce clock time.

2

First, we can solve a parts of data hazard with forwarding. However, there are still some of situation we cannot solve. Therefore, we need to detect whether the hazard happens with hazard detection unit and flush the instruction if hazard happens.

3

We have to handle the situation of the branch misprediction with flushing the instruction and stalling.

4

workload 1: It's a long loop, that is, it is not that often to process branch instructions.
workload 2: There are many blocks in workload 2 and also many branch instructions.
workload 3: It's a shorter loop, that is, it is often to process fixed branch instructions.

I think the workload 2 can be improved tremendously because there are more branch instructions and it will definitely jump to another block.

5

No. Once we insert another stage, we need extra registers and resources so that the total overhead will increase. When the number of stages exceeds a number, then the latency will become higher than the time that inserting stages saves.