CS224: Assignment 5

Weightage: 10%

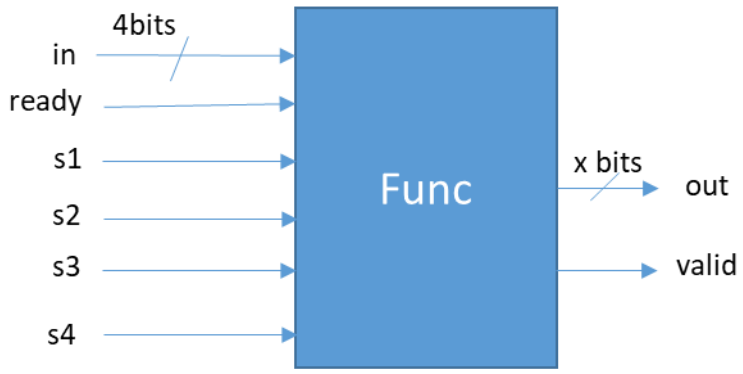
Date of Demonstration: 18th March 2025 (2PM-5PM) in H/W Lab.

Problem Statement: RTL Implement the following function in Verilog and demonstrate using FPGA.

Implementation using FPGAs

```
func(x, dx, u, a, y){
    input: x, dx, u, a;
    output: y
    while (x < a) {
            u1 = u - (3*x*u*dx) - (3*y*dx);
            y1 = y + (u*dx);
            x1 = x + dx;
            x = x1, y = y1, u = u1;
    }
}
```

1. Write the Verilog code and test bench and show the simulation results.
2. In hardware implementation, consider all inputs are of 4 bits and decide the width of each intermediate variable and outputs as needed.
3. Since the FPGA board given to you does not have these many inputs switches, read four inputs using a single port only as shown below. the figure shows the interface pf your hardware implementation. The set signal s1, s2, s3 and s4 are corresponding to reading inputs x, dx, a, y, respectively. Set them one by one to read inputs from the input ports. Once all values are read, set the ready to 1 to start the computation. Once the output is ready, set the valid port to 1 to indicate when is your output is valid. Use the switch for in, ready, s1, s2, s3 and s4. The out and valid will be shown using the outputs in the FPGA board.



4. As discussed in tutorials, your objective is to create a datapath and a controller FSM to execute the behavior using minimum number of resources. Obviously, you need some K (latency) number of time steps to complete the execution.
5. There will tradeoff between the resource and latency. Your objective is to optimize the area/latency product of the design.
6. First read the inputs. Then, plan the number of registers and adders and multipliers/adders needed. Plan clock wise execution of the operations and the number of time steps needed. Write the code for datapath and controller.

Guidelines:

- All the member of the group needs to be present at the time of Demonstration of the assignment. All the absent members will be awarded 0 marks for the assignment. Please show your ID card at the time of demonstration.
- The grading will be based on (a) Correctness, (b) Quality of design, (c) resource*latency optimization, (e) Cleanliness/modular design, (f) Use of proper Comment/Naming of the design components and (g) Questionnaire and explanation and (h) correctness of your Verilog implementation.
- The Verilog implementation will also be checked during evaluation.

Submission:

You need to submit following items in a zip folder. For each group, one of the member must submit the report. One submission per group. We will share the marks in teams against your submission each Assignment.

1. A PDF file containing (i) clear diagram of the design (ii) Logic behind the circuit obtained. The report must be available during Lab evaluation.
2. Verilog code of your design
3. Testbench file