CS224: Assignment 4

Weightage: 7%

Date of Demonstration: 18th February 2025 (2PM-5PM) in H/W Lab.

Problem Statement: Implement a 4-bit Synchronous Binary UP or UP/Down counter in Breadboard.

Implementation using Breadboard and ICs

(Marks: 75%) Implement a 4-bit Synchronous Binary UP counter. The counter has four inputs: (i) clock, (ii) reset (1 bit) (iii) set (1 bit) and (iv) value (4 bits). The counter counts from 0 to 15 and then backs to 0. In each clock, the counter value is up by 1. Once it reaches 15, the next value is 0. By default, the set and reset are zero. When reset signal is 1, the counter value reset to 0 in the next clock. When set value is 1, the counter set to the "value". The reset has higher priority over set. Use automatic clock available in the breadboard for demonstration purpose. Show counter outputs to LEDs of the breadboard.

(Additional Marks 25%) There will be higher weightage for implementing UP/DOWN counter. In addition to above features, it has It has an "up" control input. When the up input is 1, the circuit counts up. When the up input is 0, it counts down. The reset has higher priority over set and up/down. Set has higher priority over up/down. You are allowed to use any flipflop or register. However, you cannot use the counter IC.

You have to implement either UP or UP/DOWN counter. The TA will evaluate only one.

Guidelines:

- All the member of the group need to be present at the time of Demonstration of the assignment. All the absent members will be awarded 0 marks for the assignment. Please show your ID card at the time of demonstration.
- The grading will be based on (a) Correctness, (b) Quality of design, (c) Wire optimization, (d) Optimum number of IC used, (e) Cleanliness in design (Wire and Chips should be organized to look good), (f) Use of proper Comment/Naming/Labeling of the wires and (g) Questionnaire and explanation and (h) correctness of your Verilog implementation.
- Submission: (i) Verilog code of the above counter (ii) Test bench of the counter (iii) A clean diagram to shown the IC used in your breadboard implementation. Put all of them in a single folder and submit as zip file.
- The Verilog implementation will also be checked during evaluation.

Submission:

You need to submit following items in a zip folder. For each group, one of the member must submit the report. One submission per group. We will share the marks in teams against your submission each Assignment.

1. A PDF file containing (i) clear diagram of the design of your counter (ii) Logic behind the circuit obtained and (iii) A clean diagram to shown the IC used in your breadboard implementation. The report must be available during Lab evaluation.
2. Verilog code of the counter
3. Testbench file