CS224: Assignment 3

Weightage: 10%

Date of Demonstration: 11th February 2025 in H/W Lab (3PM-6PM)

Problem Statements:

1. Implement a 4 bits two inputs Carry Look Ahead Adder (CLA) in Verilog. Make the code modular. Write test bench for simulation. Synthesize and simulate your design using Vivado/Xilinx ISE tool. Write test bench for simulation. Download bit file of your design to FPGA board and demonstrate the working of your design on FPGA.
2. Implement a 3 bits two inputs Carry Look Ahead Adder in Breadboard. Show the Demo during evaluation.
3. Implement a 32 bits three inputs Carry Save Adder (CSA) in Verilog. You can use a ripple carry adder (RCA) for the second stage of the CSA. Synthesize and simulate your design using Vivado/Xilinx ISE tool. Compare the area and delay of the design with respect to a 32 bits three inputs Ripple Carry Adder. Learn about CSA: https://en.wikipedia.org/wiki/Carry-save_adder
4. Find the number of 2 inputs gates needed for a 32 bits three inputs CLA (no need to implement 32 bits 3 inputs CLA, just calculate).

Guidelines:

- All the member of the group needs to be present at the time of Demonstration of the assignment. All the absent members will be awarded 0 marks for the assignment. Please show your ID card at the time of demonstration.
- Grading will be based on (a) Correctness, (b) Quality of design, (c) modular design, (d) Use of proper Comment/Naming/Labeling of the wires and (e) Questionnaire and explanation.
- The quality of the Verilog design will be based on FPGA resource utilization (Synthesis Report: number of LUTs, register, FF, DSP, BRAM etc.) and timing (Clock period).

Support:

- All the TAs and Instructor of CS224 will be available in Lab timing. You can ask TAs about the version and licensing and installation of Xillinx ISE/Vivado software.

- Mr. Hemanta Nath will issue up to two FPGA Boards (At most of one BASYS/one ZYBO/one ATLYS/one Nexys A7) for each group for the entire semester. You need to keep the board with you for the entire semester and you are allowed to take issued FPGA board to your Hostel.

- Based on your requirement, please issue the board from Lab in charge. We have tested working of Xilinx ISE/Vivado on Window 10 and Ubuntu 20/22.04 PC.

- **Link for download the software**: http://jatinga.iitg.ernet.in/download/

- **License info**: Set the following:

  XILINXD_LICENSE_FILE=2103@172.16.112.7

- The software is already installed in the Lab PC. If not, please install on the lab PC and use the above license to use the software. Get familiar with the Software. We are going to use this in the entire assignment.

Upload:

- A zip folder (in group name) containing the following: (i)Verilog file of the RCA, CSA and CLA (ii) Verilog file representing the test bench. (iii) simulation results. (iv) A brief report on performance comparison. (v) Clearly mention the ICs used for your breadboard implementation.
- Deadline 11th February 2025 EOD.