

# Ho Seok Kim

<https://hskim1324.github.io> | thomas1324@korea.ac.kr

## RESEARCH INTERESTS

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Computer Architecture, Energy-efficient Computing, DRAM Reliability

## EDUCATION

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### Korea University

*M.S. in Computer Science and Engineering*

- Advised by Professor Sung Woo Chung
- GPA: 4.44 / 4.5

Mar. 2023 – Feb. 2025 (Expected)

Seoul, Korea

### Korea University

*B.S. in Computer Science and Engineering*

- Graduated with Honors
- GPA: 3.91 / 4.5 (Major GPA: 4.08 / 4.5)
- Two-year break for military service (Apr. 2019 - Nov. 2020)

Mar. 2017 – Feb. 2023

Seoul, Korea

## PUBLICATIONS

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**Hoseok Kim**, Seung Hun Choi, Young-ho Gong, Joonho Kong, and Sung Woo Chung, “**Sparrow ECC: A Lightweight ECC Approach for HBM Refresh Reduction towards Energy-efficient DNN Inference**”, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, 2024. (**Best Paper Award**)

Yeonho Yoo, Gyeongsik Yang, Jeunghwan Lee, Changyong Shin, **Hoseok Kim**, and Chuck Yoo, “**TeaVisor: Network Hypervisor for Bandwidth Isolation in SDN-NV**”, *IEEE Transactions on Cloud Computing (TCC)*, 2022.

(Domestic) **Hoseok Kim**, Yeonho Yoo, Gyeongsik Yang, and Chuck Yoo, “**Predicton of Multi-Path Weights for Accurate Traffic Distribution of Datacenter Switches**”, *Korea Computer Congress (KCC)*, 2022.

(Domestic) **Hoseok Kim**, Yeonho Yoo, Gyeongsik Yang, and Chuck Yoo, “**Analysis of Multipath Routing Techniques for Datacenter Switches**”, *Korea Software Congress (KSC)*, 2021.

## RESEARCH EXPERIENCE

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### Research Assistant

*SoC & Microprocessor Research Lab. (Advisor: Professor Sung Woo Chung)*

Mar. 2023 – Current

Seoul, Korea

- Designed an error correction code (ECC) for energy-efficient and accurate DNN inference on HBM, leveraging data patterns found during undergraduate research. (**paper based on work accepted for ISLPED 2024**)
- Conducted power and thermal simulations of a real-world processing-in-memory (PIM) device (GDDR6-AiM) when running various DNN inference applications using Gem5-Aladdin, DRAMsim3, and HotSpot 7.0.
- Gave oral presentation on “Sparrow ECC: A Lightweight ECC Approach for HBM Refresh Reduction towards Energy-efficient DNN Inference” at ISLPED 2024, **best paper award** among 167 submissions.
- Gave poster presentation on “Sparrow ECC: A Lightweight ECC Approach for HBM Refresh Reduction towards Energy-efficient DNN Inference” at DAC 2024 Young Fellows Program.

### Undergraduate Researcher

*SoC & Microprocessor Research Lab. (Advisor: Professor Sung Woo Chung)*

Sept. 2022 – Feb. 2023

Seoul, Korea

- Conducted research to identify data patterns in DNN weights across various numerical formats and models.

### Undergraduate Researcher

*Operating Systems Lab. (Advisor: Professor Chuck Yoo)*

Jun. 2021 – Aug. 2022

Seoul, Korea

- Designed an accurate weighted multi-path routing algorithm for datacenter network switches, especially for virtual network switches such as Open vSwitch, published and submitted papers based on work.
- Gave poster presentation on “Predicton of Multi-Path Weights for Accurate Traffic Distribution of Datacenter Switches” at KCC 2022.
- Gave virtual presentation on “Analysis of Multipath Routing Techniques for Datacenter Switches” at KSC 2021.

## HONORS AND AWARDS

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<b>Best Paper Award</b> , ACM/IEEE International Symposium on Low Power Electronics and Design	Aug. 2024
<b>Young Fellow</b> , Design Automation Conference	Jun. 2024
<b>Semester High Honors</b> , Korea University	Spring 2021, Fall 2021, Spring 2022, Fall 2022
<b>Participation Award</b> , Korea Computer Congress	Jul. 2022
<b>Participation Award</b> , Korea Software Congress	Dec. 2021

## PATENTS

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(Domestic) Sung Woo Chung, **Hoseok Kim**, and Seung Hun Choi, “**Error Correction Code of High-Bandwidth Memory Device and Operating Method Thereof**”, *Korea Application Number: 10-2024-0140286*, 2024.

## TEACHING EXPERIENCE

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<b>Teaching Assistant</b>	Fall 2023
<i>Logic Design (Instructor: Professor Sung Woo Chung)</i>	<i>COSE221</i>
<ul style="list-style-type: none"><li>Undergraduate level course, 80+ students.</li><li>Gave six 1.25 hour lectures on basics of Verilog HDL and logic synthesis using an Altera DE2 FPGA board.</li><li>Designed several Verilog HDL coding assignments.</li></ul>	

## TECHNICAL SKILLS

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**Advanced:** C, C++, Python, Shell  
**Moderate:** Verilog, ARM Assembly, Linux  
**Novice:** Java

## PROFESSIONAL SERVICE

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<b>Reviewer</b>	ACM/IEEE International Conference on Computer-Aided Design (ICCAD) 2024
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## LANGUAGE PROFICIENCY

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<b>IBT TOEFL</b>	109 (Reading: 30, Listening: 30, Speaking: 22, Writing: 27)
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## REFERENCES

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<b>Sung Woo Chung</b> Professor Department of Computer Science and Engineering College of Informatics Korea University	Email: swchung@korea.ac.kr <a href="http://smr1.korea.ac.kr">http://smr1.korea.ac.kr</a>
<b>Gyeongsik Yang</b> Assistant Professor Department of Computer Science and Engineering College of Informatics Korea University	Email: g_yang@korea.ac.kr <a href="https://ss.korea.ac.kr">https://ss.korea.ac.kr</a>