Hoseok Kim

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RESEARCH INTERESTS

Energy-efficient Edge Computing, NPU Architecture

EDUCATION

Purdue University   Aug. 2025 – Current
Ph.D. in Electrical and Computer Engineering   *West Lafayette, IN*
- Advisor: Professor Vijay Raghunathan

Korea University   Mar. 2023 – Feb. 2025
M.S. in Computer Science and Engineering   *Seoul, Korea*
- Advisor: Professor Sung Woo Chung
- GPA: 4.44 / 4.5

Korea University   Mar. 2017 – Feb. 2023
B.S. in Computer Science and Engineering   *Seoul, Korea*
- GPA: 3.91 / 4.5 (Major GPA: 4.08 / 4.5)
- Two-year break for military service (Apr. 2019 - Nov. 2020)

PUBLICATIONS

Hoseok Kim, Seung Hun Choi, Young-ho Gong, Joonho Kong, and Sung Woo Chung, **"Sparrow ECC: A Lightweight ECC Approach for HBM Refresh Reduction towards Energy-efficient DNN Inference"**, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, 2024. ***(Best Paper Award)***

Yeonho Yoo, Gyeongsik Yang, Jeunghwan Lee, Changyong Shin, **Hoseok Kim**, and Chuck Yoo, **"TeaVisor: Network Hypervisor for Bandwidth Isolation in SDN-NV"**, *IEEE Transactions on Cloud Computing (TCC)*, 2022.

(Domestic) **Hoseok Kim**, Yeonho Yoo, Gyeongsik Yang, and Chuck Yoo, **"Predicton of Multi-Path Weights for Accurate Traffic Distribution of Datacenter Switches"**, *Korea Computer Congress (KCC)*, 2022.

(Domestic) **Hoseok Kim**, Yeonho Yoo, Gyeongsik Yang, and Chuck Yoo, **"Analysis of Multipath Routing Techniques for Datacenter Switches"**, *Korea Software Congress (KSC)*, 2021.

RESEARCH EXPERIENCE

Research Assistant   Mar. 2023 – Current
SoC & Microprocessor Research Lab. (Advisor: Professor Sung Woo Chung)   *Seoul, Korea*
- Designed an error correction code (ECC) for energy-efficient and accurate DNN inference on HBM, leveraging data patterns found during undergraduate research. (***a paper based on this work won the best paper award in ISPLED 2024***)
- Conducted power and thermal simulations of a real-world processing-in-memory (PIM) device (GDDR6-AiM) when running various DNN inference applications using Gem5-Aladdin, DRAMsim3, and HotSpot 7.0.
- Gave oral presentation on "Sparrow ECC: A Lightweight ECC Approach for HBM Refresh Reduction towards Energy-efficient DNN Inference" at ISLPED 2024, **best paper award** among 167 submissions.
- Gave poster presentation on "Sparrow ECC: A Lightweight ECC Approach for HBM Refresh Reduction towards Energy-efficient DNN Inference" at DAC 2024 Young Fellows Program.

Undergraduate Researcher   Sept. 2022 – Feb. 2023
SoC & Microprocessor Research Lab. (Advisor: Professor Sung Woo Chung)   *Seoul, Korea*
- Conducted research to identify data patterns in DNN weights across various numerical formats and models.

Undergraduate Researcher   Jun. 2021 – Aug. 2022
Operating Systems Lab. (Advisor: Professor Chuck Yoo)   *Seoul, Korea*
- Designed an accurate weighted multi-path routing algorithm for datacenter network switches, especially for virtual network switches such as Open vSwitch, published and submitted papers based on work.
- Gave poster presentation on "Predicton of Multi-Path Weights for Accurate Traffic Distribution of Datacenter Switches" at KCC 2022.
- Gave virtual presentation on "Analysis of Multipath Routing Techniques for Datacenter Switches" at KSC 2021.

Honors and Awards

Best Paper Award, ACM/IEEE International Symposium on Low Power Electronics and Design	Aug. 2024
Young Fellow, Design Automation Conference	Jun. 2024
Semester High Honors, Korea University	Spring 2021, Fall 2021, Spring 2022, Fall 2022
Participation Award, Korea Computer Congress	Jul. 2022
Participation Award, Korea Software Congress	Dec. 2021

Patents

(Domestic) Sung Woo Chung, <u>**Hoseok Kim**</u>, and Seung Hun Choi, **"Error Correction Code of High-Bandwidth Memory Device and Operating Method Thereof"**, *Korea Application Number: 10-2024-0140286*, 2024.

Teaching Experience

Teaching Assistant — Fall 2023
Logic Design (Instructor: Professor Sung Woo Chung) — *COSE221*

- Undergraduate level course, 80+ students.
- Gave six 1.25 hour lectures on basics of Verilog HDL and logic synthesis using an Altera DE2 FPGA board.
- Designed several Verilog HDL coding assignments.

Technical Skills and Tools

Skills: C, C++, Python, Shell, Verilog, ARM Assembly
Tools: PyTorch, Gem5-Aladdin, DRAMsim, HotSpot

Language Proficiency

IBT TOEFL — 109 (Reading: 30, Listening: 30, Speaking: 22, Writing: 27)

References

Vijay Raghunathan
Professor
Elmore Family School of Electrical and Computer Engineering — Email: vr@purdue.edu
Purdue University — https://engineering.purdue.edu/ESL/

Sung Woo Chung
Professor
Department of Computer Science and Engineering
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