Instruction Set Architecture

Computer Architecture & Design

Basic Architecture:

This machine has 16 16-bit registers directly visible to the programmer. It has 16 address lines, and it can address 2^{16} = 65536 16-bit memory words. Negative numbers are represented in two's complement notation.

The machine has a 4-bit condition code register organized from most significant to least significant with the following bits: carry, overflow, negative, zero. Condition codes are set by arithmetic operations, and they control conditional branches.

Startup & Operation:

The architecture includes eight vectored address entries in memory locations 0, 1, 2, 3, 4, 5, 6, and 7. The program starting address is found in memory location 0 when the processor emerges from receiving a reset signal input. Thus, initial startup requires that the initial program address be fetched from memory address 0 prior to starting the standard fetch-execute cycle.

The architecture also has a single external asynchronous interrupt input. Interrupts are handled by placing the return address in general-purpose register 15. Control is then transferred to the address contained in memory address 1. Thus, it is possible to place the interrupt service routine (ISR) anywhere in memory with a pointer to the start of the ISR placed in memory location 1.

Instruction Set:

Instruction	Operands	Description
Memory Transfer		
LD	Dest, Base, Offset	Load destination register from memory: Calculate address as sum of base register contents plus unsigned offset.
ST	Src, Base, Offset	Store source register contents in memory: Calculate address as sum of base register contents plus unsigned offset
Register Transfer		
MOV	Dest, Src	Copy contents of source register into destination register
Load Immediate		
LIL	Dest, Value	Load destination register with sign extended value
LIH	Dest, Value	Load upper half of destination register with value and leave lower half unchanged
Arithmetic		
ADD	Dest, Src	Add contents of source register to contents of destination register and place result in destination register. Set condition codes.
ADC	Dest, Src	Add contents of source register to contents of destination register. Add 1 if the carry condition code is 1. Then place result in destination register. Set condition codes.
SUB	Dest, Src	Subtract source register contents from destination register contents and place result in destination register. Set condition codes.
SBC	Dest, Src	Subtract contents of source register from contents of destination register considering the carry condition code and place result in destination register. Set condition codes
Logical		
AND	Dest, Src	Logical AND contents of source register to contents of destination register and place result in destination register.
OR	Dest, Src	Logical OR contents of source register to contents of destination register and place result in destination register.
XOR	Dest, Src	Logical XOR contents of source register to contents of destination register and place result in destination register.
NOT	Dest, Src	Bitwise complement contents of source register and place result in destination register.

Instruction	Operands	Description
Shifts and Rotates		
SL	Dest, Src	Shift the source register contents left by one bit. Discard the most significant bit and shift in 0 from the right. Place the result in the destination register. Condition codes are not changed.
SRL	Dest, Src	Perform a logical right shift of the source register and place the result in the destination register. Discard the least significant bit and shift in 0 from the left. Condition codes are not changed.
SRA	Dest, Src	Perform an arithmetic right shift of the source register and place the result in the destination register. Discard the least significant bit and retain a copy of the most significant bit in the MSB position. Condition codes are not changed.
RRA	Dest, Src	Perform an arithmetic right rotate of the source register and place the result in the destination register. Copy the least significant bit from the source register into the carry condition bit and copy the most significant bit from the source register into the two most significant bits of the destination register.
RR	Dest, Src	Perform a right rotate of the source register and place the result in the destination register. Copy the least significant bit from the source register into the carry condition bit, and copy the carry condition bit into the most significant bit of the destination register.
RL	Dest, Src	Perform a left rotate of the source register and place the result in the destination register. Copy the carry condition bit into the least significant bit of the destination, and copy the most significant bit of the source into the carry condition bit.
Jump and Branches		
JMP	Base, Offset	*Unconditional Jump*: Add the contents of the base register with the sign-extended offset and place this value in the program counter.
JAL	Base, Offset	*Unconditional Jump and Link*: Add the contents of the base register with the sign-extended offset and place this value in the program counter. Place the address of the instruction following this JAL (the return address) in register 14.
BR	Offset	*PC-Relative Unconditional Branch*: Add the sign-extended offset to the address of this instruction to determine the address of the next instruction.
BC	Offset	*PC-Relative Branch on Carry*: If the carry condition bit is 1, add the sign-extended offset to the address of this instruction to determine the address of the next instruction.
BO	Offset	*PC-Relative Branch on Arithmetic Overflow*: If the arithmetic overflow condition bit is 1, add the sign-extended offset to the address of this instruction to determine the address of the next instruction.
BN	Offset	*PC-Relative Branch on Negative*: If the negative condition bit is 1, add the sign-extended offset to the address of this instruction to determine the address of the next instruction.
BZ	Offset	*PC-Relative Branch on Zero*: If the zero condition bit is 1, add the sign-extended offset to the address of this instruction to determine the address of the next instruction.
Other		
NOP		No Operation
EI		Enable Interrupt – Enables the handling of external interrupt signals
DI		Disable Interrupt – Disables the handling of external interrupt signals
SWI	Number	Software Interrupt – The number is 3-bits unsigned. The memory address given by this number (0-7) contains the address to be placed in the program counter. The next program counter value (the return address) is saved in register 15. The processor mode is switched to “supervisor.”
USR		Switch processor to “user” mode.

Instruction Coding:

The architecture encodes these instructions so that every instruction can fit within a single 16-bit instruction word. The most significant three bits of this word contain an operation code that identifies the instruction type. Several instruction types include other fields within the word that further identify the instruction. The shaded fields must be assigned as shown, but they are not used by the instruction.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
EI	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
DI	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
SWI	0	0	0	0	0	0	0	0	0	0	0	1	0	Int Number		
USR	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
LD	0	0	1	Dest Reg ID				Base Reg ID				Unsigned Offset Value				
ST	0	1	0	Src Reg ID				Base Reg ID				Unsigned Offset Value				
MOV	0	1	1	Dest Reg ID				Src Reg ID				0	0	0	0	0
LIL	1	0	0	Dest Reg ID				0	Signed Value							
LIH	1	0	0	Dest Reg ID				1	Signed Value							
ADD	1	0	1	Dest Reg ID				Src Reg ID				0	0	0	0	0
ADC	1	0	1	Dest Reg ID				Src Reg ID				0	0	0	0	1
SUB	1	0	1	Dest Reg ID				Src Reg ID				0	0	0	1	0
SBC	1	0	1	Dest Reg ID				Src Reg ID				0	0	0	1	1
AND	1	0	1	Dest Reg ID				Src Reg ID				0	0	1	0	0
OR	1	0	1	Dest Reg ID				Src Reg ID				0	0	1	0	1
XOR	1	0	1	Dest Reg ID				Src Reg ID				0	0	1	1	0
NOT	1	0	1	Dest Reg ID				Src Reg ID				0	0	1	1	1
SL	1	0	1	Dest Reg ID				Src Reg ID				0	1	0	0	0
SRL	1	0	1	Dest Reg ID				Src Reg ID				0	1	0	0	1
SRA	1	0	1	Dest Reg ID				Src Reg ID				0	1	0	1	0
RRA	1	0	1	Dest Reg ID				Src Reg ID				0	1	1	1	0
RR	1	0	1	Dest Reg ID				Src Reg ID				0	1	1	0	1
RL	1	0	1	Dest Reg ID				Src Reg ID				0	1	1	0	0
JMP	1	1	0	Base Reg ID				0	Signed Offset Value							
JAL	1	1	0	Base Reg ID				1	Signed Offset Value							
BR	1	1	1	0	0	0	0	0	Signed Offset Value							
BC	1	1	1	1	0	0	0	0	Signed Offset Value							
BO	1	1	1	0	1	0	0	0	Signed Offset Value							
BN	1	1	1	0	0	1	0	0	Signed Offset Value							
BZ	1	1	1	0	0	0	1	0	Signed Offset Value							