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XEROX

To EIA Board Users

From

Rick Tiberi

The following notes document specifics of which the user should be aware when developing software to deal with the EIA interface board.

Subject

NotesDateDecember 5, 1977

1) SIT instruction. This is the Alto emulator instruction used to enable polling of the EIA interrupt status. If it is necessary to disable interrupts from the EIA interface alone, it may be tempting to try an SIT with AC0 = 0. However, note that since (see Alto Hardware Manual) the instruction OR's its state from AC0, this will not work. The following sequence should produce better results:

DisableInterrupts()

let oldBits = @ITIBITS

@ITIBITS = 0

EnableInterrupts()

//no EIA interrupts here

@ITIBITS = oldBits

SIT(3)

Note that the final SIT(3) is necessary because the interval timer may have received an interrupt while in the disabled state and turned itself off.

2) Status. Reading the status word causes the board to begin setup for reading the Data register. This makes it impossible to read the status more than once per interrupt; if a second attempt is made, the input data will appear instead. This condition is reset by the control command to acknowledge the interrupt (resetInterrupt).

Internal Memo

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XEROX

To EIA board users

From

Rick Tiberi

The streams package provided to drive the EIA interface boards provides the following interface to programmers:

Subject

EIA Streams

package

Date

December 9, 1977

Files. The package is divided into two files, EIAStream.br and InitEIAStream.br. This division is to allow the initialization code to be overlayed. InitEIAStream.br contains only the Open routine, and thus may be thrown out after all opens have been accomplished. The file EIAStream.d contains definitions of the EIAStream structure, control and status word formats, and various other useful definitions.

Procedures.

OpenEIAStream(inBufferLength[0], outBufferLength[0], async[false], baudRate[300], dataSet[false], halfDuplex[false], noParity[false], evenParity[false], dataBits[8], stopBits[2], syncChar[SYN], fillChar[NULL], line[0], interruptMask[#400], stackLength[100], zone[sysZone], errorRoutine[CallSwat]) = a stream. Buffer lengths are in words. Baud rate is in actual baud (300, 600, 2400, etc.). If 1.5 stop bits are desired at 5 data bits, 2 stop bits should be specified. Line is [0..7], indicating the switch setting on the board to be used. Stack length is for the interrupt process; the default should be sufficient for normal use, but more space may be required if elaborate error routines are used.

Gets(EIAStream) = the next available character, or -1 if the buffer is empty.

Puts(EIAStream, char) = true or false, indicating whether or not there was room in the buffer for the character.

Endofs(EIAStream, out[false]) = true or false. If out is false, indicates whether the input buffer is empty; if out is true, indicates whether the output buffer is full.

Stateofs(EIAStream) = the last status word returned on the line associated with the EIAStream.

Resets(EIAStream) = a null operation.

Revisions										
LAL	Rev	Description	Date	Approved						
В	В	Added Note to sheet 2 paragraph A section 1.1	10-17-78							
С	С	Corrected Add List Sheet 2 was J06-115 and J15-115	10-30-78							
D	D	Deleted WireWrap sheet 2 Clarified addressing sheet 5	06-12-79							

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FILE: [OLY]<REYES>SCCM-EIA-KIT.PRESS

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Next Assy.		18338	A	217406 -Charted		D	
First Use		Scale	Do	Do Not Scale Drawing S		1	

Notes: Unless Otherwise Specified

- A. The Serial Communication Control Module Kit configuration consists of two (2) kits identified by a dash number.
- 1.0 Kit Assembly No. 217406-001 is the basic configuration consisting of:

1-SERIAL COMMUNICATION CONTROL MODULE
1-SERIAL COMMUNICATION CONTROL RIBBON CABLE
1-DATA SET CABLE
ASSY 217328
ASSY 217405
ASSY 217049

1-PLATE, CONNECTOR ASSY 217335

2-SETS CONNECTOR MOUNTING HARDWARE 1-NAMEPLATE

1.1 Modify Altoll backplane per Add/Delete list. Typewrite nameplate as follows and adhere to top surface of the processor chassis. ASSY,KIT EIA SERIAL COMMUNICATION CONTROL INTERFACE DWG. 217406-Charted

<u>Delete</u> :	From J05-1 J06-1	J06-1	Note: GATEWAY MICROCODE SOFTWARE REQUIRES AN ALTOIL WITH EXTENDED MEMORY OPTION (THOUGH ONLY 64K OF MEMORY IS REQUIRED)
ADD:	J05-1 J06-2 J06-1 -J06-62 J06-53 -J06-116 J15-116 J10-13	J06-2 J07-1 J15-1 J15-62 J06-54 J15-54 J16-54 J11-109	ALTO'S NOT USING THE GATEWAY MICROCODE SOFTWARE AND DO NOT HAVE THE EXTENDED MEMORY OPTION INSTALLEDDELETE WIRE J10-13 TO J11-109 FROM ADD LIST.

- 1.2 Install Serial Communication Control module (SCCM) in processor J06 (line 0).
- 1.3 Remove connectors J1 thru J7, power cable and power cable strain relief from connector plate P/N 216418. Remove existing connector plate and return to stock, replace with connector plate P/N 217335.
- 1.4 Install Serial Communication Control ribbon cable Assy. 217405 on J03 of Serial Communication Control module (even numbers up). Install 25 pin and socket connectors on rear connector plate.
- 2.0 Kit Assembly 217406-002 additional Serial Communication Control module(s).

1-SERIAL COMMUNICATION CONTROL MODULE ASSY 217328
1-SERIAL COMMUNICATION CONTROL RIBBON CABLE (INTERNAL) ASSY 217405

1-DATA SET CABLE ASSY 217049 1-SERIAL COMMUNICATION CONTROL MODULE INTERCONNECTION CABLE (INTERNAL) ASSY 217404

2-SETS CONNECTOR MOUNTING HARDWARE

1- NAMEPLATE

- 2.1 Install additional SCCM(s) in processor J15, (line 1) and J16 (line 2).
- 2.2 Install Serial Communication Control ribbon cable Assy. 217405 on J03 of Serial Communication Control module (even numbers up). Install 25 pin and socket connectors on rear connector plate.
- 2.3 Install Serial Communication interconnection cable Assy. 217404 on J02 of SCCM line 0, SCCM line 1 and SCCM line 2 odd numbers up.
- B. Connector 25 pin presents the Serial Communication Control module as a Data Terminal Equipment (DTE).
 Connector 25 socket presents the Serial Communication Control module as a Data Communication Equipment (DCE)

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C. Control Word Format

1. Initialize Interface Circuits (INITIF)

	BO	B1	B2	В3	B4	B5	B6	B7	B8	В9	B10	B1	B12	B13	B14	B15
1	1	0	0	0	LIN	NE		DS	HD	S	STD	X	BA	UD RA	TE	

LINE: ADDRESSES CONTROL WORD TO SELECT LINE CONTROL: UP TO (3) FULLY PROGRAMMABLE, FULL DUPLEX LINE CONTROLS MAYBE ACCOMMODATED IN ONE ALTOH PROCESSOR.

DS: WHEN SET, SELECTED CONTROL WILL COMMUNICATE WITH A DATA SET; DEFAULT TO DATA TERMINAL.

HD: WHEN SET, SELECTED CONTROL WILL OPERATE HALF-DUPLEX; DEFAULT FULL DUPLEX.

S: INDICATES ALTO SENDING WHEN SET(1) IN HALF-DUPLEX.

STD: SETS SECONDARY REQUEST TO SEND (2SCA) TO ON WHEN SET AND INTERFACE IS TO DATA SET. SETS SECONDARY CARRIER DETECT TO ON WHEN SET AND INTERFACE IS TO DATA TERMINAL.

BAUD RATE: SELECTS BAUD RATE AT WHICH LINE WILL OPERATE.

BITS-	12	13	14	15		12	13	14	<u>15</u>		12	13	14	15	
	0	0	1	0	50	0	1	1	1	2400	1	1	0	0	2400
	0	0	1	1	75					9600					300
	0	1	0	0	134.5	1	0	0	1	4800	1	1	1	0	150
	0	1	0	1	200	1	0	1	0	1800					
	0	1	1	Ω	600					1200				•	•

2. Initialize Receiver/Transmitter (INITRT)

_B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
1	0	0	1	LIN	E		ND	3	NPB	A/S	POE	NSB	х	Х	х

NDB: SELECTS NUMBER OF DATA BITS PER CHARACTER.

BITS-	7	8	DATA BIT
	0	0	5
	0	1	6
	1	0	7
	1	1	8

NPB: NO PARITY BIT WHEN SET.

A/S: SELECTS ASYNCHRONOUS (UART) OPERATION WHEN SET; DEFAULT TO SYNCHRONOUS OPERATION (USRT).

POE: SELECTS EVEN PARITY WHEN SET, ODD PARITY WHEN NOT SET.

NSB: SELECTS NUMBER OF STOP BITS PER CHARACTER WHEN ASYNCHRONOUS OPERATION IS SELECTED. SELECTS 2 STOP BITS WHEN SET; 1 STOP BIT WHEN NOT SET (EXCEPTION: SELECTS 1.5 STOP BITS WHEN NOT SET AND 5 DATA BITS ARE SELECTED).

3. Initialize Registers (INITRG)

BO	B1	B2	В3	B4	B5	B6	B7	B8 B15
1	0	1	0	LIN	E		F/S	DATA FIELD

F/S: WHEN SET CAUSES DATA FIELD TO BE LOADED INTO USRT TRANSMITTER FILL CHARACTER REGISTER. WHEN NOT SET DATA FIELD WILL BE LOADED INTO USRT RECEIVER SYNC CHARACTER REGISTER.

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C. Control Word Formats continued.

4. Generate Controller Resets (Reset)

BO	B1	B2	В3	B4	B5	В6	В7	В8	В9	B1	0				B15
1	0	1	1	LII	NE		D	RRT	RR	х	Х	Х	Х	x	х

D: GENERATES A LINE DISCONNECT/MASTER CLEAR OF THE SELECTED LINE WHEN SET.

RRT: CLEARS THE RECEIVER/TRANSMITTER (UART/USRT) WHEN SET.

RR: RESETS SYNCHRONOUS RECEIVER, CLEARS STATUS REGISTER, RESTARTS SYNCHRONOUS RECEIVER IN THE BIT TRANSPARENT MODE FOR SYNC SEARCH.

5. Force the Deselected Control to Request an Interrupt (SWI)

BO	B1	B2	<u>B3</u>	B4	B5	B6	B7								B15
1	1	0	0	LII	NE		x	X	X	X	X	X	X	X	х

6. Interrupt Acknowledge to the Selected Line (INTA)

<u>B0</u>	<u>B1</u>	B2	B3	B4	B5	B6	B7								B15
1	1	0	1	LII	NE		X	X	X	х	X	х	X	х	x

D. Status Word Format

<u>B0</u>	B1	B2	B3	B4	B5	B6	B7	B8	B9 B10 B11	B12 B13 B14 B15
D	CD	RI	SI	LIN	NE		SRD	RDA	TB SCRFCT	RPE RORRFE IN

1. Interface Status (High Order Byte)

D: DISCONNECT FLAG: WHEN SET, THIS BIT INDICATES LOSS OF RS-232 LINE; DATA SET READY IF DATA SET INTERFACE IS SELECTED. DATA TERMINAL READY IF DATA TERMINAL INTERFACE IS SELECTED.

CD: CARRIER DETECT FLAG

RI: RING INDICATOR FLAG

SI: SEND INDICATOR FLAG: WHEN BIT IS SET, INDICATES PRESENCE OF CLEAR TO SEND IF DATA SET INTERFACE IS SELECTED. REQUEST TO SEND IF DATA TERMINAL INTERFACE IS SELECTED.

SRD: REMOTE HALF-DUPLEX BREAK: IN HALF-DUPLEX THIS BIT GOING TO A ZERO SIGNALS A BREAK BY THE REMOTE RECEIVING STATION.

2. Receiver/Transmitter Status (low Order Byte)

RDA: RECEIVE DATA AVAILABLE.

TBMT: TRANSMIT BUFFER EMPTY.

SCR: SYNC CHARACTER RECEIVED (USRT)

FCT: FILL CHARACTER TRANSMITTED (USRT)

RPE: RECEIVE PARITY ERROR

ROR: RECEIVE OVERFLOW ERROR

RFE: RECEIVE FRAMING ERROR (UART)

INTP: INTERRUPT FLAG: INTP' = D' + CD' + RI + SI' + RDA + TBMT + SCR + (SRD' SEND HDUP)

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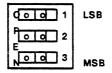
C

E. Data Word Format (Receive or Transmit)

B0	B1	B2	В3	B4	B5	B6	B7	B8 B15
0	x	x	x	LIF	NE		x	DATA FIELD

F. Serial Communication Control Module Addressing

THREE DIP TYPE SWITCHES HAVE BEEN PROVIDED ON THE PRINTED CIRCUIT BOARD



SWITCHES ARE SHOWN IN THE OPEN POSITION (0 0 0) SCCM LINE POSITION ZERO.

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