Design of the Flight Controller Software Update System of Missiles With GJB 1188A Interface Under Whole Missile State

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***Abstract*—With the rapid development of missile weaponry in the new era, intelligent software update has become an important direction for future development of missile weaponry system. In order to update the flight controller software of the airborne missile under the whole missile state, this paper designed a flight controller software update system of missiles with GJB 1188A interface under the whole missile state. The host computer of this system first transmits the compiled target files to the missile flight controller through 1553B bus of GJB 1188A interface. Then the flight controller independently writes the received file into the program storage based on IAP (In Application Programming). Finally, the host computer verifies the software update. This system has high reliability, strong flexibility in field experiments, electric missile joint-tests and other application scenarios, solving the problem of flight controller software update of missiles with GJB 1188A interface under the whole missile state.**

Keywords—GJB 1188A, software update under the whole missile state, IAP

I. INTRODUCTION

With the rapid development of missile weaponry in the new era, intelligent ammunition promotes the upgrading of missile weaponry system, and intelligent software update has become an important direction for future development of missile weaponry system [1]. In missile field experiments, the shooter should adjust the control model and trajectory information based on the target of missile attack (i.e., tanks, armored vehicles and so on) [2], and update the missile flight controller software under the whole missile state, i.e., on the premise of not disassembling the missile, the flight controller software is updated according to the external interface of the missile itself. The traditional method of flight controller software update is JTAG (Joint Test Action Group) online programming [3][4], which uses boundary scan to access the chip and program the storage FLASH. The effective transmission distance of the JTAG signal is short. If the JTAG signal is connected to the missile's external interface through the cable, the signal will be too weak to be received and utilized by the simulator, because the cable is too long. Therefore, to update the flight controller software in the traditional way, it is necessary to first dismantle the missile and take out the flight controller, and then update the software online through JTAG signals of the flight controller. In this way, the disassembling and installation of the missile is so complicated that the cost of time and manpower is huge. Therefore, it is urgent to update the flight controller software directly under the whole missile state.

In order to meet the requirements of software update under a whole machine state, the software update method based on IAP (In Application Programming) [5][6] emerged. In this way, the machine can update the program storage by software segments dedicated to read, write and erase. Research on IAP-based software update under a whole machine state mainly involves the following modes, i.e., serial port [7], USB bus [8], Ethernet port [9], Bluetooth [10], 1553B bus [11], Wi-Fi Wireless LAN[12], etc. However, there is no relevant research on the GJB 1188A interface missile software update under the whole missile state based on IAP technology. Based on IAP, this study designs a flight controller software update system of missiles with GJB 1188A interface under the whole missile state, adopting the 1553B bus of GJB 1188A interface as the communication bus between the host computer and the flight controller. This system can be quickly connected to the missile GJB 1188A interface under the whole missile state to realize the software update of the missile flight controller.

II. AN OVERVIEW OF THE FLIGHT CONTROLLER SOFTWARE UPDATE SYSTEM UNDER THE WHOLE MISSILE STATE

This study aims to design a software update system of the flight controller—a part of the missile with GJB 1188A mission store interface (MSI)—under the whole missile state. *GJB 1188A-99 Requirements of Interface for Aircraft/Store Electrical Interconnection System* (hereafter GJB 1188A)[13] is a general standard used by the aircraft and all kinds of store. The flight controller is an important part of the missile, mainly realizing the functions of communication, power management, model resolving and actuator command generation [14] [15]. Taking a certain type of airborne missile flight controller as an example, this study examines a software update system applicable to the flight controller of missiles with GJB 1188A interface, whose main chip adopts domestically-made SOPC (System on Programmable Chip), embedded with

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ARM926EJ-S kernel and XILINX XC2V1000 FPGA (Field Programmable Gate Array), with the program stored in its internal SPI FLASH (Serial Peripheral Interface FLASH).

The design of the software update system for the flight controller under the whole missile state is divided into two parts: hardware design and software design. The former realizes the docking function of MSI, direct current (DC) power supply, 1553B bus control, 1553B signal coupling, and release consent setting, interlock setting, RT (Remote Terminal) address setting [16]. Software design is divided into communication mechanism design, host computer software design and flight controller IAP software module design. Communication mechanism regulates the period and content of messages between the host computer and the flight controller. The host computer software is designed to realize the function of target file reading, 1553B communication and human-computer interaction. The flight controller IAP software module is designed to realize the functions of downloading mode and reading mode. The architecture of the design of the entire flight controller software update system is shown in Fig. 1.

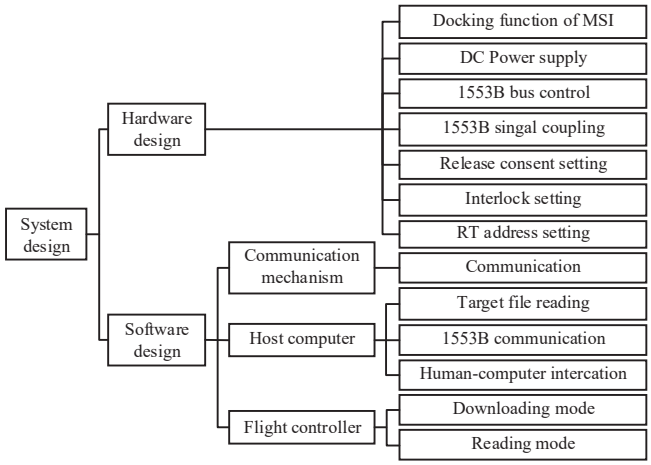

Fig. 1 Architecture of the system design

III. THE PROPOSED METHOD

A. Hardware Design

The hardware of the system consists of the following parts, namely the host computer (including 1553B board), DC power, cables, 1553B coupler and the system connector. The missile flight controller software update can be realized through the direct docking between the system interface and the missile MSI. The hardware composition of this system is shown in Fig. 2.

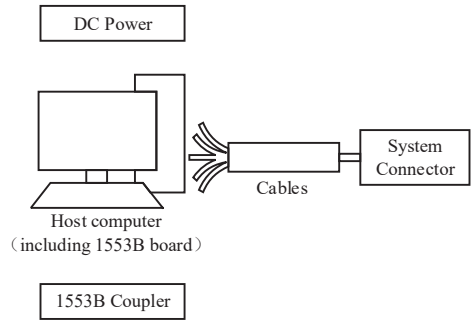

Fig. 2 The hardware composition of the software update system

The interface signal of this system includes MUX A, MUX B, release consent, interlock and interlock return, RT address and address return, 28.5V DC power 1 and power 1 return, 28.5V DC power 2 and power 2 return. The signal definition of this interface is shown in Fig. 3. The host computer consists of a personal computer and 1553B board, whose two channels of 1553B signals are connected to the bus coupler by shielded twisted pair, and then connected to MUX A and MUX B of the system connector in an indirect coupling way to achieve double redundancy of signals. The DC power provides 28.5V power for the missile and flight controller, which is connected to the system connectors 28.5V DC power 1 and 28.5V DC power 2. The RT address is the only symbol to identify the missile flight controller, which is assigned by RT address and address return. This system sets RT address as 6. Release consent and interlock signal are used for the launch mode, and this system configures signals disconnected from their return.

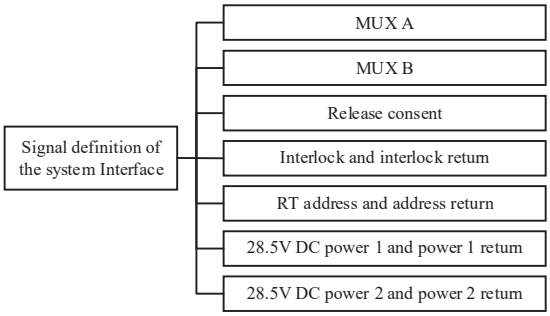

Fig. 3 Signal definition of the interface of the software update system

B. Software Design

1) Communication mechanism

Given that GJB 1188A has regulated certain subaddresses for specialized uses, the software update system in this study adopts subaddresses that can be defined by individual users. The format of data word between the host computer and the flight controller are divided into two types, as shown in TABLE I and TABLE II respectively. The message in TABLE I occupies subaddress 2, which realizes the command interaction, i.e., the host computer commands the flight controller to enter either the downloading mode or reading mode, and assign the message with a length of 20 words (1 word equals to 2 bytes), among which the frame header (FH) occupies 1 word, the command 1 word, the checksum 1 word, while the rest words are reserved. The message in TABLE II occupies subaddresses 20-26 and 28, which realizes the data interaction, and its length is also 20 words, among which FH occupies 1 word, message number 2 words, checksum 1 word, and the remaining 16 words are used for the valid data of the target file. The message numbers are accumulated in sequence to prevent frame loss. A special kind of algorithm defined by GJB 1188A is adopted for the check sum.

One group of information interaction between the host computer and the flight controller includes the transmission of 8-subaddress messages, i.e., the 256-byte data that can be written into one page of SPI FLASH is transmitted to the flight controller in turn through 8 subaddresses. The valid data of each message is 32 bytes, namely 16 words.

The vector word format is shown in TABLE III, which is obtained by the host computer with a fixed period of 20ms. Bit b0 is always set as 1, indicating that the vector word format is the asynchronous action demand. Bits b1 and b2 are

downloading mode identifications, informing the host computer whether the data received has been written or not. Bits b3 and b4 are reading mode identifications, informing the host computer whether the reading has been completed or not.

TABLE I. DATA WORD FORMAT OF SUBADDRESS 2

Word	Word 1	Word 2	Word 3—Word 19	Word 20
Meaning	FH	command	Reserved	checksum

TABLE II. DATA WORD FORMAT OF SUBADDRESS 20-26, 28

Word	Word 1	Word 2, Word 3	Word 4—Word 19	Word 20
Meaning	FH	message number	valid data	checksum

TABLE III. VECTOR WORD FORMAT

Bit	b0	b1	b2	b3	b4	b5—b15
Meaning	set as 1	downloading mode		reading mode		reserved

2) Software design of the host computer

The host computer runs application software, whose development is based on VC++6.0, realizing the function of target file reading and friendly human-computer interaction [17], and the 1553B board driver is called for secondary development to realize the function of Bus Controller (BC) in communication. The software workflow diagram is shown in Fig. 4.

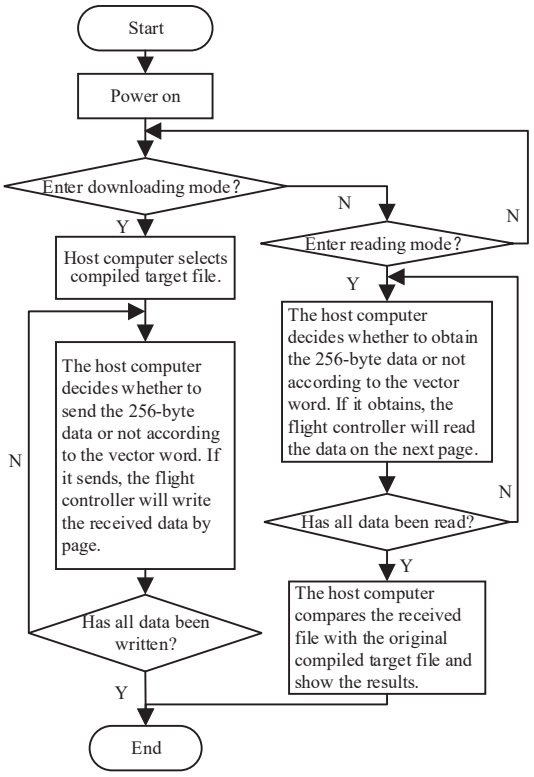

Fig. 4 Workflow diagram of the software update system

3) Software design of the flight controller

The flight controller software realizes RT function in communication, which can be divided into two software modules, namely downloading module and reading module. The flight controller adopts interrupt mode to deal with 1553B message. The interrupt mechanism of 1553B bus is EOM (End of Message), which triggers interrupt after message interaction.

The host computer sends BC→RT message with the format shown in TABLE I, enabling the flight controller to enter the downloading mode. Then the host computer sends BC→RT message with the format shown in TABLE II, trigging the flight controller to enter the interrupt service subroutine. This subroutine then gets the data from the shared RAM (Random Access Memory), and the main function verifies the checksum and decodes the data. Till the 8-frame messages are all received, the flight controller writes the received data into the program storage, and then sets the vector word downloading mode identification bits b1 and b2 valid, informing the host computer that this communication is completed and can start the next. When the host computer obtains valid vector word, the flight controller clears the vector word immediately.

The host computer sends BC→RT message with the format shown in TABLE I, enabling the flight controller to enter the reading mode. When the host computer quires that the vector word reading mode identification bits b3 and b4 are valid, it sends RT→BC message to obtain the 8-frame messages, whose format is shown in TABLE II. When the flight controller enters the interrupt service subroutine, indicating that the 8-frame messages have been sent already, it proceeds to read the SPI FLASH data on the next page and sets the vector word reading mode identification bits b3 and b4 valid. When the host computer obtains valid vector word, the flight controller clears the vector word immediately.

According to Fig. 4, a software example is designed as follows:

```
Init_system ();
Init_1553_rt ();
Init_interrupt ();
// judged as the downloading mode
If (Work_mode == DOWNLOAD_MODE)
{
    While (1)
    {
        1553_data_judgement ();
        Write_spi_flash ();
    }
}
// judged as the reading mode
If (Work_mode == SPI_READ_MODE)
{
    While (1)
    {
        1553_data_judgement ();
        Read_spi_flash ();
    }
}
```

IV. EXPERIMENTAL RESULTS

The flight controller software update under the whole missile state is divided into three steps. The first step is to

select the target file that needs to be updated. The second step is entering the software downloading mode and updating the software. After the flight controller enters the software downloading mode, the host computer packs the compiled file frame by frame and sends it to the flight controller. The flight controller will decode and verify the received data frame by frame and write the valid data into the SPI FLASH. The third step is entering the reading mode and verifying the program. After the flight controller is reset, it enters the reading mode, then reads the program storage SPI FLASH data page by page and sends it to the host computer in turn. The host computer receives and stores the valid data and verifies it with the original compiled target file. After confirmation, the software update is completed.

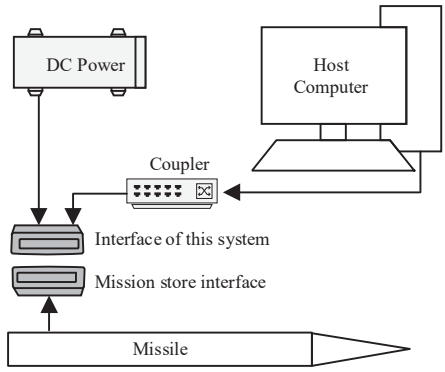

Fig. 5 Working diagram of the software update system

An experiment of the software update system under the whole missile state in an electric missile joint-test is to be illustrated in the following. The hardware was connected according to Fig. 5. The application software interface of the host computer is shown in Fig. 6. This hexadecimal target file with 200K Bytes can be updated in accordance with the above operation steps. 6,309 messages were communicated in both the downloading mode and the reading mode, taking about 6 minutes in total. When the application software interface shows the conclusion as "successful", it indicates that the software update was successful.

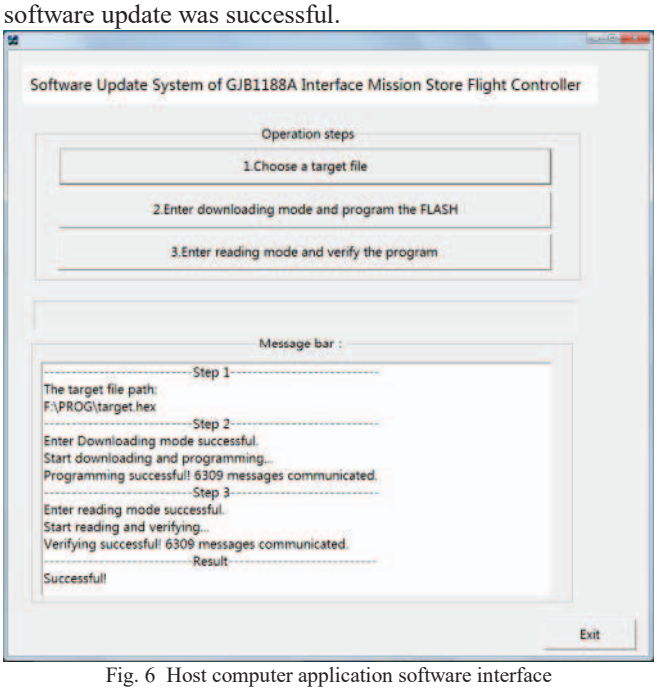

Fig. 6 Host computer application software interface

V. Conclusion

The missile with GJB 1188A interface is a kind of standard airborne missile. This study designed a flight controller software update system applicable to this interface under the whole missile state. The proposed system in this study has the universality for missiles with GJB 1188A interface standard. The experimental results show that this system can solve the problem of the flight controller software update of missiles with GJB 1188A interface under the whole missile state in application scenarios such as field experiments, electric missile joint-tests, etc. It has strong reliability and high stability. In addition, this system provides guidance and application basis for software update of the missile electronic components on future aircrafts, with significant promotional value.

In addition, intelligent ammunition promotes the upgrading of missile weaponry system. As an important element of intelligent ammunition, the technology of software update can greatly improve the operational flexibility and mobility in future operations. It can be expected soon that the software update of electronic components under the whole missile state on airplane will be realized.

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