EE214 - Report 4

Implementing BCD Adder

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FR-19/T-19

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Contents

Introduction

In this report, I have presented my work done on Quartus using VHDL during the third lab.

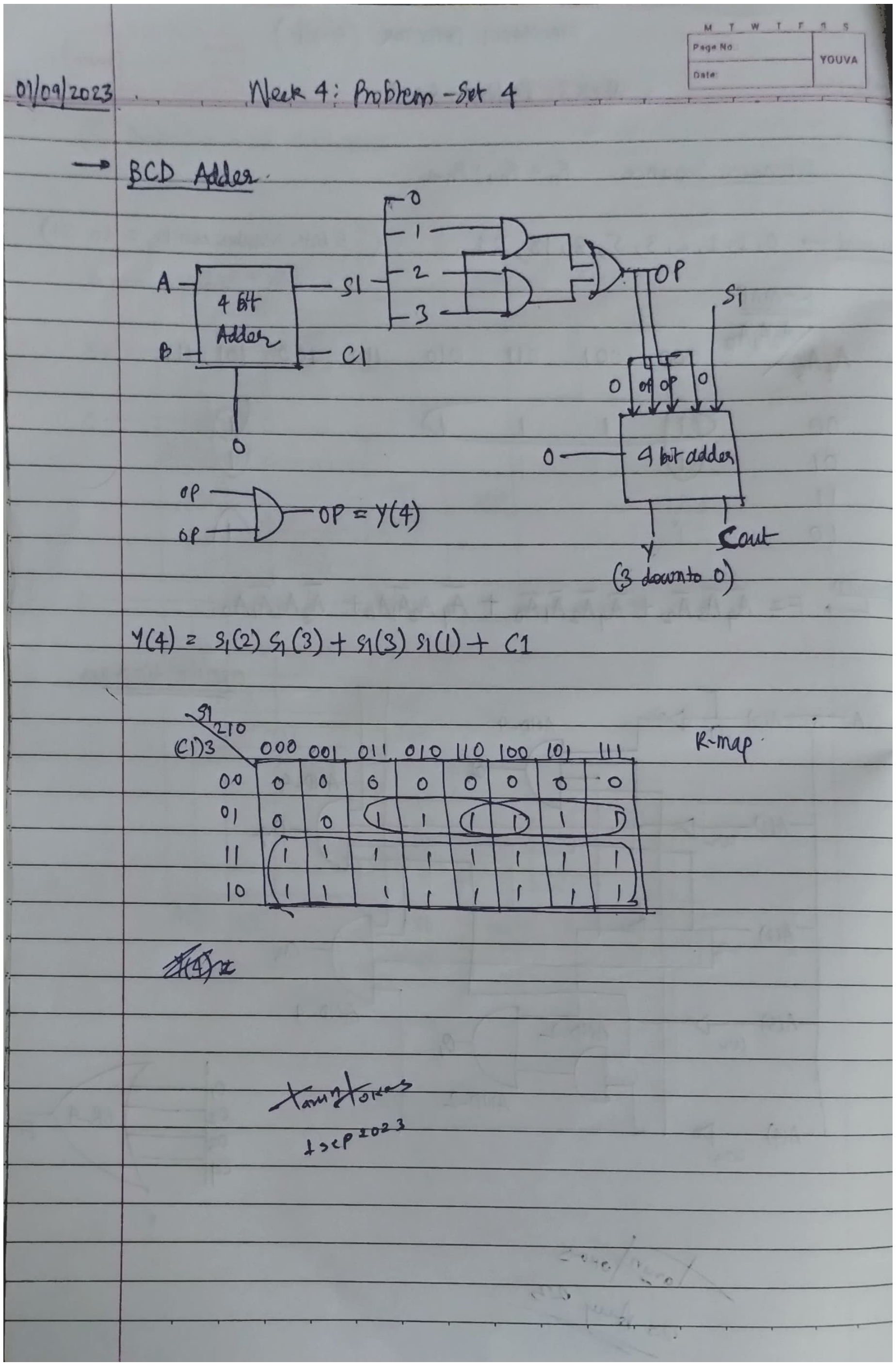
I have also done design verification using ScanChain tool on Xen-10 FPGA board and verified my design.

The circuit presented in the report has the RTL Viewer followed by the ModelSim Waveform obtained from Quartus.

Chapter 1

K-Maps and Circuit Diagrams

This section contains the k-map and the diagram of the circuit made in the lab.


01/09/2023
Week 4: Problem-Set 4
BCD Adder
A
B
4 bit Adder
S1
C1
0
OP
S1
0 OP OP 0
4 bit adder
Y
Cout
(3 downto 0)
OP = Y(4)
Y(4) = S1(2) S1(3) + S1(3) S1(1) + C1
K-map

Chapter 2

BCD Adder

The concept of BCDAdder was to take in 2 4-bit decimal numbers (0 to 9) and then adding them such that the output also followed the BCD system.

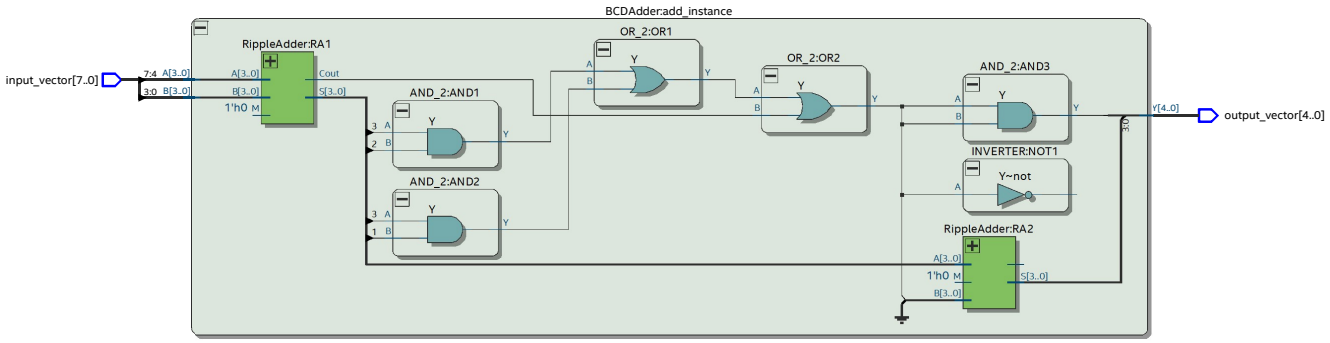
A few examples to demonstrate BCD Addition.

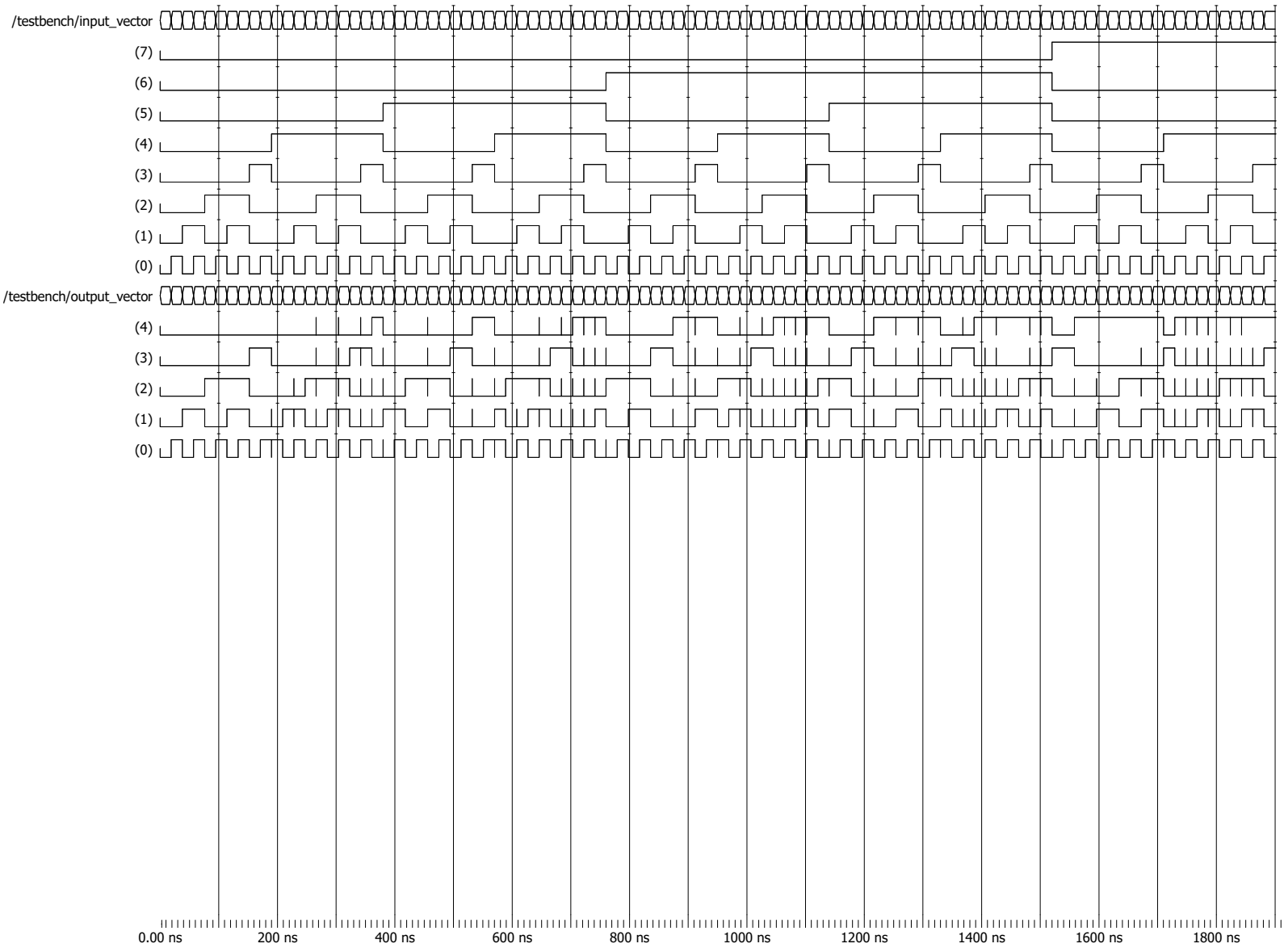
$A(3)$	$A(2)$	$A(1)$	$A(0)$	$B(3)$	$B(2)$	$B(1)$	$B(0)$	$Y(4)$	$Y(3)$	$Y(2)$	$Y(1)$	$Y(0)$	Decimal
0	0	1	0	0	0	1	1	0	0	1	0	1	09
1	0	0	1	0	1	0	0	1	0	0	1	1	13
1	0	0	0	0	1	1	1	1	0	1	0	1	15
1	0	0	1	1	0	0	1	1	1	0	0	0	18

Table 2.1: Some of the input-output mappings of a BCDAdder

I used the 4-bit Full Adder-Subtractor (also called as Ripple Adder) and the basic gates to implement the BCD Adder Circuit which can be seen in the RTL Viewer in the following page.

Date: September 02, 2023 Project: BCDAdder

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(7)
(6)
(5)
(4)
(3)
(2)
(1)
(0)
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(3)
(2)
(1)
(0)
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400 ns
600 ns
800 ns
1000 ns
1200 ns
1400 ns
1600 ns
1800 ns
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THANK YOU!