EE214 - Report 9

Traffic Signal Controller

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Contents

Introduction

0.1 Objective

The aim of the assignment was to design a controller (FSM) to control the traffic lights of each lane in a four-way crossing with mentioned functionality.

- There will be 3 traffic lights : RED, YELLOW and GREEN
- The traffic light pattern for each signal is as follows RED ⇒ YELLOW ⇒ GREEN ⇒ YELLOW ⇒ RED
- GREEN signal will be turned ON in clockwise direction of the traffic signals
- For an individual signal one of the 3 color must be "ON" all of the time.
- For an individual signal, no two color can be ON at the same time.
- No two signal can be GREEN at the same time.
- Two adjacent signal will be YELLOW at the same time in clockwise direction.
- For each signal GREEN light will be "ON" for 5 sec and YELLOW light will be "ON" for 1 sec.

We had to generate a delay of 5 sec and 1 sec using the Master Clock of 50MHz.

We had to verify the functionality by implementing it on a Xen10 Board with proper pin planning.

0.2 Overview

In this report, I have presented my work done on Quartus using VHDL during the eighth lab.

I have also done functional verification with pin planning on Xen-10 FPGA board and verified my design.

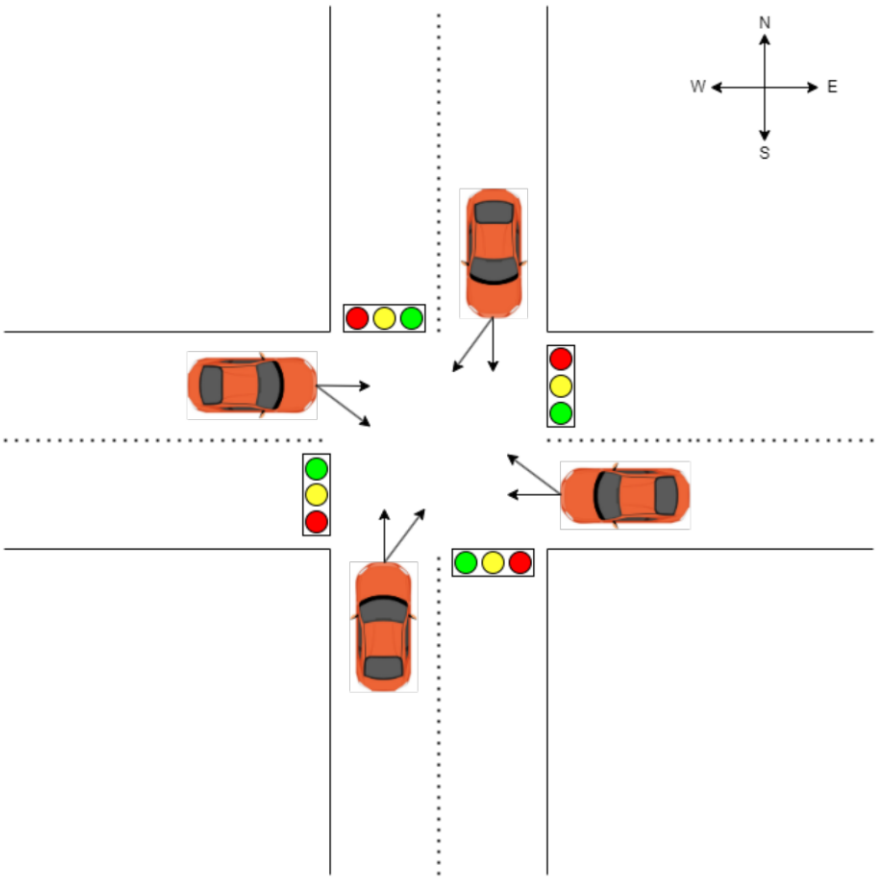


Figure 1: Traffic Signal at a 4-way crossing

Chapter 1

Transition Table and State Diagram

This section contains the Transitioning Table for the Traffic Light and the State Diagram.

Assuming the reset is applied at t=0, the transition table is

Direction	$t = 0s$	$t = 5s$	$t = 6s$	$t = 11s$	$t = 12s$	$t = 17s$	$t = 18s$	$t = 23s$
North	GREEN	YELLOW	RED	RED	RED	RED	RED	YELLOW
East	RED	YELLOW	GREEN	YELLOW	RED	RED	RED	RED
South	RED	RED	RED	YELLOW	GREEN	YELLOW	RED	RED
West	RED	RED	RED	RED	RED	YELLOW	GREEN	YELLOW

Table 1.1: Traffic Light Transitioning Table

The state diagram for the controller is shown on the following page

20/10/2023

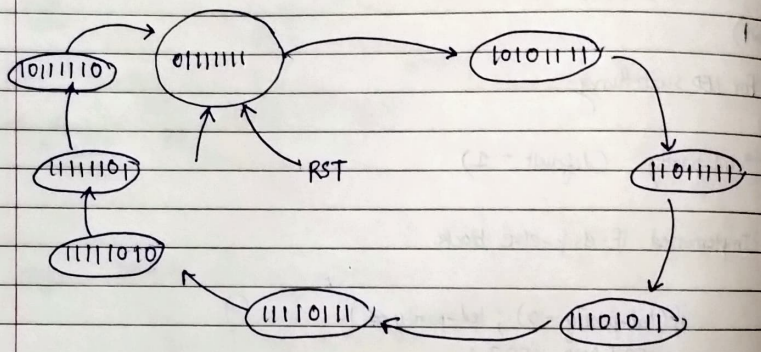
Week 9 : Problem - Set 9

50MHz → on-board clock

① For 5s delay :- $\left(f = \frac{1}{5}Hz\right)$ ⇒ 125000000 = count

② For 1s delay :- $(f = 1Hz)$ ⇒ 25000000 = count.

$N_1N_0E_1E_0S_1S_0W_1W_0$ = order of output bits.



State Diagram

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20 Oct 2023

Chapter 2

Traffic Signal Controller

2.1 State Machine Viewer

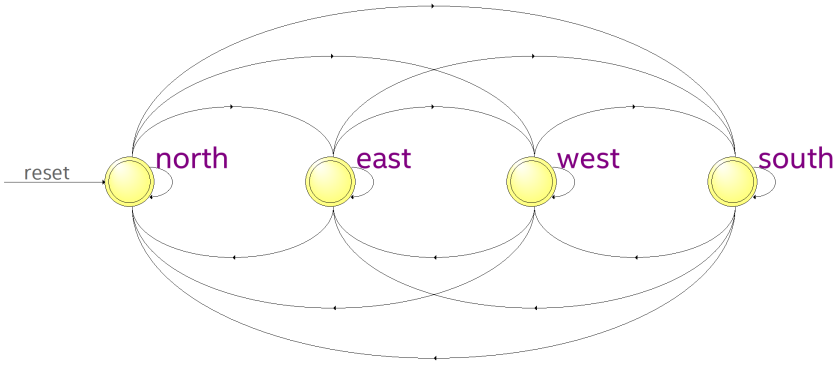

Figure 2.1: Control State Diagram

2.2 Circuit and Pin Planning

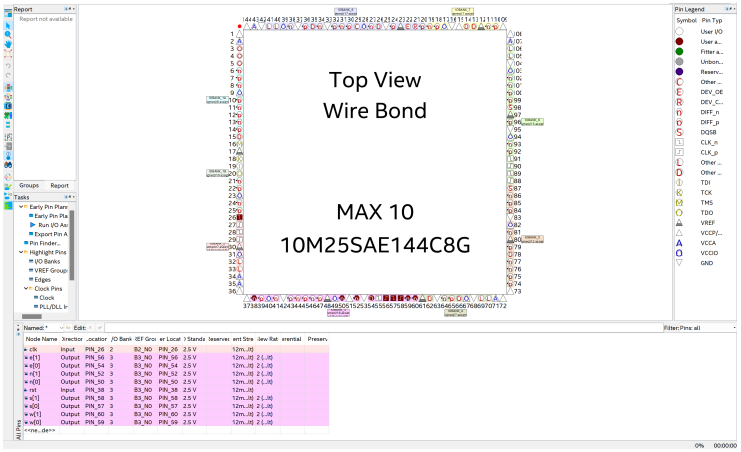

Figure 2.2: Pin Planner

Figure 2.3: RTL Viewer - TrafficLight

THANK YOU!