EE214 - Report 1

Designing Circuits using Universal Gate "NOR"

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11th August 2023

Contents

Introduction

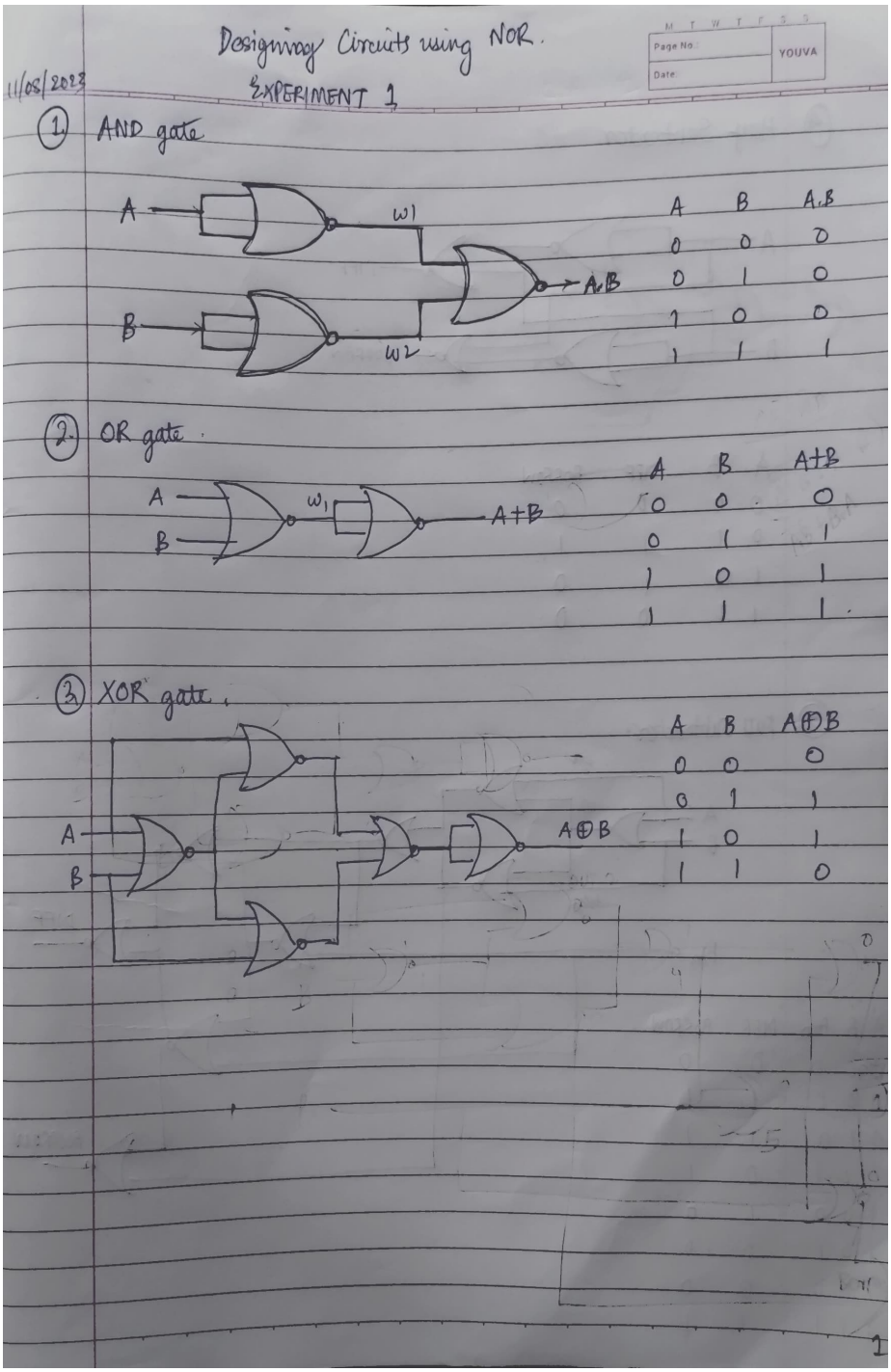
In this report, I have presented my work done on Quartus using VHDL during the first lab.

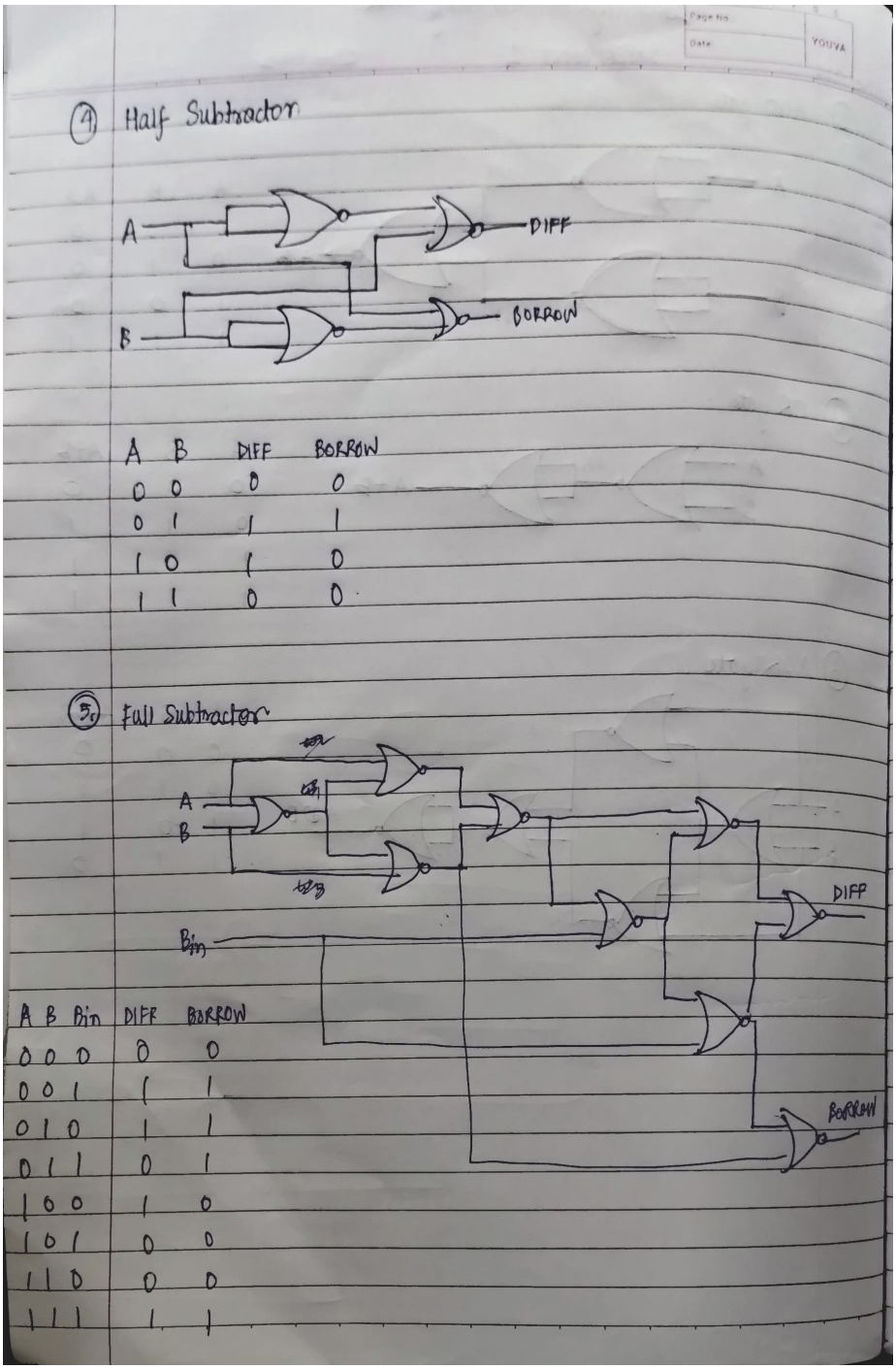
All the gates presented in the report have the RTL Viewer followed by the ModelSim Waveform obtained from Quartus.

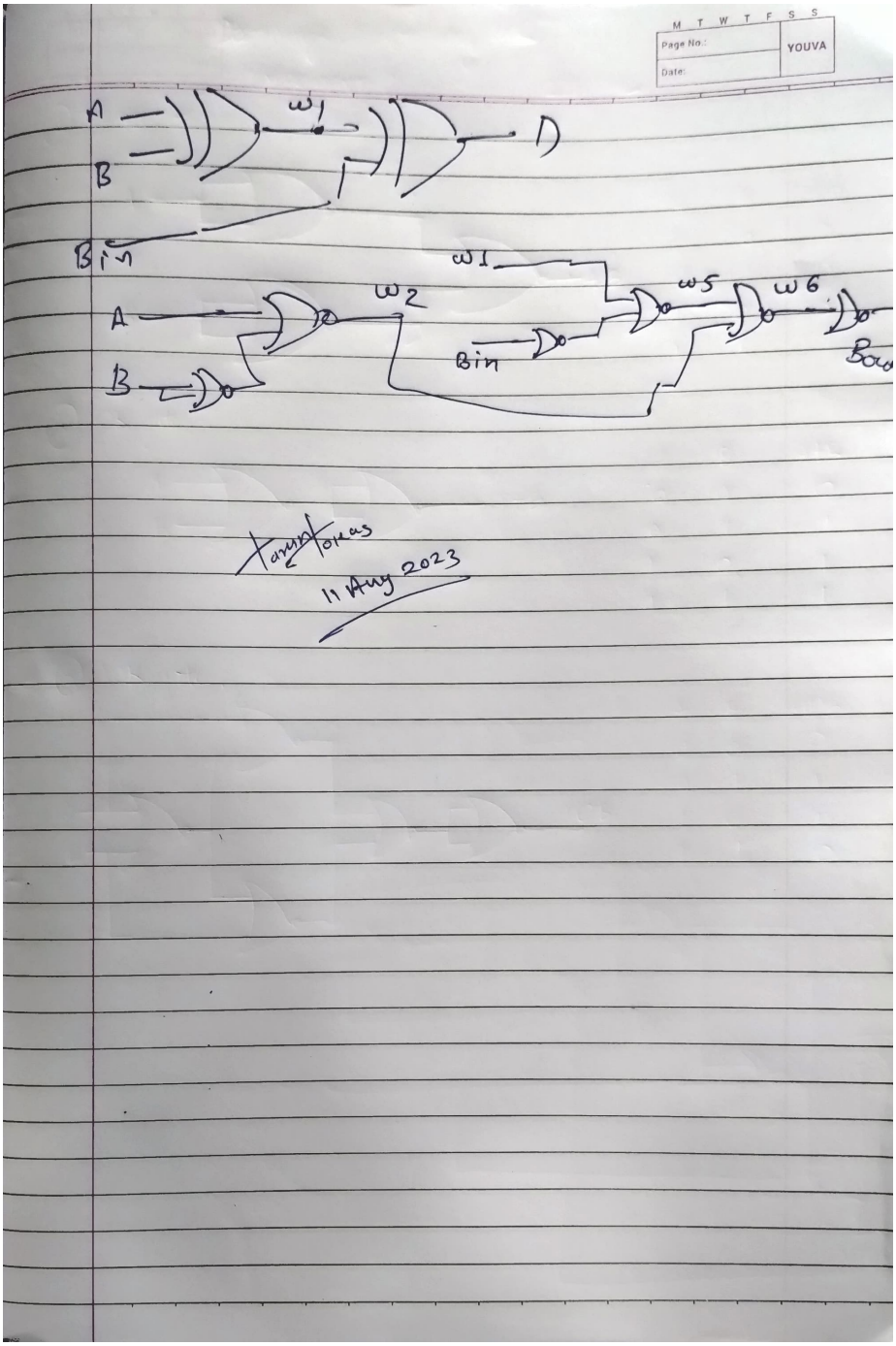
Chapter 1

Lab Diagrams

This section contains the diagrams of the gates made in the lab.


Designing Circuits using NOR.
11/08/2023
EXPERIMENT 1
Page No.
Date:
YOUVA
1. AND gate
A
B
W1
W2
A.B
A B A.B
0 0 0
0 1 0
1 0 0
1 1 1
2. OR gate.
A
B
W1
A+B
A B A+B
0 0 0
0 1 1
1 0 1
1 1 1
3. XOR gate.
A
B
A⊕B
A B A⊕B
0 0 0
0 1 1
1 0 1
1 1 0


Page No.
Date
YOUVA
4) Half Subtractor
A
B
DIFF
BORROW
A B DIFF BORROW
0 0 0 0
0 1 1 1
1 0 1 0
1 1 0 0
5) Full Subtractor
A
B
Bin
DIFF
BORROW
A B Bin DIFF BORROW
0 0 0 0 0
0 0 1 1 0
0 1 0 1 0
0 1 1 0 1
1 0 0 1 0
1 0 1 0 0
1 1 0 0 0
1 1 1 1 1

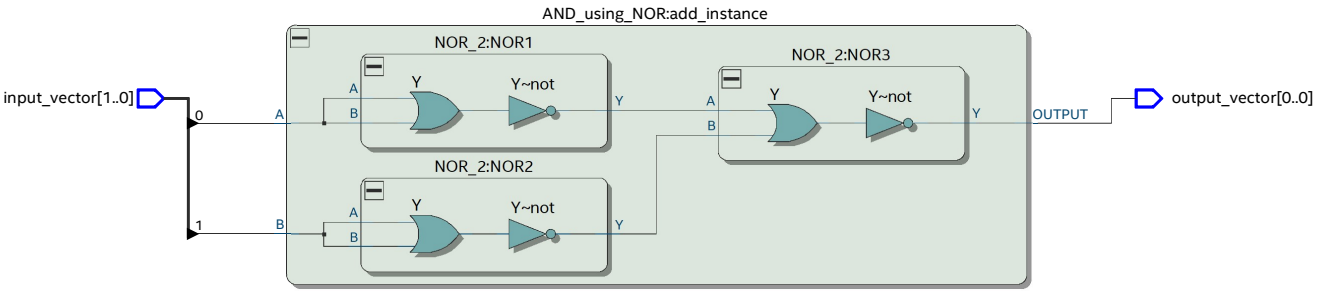

M T W T F S S
Page No.:
Date:
YOUVA
A
B
Bin
w1
D
w2
w5
w6
Tanmay Tokas
11 Aug 2023

Chapter 2

AND using NOR

Date: August 13, 2023

Project: AND_using_NOR



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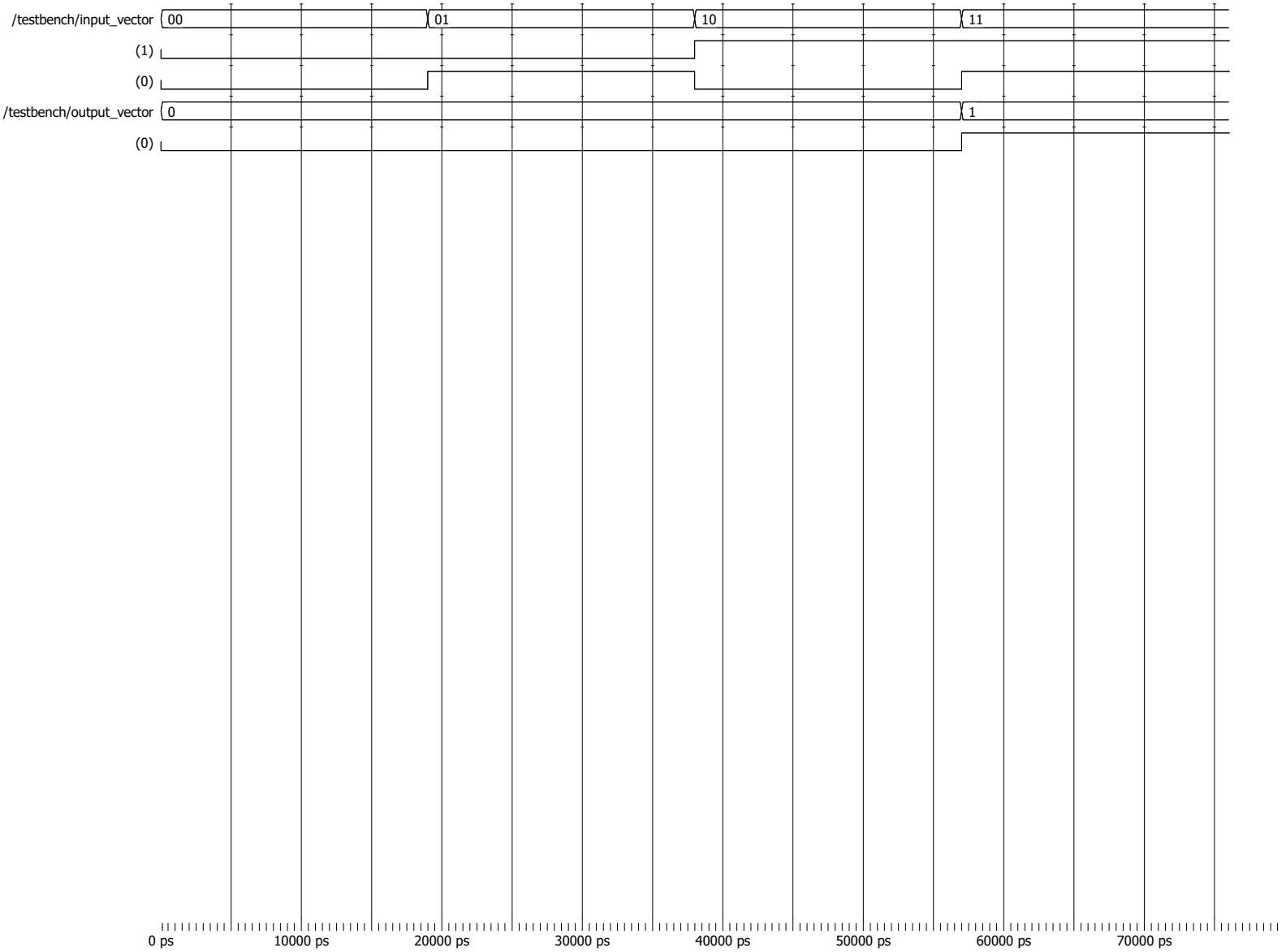
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10
11
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(0)
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30000 ps
40000 ps
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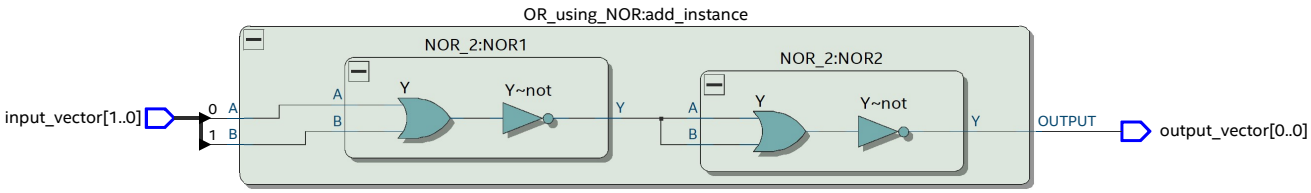
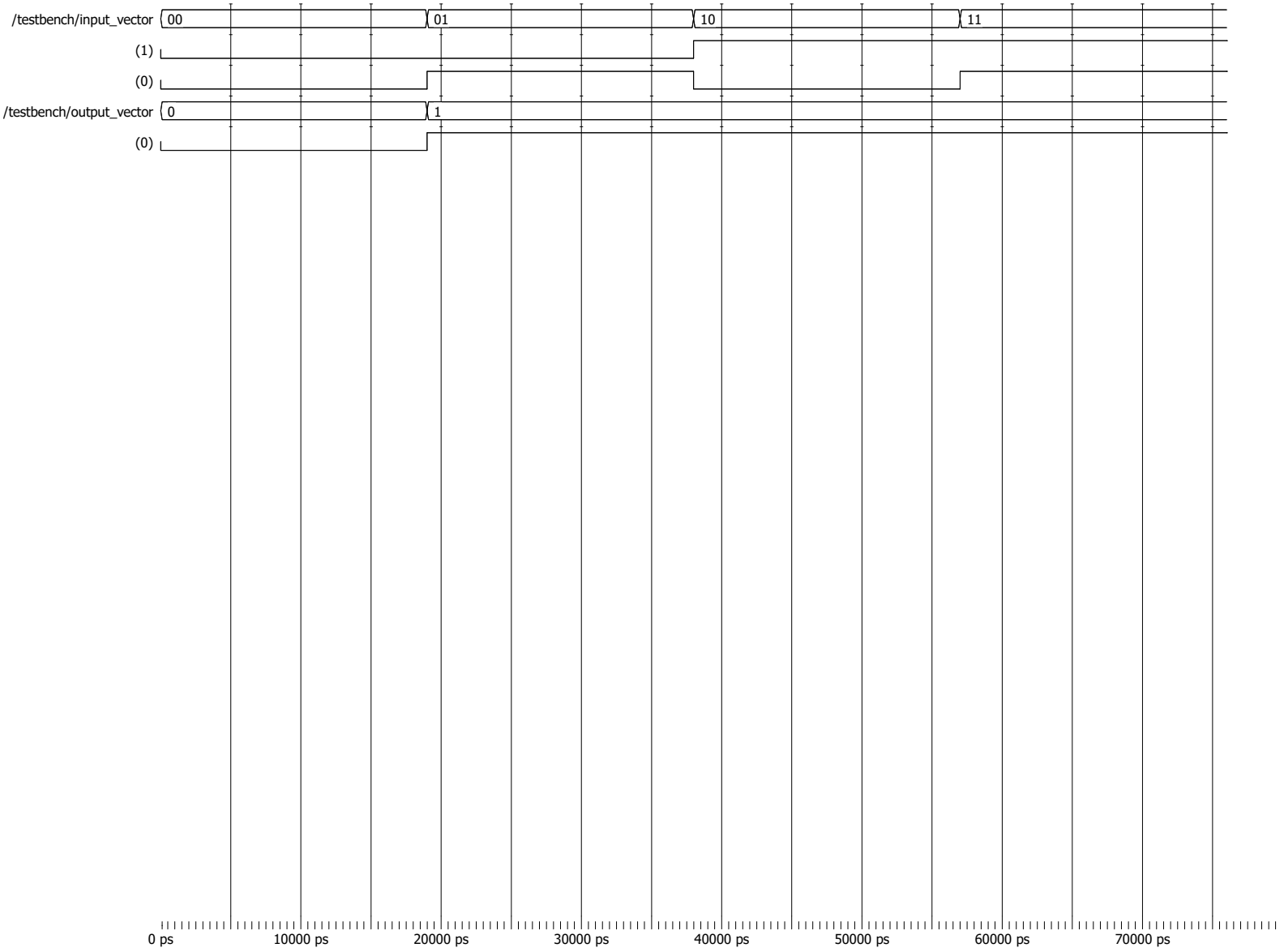
Chapter 3

OR using NOR

Date: August 12, 2023 Project: OR_using_NOR

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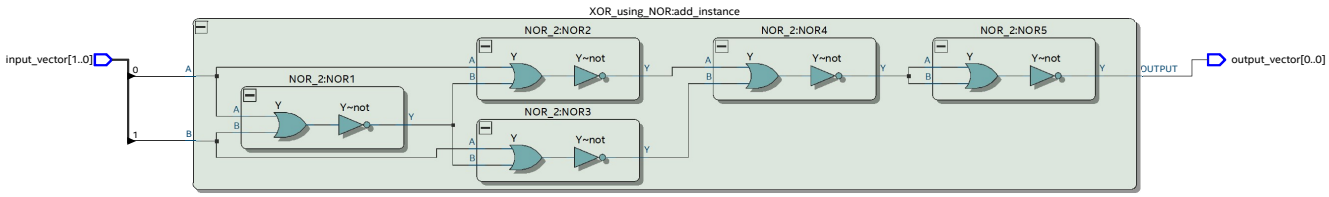
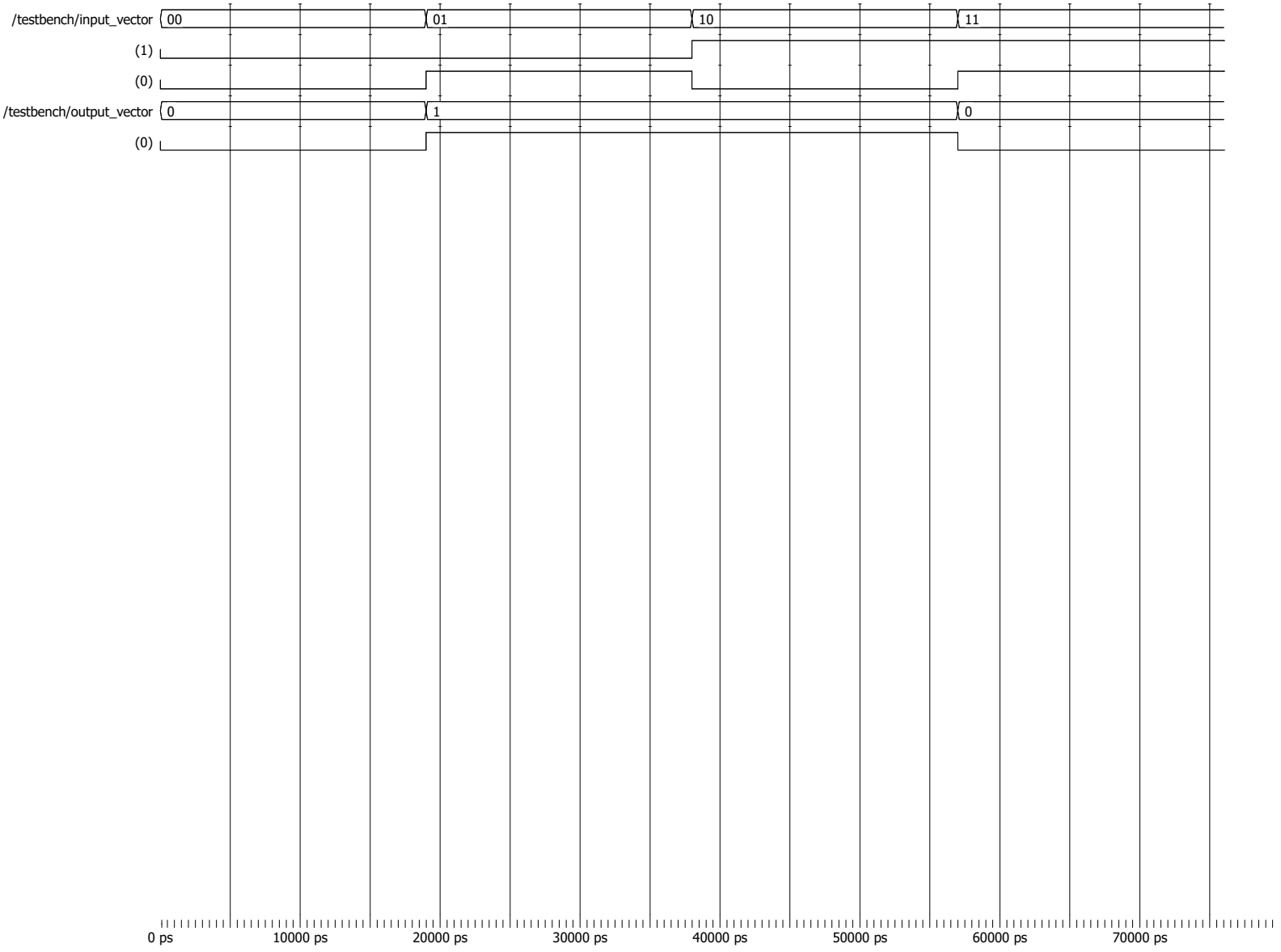
Chapter 4

XOR using NOR

Date: August 12, 2023 Project: XOR_using_NOR





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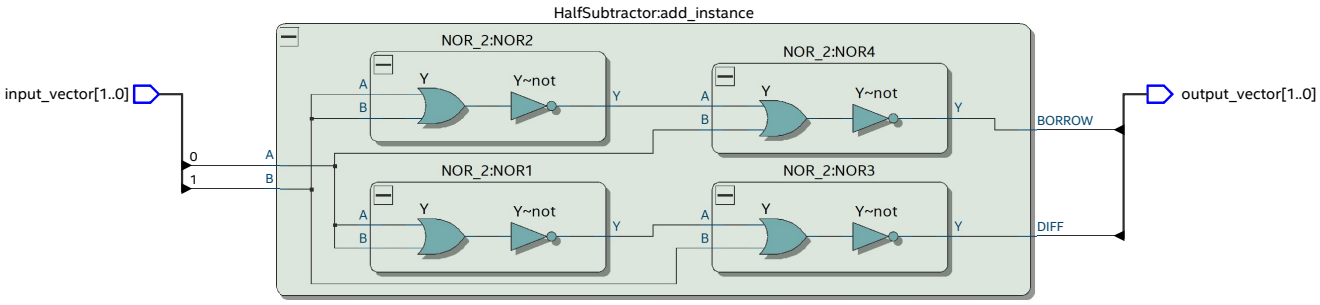
Chapter 5

Half Subtractor

Date: August 12, 2023

Project: HalfSubtractor



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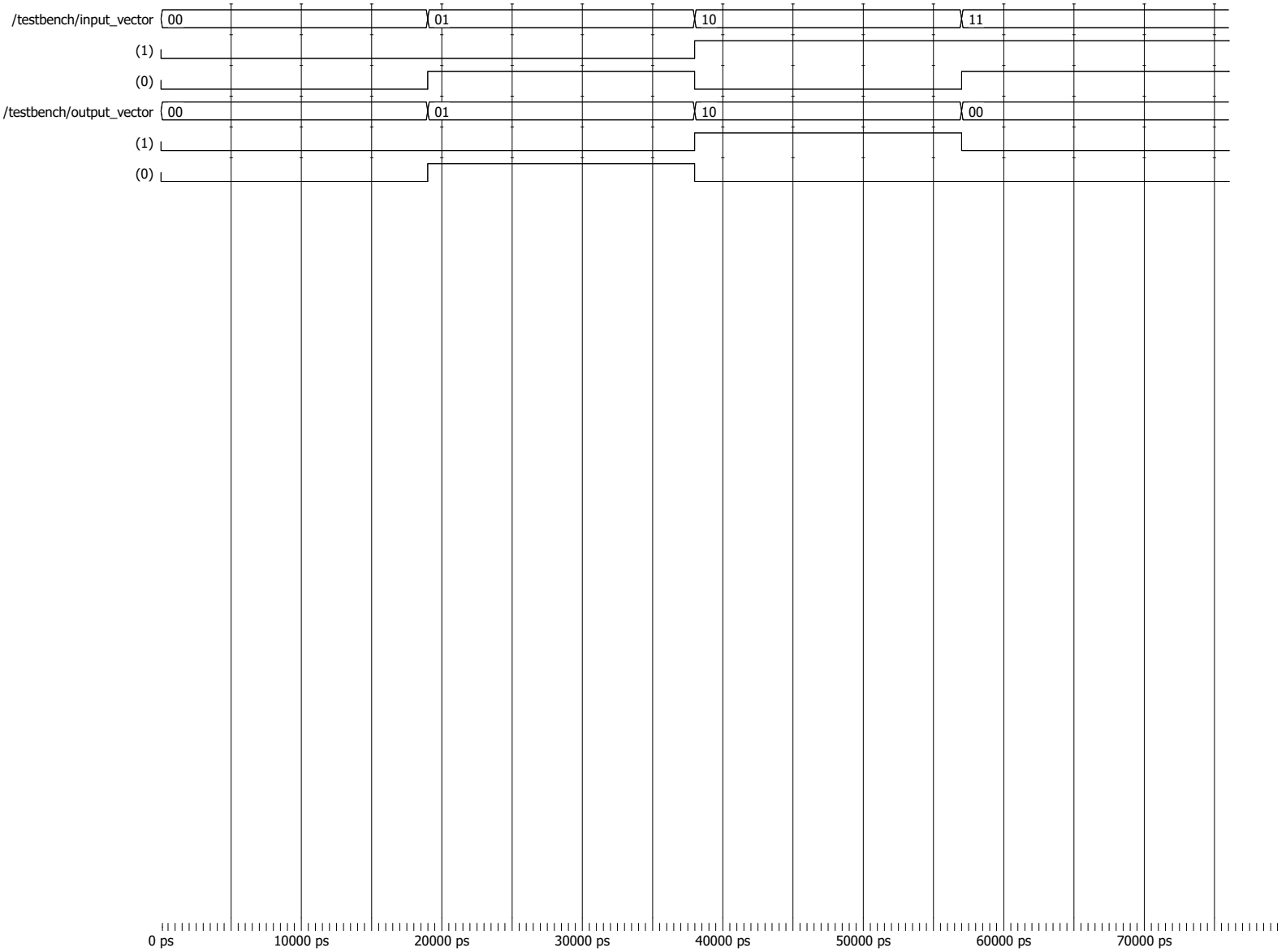

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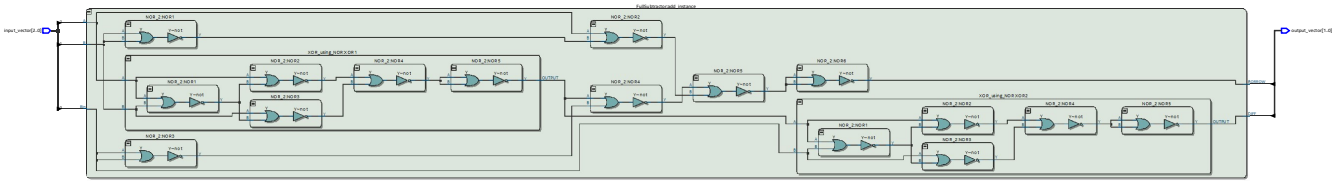
Chapter 6

Full Subtractor using XOR and NOR

Date: August 12, 2023

Project: FS_XOR



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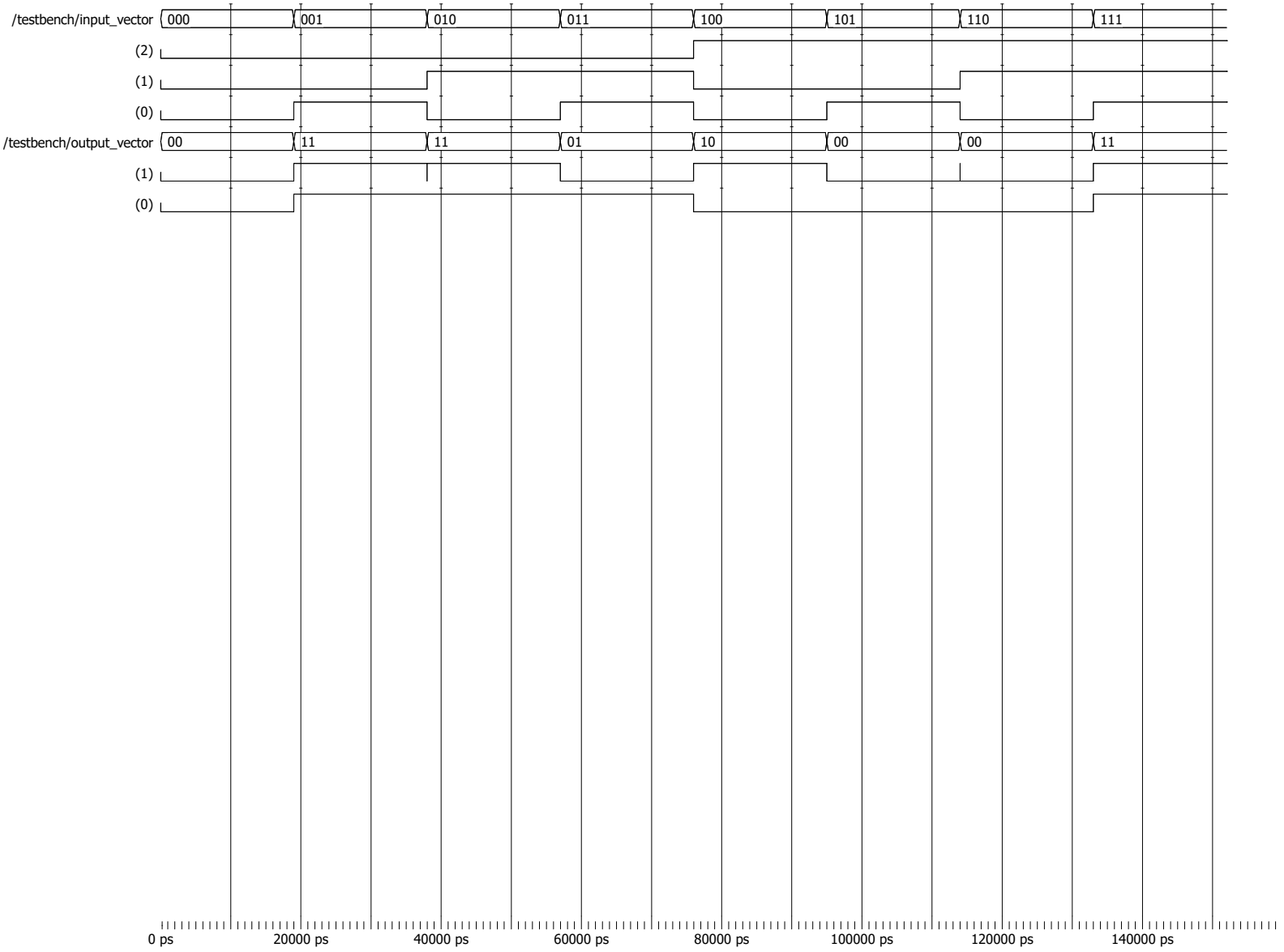

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THANK YOU!