EE214 - Report 3

Fibonacci Detector

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FR-19/T-19

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Introduction

In this report, I have presented my work done on Quartus using VHDL during the third lab.

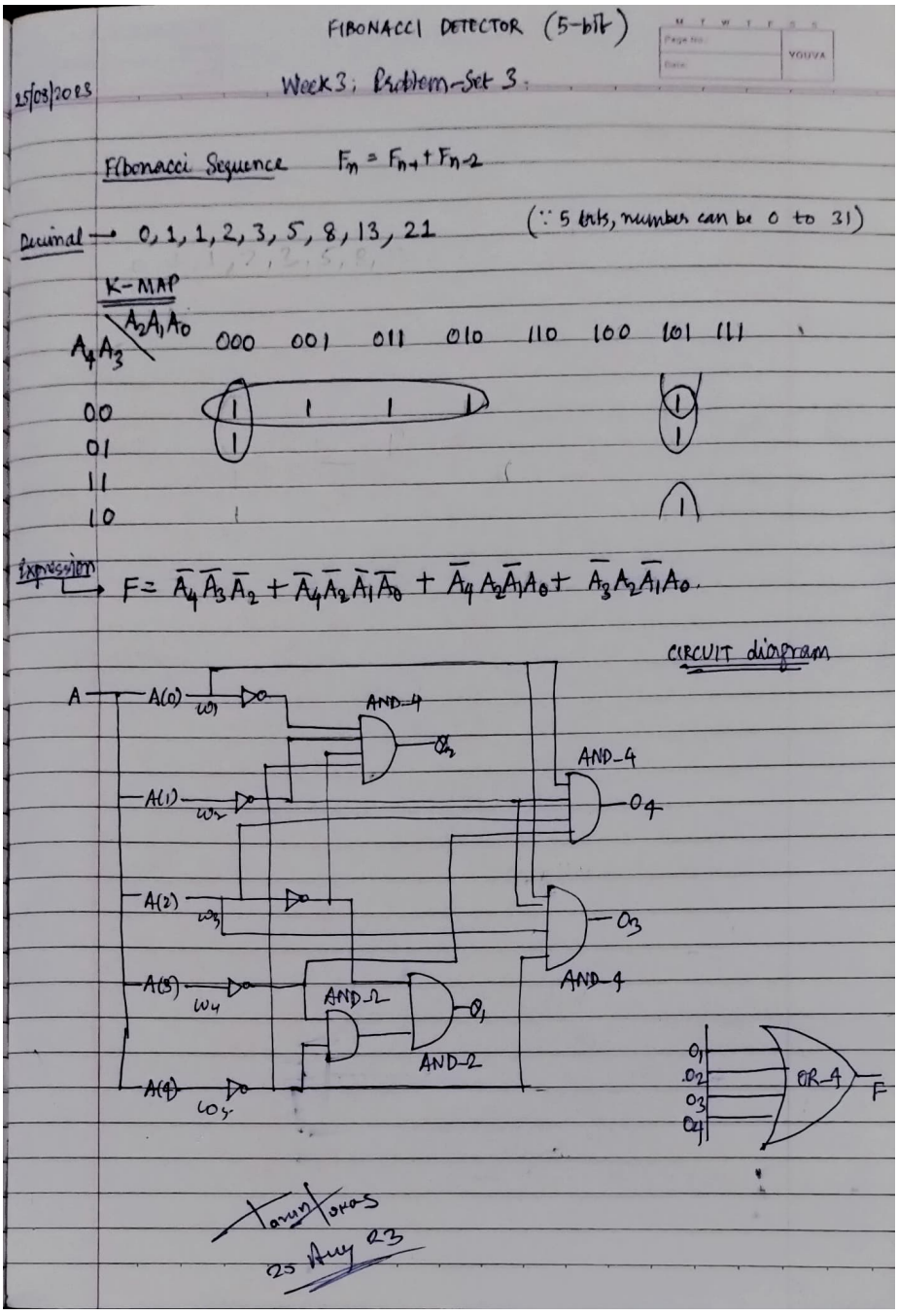
I have also done design verification using Xen-10 FPGA board and verified my design. The pin planner is also included in the report.

The circuit presented in the report has the RTL Viewer followed by the ModelSim Waveform obtained from Quartus.

Chapter 1

K-Maps and Circuit Diagrams

This section contains the k-map and the diagram of the circuit made in the lab.

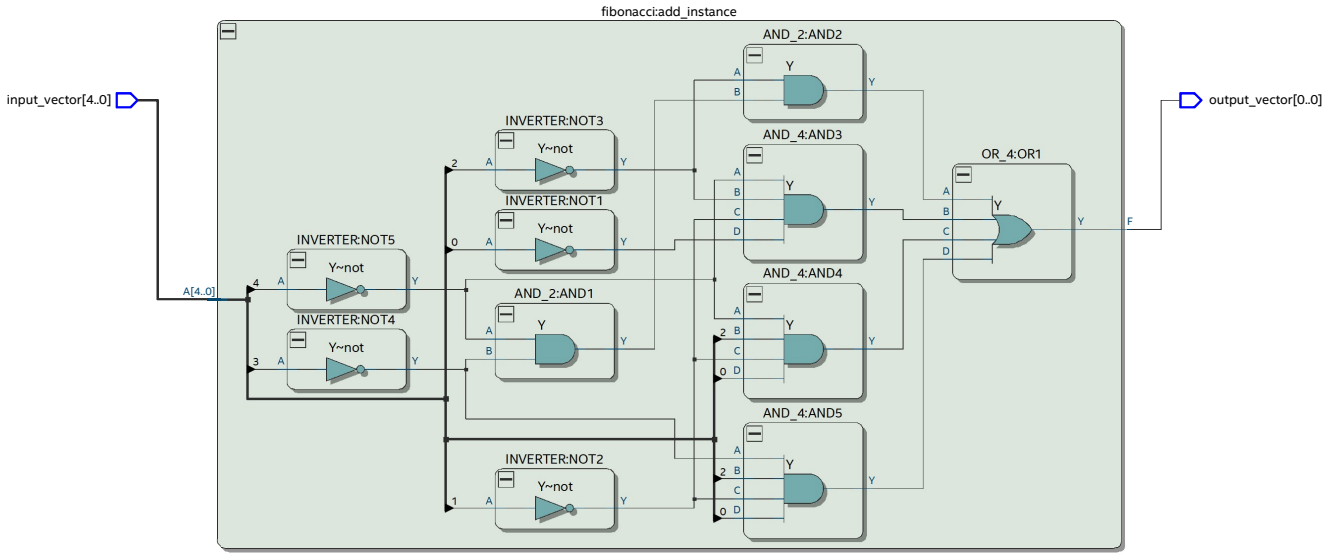

FIBONACCI DETECTOR (5-bit)
25/03/2023
Week 3; Problem-Set 3:
Fibonacci Sequence $F_n = F_{n-1} + F_{n-2}$
Decimal → 0, 1, 1, 2, 3, 5, 8, 13, 21 (∵ 5 bits, number can be 0 to 31)
K-MAP
$A_2A_1A_0$
A_4A_3
000 001 011 010 110 100 101 111
00
01
11
10
Expression → $F = \bar{A}_4\bar{A}_3\bar{A}_2 + \bar{A}_4A_2\bar{A}_1\bar{A}_0 + \bar{A}_4A_2\bar{A}_1A_0 + \bar{A}_3A_2\bar{A}_1A_0$
CIRCUIT diagram
A
A(0)
A(1)
A(2)
A(3)
A(4)
AND-4
AND-4
AND-4
AND-2
AND-2
OR-4
F
25 Aug 23

Chapter 2

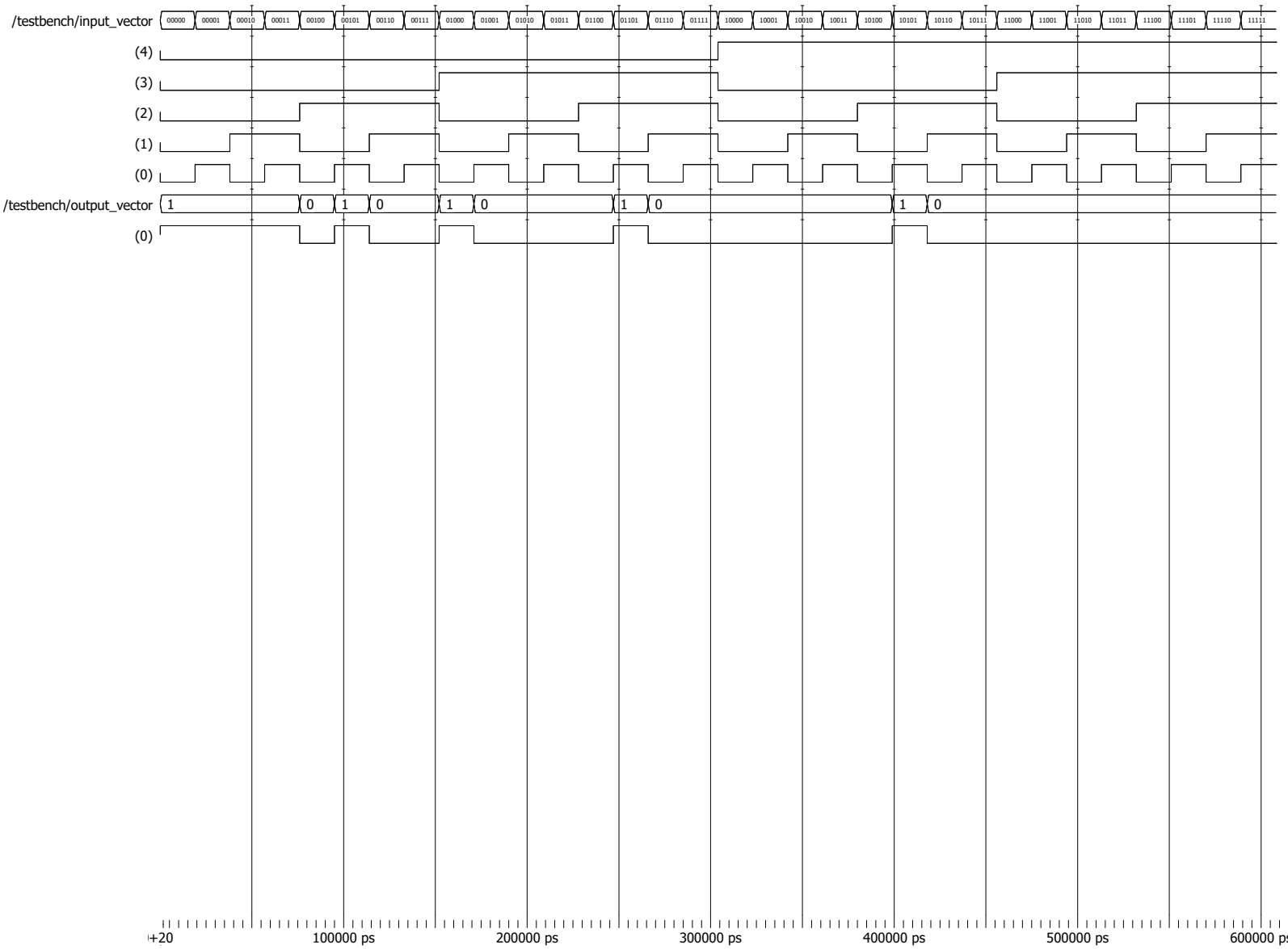
Fibonacci Detector

Date: August 25, 2023

Project: Fibonacci



Revision: DUT



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Chapter 3

Pin Planner

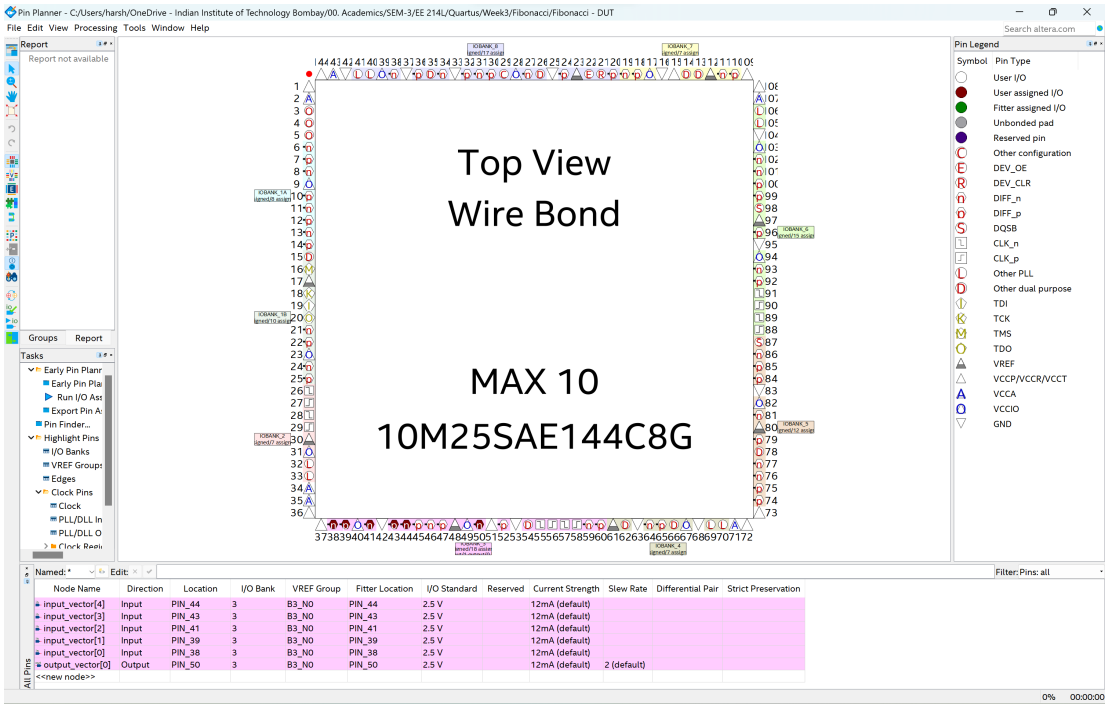

Figure 3.1: Pin Planner for FPGA using Quartus

THANK YOU!