

EE214 - Report 6

Sequence Generator

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Contents

0.1	Objective	2
0.2	Overview	2
1	State Diagram and K-Maps	3
2	Sequence Generator	6
2.1	RTL Viewer	6
2.2	ModelSim and RTL Simulations	7
2.3	ScanChain	8

Introduction

0.1 Objective

The aim of the assignment was to implement a Sequence Generator to print (110011) repeatedly as shown in the figure below using Structural-Dataflow design using D-Flipflops.

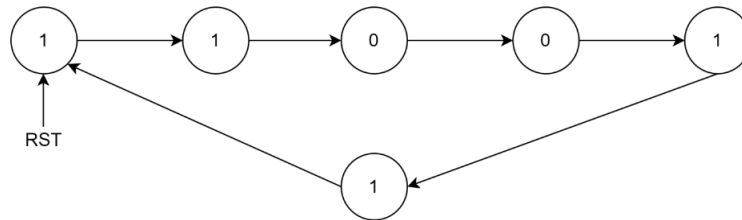


Figure 1: Sequence Generator

Following that, we also had to perform an RTL and then a ScanChain Simulation of the design.

0.2 Overview

In this report, I have presented my work done on Quartus using VHDL during the sixth lab.

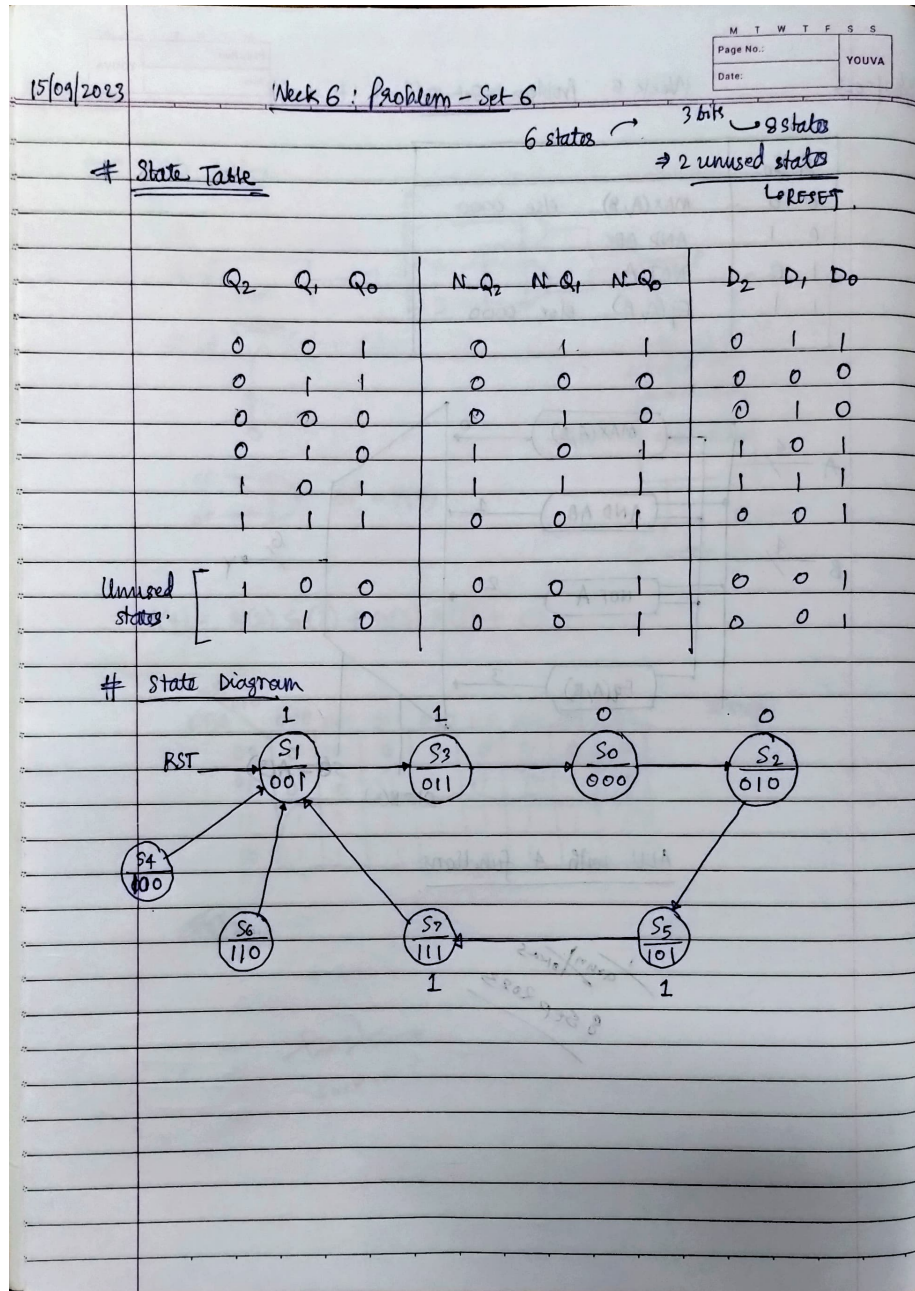
I have also done design verification using ScanChain tool on Xen-10 FPGA board and verified my design. The ScanChain output is also shown in the report.

The circuit presented in the report has the RTL Viewer followed by the ModelSim Waveform and Transcript obtained from Quartus.

Chapter 1

State Diagram and K-Maps

This section contains the outline of the `Sequence Generator` made in the lab.



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K-Map

$D_2:$

$Q_2 \backslash Q_1 Q_0$	00	01	11	10
0	0	0	0	1
1	0	1	0	0

$D_2 = Q_2 \bar{Q}_1 Q_0 + \bar{Q}_2 Q_1 \bar{Q}_0$

$D_1:$

$Q_2 \backslash Q_1 Q_0$	00	01	11	10
0	1	1	0	0
1	0	1	0	0

$D_1 = \bar{Q}_2 \bar{Q}_1 + \bar{Q}_1 Q_0$

$D_0:$

$Q_2 \backslash Q_1 Q_0$	00	01	11	10
0	0	1	0	1
1	1	1	1	1

$D_0 = Q_2 + \bar{Q}_1 Q_0 + Q_1 \bar{Q}_0$

~~Transfers~~
 15 sep 2023

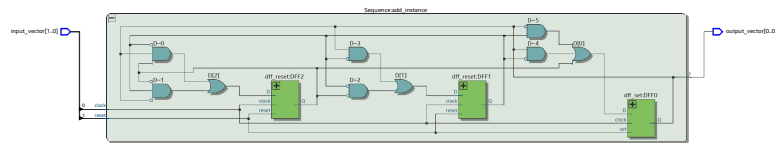
Chapter 2

Sequence Generator

2.1 RTL Viewer

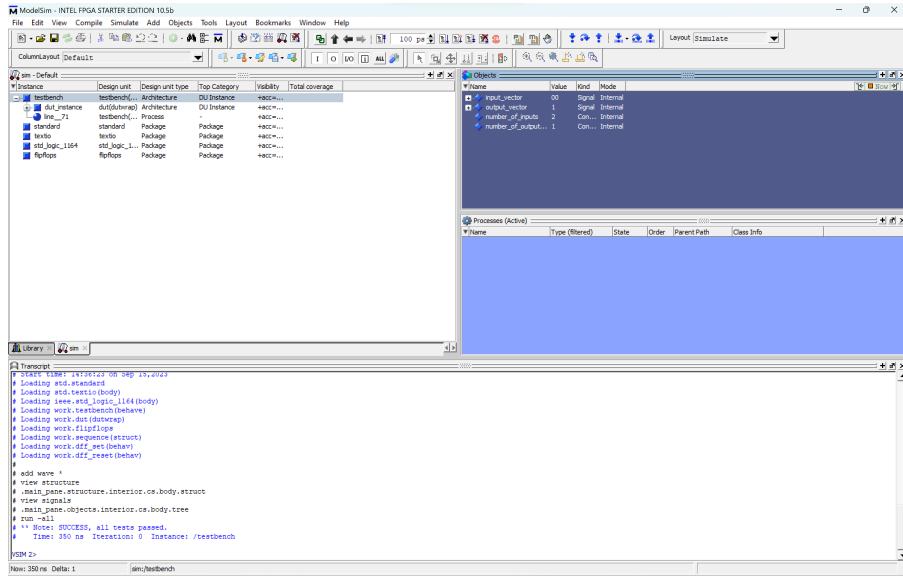
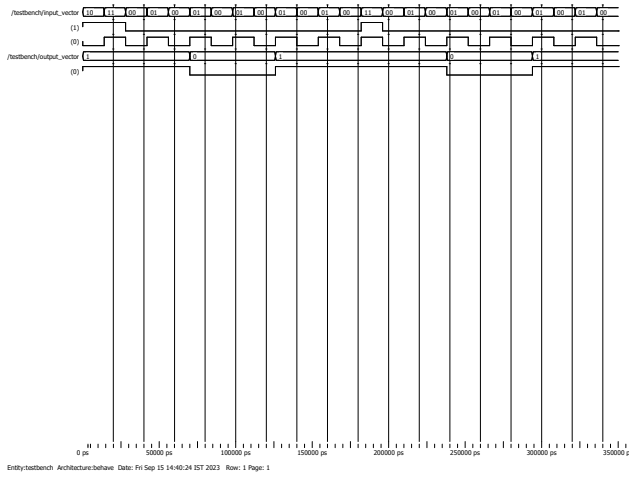
Date: September 15, 2023

Project: Sequence



Page 1 of 1

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2.3 ScanChain

The ScanChain after dumping the `.svf` file gave the following output in `out123.txt`

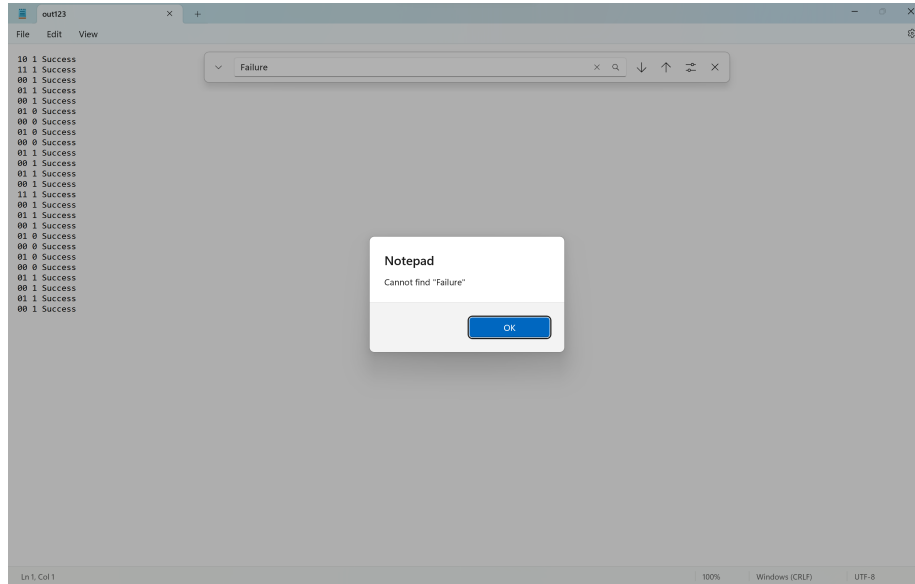


Figure 2.2: Not a single Failure in the ScanChain output.

THANK YOU!