

EE214 - Report 5

ALU - Behavioral Modelling

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FR-19/T-19

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Introduction

In this report, I have presented my work done on Quartus using VHDL during the third lab.

I have also done design verification using ScanChain tool on Xen-10 FPGA board and verified my design. The ScanChain output is also shown in the report.

The circuit presented in the report has the RTL Viewer followed by the ModelSim Waveform and Transcript obtained from Quartus.

Chapter 1

Lab Diagrams

This section contains the outline of the `Behavioral MUX` made in the lab.

8/09/2023

Week 5: Problem - Set 5

M	T	W	T	F	S	S
Page No.						YOUVA
Date						

S ₁	S ₀	Function
0	0	MAX(A, B) else 0000
0	1	AND AB
1	0	NOT A
1	1	Eq(A, B) else 0000

$S1 = B(3)$ $S0 = A(3)$

ALU with 4 functions

8 SEP 2023

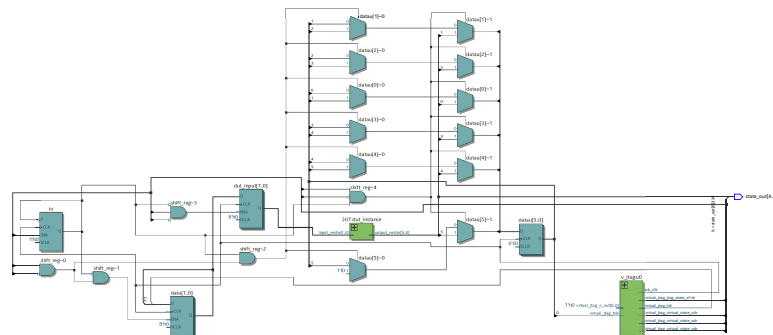
Chapter 2

ALU (Arithmetic Logic Unit)

2.1 RTL Viewer

Date: September 08, 2023

Project: ALU

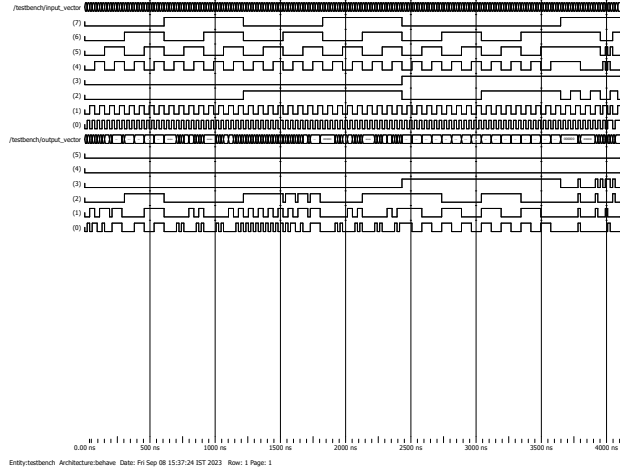


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Revision: DUT

2.2 ModelSim and RTL Simulations

RTL simulations of MUX gave the following ModelSim Waveform



RTL simulations of MUX gave the following transcript

```

Transcript
File Edit View Bookmarks Window Help
# Errors: 0, Warnings: 0
# vcom -93 -work work [C:/Users/harsh/OneDrive - Indian Institute of Technology Bombay/00. Academics/SEM-3/EE 2145/Quartus/Week5/ALU/DUT.vhdl]
# Model Technology ModelSim - Intel FPG Edition vcom 10.5b Compiler 2016.10 Oct 5 2016
# Start time: 15:39:04 on Sep 08, 2023
# vcom -reportprogress 300 -93 -work work C:/Users/harsh/OneDrive - Indian Institute of Technology Bombay/00. Academics/SEM-3/EE 2145/Quartus/Week5/ALU/DUT.vhdl
# -- Loading package STANDARD
# -- Loading package std_logic_1164
# -- Compiling entity DUT
# -- Compiling architecture DUT of DUT
# End time: 15:39:04 on Sep 08, 2023, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# vcom -93 -work work [C:/Users/harsh/OneDrive - Indian Institute of Technology Bombay/00. Academics/SEM-3/EE 2145/Quartus/Week5/ALU/DUT.vhdl]
# Model Technology ModelSim - Intel FPG Edition vcom 10.5b Compiler 2016.10 Oct 5 2016
# Start time: 15:39:04 on Sep 08, 2023
# vcom -reportprogress 300 -93 -work work C:/Users/harsh/OneDrive - Indian Institute of Technology Bombay/00. Academics/SEM-3/EE 2145/Quartus/Week5/ALU/DUT.vhdl
# -- Loading package STANDARD
# -- Loading package std_logic_1164
# -- Compiling entity alu_beh
# -- Compiling architecture al of alu_beh
# End time: 15:39:04 on Sep 08, 2023, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# vcom -93 -work work [C:/Users/harsh/OneDrive - Indian Institute of Technology Bombay/00. Academics/SEM-3/EE 2145/Quartus/Week5/ALU/Testbench.vhdl]
# Model Technology ModelSim - Intel FPG Edition vcom 10.5b Compiler 2016.10 Oct 5 2016
# Start time: 15:39:04 on Sep 08, 2023
# vcom -reportprogress 300 -93 -work work C:/Users/harsh/OneDrive - Indian Institute of Technology Bombay/00. Academics/SEM-3/EE 2145/Quartus/Week5/ALU/Testbench.vhdl
# -- Loading package STANDARD
# -- Loading package std_logic_1164
# -- Compiling entity Testbench
# -- Compiling architecture Behave of Testbench
# End time: 15:39:04 on Sep 08, 2023, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
#
# vsim -lps -l altera -l lpm -l ngate -l altera_gd -l altera_insim -l fifyfivevm -l rtl_work -l work -l v_tag -voptargs="+acc" Testbench
# Start time: 15:39:04 on Sep 08, 2023
# Loading std.standard
# Loading std.testio(body)
# Loading tree_std_logic_1164(body)
# Loading work.testbench(behave)
# Loading work.interrupt
# Loading work.alu_beh(al)
#
# add wave *
# view structure
# main.panel.structure.interior.ca.body.structure
# view signals
# main.panel.objects.interior.ca.body.tree
# run -all
# ** Note: SUCCESS, all tests passed.
# Time: 4104 ns Iteration: 0 Instance: /testbench
VSIOM 2>

```

Figure 2.1: Successful Transcript of Behavioral MUX

2.3 ScanChain

The ScanChain after dumping the `.svf` file gave the following output in `out123.txt`

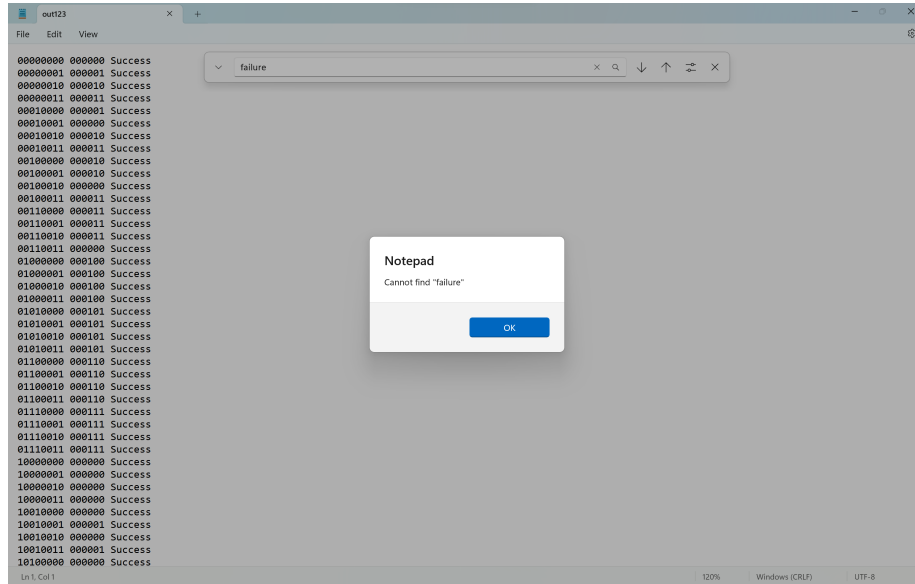


Figure 2.2: Not a single Failure in the ScanChain output.

THANK YOU!