

EE214 - Report 8

Clock Divider

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FR-19/T-19

14th October 2023

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Introduction

0.1 Objective

The aim of the assignment was to implement a clock divider which alternatively prints '0' and '1' at a specific frequency by using the Master Clock input of 50MHz. This was to be implemented using Behavioural modelling.

There is also a `reset` input that can be used to hold the `new_clock` to either '1' or '0'.

After that, we had to perform RTL Simulation with a Testbench to ensure that the design was correct.

Finally we also had to implement it on a Xen10 Board with proper pin planning.

0.2 Overview

In this report, I have presented my work done on Quartus using VHDL during the eighth lab.

I have also done design verification with pin planning on Xen-10 FPGA board and verified my design.

The circuit presented in the report has the ModelSim Waveform obtained from Quartus for frequencies of 250 Hz and 0.5 Hz.

Chapter 1

Lab Design

This section contains the outline of the logic made in the lab for implementing the clock divider and LED output.

13/10/2023

Week 8: Problem-Set 8

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50MHz 250Hz
0.5Hz

① $\text{count} = \frac{50\text{MHz}}{2 \times 250\text{Hz}} = 100000$

② $\text{count} = \frac{50\text{MHz}}{2 \times 0.5\text{Hz}} = 50000000$

Switch (SW)

For LED switching

SW = 0 → led-parity (default = 1)

Implemented if-else block.

```

if (led-parity == 0); led-parity ← 1
    LED 1 AND LED 2;
elseif (led-parity == 1); led-parity ← 2
    LED 3 AND LED 4;
elseif (led-parity == 2); led-parity ← 3
    LED 5 AND LED 6;
else; led-parity ← 0
    LED 7 AND LED 8
  
```

PSEUDOCODE for implementation -

SW = 1

128 → 64

```

if (counter ≤ 64)
  counter ← 128;
i (counter ≥ 64)
  counter = counter - 1;
  
```

~~Amstorkus~~
13 Oct 2023

Chapter 2

Clock Divider

2.1 ModelSim and RTL Simulations

RTL simulations of Clock Divider gave the following ModelSim Waveforms for the frequencies 250 Hz and 0.5 Hz. The frequency can be verified by calculating the number of pulses in a given time interval.

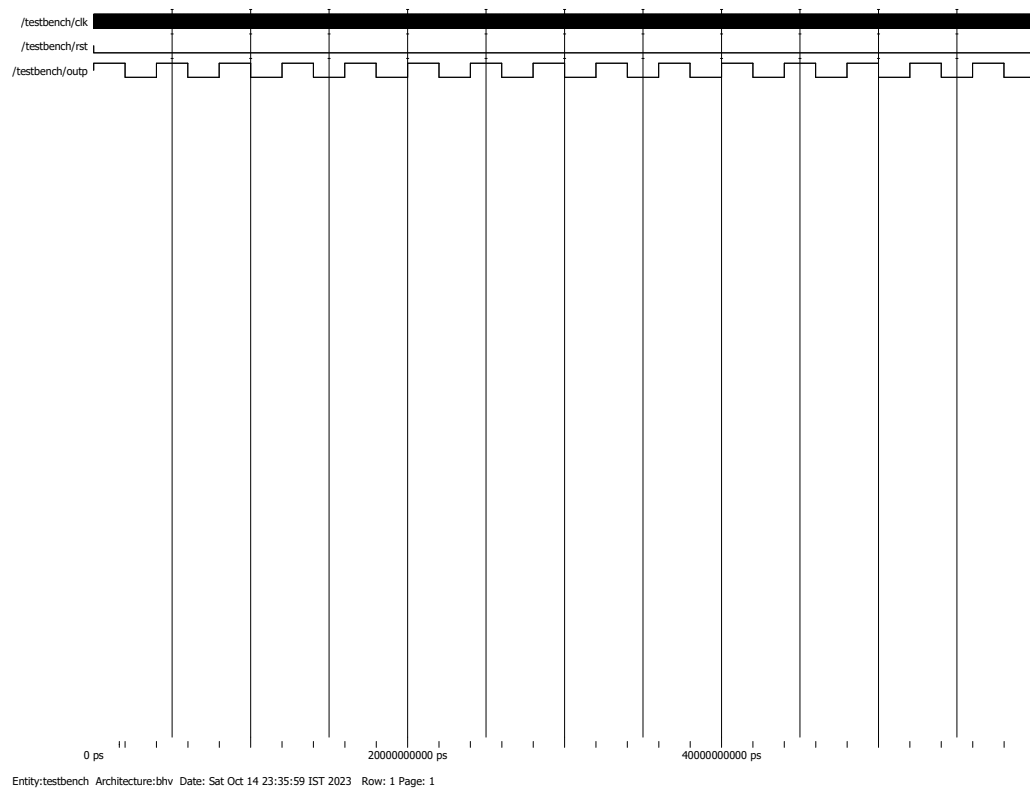


Figure 2.1: $f = 250 \text{ Hz}$

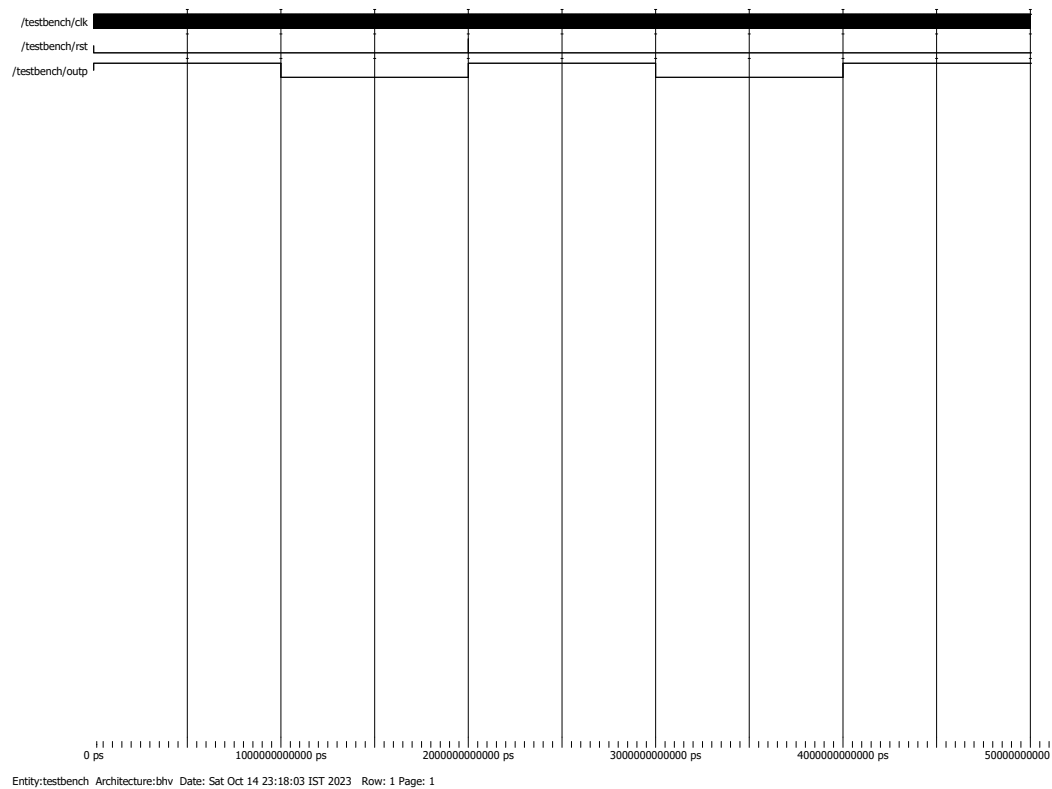


Figure 2.2: $f = 0.5 \text{ Hz}$

THANK YOU!