EE214 - Report 2

Designing Multiplexers (MUX)

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FR-19/T-19

18th August 2023

Contents

Introduction

In this report, I have presented my work done on Quartus using VHDL during the second lab.

All the gates presented in the report have the RTL Viewer followed by the ModelSim Waveform obtained from Quartus.

Chapter 1

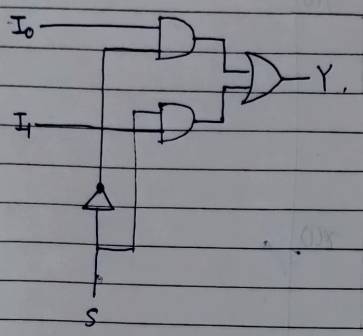
Lab Diagrams

This section contains the diagrams of the gates made in the lab.

16/08/2023 Week 2: Problem-Set 2.

* Problem Statement :-

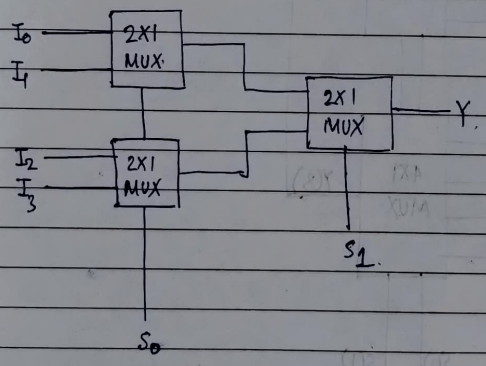
① Part-A: 2X1 Mux.

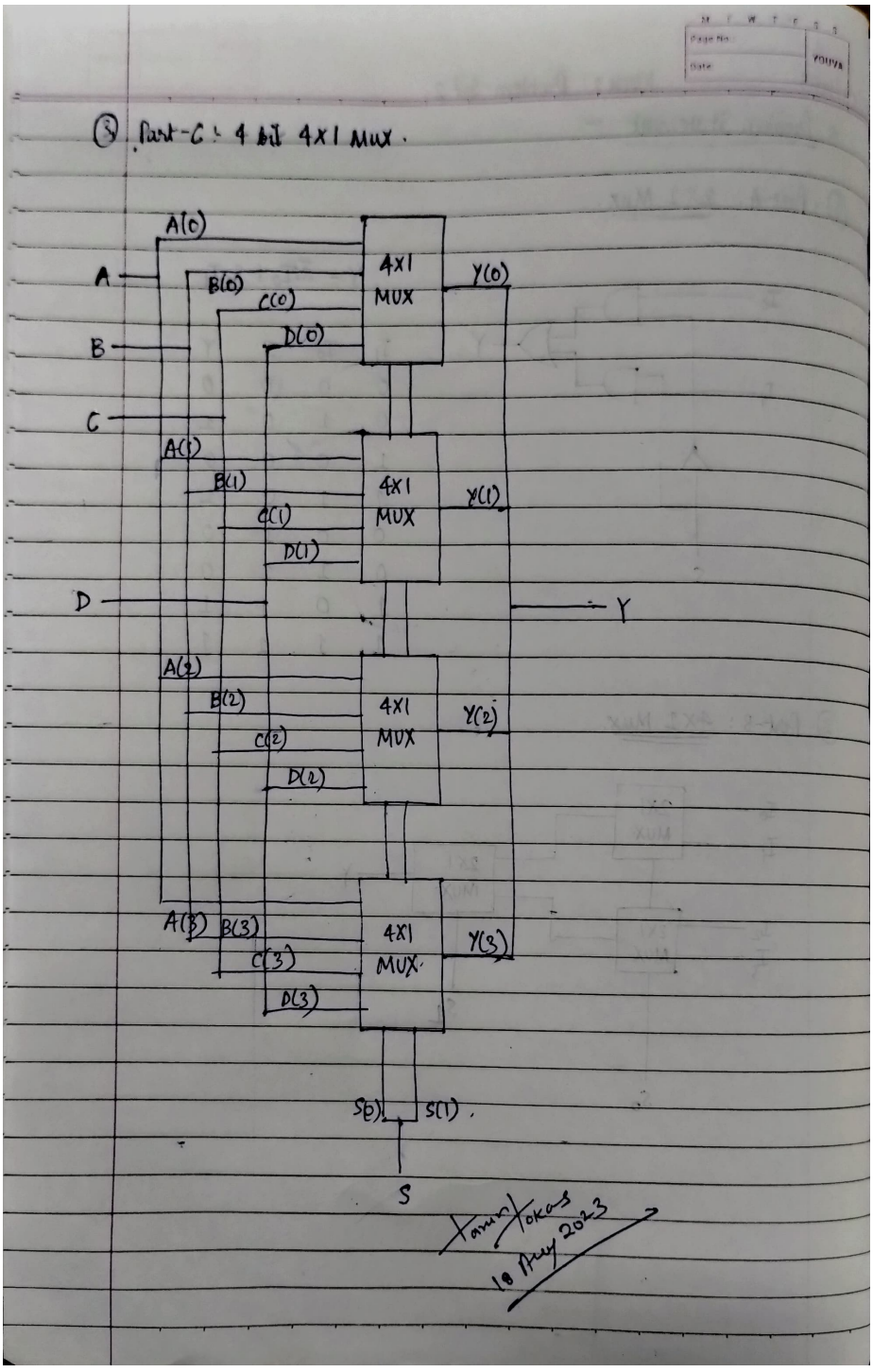


$Y = \bar{S}.I_0 + S.I_1$

I_1	I_0	S	Y
0	0	0	0
0	1	0	1
1	0	0	0
1	1	0	1
0	0	1	0
0	1	1	0
1	0	1	1
1	1	1	1

② Part-B: 4X1 Mux.



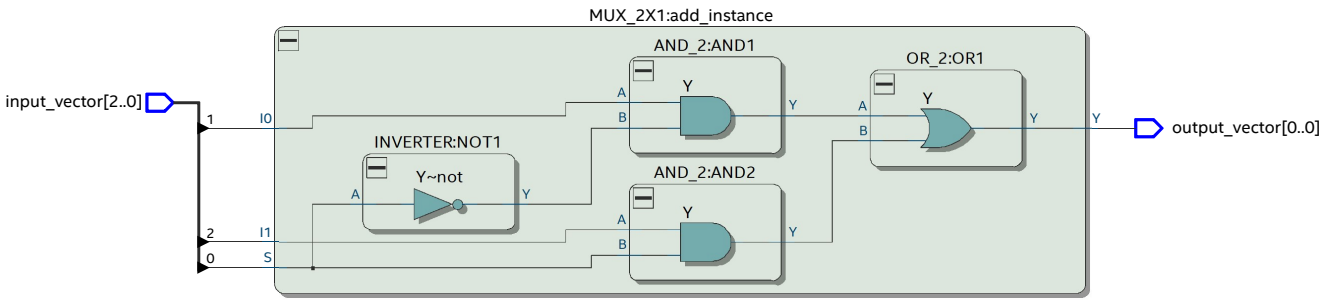

3. Part-C : 4 bit 4x1 Mux.
A(0)
A
B(0)
C(0)
D(0)
B
C
A(1)
B(1)
C(1)
D(1)
D
A(2)
B(2)
C(2)
D(2)
A(3)
B(3)
C(3)
D(3)
4x1 MUX
4x1 MUX
4x1 MUX
4x1 MUX
Y(0)
Y(1)
Y(2)
Y(3)
Y
S(0)
S(1)
S
Tanmay Tokas
18 May 2023

Chapter 2

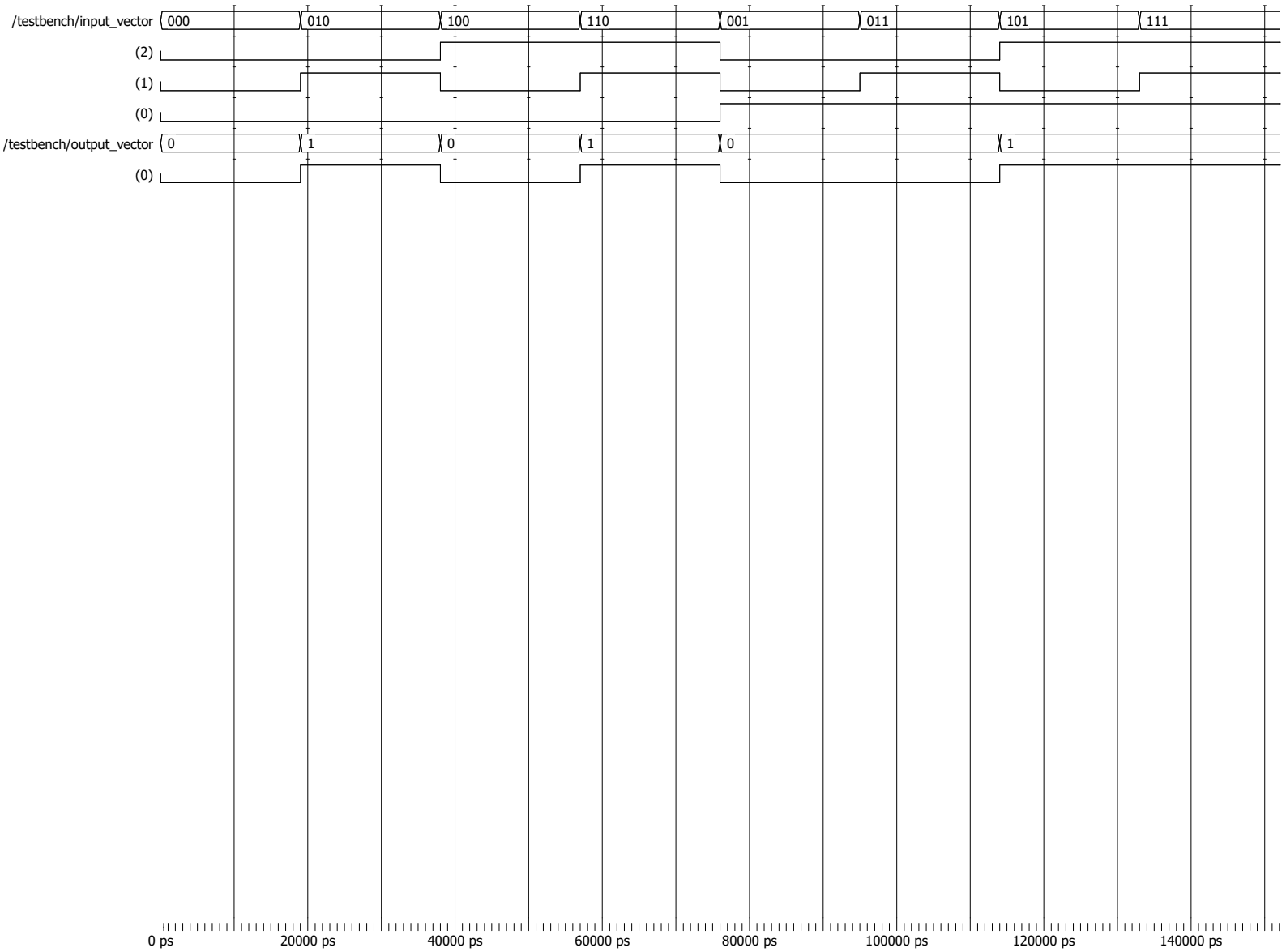
2x1 MUX (Multiplexer)

Date: August 18, 2023

Project: MUX_2X1



Revision: DUT



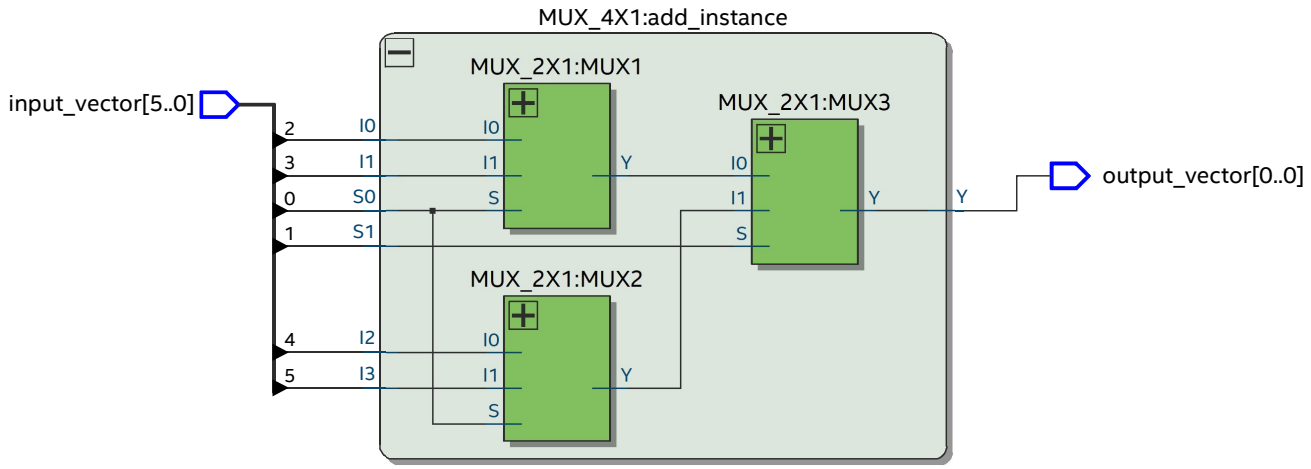
Entity:testbench Architecture:behave Date: Fri Aug 18 15:50:35 IST 2023 Row: 1 Page: 1

Chapter 3

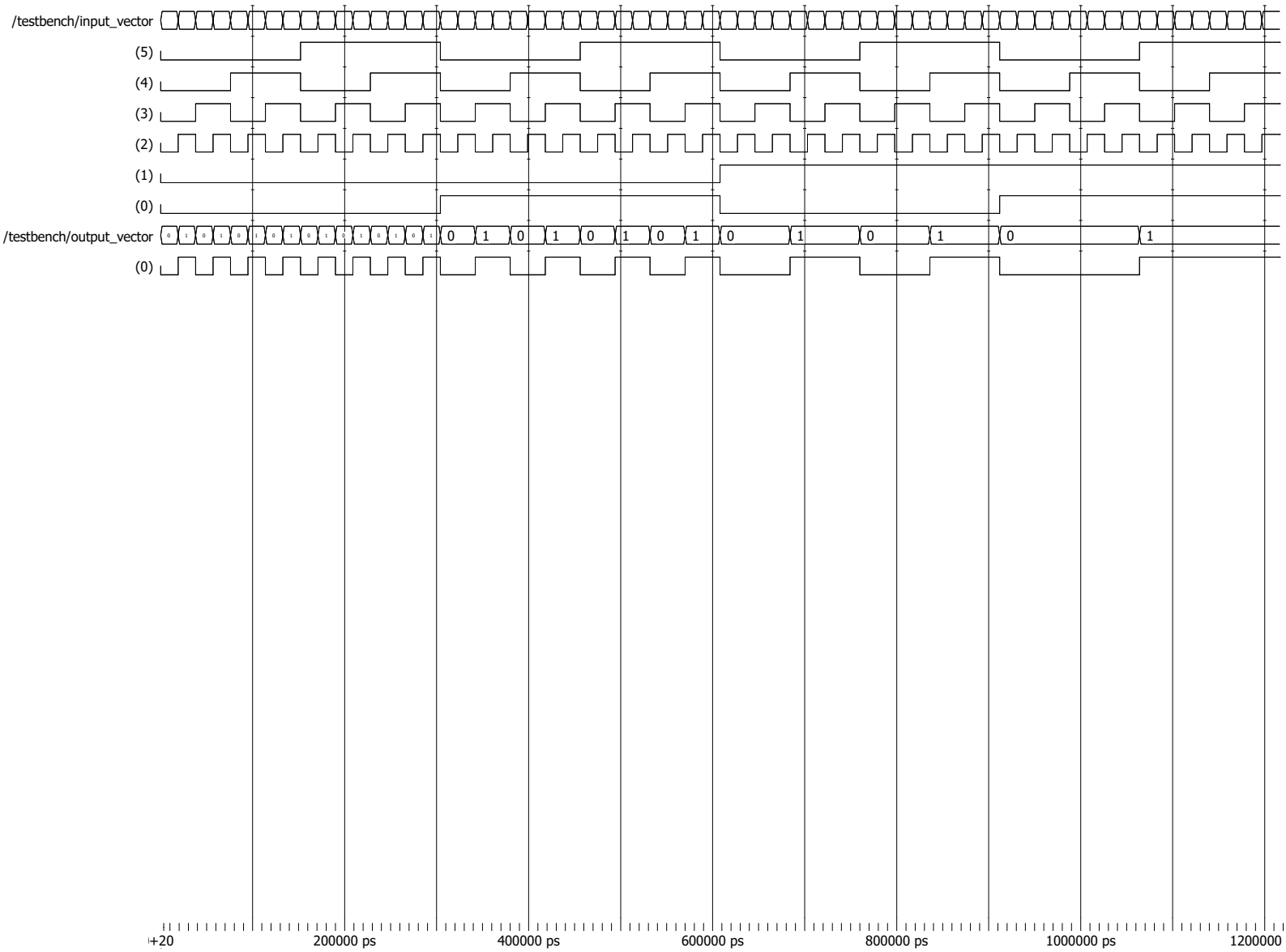
4X1 MUX (Multiplexer)

Date: August 18, 2023

Project: MUX_4X1



Revision: DUT



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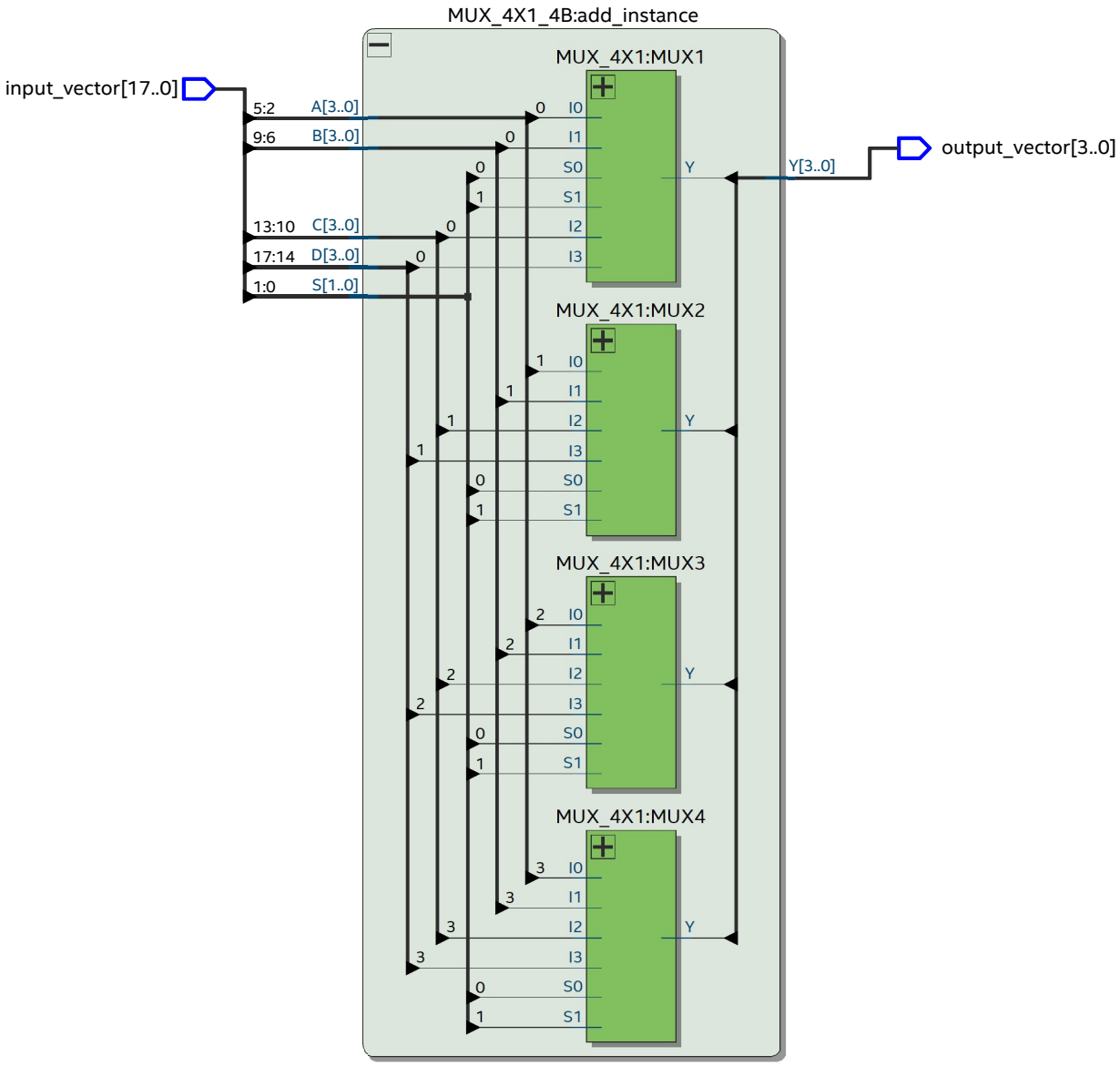
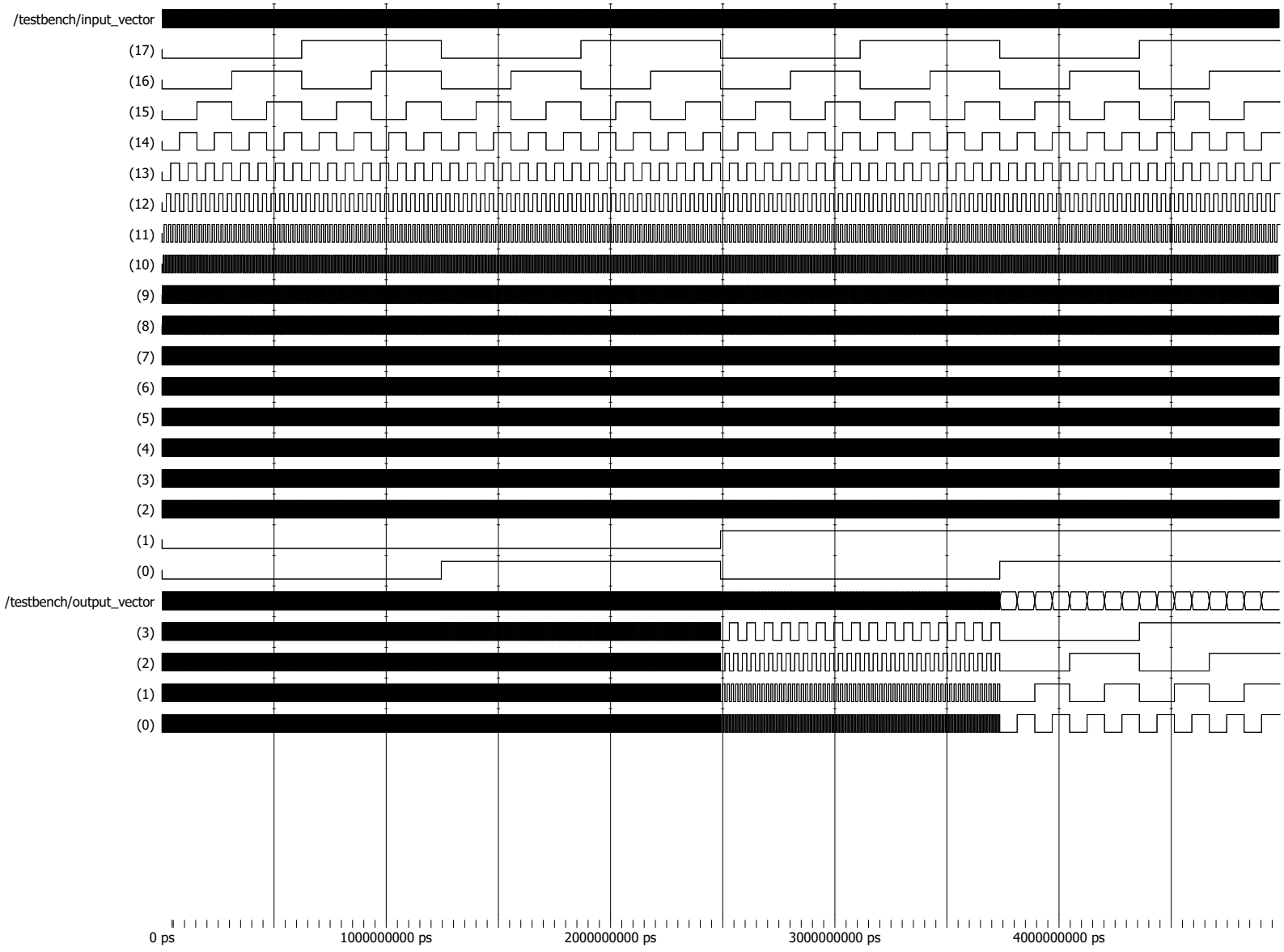
Chapter 4

4-bit 4X1 MUX


MUX_4X1_4B:add_instance
MUX_4X1:MUX1
MUX_4X1:MUX2
MUX_4X1:MUX3
MUX_4X1:MUX4
input_vector[17..0]
output_vector[3..0]
Y[3..0]
5:2 A[3..0]
9:6 B[3..0]
13:10 C[3..0]
17:14 D[3..0]
1:0 S[1..0]
I0
I1
I2
I3
S0
S1
Y



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THANK YOU!