PRODUCT SPECIFICATION

TFT-LCD MODULE

Model No:FRD400B25025-A-CTK

For Customer's Acceptance	
Approved by	**Comment**

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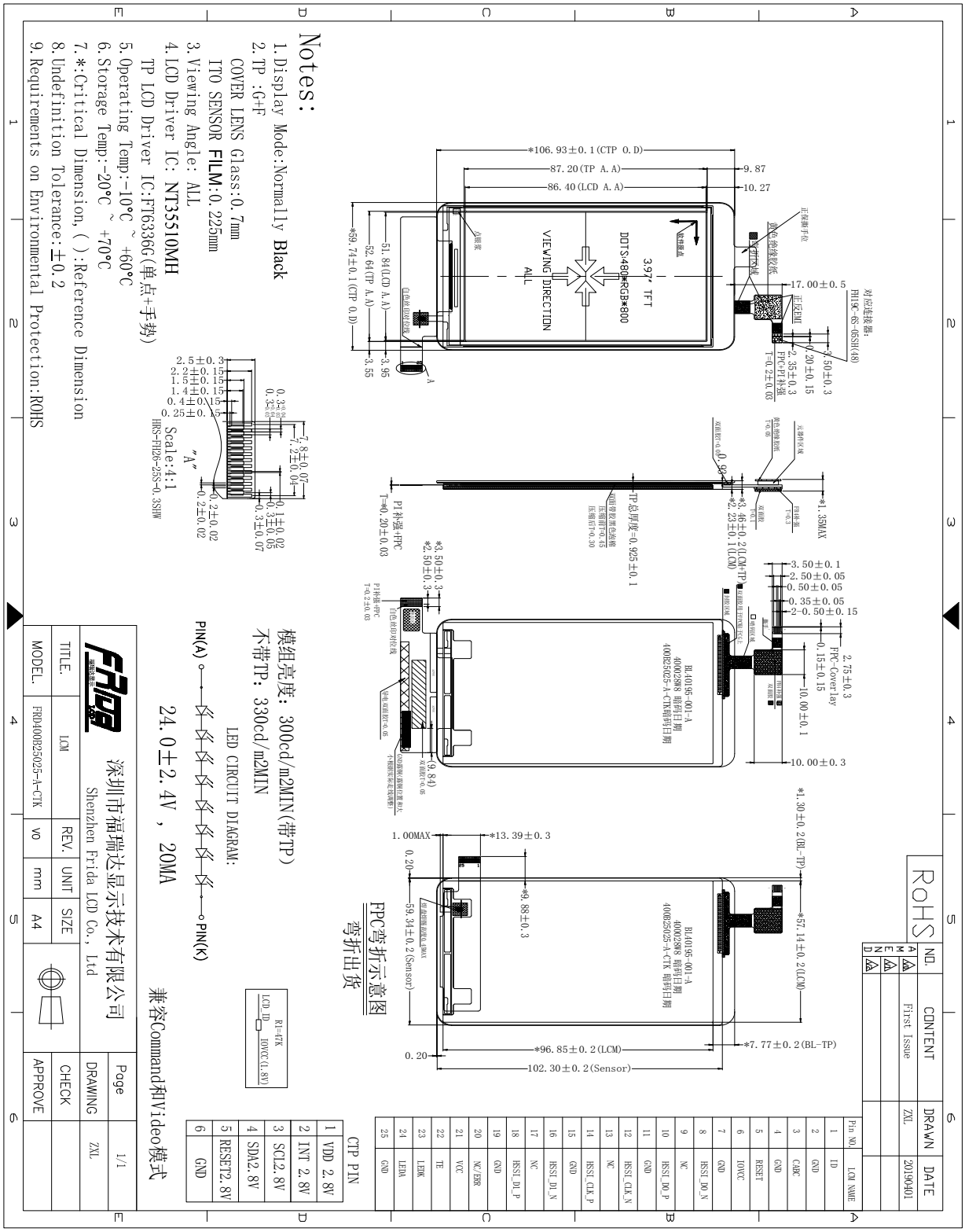
Document Revision History :

1. DOCUMENT REVISION	DATE	DESCRIPTION	PREPARED BY
A	2019-04-18	First Release.	

2. General Description

No	Item	Specification	Remark
1	Screen Size	4.0 inch	
2	Display Mode	Normally Black	
3	Resolution	480 × RGB × 800	
4	Active Area	51.84*86.40	
5	Outline Dimension	59.74*106.93*3.46	
6	Viewing Direction	ALL	
7	Driver IC	NT35510MH	参照NT35510_V3.0
8	Interface	MIPI	
9	Back Light	White Led*8	
10	Touch Panel	CTP Controller FT6336G	I2C Slave Address 0x70

3. Outline Dimension



Pin NO.	LCM NAME
1	ID
2	GND
3	CABC
4	GND
5	RESET
6	IOVCC
7	GND
8	HSD1_D0_N
9	NC
10	HSD1_D0_P
11	GND
12	HSD1_CLK_N
13	NC
14	HSD1_CLK_P
15	GND
16	HSD1_D1_N
17	NC
18	HSD1_D1_P
19	GND
20	NC/IERR
21	VCC
22	TE
23	LEDK
24	LEDA
25	GND

CTP PIN	
1	VDD 2.8V
2	INT 2.8V
3	SCL2.8V
4	SDA2.8V
5	RESET2.8V
6	GND

4. Interface Specification

Pin No	Symbol	Description	Note
1	ID	ID read PIN for ID circuit.	Note1
2	GND	Ground	
3	CABC	PWM (Pulse Width Modulation) Signal Of LED Driving.	
4	GND	Ground	
5	RESET	Reset Signal input pin.	
6	IOVCC	Power Supply For I/O.	
7	GND	Ground	
8	HSSI_D0N	Negative polarity of low voltage differential data 0 signal	
9	NC	No Connection.	
10	HSSI_D0P	Positive polarity of low voltage differential data 0 signal	
11	GND	Ground	
12	HSSI_CLKN	Negative polarity of low voltage differential clock signal	
13	NC	No Connection.	
14	HSSI_CLKP	Positive polarity of low voltage differential clock signal	
15	GND	Ground	
16	HSSI_D1N	Negative polarity of low voltage differential data 1 signal	
17	NC	Data bus	
18	HSSI_D1P	Positive polarity of low voltage differential data 1 signal	
19	GND	Ground	
20	NC/ERR	No Connection.	
21	VCC	Power Supply For LCD.	
22	TE	Frame head pulse for tearing effect.	
23	LEDK	Power Supply For LED Backlight Cathode Input.	
24	LEDA	Power Supply For LED Backlight Anode Input.	
25	GND	Ground	

Note1：ID Circuit diagram

CTP接口定义

Pin No	Symbol	Description	Note
1	VDD 2.8V	Power supply for CTP	
2	INT 2.8V	Interrupt request signal For CTP	
3	SCL 2.8V	Serial clock signal pin For CTP	
4	SDA 2.8V	Serial data input/output pin For CTP	
5	RESET2.8V	Reset signal input Pin For CTP	
6	GND	Ground.	

5.Absolute Maximum Ratings

Electrical Maximum Ratings – for IC Only

Parameter	Symbol	Min.	Max.	Unit	Note
Power supply voltage (VCC)	VCC	-0.3	+5.5	V	1
Power supply voltage (IOVCC)	IOVCC	-0.3	+5.5	V	1

Note:

1.IOVCC,VCC, GND must be maintained.

2.The modules may be destroyed if they are used beyond the absolute maximum ratings.

6. Electrical Specifications

At Ta = 25 ℃, VCC= 2.5V to 3.6V, IOVCC= 1.65V to 3.6V GND=0V.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (analog)	VCC-GND		2.3	3.7	4.8	V
Supply voltage (logic)	IOVCC-GND		1.65	1.8	3.3	V
Supply current (Logic & LCD)	VCC	VCC=2.8V	-	-	-	mA
Supply voltage of white LED backlight	VLED	Forward current =20mA Number of LED = 8	-	24	-	V

7.Timing Characteristics

7.6.5.1 HIGH SPEED MODE

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	-	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	2	-	12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3xUI	ps	

Note) Dn = D0 and D1.

Fig. 7.6.4 DSI clock channel timing

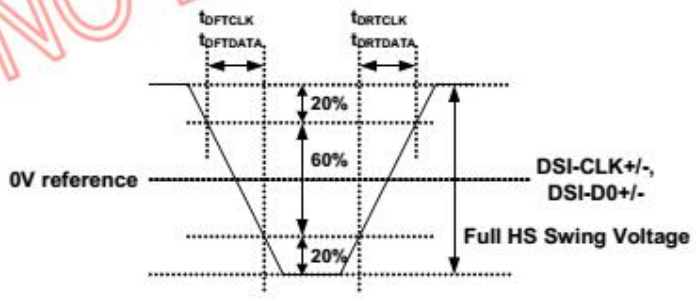


Fig. 7.6.5 Rising and fall time on clock and data channel

7.6.5.2 LOW POWER MODE

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	2xT_{LPXD}	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	5xT_{LPXD}	-	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	4xT_{LPXD}	-	-	ns	Output

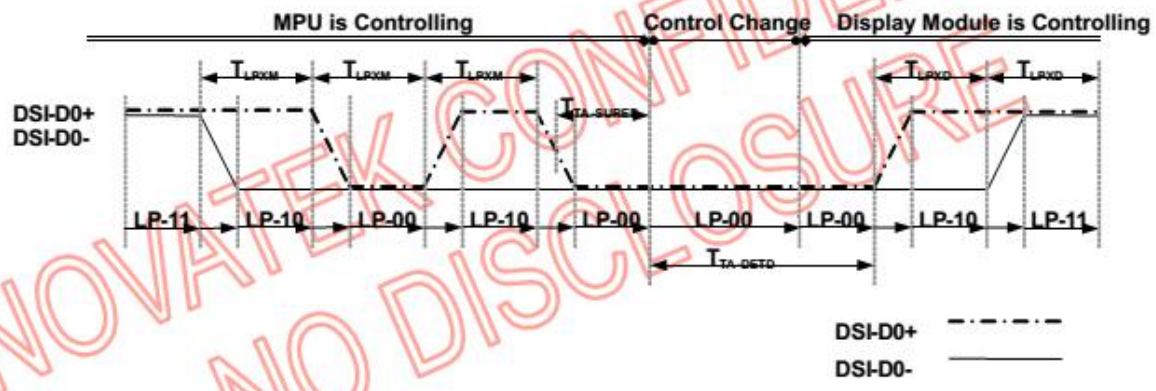


Fig. 7.6.6 Bus Turnaround (BAT) from MPU to display module Timing

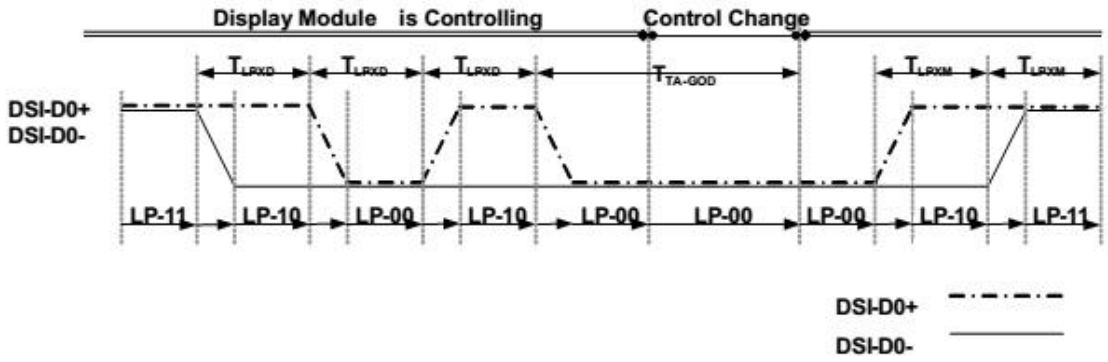


Fig. 7.6.7 Bus Turnaround (BAT) from display module to MPU Timing

7.6.5.3 DSI BURSTS

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.3V, VDD=2.3V to 4.8V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T_{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	$T_{HS-TERM-EN}$	Time to enable data receiver line termination measured from when Dn crosses V_{ILMAX}	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	$T_{CLK-POS}$	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note) Dn = D0 and D1.

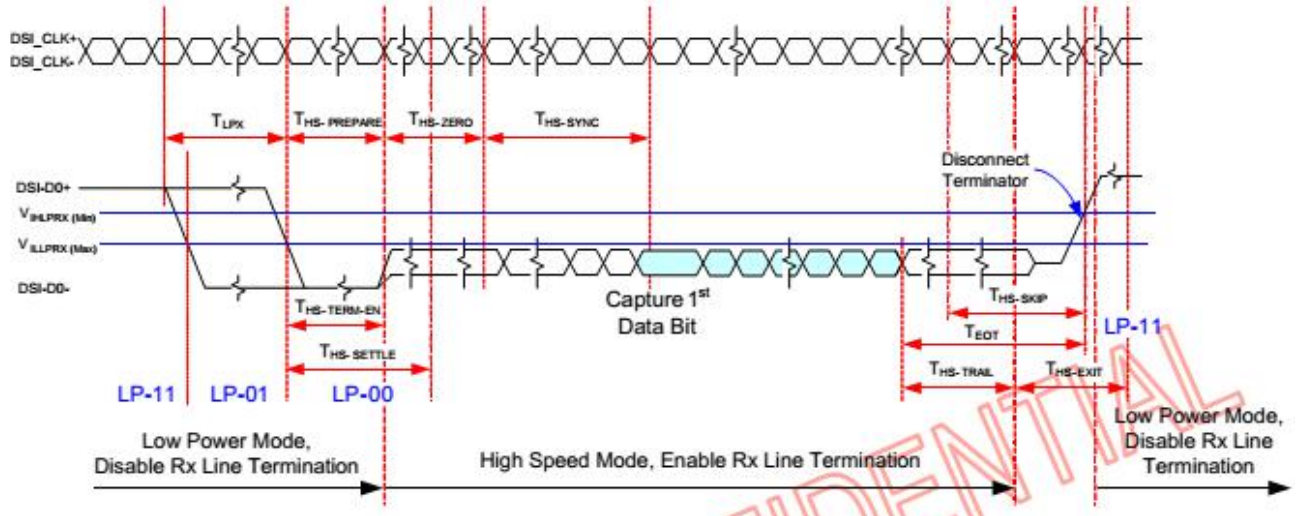


Fig. 7.6.8 Data lanes-Low Power Mode to/from High Speed Mode Timing

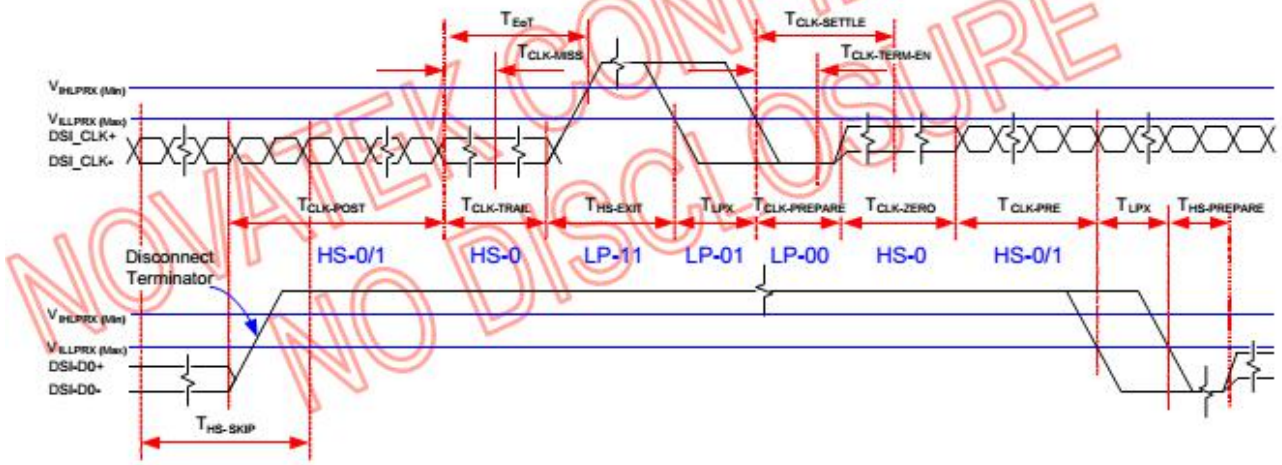


Fig. 7.6.9 Clock lanes- High Speed Mode to/from Low Power Mode Timing

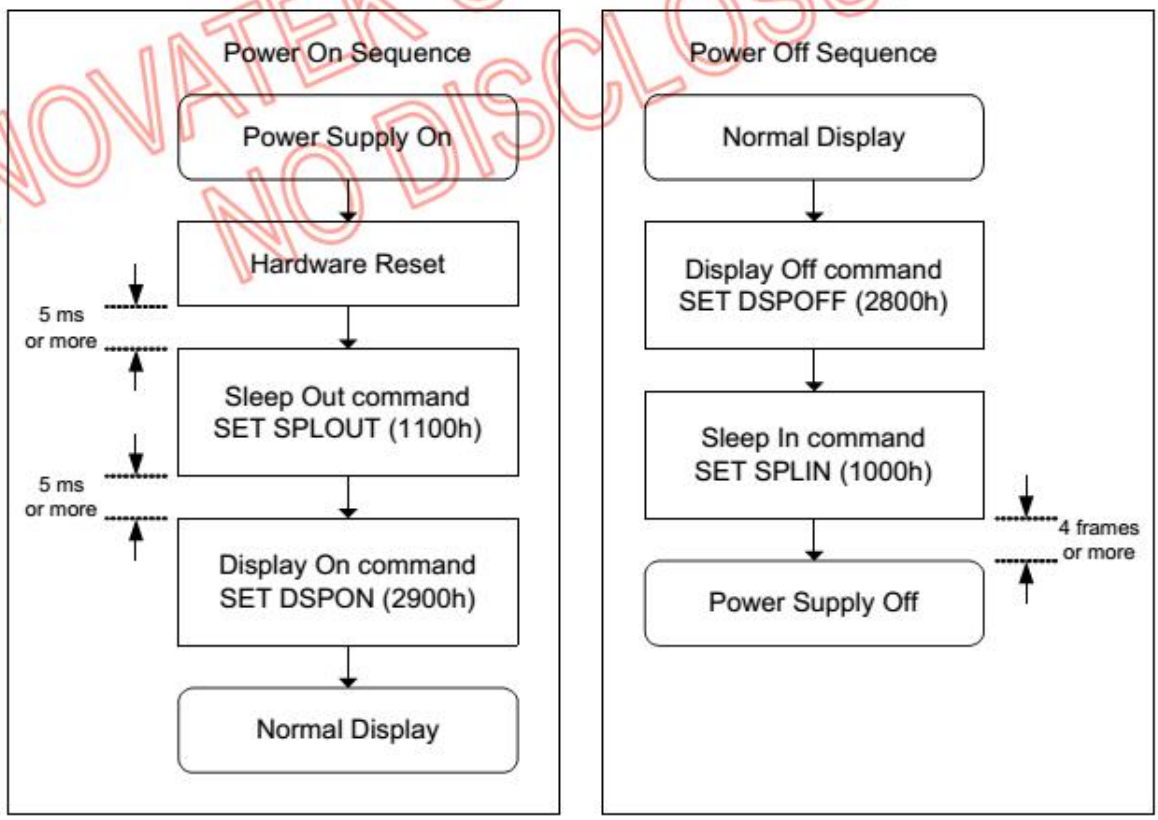
8. Power Supply Configuration

5.12 Power On/Off Sequence

VDDI and VDD (VDDA) can be applied in any order.
VDD (VDDA) and VDDI can be powered down in any order.
During power off, if LCD is in the Sleep Out mode, VDD (VDDA) and VDDI must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or VDD (VDDA) can be powered down minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.
Notes:

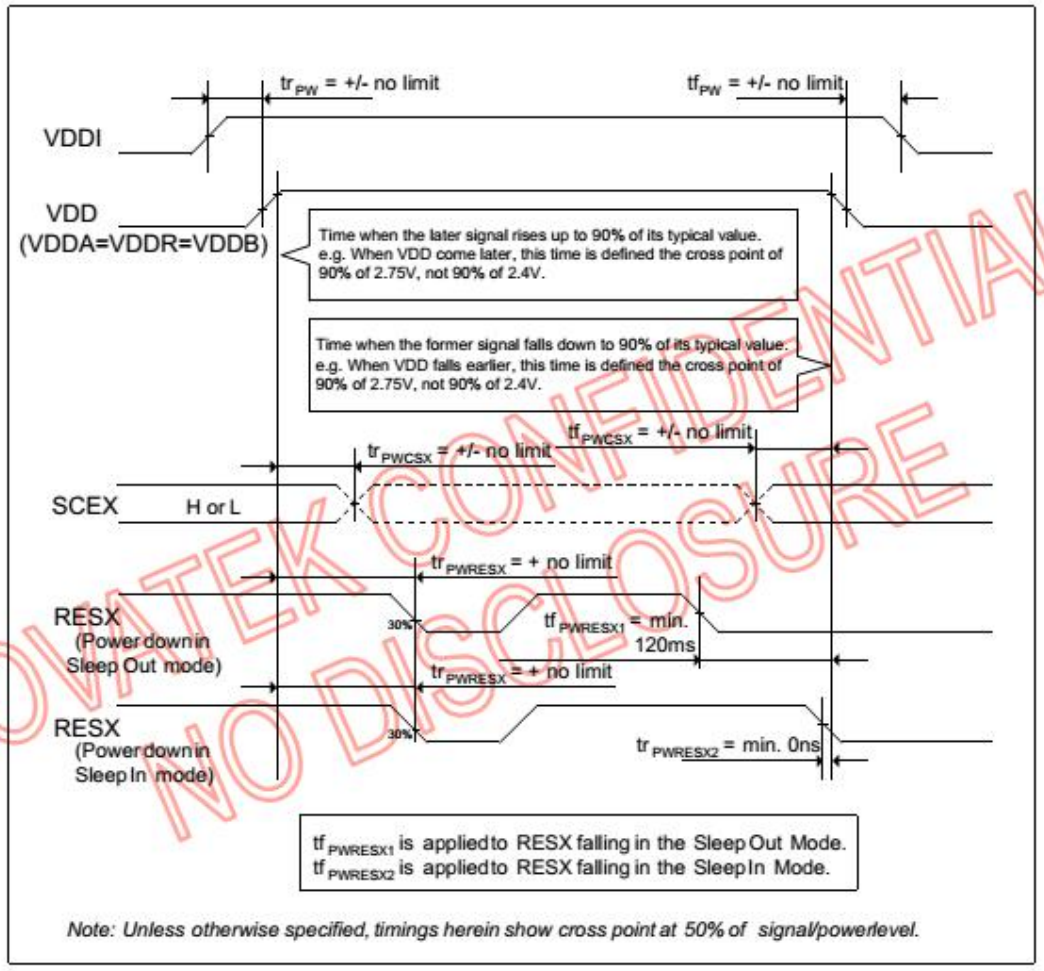
1. *There will be no damage to the display module if the power sequences are not met.*
2. *There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.*
3. *There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.*
4. *If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.12.1 and 5.12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.*
5. *There is not a limit for Rise/Fall time on VDDI and VDD (VDDA).*
6. *The display module can also initialize and calibrate DSI-CLK+/- and DSI-D0+/- lanes within 5ms after LP-11 (Clock and Data Channels), VDDI and VDD (VDDA) are applied and H/W Reset is not active (5ms is as same as the Reset Cancelling Time).*

The power supply ON/OFF setting for Display ON/OFF, Standby Set/Exit, and Sleep Set/Exit sequences is illustrated in figure below.



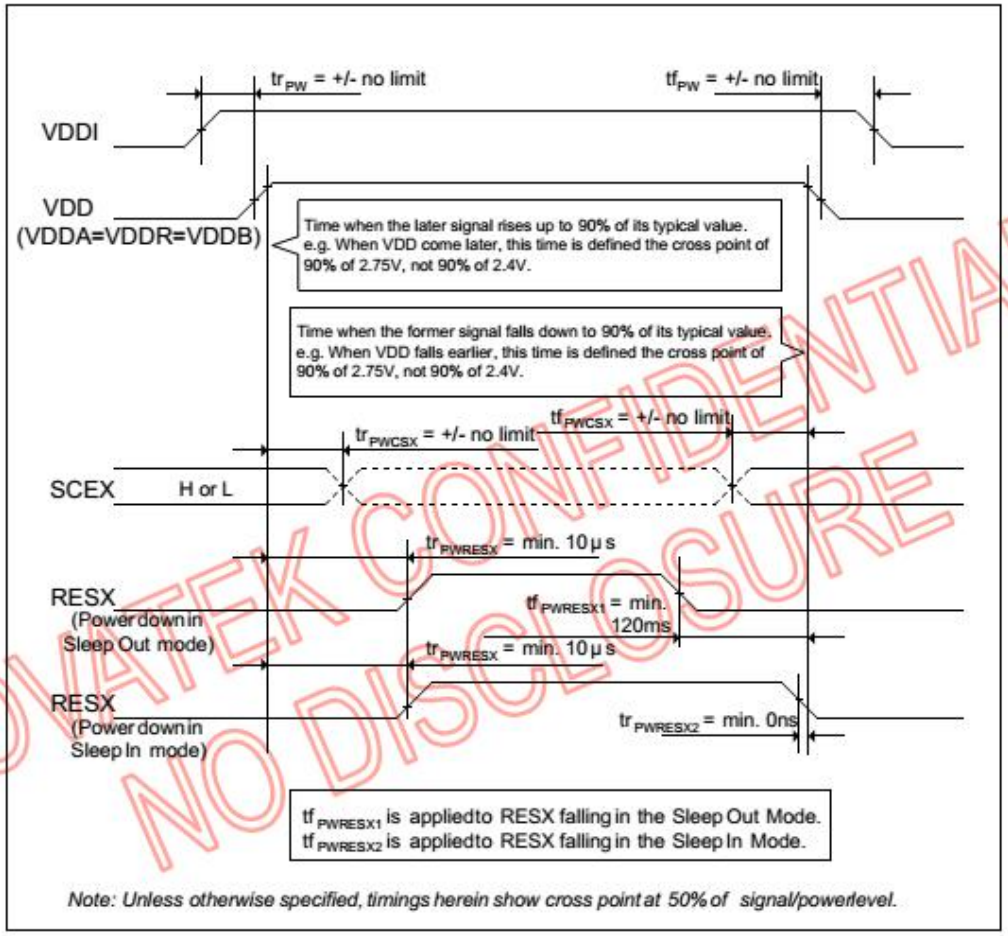
5.12.1 Case 1 – RESX line is held High or Unstable by Host at Power On

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD (VDDA) and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



5.12.2 Case 2 – RESX line is held Low by host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VDD (VDDA) and VDDI have been applied.



5.12.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

9.Optical Specification

Item 项目	Symbol 符号	Condition 条件	Min 最小值	Typ 典型值	Max 最大值	Unit 单位	Note 备注
Response time 响应时间	Tr+Tf	Θ=0° Ø=0° Ta=25°C	-	35	-	ms	1
Contrast ratio 对比度	Cr		550	800	-	-	2
Color gamut 饱和度	S(%)		-	-	-	%	-
Luminance uniformity 均匀度	δWHITE		80	-	-	%	3
Viewing angle range 视角范围	Θx+	CR≧10 Ta=25°C	-	85	-	deg	4
	Θx-		-	85	-	deg	
	Θy+		-	85	-	deg	
	Θy-		-	85	-	deg	
LCM Luminance LCM 亮度	Lv	Θ=0° Ø=0° Ta=25°C	300	-	-	Cd/m²	5
CIE (X,Y) Chromaticity 色度坐标	White(X)		0.25	0.28	0.31	-	6
	White(Y)		0.30	0.33	0.36	-	

Note1.Response time is the time required for the display to transition from White to black(Rise Time,Tr)and from black to white(Decay Time,Tf).For additional information see FIG1...

Note2.contrast Ratio(CR) is defined mathematically by the following formula ,For more information see FIG2.

Contrast Ratio(CR)=Average Surface Luminance with all white pixels/ Average Surface Luminance with all black pixels

Note3.The uniformity in surface luminance(WHITE) is determined by measuring luminance at eath test position, and then dividing the maximum luminance of all white pixels by minimum luminance of all white pixels,For more information seeFIG2.

WHITE=Minimum Surface Luminance with all white pixels(P1,P2,.....)/Maximum Surface Luminance with all white pixels(P1,P2,.....)

Note4.Viewing angle is the angel at which contrast ratio is greater than a specific value.For TET module,the specific value of contrast ratio is 10.For monochrome and color stn module,the specific value of contrast ratio is

2.The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface.For more information see FIG3

Note5. Surface luminance is the LCD surface luminance with all white pixels,For more information see FIG2. LV=Average Surface Luminance with all white pixels(P1,P2,.....)

Note6.CIE(X,Y)chromaticity is the Center point value.For more information see FIG2.

Note7.For Viewing angle and response time testing,the testing date is base on Autronic-Melchers's ConScope.Series instruments.For contrast ratio,Surface Luminance,Luminance uniformity and CIE,the testing date is base on CS-2000 photo detector.

Note8.For TN type TFT transmissive module,Gray scale reverse occurs in the direction of panel viewing angle

FIG1. The definition of Response time

响应时间定义

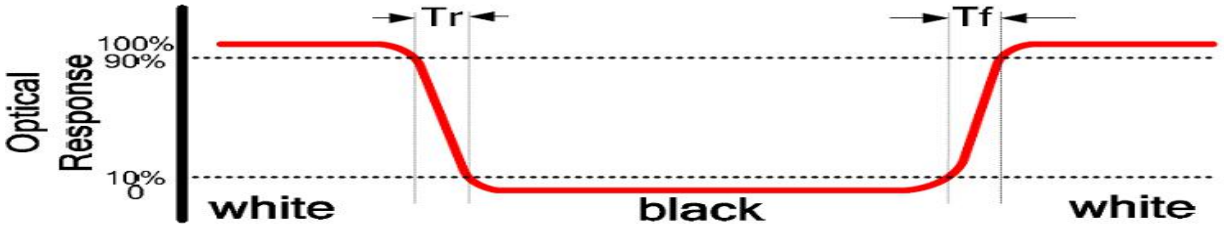
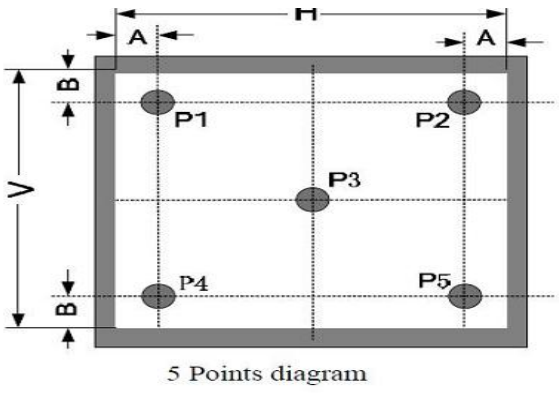
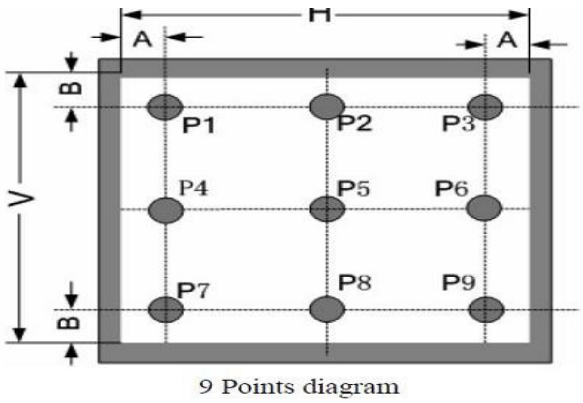


FIG2. Measuring method for Contrast ratio,surface luminance,Luminance uniformity,CIE(X,Y)chromaticity.

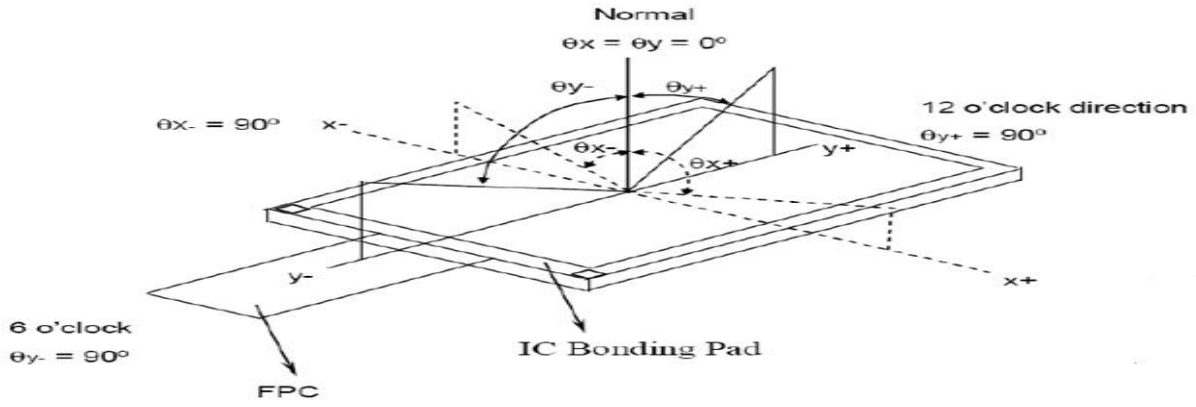


5 Points diagram



9 Points diagram

FIG3 The definition of viewing angle 视角定义



10.Reliability Test Items

Item	Test Condition	Criterion
High Temperature Storage	70 ℃, 48 hrs	Note1,Note2
Low Temperature Storage	-20 ℃, 48 hrs	
High Temp. & High Humidity Storage	40 ℃, 80% RH, 48hrs	

Thermal Shock (Static)	-20℃, 30 min /70℃, 30 min, 20 cycles	
High Temperature Operation	60 ℃, 48 hrs	
Low temperature Operation	-10 ℃, 48 hrs	

Note1:Evaluation should be tested after storage at room temperature for two hours.

Note2:

Pass: Normal display image no line defect.

Fail: No display image, or line defects.

Partial transformation of the module parts should be ignored.

11.Precautions

Please pay attentions to the followings as using the LCD module.

Handling

(a) Do not apply strong mechanical stress like drop, shock or any force to LCD module. It may cause improper operation, even damage.

(b) Because the polarizer is very fragile and easy to be damaged, do not hit, press or rub the display surface with hard materials.

(c) Do not put heavy or hard material on the display surface, and do not stack LCD modules.

(d) If the display surface is dirty, please wipe the surface softly with cotton swab or clean cloth.

(e) Avoid using Ketone type materials (e.g. Acetone), Toluene, Ethyl acid or Methyl chloride to clean the display surface. It might damage the touch panel surface permanently. The recommended solvents are water and Isopropyl alcohol.

(f) Wipe off water droplets or oil immediately.

(g) Protect the LCD module from ESD. It will damage the LSI and the electronic circuit.

(h) Do not touch the output pins directly with bare hands.

(i) Do not disassemble the LCD module.

(j) Do not lift the FPC of Touch Panel.

Storage

(a) Do not leave the LCD modules in high temperature, especially in high humidity for a long time.

(b) Do not expose the LCD modules to sunlight directly.

(c) The liquid crystal is deteriorated by ultraviolet. Do not leave it in strong ultraviolet ray for a long time.

(d) Avoid condensation of water. It may cause improper operation.

(e) Please stack only up to the number stated on carton box for storage and transportation. Excessive weight will cause deformation and damage of carton box.

Operation

(a) When mounting or dismounting the LCD modules, turn the power off.

(b) Protect the LCD modules from electric shock.

(c) The Driver IC control algorithms stated above should always obeyed to avoid damaging the LSI and electr onic circuit.

(d) Be careful to avoid mixing up the polarity of power supply for backlight.

(e) Absolute maximum rating specified above has to be always kept in any case. Exceeding it may cause non-recoverable damage of electronic components or, nevertheless, burning.

(f) When a static image is displayed for a long time, remnant image is likely to occur.

(g) Be sure to avoid bending the FPC to an acute shape, it might break FPC.

(h) Most of the touch screens have air vent to equalize the inside air pressure to the outside one. The air ven t must be open and liquid contact must be avoided as the liquid may be absorbed if the liquid is accumul ated near the air vent.

(i) For the fragility of ITO film, it should avoid to use too tapering pen as the input material.

Touch Panel Mounting Notes

(a) If a cushion is used between bezel/housing and film must be choose as free as enough to absorb the expa nsion and contraction to avoid the distortion of film.

(b) The cushion must be placed out of the Viewing Area.

(c) Bezel/Housing edge must be posited between Key Area and Viewing Area. The edge enters the Key Area may cause unexpected input if the gap is too narrow or foreign particles like dusts exist between Bezel/Ho using and ITO film.

(d) Mounting example:

The corner part has conductivity. Do not touch any metal part after mounting.

Others

a) If the liquid crystal leaks from the panel, it should be kept away from the eyes or mouth.

b) For the fragility of polarizer, it is recommended to attach a transparent protective plate over the display su rface.

c) It is recommended to peel off the protection film on the polarizer slowly so that the electrostatic charge c an be minimized.