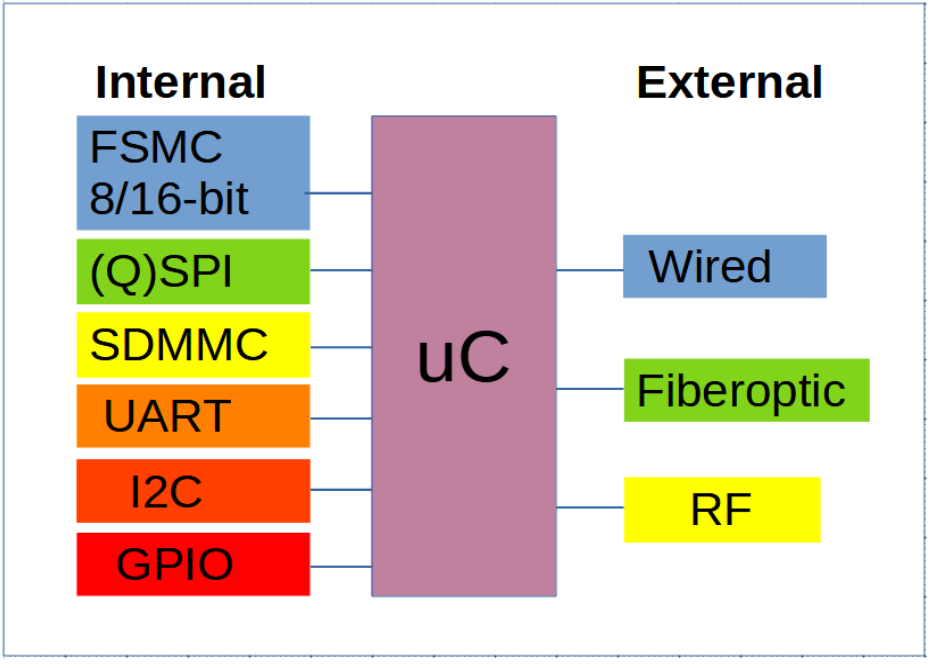
ES Communication Interfaces



Definition of Communication

Communication is transfer of data from a transmitter to a receiver.

One direction communication is called simplex transfer, both directions at different time – half duplex, both directions at the same time – full duplex.

Transceiver = transmitter + receiver.

Peer to peer communication

Multicast communication (addressing, like in I2C, or radio transmission).

Quad SPI Memory Interface

The Quad SPI is a specialized communication interface targeting single, dual or quad SPI flash memories. It can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the QUADSPI registers
- Status polling mode: the external flash status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external Flash is memory mapped and is seen by the system as if it were an internal memory

Quad SPI Interface Features

- Fully programmable opcode for indirect and memory mapped mode
- Fully programmable frame format (indirect/memory mapped mode)
- Each of the 5 following phases can be configured independently (enable, length, single/dual/quad communication): Instruction phase, Address phase, Alternate bytes phase, Dummy cycles phase, Data phase;
- Integrated FIFO for reception and transmission
- 8, 16, and 32-bit data accesses are allowed
- DMA channel for indirect mode operations
- Programmable masking for external flash flag management
- Interrupt generation on FIFO threshold, timeout, status match, operation complete, and access error

Serial Peripheral Interface

Three SPI interfaces allow communication up to 40 Mbits/s in master and up to 24 Mbits/s in slave modes, in half-duplex, full-duplex and simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

The SPI interfaces support NSS pulse mode, TI mode and Hardware CRC calculation.
All SPI interfaces can be served by the DMA controller.

SPI interface can be constructed of a USART, and has 4 signal pins:

MISO – Master Input Slave Output, MOSI – Master Output Slave Input, SCK – Serial Clock, NCS – Negative Chip Select; and GND – Ground.

SDMMC

Secure Digital input/output and MultiMediaCards interface provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards and SDIO cards.

The SDMMC features include the following:

• Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit

• Full compliance with SD Memory Card Specifications Version 2.0

• Data transfer up to 48 MHz for the 8 bit mode

USART/UART

As the abbreviation suggests, they are Universal Synchronous/Asynchronous Receiver Transmitter **devices**. Modern microcontrollers have several USART/UART units in them.

STM32L475 uC has 3 USARTs, 2 UARTs and 1 Low-Power UART.

All USARTs in STM32L475 have a clock domain independent from the CPU clock, allowing the USARTs to wake up the MCU from Stop mode using baudrates up to 204 Kbaud. The wake up events from Stop mode are programmable and can be: start bit detection, any received data frame, a specific programmed data frame. All USART interfaces can be served by the DMA controller.

UART Features

UARTs are asynchronous, they have to rely on a stable and accurate clock in both Transmitter and Receiver. These clock speeds are standardized to be: 300bps to 921600bps. Data is sent in packets of 7 or 8 bits, LSB first. There are 1 start bit and 1 to 2 stop bits.

Here is 1 start bit (after 1st falling edge), 1 0 0 0 1 1 0 0 – data, 1 stop bit:

Read the data from right to left: 0x31 => 1 in ASCII.

UART is not RS-232 – it works with CMOS/TTL levels of signals.

Inter-Integrated Circuit interface (I2C)

Microcontrollers may have several I2C. STM32L475 has three.

The I2C bus interface handles communications between the microcontroller and other devices having I2C bus. It controls all I2C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- I2C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s

I2C Features

– Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os

– 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses

– Programmable setup and hold times

– Optional clock stretching

• System Management Bus (SMBus) specification rev 2.0 compatibility:

– Hardware PEC (Packet Error Checking) generation and verification with ACK control

– Address resolution protocol (ARP) support

– SMBus alert

General-Purpose Inputs/Outputs (GPIOs)

GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

Pins as outputs can drive LEDs , buzzers, optocouples, drivers.

GPIO Typical Parameters

“Unless otherwise specified, typical data are based on TA = 25 °C, VDD = VDDA = 3 V. They are given only as design guidelines and are not tested.”

Output current sourced by any I/O and control pin is <= 8mA.

Output current sunk by any I/O and control pin is >= -8mA.

Exposure to maximum rating conditions for extended periods may affect device reliability.

The rule: to drive LED by an output of microcontroller always use a current limiting resistor. For high current control use drivers.

GPIO Maximum Voltage Values

Ratings	Min	Max
External main supply voltage (including V_{DD}, V_{DDA}, V_{DDUSB}, V_{BAT})	-0.3	4.0
Input voltage on FT_xxx pins	V_{SS}-0.3	min (V_{DD}, V_{DDA}, V_{DDUSB}) + 4.0[(3)(4)]
Input voltage on TT_xx pins	V_{SS}-0.3	4.0
Input voltage on BOOT0 pin	V_{SS}	9.0
Input voltage on any other pins	V_{SS}-0.3	4.0

Absolute Maximum Current Values

Symbol	Ratings	Max
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	150
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	150
$IV_{DD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100
$IV_{SS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin except FT_f	20
	Output current sunk by any FT_f pin	20
	Output current sourced by any I/O and control pin	20
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	100
	Total output current sourced by sum of all I/Os and control pins(2)	100

Communication with External Devices

Embedded System has to have some communications with external devices (off the PCBA): central microcontroller or computer. This type of communication assumes longer distances than on PCB and requires specialized interfaces (RF, Opto) or buses: CAN, USB, Ethernet, eSATA and so on. Except the RS-232 interface, the other all have differential pairs of wires – to reduce errors caused by common mode noise. Moreover, to reduce EMI (transmitted and received), the cables must be shielded.

RS-232 vs. UART

Modern microcontrollers have several USART/UART units in them but UART is not RS-232, it works with CMOS/TTL levels of signals.

BTW, RS stands for Recommended Standard (60 year ago). RS-232 (for longer range communications has these levels of signals:

RS-232 logic and voltage levels

Data circuits	Control circuits	Voltage
0 (space)	Asserted	+3 to +15 V
1 (mark)	Deasserted	−15 to −3 V

Controller Area Network (CAN)

The CAN peripheral supports:

- Supports CAN protocol version 2.0 A, B - Active
- Bit rates up to 1 Mbit/s
- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - 14 Scalable filter banks
  - Identifier or CAN-ID for priority of message, 2^11 levels
  - Configurable FIFO overrun

USB

Universal Serial Bus is one of the most popular buses for communication on short, a few meters, distances. It is about 20 years old and grew up from USB 1.1 (12Mbps) to USB 3.2 (20Gbps).

USB cables have two twisted wires for signal, and two – for power, typically 5 Volts. One end of the shielded cable has type A connector, another end – type B mini or micro connector:

USB Ports in IoT Board

The STM32L475xx USB interface is fully compliant with the USB specification version 2.0 and is USB-IF (USB Implementers Forum) certified (for Full-speed device operation).

Full-speed for USB 2.0 is 12Mbps, and Low-speed is 1.5Mbps).

One port, micro B female, marked as ST-Link USB, is a “device” port – to communicate to and to get power from – a computer. Another port, micro B female, marked as OTG (On-The-Go) USB, is a“host” port – to communicate with and provide power to – other USB devices: mouse, keyboard, USB Memory stick, and so on.

Bluetooth SPBTLE-RF module

Bluetooth V4.1 compliant (supports master and slave modes,Embedded ST BlueNRG-MS:

Ultra Low Power Cortex-M0,

Operating PS voltage: 1.7 to 3.6 V

Module's Tx power: + 4 dBm,

Host interface: SPI, IRQ, and RESET,

Embedded Bluetooth low-energy protocol stack,

On-board chip antenna

Sub-GHz RF module SPSGRF-915

Programmable radio features:– Based on Sub-1GHz SPIRIT1 transceiver and integrated Balun (BALF-SPI-01D3)

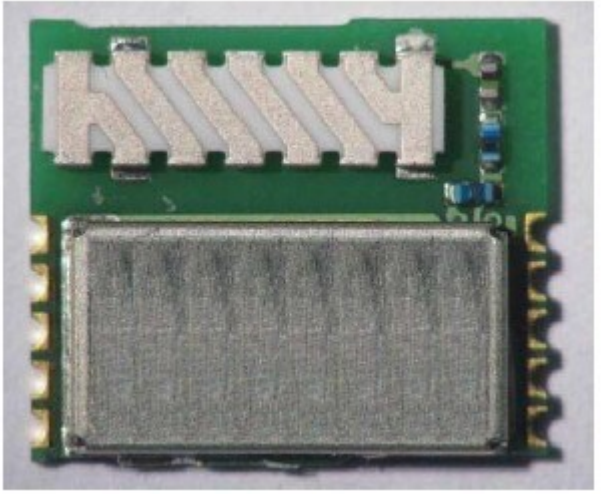
– Modulation schemes: 2-FSK, GFSK, MSK, GMSK, OOk and ASK

– Air data rate from 1 to 500 kbps

– On-board antenna

• Programmable RF output power up to +11.6 dBm

• Host interface: SPI



Wi-Fi module ISM43362-M3G-L44

- Works in ISM band 2.4GHz
- Based on the Broadcom BCM43362 MAC/Baseband/Radio device
- Has USB, SPI and UART interfaces
- Based on Arm® Cortex®-M3 32-bit RISC core from ST Microelectronics
- Complies with Wi-Fi 802.11b/g/n IEEE 802.11 standards
- IEEE 802.11i (Security)