Selecting a Microcontroller

Processing Speed
Memory (Types and Volumes)
Timers/Counters, ADCs, DACs
Number of GPIOs
Interfaces (Types and Quantities)
Interrupts (Numbers and Priorities)
Power (Modes and Limits)
Environmental Requirements (Commercial, Industrial, Automotive…)
Cost (of Microcontroller itself and Development efforts)

Processing Speed

Interrupt Latencies: uC must be fast enough for time constrains.

Length of the Polling Loop must be short for interrupt-driven system.

Memory Access Wait States

Oscillator Clock vs. System Clock: Old uChip PIC, vs. ARM w. PLLs.

Start-up Clock Speed p. 33-DS

Instruction Set: Multiply

Clocks for Peripherals: our concern is about SPI for FRAM @40MHz – in this case we need at least 80MHz System clock.

Memory (Types and Volumes)

RAM: Number of bytes in variables + sum of bytes in internal buffers + sum of bytes in FIFO + bytes in stacks = amount of RAM required.

Program Memory: Flash – no ROM anymore. Some modern microcontrollers (TI) have FRAM-based program memory.

Size: program + all look-up tables (mo-co, sensors), constants, etc.

Almost all modern microcontrollers have EEPROM to keep calibration data or some other small amount of information. Their size range is from several bytes to several kilobytes.

See the attached article Code Size Vs. Memory Footprint.

Timers/Counters, ADCs, DACs

Timers and counters are the essential blocks of the microcontroller, providing easy generation of PWM signals required for motor control, actuators and power supplies. They can be used for counting pulses from external devices, for providing measured delays, and as an RTC – Real Time Clock (including a calendar).

Internal **ADC**s make it convenient to acquire analog signals from sensors, digitize them and store in the memory. Resolution of internal ADCs can be from 10 to 24-bit.

Internal **DAC**s are used to generate analog signals, levels and waveforms of any desired shape.

GPIOs, Interfaces

I will show later that the same type of uC may have different packages and different number of pins. GPIOs (General Purpose Input/Output) are combined into ports: PORTA, PORTB… Ports can be from 4 to 32 bit long. Every pin of port can be configured as input or output either once, in the beginning of the code, or dynamically – during the code execution.

The following interfaces can be found in a uC: UART, I2C, SPI, CAN, LIN (Local Interconnect Network), IrDA (InfraRed Data Association), USB. Some uC have Serial Audio Interfaces (SAI): The SAI bus interface provides communications between the microcontroller and the external audio device via serial audio protocol (example: I2S).

Interrupts

Modern uCs embed a Nested Vectored Interrupt Controller (NVIC).

The NVIC benefits are the following:

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Processing of late arriving higher priority interrupts
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency at 16 priority levels from up to 80 maskable interrupt channels.

Power Requirements

Battery-powered devices are required to consume lowest power, or, to be more accurate, energy. Battery stores energy – not V or I.

E = I(t)*V(t)*t. Here, the V(t) does not change much compare to the current I(t) which changes a lot. For example,

Shutdown mode (5 wakeup pinsare awaik) 30 nA

Run mode at 80MHz (– 100 μA/MHz) 8mA

So, the Power consumed by microcontroller is not a constant value – it depends on the mode of microcontroller's work: speed of the uC, number of peripherals activated, loads on pins, temperature, etc.

Environmental Requirements

The temperature range is defined by the product requirements:

Commercial devices: 0 – 70C

Industrial: -40 – 85C

Automotive: -40 – 105C

Military: -55 – 125C

Chip manufacturers may have different different ranges definitions.

Other requirements: immunity to radiation, magnetic field, ESD.

Cost

The cost of the uC is not a critical factor for most of the Embedded Systems: cost of a high speed ADC, or memory, or some sensors may be higher. Cost depends of the complexity of the uC and on quantity of purchased components.

The cost of the product (ES) will include a part of the cost of development (HW, FW, SW, testing) which depends on the: experience of the engineers involved in development,

cost of the tools: EDA, CAD, RTOS, etc.

When the production quantity is small, the development cost becomes very important, in mass production this cost can be amortized in the product cost.

Modern Microcontrollers (DSCs)

Most of the modern programmable digital devices are microcontrollers or DSCs (Digital Signal Controllers). What differentiates them from microprocessors and digital signal processors is the presence on the same chip the three types of memories: Flash, EEPROM, SRAM, and a rich spectrum of peripheral units: several timers/counters (including RTC and WDT), ADC, DAC, analog comparators, USARTs (SPI, UART, I2C, CAN, etc), Brown-Out Detector, and others.

There is a term PSoC – Programmable System on Chip, introduced by Cypress in the year 2005.

PSoC® 5LP Highlights

- 32-bit Arm Cortex-M3 CPU, 32 interrupt inputs, up to 80 MHz,
- 24-channel direct memory access (DMA) controller with data transfer between both peripherals and memory,
- 24-bit fixed-point digital filter processor (DFB),
- 20+ Universal Building Blocks and Precise Analog Peripherals,
- Up to 62 CapSense® sensors with SmartSense™ Auto-tuning,
- Multiplexed AFE with programmable Opamps, 8- to 20-bit delta-sigma ADC, two 12-bit SAR ADC and four 8-bit DAC
- 736 segments LCD drive for custom displays,
- Packages: 68-pin QFN, 99-pin WLCSP, 100-pin TQFP.

Operating Characteristics of PSoC® 5LP

Voltage range: 1.71 to 5.5 V, up to 6 power domains
Temperature range (ambient): –40 to 85 °C [1]
Extended temperature parts: –40 to 105 °C
DC to 80-MHz operation
Power modes
- Active mode 3.1 mA at 6 MHz, and 15.4 mA at 48 MHz
- 2-µA sleep mode
- 300-nA hibernate mode with RAM retention

Boost regulator from 0.5V input up to 5V output

Memories and Clocks of PSoC® 5LP

Up to 256 KB program flash, with cache and security features
Up to 32 KB additional flash for error correcting code (ECC)
Up to 64 KB RAM
2 KB EEPROM;

3- to 74-MHz internal oscillator, 1% accuracy (class) at 3 MHz
4- to 25-MHz external crystal oscillator
Internal PLL clock generation up to 80 MHz
Low-power internal oscillator at 1, 33, and 100 kHz
32.768-kHz external watch crystal oscillator
12 clock dividers routable to any peripheral or I/O

TI's 16-bit MSP430FR5964

16-bit RISC Architecture up to 16MHz Clock
Non-volatile (FRAM) Memory (kB) - 256,
RAM - 8kB,
ADC - 12-bit SAR, 20 channels,
GPIO pins - 68
I2C - 4 buses
SPI - 8 buses
UART - 4 units
Comparator - 6 channels
Packages: 48-VQFN, 64 and 80-LQFP, 87-NFBGA

Features of MSP430FR5964

- Wide Supply Voltage Range From 3.6 V Down to 1.8 V
– Ultra-Low-Power Writes at 125 ns Per Word (64KB in 4 ms)
– Optimized Ultra-Low-Power Modes: – Active Mode: 118 µA/MHz
  – Standby With VLO (LPM3): 500 nA
  – Standby With Real-Time Clock (RTC) (LPM3.5): 350 nA (1)
– Flexible Allocation of Data and Application Code in Memory
– 10^15 Write Cycles Endurance
– Radiation Resistant and Nonmagnetic
– All Pins Support Capacitive-Touch Capability
– 128- or 256-Bit AES Security Encryption Coprocessor

Digi & Analog Peripherals in MSP430FR5964

32-Bit Hardware Multiplier (MPY)
6-Channel Internal DMA Controller
RTC With Calendar and Alarm Functions
Six 16-Bit Timers With up to Seven Capture/Compare Registers Each
32- and 16-Bit Cyclic Redundancy Check (CRC)

16-Channel Analog Comparator
12-Bit Analog-to-Digital Converter (ADC) with 20 External Input Channels, Window Comparator, Internal Reference, and Sample-and-Hold Amplifier

Atmel's 8-bit ATmega4809 Key Attributes

Internal 20MHz oscillator
Up to 16-channel, high speed 10-bit ADC
Configurable, internally generated Reference Voltage
Cyclic Redundancy Check (CRC) with SCAN
16-bit Real Time Clock
Configurable Custom Logic peripheral
6-channel Peripheral Event System
Analog Comparator with scalable reference input
Number of Comparators - 1

ATmega4809 Memories & Buses

Program Memory Flash	- 48kB
CPU Speed (MHz/DMIPS)	- 20
SRAM	- 6,144B
Data EEPROM/HEF	- 256B

Digital Communication Peripherals: 4-UART, 1-SPI, 1-I2C

Capture/Compare/PWM Peripherals: 16 Input Capture, 1PWM

Timers: five 16-bit

ATmega4809 Additional Features

Watchdog Timer (WDT)

Power-On Reset (POR)

Brown-Out Detection (BOD)

Temperature Range ©	-	-40 to 125C
Operating Voltage Range	-	1.8 to 5.5V
Pin Count	-	48

Three sleep modes: Idle

Standby

Power Down

Microchip DSC dsPIC33CH128MP508

Dual Core, 16-Bit Digital Signal Controllers with High-Resolution PWM and CAN Flexible Data (CAN FD)

28/36/48/64/80-Pin TQFP - thin quad flat package

Master/Slave Core Operation @ 180/200MHz

Independent Peripherals for Master Core and Slave Core

Dual Partition for Slave PRAM LiveUpdate

Configurable Shared Resources for Master Core and Slave Core

dsPIC33CH128MP508 Memories & Clocks

Master Core up to 128 kB of Program Flash with ECC & 16kB RAM

Slave Core with 24 Kbytes of Program RAM (PRAM) with ECC and 4K Data Memory RAM

Medium Speed Oscillator (XT Mode): 3.5 – 10MHz crystal

High-Speed Oscillator (HS Mode): 10 – 32MHz crystal

External Clock Source Operation (EC Mode): external clock source to OSCI pin – from 0 to 64MHz

LPRC Oscillator Internal – Low Power RC
FRC Oscillator Internal – Fast RC

Primary Oscillator - for a crystal on OSCI and OSCO pins

Communication Interfaces of dsPIC33

- Three UART Modules: 2 modules for Master core, 1- for Slave core,

  Support for DMX, LIN/J2602 protocols and IrDA®
- Three 4-Wire SPI/I2S Modules: 2 - in Master core, 1 – in Slave core
- CAN Flexible Data-Rate (FD) Module for the Master Core
- Three I2C Modules: 2 modules for Master, 1 – Slave core,

  Support for SMBus for low-speed system management communications

Analog Features of dsPIC33

Four ADC Modules: 1 module for Master core, 3 - for Slave core,

12-bit, 3.5 Msps ADC, up to 18 conversion channels

- Four DAC/Analog Comparator Modules: 1- Master, 3 – Slave,

  12-bit DACs with HW slope compensation, 15ns comparators

- Three PGA Modules: 3 modules for Slave core, can be read by Master ADC

- Shared DAC/Analog Outputs: DAC/analog comparator outputs,

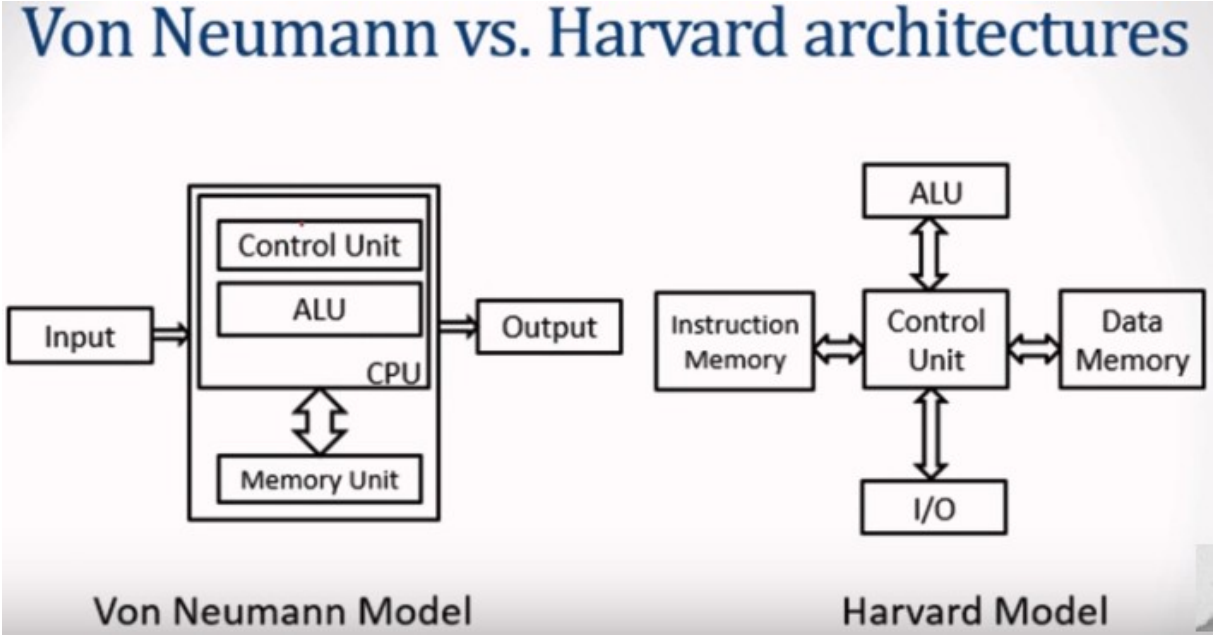
  PGA outputs

SISC vs. RISC Architectures

CISC (complex instruction set computer) refers to computers designed with a full set of computer instructions that were intended to provide needed capabilities in the most efficient way. Later, it was discovered that, by reducing the full set to only the most frequently used instructions, the computer would get more work done in a shorter amount of time for most applications.

RISC (reduced instruction set computer) is a microprocessor that is designed to perform a smaller number of types of computer instructions so that it can operate at a higher speed.

All of compared above microcontrollers are of RISC type.



https://www.youtube.com/watch?v=aigww_JJL_8

ST's 32-bit STM32L475

Ultra-low-power Arm® Cortex®-M4 32-bit MCU+FPU, 100DMIPS,
up to 1MB Flash, 128 KB SRAM, USB OTG FS, analog, audio.
1.71 V to 3.6 V power supply
-40 °C to 85/105/125 °C temperature range (Ind/Auto/Mil)
300 nA in VBAT mode: powering RTC and 32x32-bit backup registers
30 nA Shutdown mode (5 wakeup pins)
100 μA/MHz run mode
4 μs wakeup from Stop mode
Brown out reset (BOR)
Interconnect matrix

STM32L475 Clock Sources

4 to 48 MHz crystal oscillator

32 kHz crystal oscillator for RTC Low Speed External (LSE) (Oscillator)

Internal 16 MHz factory-trimmed RC (±1%)

Internal low-power 32 kHz RC (±5%)

Internal multispeed 100 kHz to 48 MHz oscillator, auto-trimmed by LSE (less than ±0.25 % error)

It has PLLs for system clock, USB, audio, ADC

STM32L475 Memories and Analog

Up to 1 MB Flash, 2 banks read-whilewrite, code readout protection

Up to 128 KB of SRAM including 32 KB with hardware parity check

External memory interface for static memories supporting SRAM, PSRAM and NOR memories

Quad SPI memory interface

3x 12-bit ADC 5 Msps, to 16-bit w. HW oversampling, 200µA/Msps

2x 12-bit DAC output channels, low-power sample and hold

2x operational amplifiers with built-in PGA

2x ultra-low-power comparators

Architecture of STM32L475