Memories in Embedded Systems

Internal to uC memories: **Flash, EEPROM, SRAM** memories,

External to uC memories which can be used in embedded systems, depending on the needs, are the following:

DRAM and **DDRAM**– volatile memory,

MRAM – nonvolatile memory,

nvSRAM. – nonvolatile memory,

FRAM - nonvolatile memory (may be inside a uC, like in TI's MSP430FR5964 which we considered last week).

DRAM

In DRAM, Dynamic Random Access Memory, information is stored in small capacitors which leak their charges and need re-writes (refreshments).

Every bit is represented by one transistor and one capacitor; this is 4 to 6 time less than in static RAM (SRAM).

The first DRAM was introduced in 1969 by Advanced Memory system, Inc of Sunnyvale, CA. The first DRAM with multiplexed row and column address lines was the Mostek MK4096 4 kbit DRAM designed by Robert Proebsting and introduced in 1973.

DRAMs, sold now by Mouser, have capacities from 4Mb to 128Gb and speed up to 2133MHz. Their prices are from $1.16 to $301/chip.

DDRAM Memories

Double Data-rate Random Access Memory – this is the same type of memory as described on the previous slide. The difference is that the DDR memory reads/writes data on both the rising and falling edges of the clock, achieving a faster data rate. Often used in notebook computers because it also consumes less power. This type of memory is characterized by millions of transfers per second: MT/s, instead of clock speed (MHz), how it is done for DRAM memory type.

DDR Version	DDR1	DDR2	DDR3	DDR 4	DDR5
Released date	2000	2003	2007	2012	Under Progress
Operating voltage	2.5V	1.8V	1.5V	1.2V	1.1V
Prefetch buffer size	2	4	8	8	16
Chip densities	128Mb-1Gb	128Mb-4Gb	512Mb-8Gb	2Gb-16Gb	8Gb-64Gb
Data rate (MT/s)	200-400	400-800	800-2133	1600-3200	3200-6400
Bank groups	0	0	0	4	8
Termination/ODT	Ω on board	ODT added	Nominal, Dynamic Modes	Park Modes	Nominal Wr/Rd

Comparison of DDR Generations

Features of MT40A256M16/MT40A512M8

Configuration – 256 Meg x 16 – in 96-ball package

Configuration – 512 Meg x 8 – in 78-ball package

Data Rate - 2400MT/s for suffix -083E, 3200MT/s – for -062E

Speed:	DDR4-2400	DDR4-3200	
IDD4R: Burst read current:			
x8	160	194	mA
x16	269	330	mA
IDD4W: Burst write current:			
x8	137	165	mA
x16	215	268	mA

nvSRAM

nvSRAM is a non-volatile Static Random-Access Memory. It is a combination of SRAM and SONOS (silicon–oxide–nitride–oxide–silicon) based memory (same as EEPROM). nvSRAM was developed by Cypress Semiconductor.

Under normal operation, nvSRAM behaves like a conventional asynchronous SRAM using standard signals and timing. nvSRAM performs parallel random access reads and writes as fast as 20 ns.

On a power failure, nvSRAM automatically saves a copy of the SRAM data into nonvolatile memory, where the data is protected for over 20 years. The transfer between SRAM and nonvolatile memory is completely parallel, allowing the operation to complete in <=8 ms.

Cypress's nvSRAM Key Features

- 64Kb to 16Mb devices
- Asynchronous parallel and ONFI 1.0 interface options
- Serial interface options
- As low as 20 ns access times
- Infinite endurance
- No batteries required to store data on power loss;
- Optional Real Time Clock (RTC)
- RoHS compliant

FRAM

FRAM is a Ferroelectric RAM (FeRAM, F-RAM or FRAM) is a random-access memory similar in construction to DRAM but using a ferroelectric layer instead of a dielectric layer to achieve non-volatility. Ramtron was the first company selling FRAMs.

As I mention in lesson 4, Texas Instruments has incorporated this type of FRAM memory into its MSP430 microcontrollers: MSP430FRxxx.

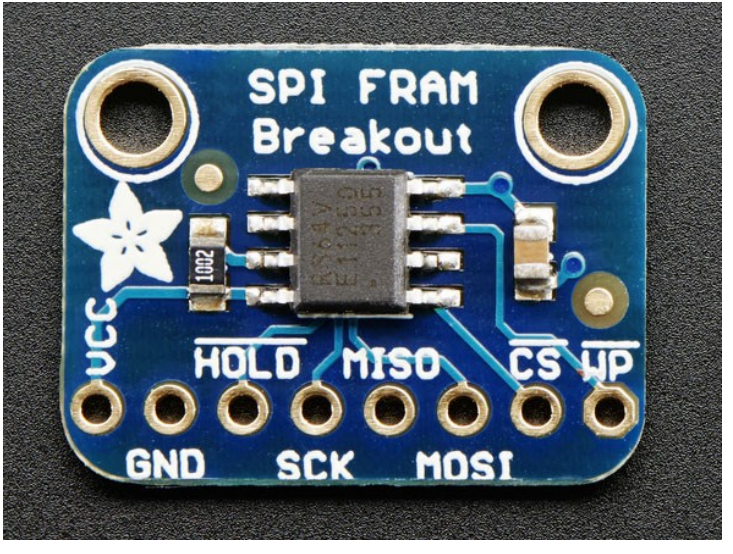
Several companies: Samsung, Matsushita, Oki, Toshiba, Infineon, Hynix and Fujitsu manufactured FRAM chips.

In 2012 Ramtron was aquired by Cypress, then, in 2019, Cypress was aquired by Infineon. Now, the FRAM can be bought from Infineon (Cypress), Rohm Semiconductor and Fujitsu.

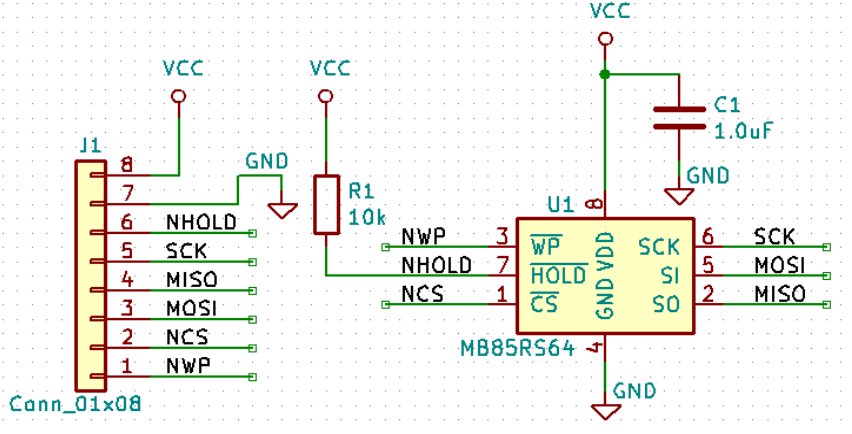
Adafruit FRAM Module

Price: $5.95

United States Postal Service FIRST-CLASS PACKAGE SERVICE - RETAIL™ : $5.65 No Delivery Estimate



Adafruit FRAM Module Schematic



Adafruit FRAM Module Wiring

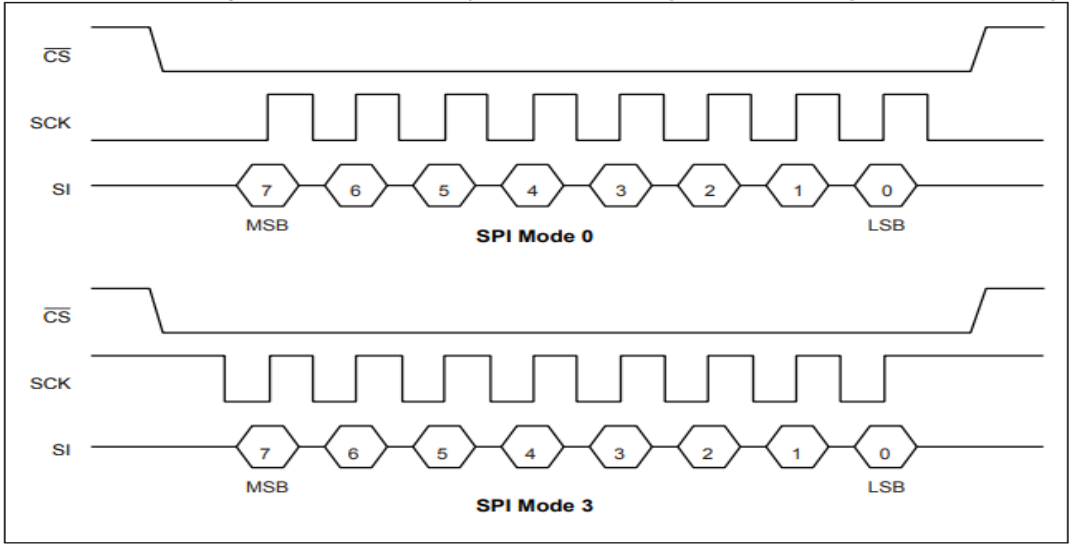
Connect Vcc to the 3.3V pin of the CN2 on the IoT board
Connect GND to common power/data ground pin
Connect the SCK pin to the SPI Clock pin on your STM IoT board
Connect the MISO pin to the SPI MISO pin on your STM IoT board
Connect the MOSI pin to the SPI MOSI pin on your STM IoT board
Connect the CS pin to the SPI CS pin on your STM IoT board.
Connect the NWP pin to the 3.3V pin of the STM IoT board
Leave the he NHOLD unconnected because it has a pullup 10k

MB85RS64V FRAM Key Features

- 64-kbit density, organized as 8k x 8
- Serial Peripheral Interface SPI, modes 0 and 3
- Operating power supply voltage: 3.0 V to 5.5 V
- Low power: 1.5mA at 20MHz and 10 μA standby current
- 1-trillion read/write cycle endurance
- No batteries required to store data on power loss
- Operation ambient temperature range : − 40 °C to + 85 °C
- Data retention: 10 years (+ 85 °C), 95 years (+ 55 °C)
- Package: 8-pin plastic SOP (FPT-8P-M02) RoHS compliant

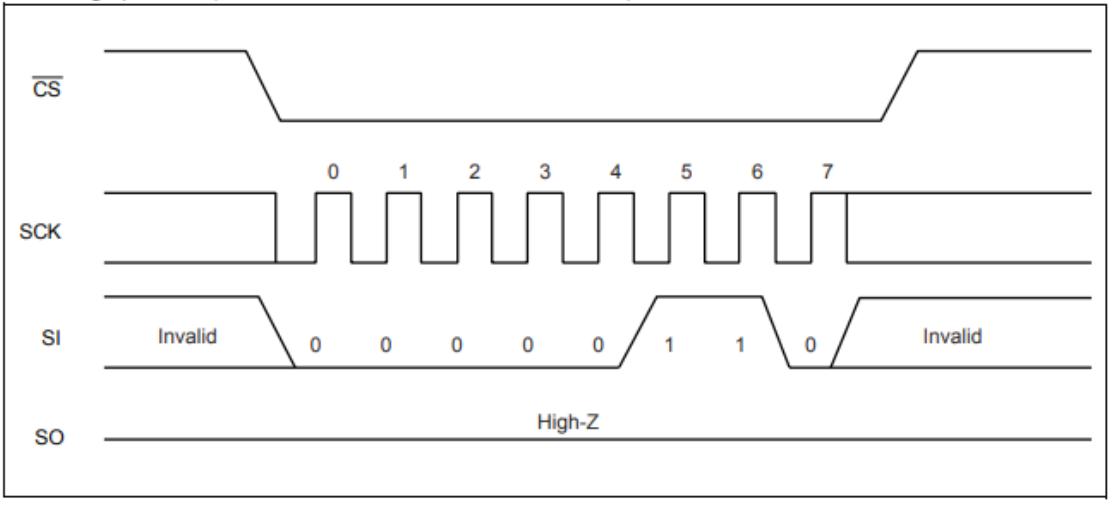
SPI Mode 0 and Mode 3

MB85RS64V corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0) , and SPI mode 3 (CPOL = 1, CPHA = 1) .



Write Enable Command

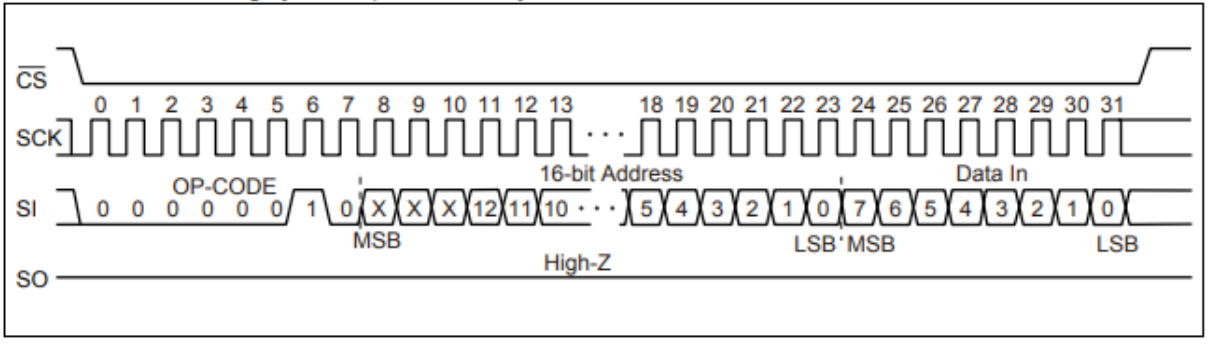
Op-Code: 0x06



Write Command

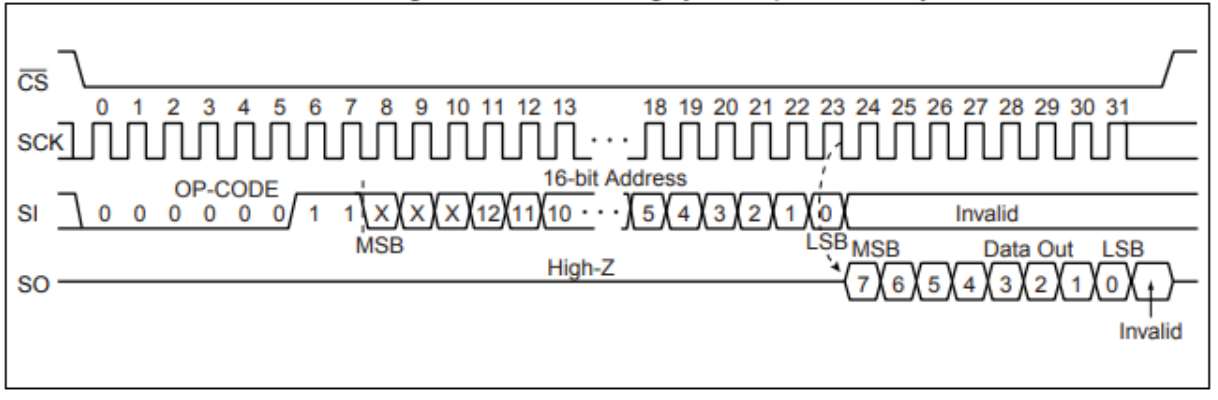
The upper 3 bits of address do not matter.

Op-Code: 0x02.



Read Command

Op-Code: 0x03



MRAM

MRAM (Magnetoresistive Random Access Memory) uses electron spin to store data. Memory cells are created by placing millions of magnetic "sandwiches" on a silicon substrate, with tiny parallel wires running in one direction on top of them and other wires running below in perpendicular direction.

Recently Spin Memory (previously Spin Transfer Technologies) announced that is has signed a licensing agreement with ARM. The license includes Spin Memory's Endurance Engine technology and IP – to be potentially used in ARM microcontrollers, as it was done by Ramtron with TI (recall lesson 4).

Features of MR10Q010

- Memory size 1Mb organized as 128k x 8
- High bandwidth – Read and Write at 52MB/sec
- Quad SPI using dual purpose pins to maintain a low pin count
- Operates in standard single SPI mode and fast quad SPI mode
- Intended for next generation RAID controllers, server system logs, and embedded system data and program memory
- Data is non-volatile with retention greater than 20 years
- Automatic data protection on power loss
- Unlimited write endurance
- Low-current sleep mode
- Dual 3.3VDD / 1.8VDDQ power supply, 100mA @ Write mode.

Flexible static memory controller (FSMC)

Flexible static memory controller (FSMC) is also named Flexible memory controller (FMC).

The main features of the FMC controller are the following:

- Interface with static-memory mapped devices in multiplexed mode including:
  - Static random access memory (SRAM)
  - NOR Flash memory
  - PSRAM
- 8-,16- bit data bus width
- Write FIFO
- The Max FMC_CLK frequency for synchro accesses is HCLK/2.

DMA

• Direct Memory Access is a feature of microcontrollers, providing high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

• The STM32L475 microcontroller has two DMA controllers having in total 14 channels, each channel providing memory access to/from one or more peripherals and each having an a’rbiter for handling priority for DMA access.

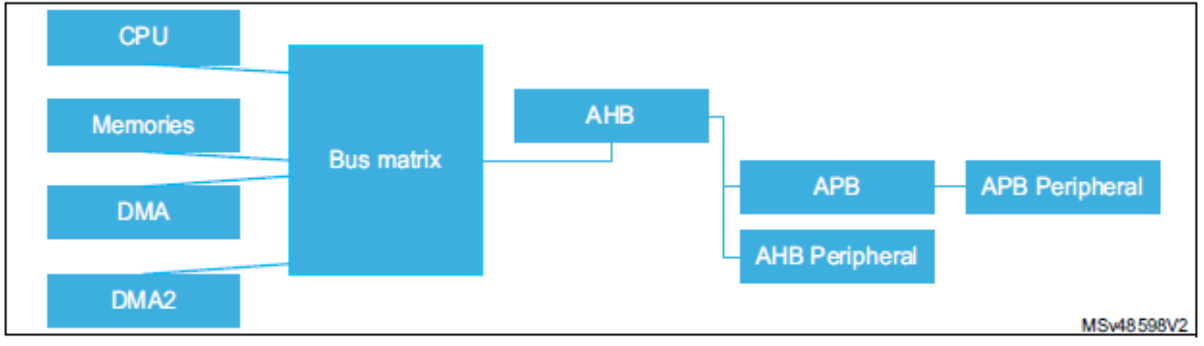
• Memory-to-memory (Flash – SRAM), peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers are available.

DMA Priorities and Data Format

- Priorities between requests from channels of one DMA are software programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has highest priority etc).
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Programmable number of data to be transferred: up to 65536.
- DMA controllers support circular buffer management.
- 3 event flags (DMA Half Transfer, DMA Transfer complete and DMA Transfer Error) logically ORed together in a single interrupt request for each channel.

Microcontroller with 2 DMA

Figure 1. DMA block diagram for products with 2 DMAs (DMA and DMA2)



1. DMA2 is only present on more complex products (see *Table 1* for details).

AHB - Advanced High-performance Bus

APB - Advanced Peripheral Bus

Bus Matrix

Bus architecture

The masters use the following buses to talk to slaves:

S0 or I-bus

This bus connects the instruction bus of the Cortex®-M4 core to the BusMatrix. This bus is used by the core to fetch instructions. The targets of this bus are the internal Flash memory, SRAM1, SRAM2 and external memories through QUADSPI.

S1 or D-bus

This bus connects the data bus of the Cortex®-M4 core to the BusMatrix. This bus is used by the core for literal load and debug access. The targets of this bus are the internal Flash memory, SRAM1, SRAM2 and external memories through QUADSPI.

Bus Matrix, 2

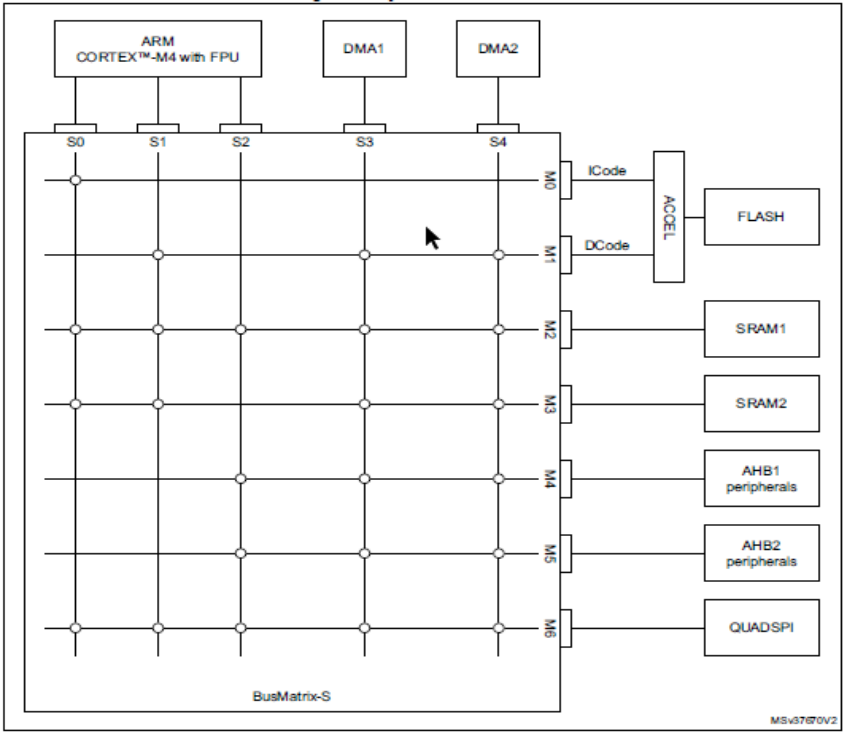
S2 or S-bus

This bus connects the system bus of the Cortex®-M4 core to the BusMatrix. This bus is used by the core to access data located in a peripheral or SRAM area. The targets of this bus are the SRAM1, the AHB1 peripherals including the APB1 and APB2 peripherals, the AHB2 peripherals and the external memories through the QUADSPI.

S3, S4: DMA-bus

This bus connects the AHB master interface of the DMA to the BusMatrix. The targets of this bus are the SRAM1 and SRAM2, the AHB1 peripherals including the APB1 and APB2 peripherals, the AHB2 peripherals and the external memories through the QUADSPI.

System Architecture



Nested Vectored Interrupt Controller

NVIC provides 16 priority levels and handles up to 80 maskable interrupt channels plus 16 interrupt lines of STM32L475.

The NVIC benefits are the following:

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 39 edge detector lines used to generate interrupt/event requests and wake-up the system from Stop mode.

Each external line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests.

The internal lines are connected to peripherals with wakeup from Stop mode capability. The EXTI can detect an external line pulse having width shorter than the internal clock period!

Up to 82 GPIOs can be connected to the 16 external interrupt lines.