- 15 K.Y. Toh, P.K. Ko, and R.G. Meyer, "An Engineering Model for Short-Channel MOS Devices," *IEEE J. Solid-State Circuits*, SC-23, 950 (1988).
- 16 H. Kawaguchi et al., "A Robust 0.15um CMOS Technology with CoSi2 Salicide and Shallow Trench Isolation," *VLSI Tech.*, 1997, p.125-126.
- 17 L.D. Yau, "A Simple Theory to Predict the Threshold Voltage in Short-Channel IG-FETs," *Solid-State Electron.*, 17, 1059 (1974).
- 18 Z.H. Liu et al., "Threshold Voltage Model for Deep-Submicrometer MOSFETs," *IEEE Trans. Electron Dev.*, ED-40, 86 (1993).
- 19 E.C. Jones and E. Ishida, "Shallow Junction Doping Technologies for ULSI," *Materials Science and Engineering*, R24, 1 (1998).
- 20 R.R. Troutman, "VLSI Limitations from Drain-Induced Barrier Lowering," *IEEE Trans. Electron Dev.*, ED-26, 461 (1979).
- 21 S.G. Chamberlain and S. Ramanan, "Drain-Induced Barrier-Lowering Analysis in VLSI MOSFET Devices Using Two-Dimensional Numerical Simulations," *IEEE Trans. Electron Dev.*, ED-33, 1745 (1986).
- 22 C. Hu, "Future CMOS Scaling and Reliability," Proc. IEEE, 81, 682 (1993).
- 23 D.A. Buchanan, "Scaling the Gate Dielectric: Materials, Integration, and Reliability," *IBM Journal of Research and Development*, 43, 245 (1999).
- 24 C.F. Codella and S. Ogura, "Halo Doping Effects in Submicron DI-LDD Device Design, "*IEDM*, 1985, p.230-233.
- 25 A. Hori et al., "A Self-Aligned Pocket Implantation (SPI) Technology for 0.2um-Dual Gate CMOS, "*IEDM*, 1991, p.641-644.
- 26 Y. Taur and T.H. Ning, Fundamentals of Modern VLSI Devices, Cambrige, New York, 1998.
- 27 「半導體製程整合專業訓練講義」,劉傳璽,民國94年一月。
- 28 「應材半導體元件與良率分析講義」,劉傳璽,民國94年七月。