參考文獻

- J.D. Plummer, M.D. Deal, and P.B. Gruffin, Silicon VLSI Techology-Fundamentals. 1 Practice and Modeling, Prentice Hall, New Jersey, 2000.
- S. Wolf and R.N. Tauber, Silicon Processing for the VLSI Era Volume I-Process 2 Technology, Lattice Press, CA, 1986.
- S. Wolf, Silicon Processing for the VLSI Era Volume II-Process Integration, Lattice 3 Press, CA, 1990.
- S. Wolf, Silicon Processing for the VLSI Era Volume III-The Submicron MOSFET, 4 Lattice Press, CA, 1995.
- M. Quirk and J. Serda, Semiconductor Manufacturing Technology, Prentice Hall, 5 New Jersey, 2001.
- H. Kawaguchi et al., "A Robust 0.15um CMOS Technology with CoSi₂ Salicide and 6 Shallow Trench Isolation," VLSI Tech., 1997, p.125-126.
- E.C. Jones and E. Ishida, "Shallow Junction Doping Technologies for ULSI," Ma-7 terials Science and Engineering, R24, 1 (1998).
- H. Xiao, Introduction to Semiconductor Manufacturing Technology, Prentice Hall, 8 New Jersey, 2001.
- C.Y. Chang and S.M. Sze, ULSI Technologies, McGraw-Hill, New York, 1996. 9
- 10 R.R. Troutman, "VLSI Limitations from Drain-Induced Barrier Lowering," IEEE Trans. Electron Dev., ED-26, 461 (1979).
- 11 C. Hu, "Future CMOS Scaling and Reliability," Proc. IEEE, 81, 682 (1993).
- 12 S.M. Sze, Semiconductor Devices-Physics and Technology, 2nd edition, Wiley, New York, 2001.
- 13 D.A. Buchanan, "Scaling the Gate Dielectric: Materials, Integration, and Reliability," IBM Journal of Research and Development, 43, 245 (1999).
- 14 C.F. Codella and S. Ogura, "Halo Doping Effects in Submicron DI-LDD Device Design, "IEDM, 1985, p.230-233.
- 15 A. Hori et al., "A Self-Aligned Pocket Implantation (SPI) Technology for 0.2um-Dual Gate CMOS, "IEDM, 1991, p.641-644.