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Hugo Tárrega

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Experience

Software Engineer — **Facephi (Alicante, Spain)** — **April 2024 – Present**

- Improved inference throughput by 40% average and reduced latency by 25% average across 15+ biometric pipelines through algorithmic optimizations and parallelization techniques.

Software Engineer — **Topcon Mirage (València, Spain)** — **Nov 2022 – Apr 2024**

- Led migration of a point cloud processing platform (Pb/day scale) in C++ to OpenVDB.
- Reduced build times by 50% for a 50-engineer team via compiler optimizations and automated library installation using Python and Conan.

Embedded Software Engineer — **Inetum (València, Spain)** — **Jun 2022 – Nov 2022**

- Rewrote public transport NFC embedded reader (C++) to handle real user behavior, powering Valencia's bus network (77M trips/year).
- Wrote technical specifications for a €27M European project proposal.

Research Assistant — **Parallel Architectures Group, UPV** — **Jun 2019 – May 2022**

- Improved CPU IPC by 15% by designing a novel L1 Cache (FTC).
- Achieved 21% energy savings and a 6.4x density increase vs. SRAM, freeing space for accelerators (e.g.,a bigger GPU).

Education

Universitat Politècnica de València — **València, Spain** — **Sep 2020 – Jun 2021**

Master's in Computer and Network Architecture
With honors on thesis: "Fusion of the L1 and L2 Levels of the Cache Memory Hierarchy Using DWM".

Universitat Politècnica de València — **València, Spain** — **Sep 2016 – Jun 2020**

Bachelor's in Informatics Engineering
With honors on thesis: "L1 Cache Design using Domain Wall Memory technology ".

Publications and Awards

- H. Tárrega et al. 2022. **Fast-track cache: A huge racetrack memory L1 data cache**. *ICS '22*, ACM, Article 23. DOI
- H. Tárrega et al. 2021. **L1 Cache Design using Domain Wall Memory**. DOI
- **Map Hacks València 2019 Hackathon Winner**. Led team developing pollution reduction app for Valencia buses.

Skills

- C++, C, Python, Assembly (x86, MIPS), Shell scripting
- Git, Linux, CPU architectures, CMake, LaTeX, Inkscape