

Spain  
(+34) 656 305 374

# Hugo Tárrega

hugots363@gmail.com  
github.com/htarrega  
www.htarrega.me

## Experience

<b>Software Engineer</b>	<b>Facephi (Alicante, Spain)</b>	<b>April 2024 – Present</b>
<ul style="list-style-type: none"><li>Improved inference throughput by 40% average and reduced latency by 25% average across 15+ biometric pipelines through algorithmic optimizations and parallelization techniques.</li></ul>		
<b>Software Engineer</b>	<b>Topcon Mirage (València, Spain)</b>	<b>Nov 2022 – Apr 2024</b>
<ul style="list-style-type: none"><li>Led migration of a point cloud processing platform (Pb/day scale) in C++ to OpenVDB.</li><li>Reduced build times by 50% for a 50-engineer team via compiler optimizations and automated library installation using Python and Conan.</li></ul>		
<b>Embedded Software Engineer</b>	<b>Inetum (València, Spain)</b>	<b>Jun 2022 – Nov 2022</b>
<ul style="list-style-type: none"><li>Rewrote public transport NFC embedded reader (C++) to handle real user behavior, powering Valencia's bus network ( 77M trips/year).</li></ul>		
<b>Research Assistant</b>	<b>Parallel Architectures Group, UPV</b>	<b>Jun 2019 – May 2022</b>
<ul style="list-style-type: none"><li>Improved CPU IPC by 15% by designing a novel L1 Cache (FTC).</li><li>Achieved 21% energy savings and a 6.4x density increase vs. SRAM, freeing space for accelerators (e.g., a bigger GPU).</li></ul>		

## Education

<b>Universitat Politècnica de València</b>	<b>València, Spain</b>	<b>Sep 2020 – Jun 2021</b>
<i>Master's in Computer and Network Architecture</i> With honors on thesis: "Fusion of the L1 and L2 Levels of the Cache Memory Hierarchy Using DWM".		
<b>Universitat Politècnica de València</b>	<b>València, Spain</b>	<b>Sep 2016 – Jun 2020</b>
<i>Bachelor's in Informatics Engineering</i> With honors on thesis: "L1 Cache Design using Domain Wall Memory technology".		

## Publications and Awards

- AI Writing Course Instructor** (Oct 2025). Taught 4-week course on AI for creative writing.
- H. Tárrega et al. 2022. **Fast-track cache: A huge racetrack memory L1 data cache**. *ICS '22*, ACM, Article 23. [DOI](#)
- H. Tárrega et al. 2021. **L1 Cache Design using Domain Wall Memory**. [DOI](#)
- Map Hacks València 2019 Hackathon Winner**. Led team developing pollution reduction app for Valencia buses.

## Skills

- C++, C, Python, Assembly (x86, MIPS), Shell scripting
- Git, Linux, CPU architectures, CMake, LaTeX, Inkscape