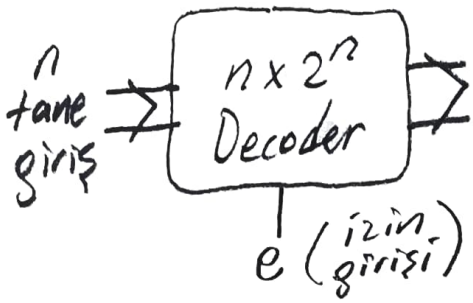
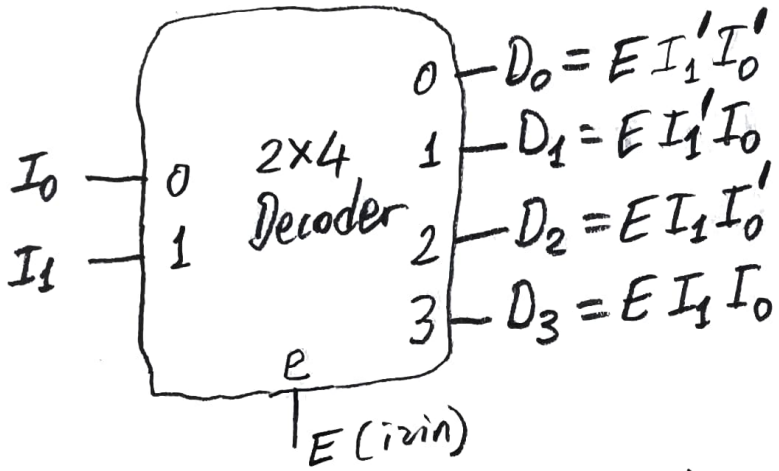
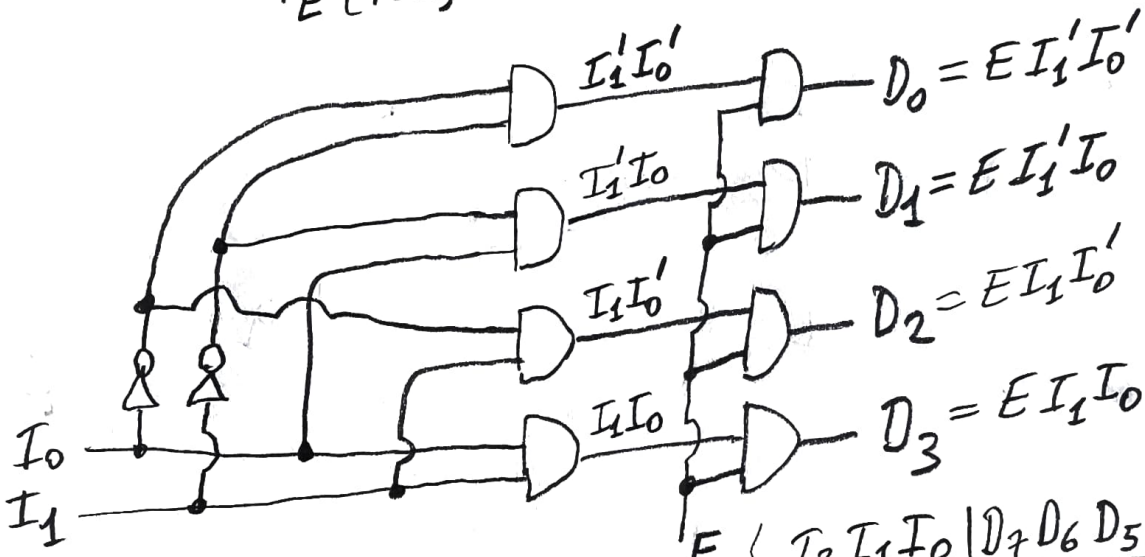
Decoders (Kod Çözücüler)

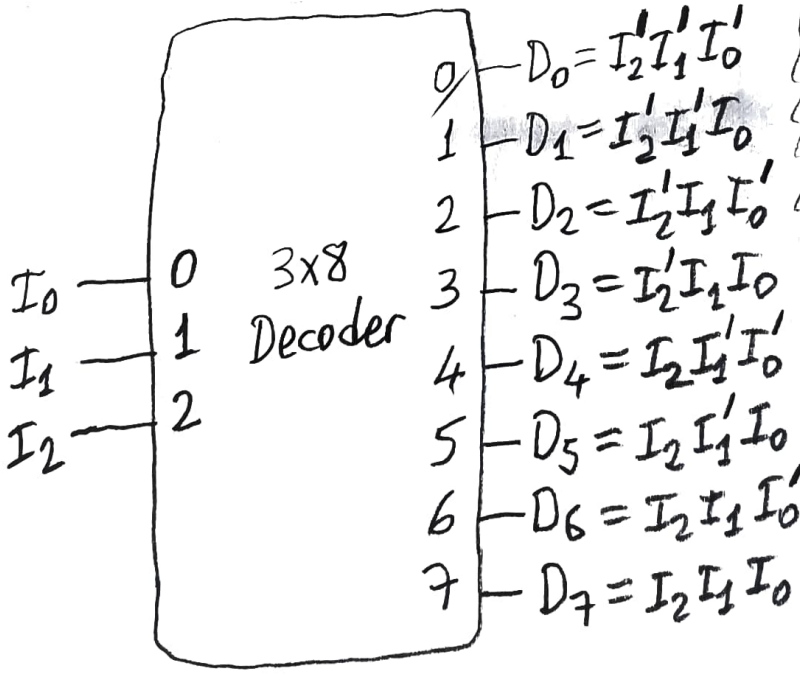


n bitlik seçme girişinin durumuna göre 2^n tane çıkıştan sadece bir tanesi 1, diğerleri 0 olur. İzin girişi aktif ise kod çözücü iş görür.



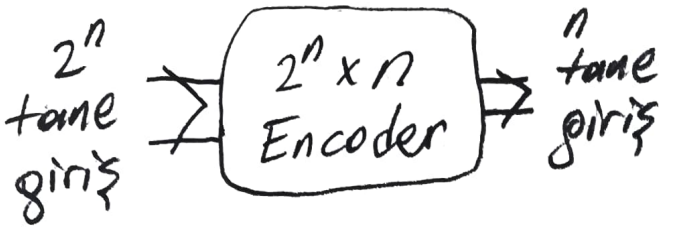
E	I_1	I_2	D_3	D_2	D_1	D_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0





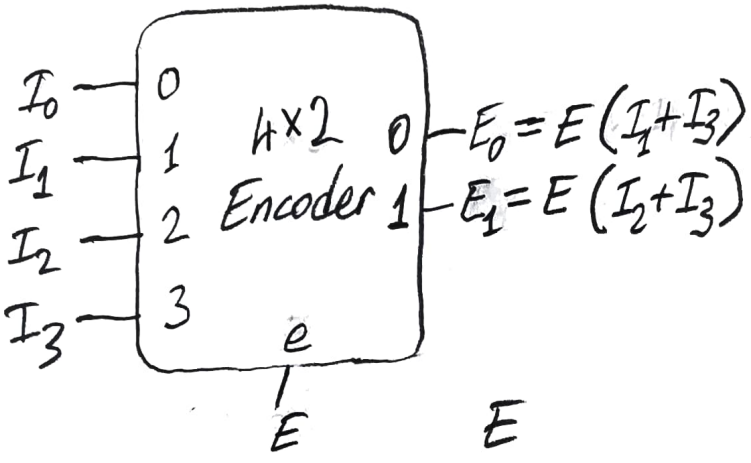
I_2	I_1	I_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Encoders (Kodlayıcılar)

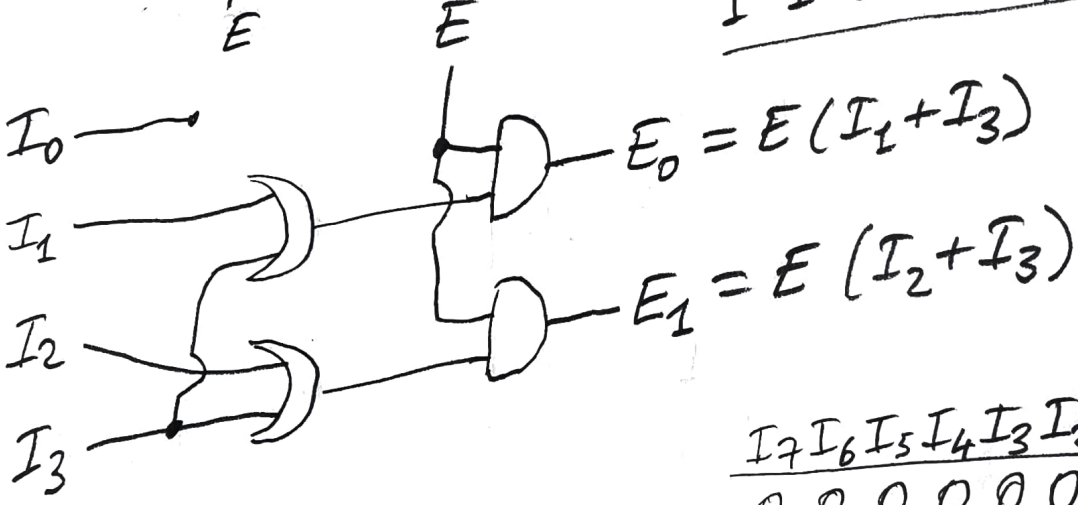


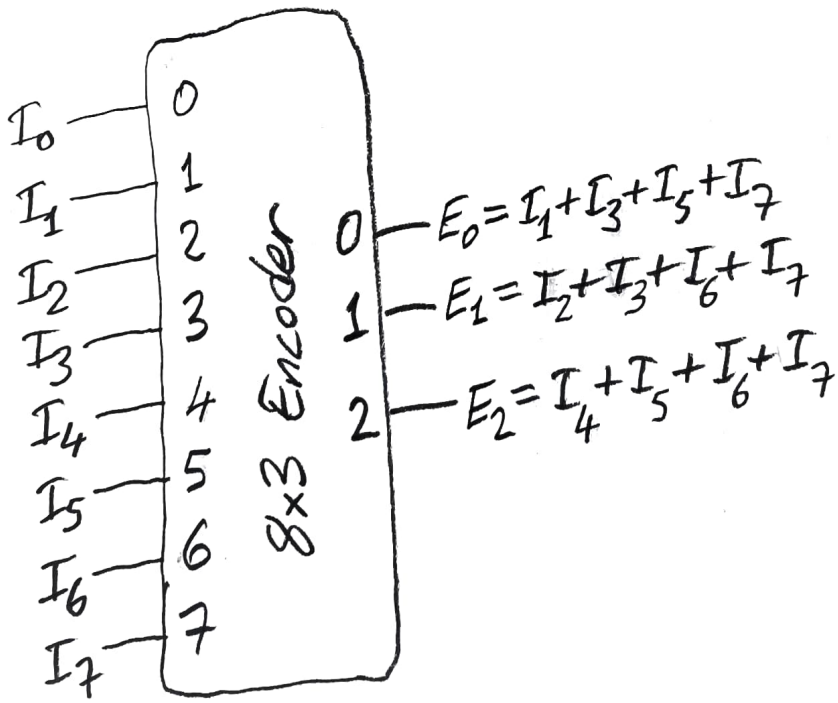
2^n tane girişten sadece bir tane 1, diğerleri 0 olmalıdır. İzin girişi aktifse kodlayıcı iş görür.

Kodlayıcı ile Kod Çözücü birbirinin tersi iş görür.



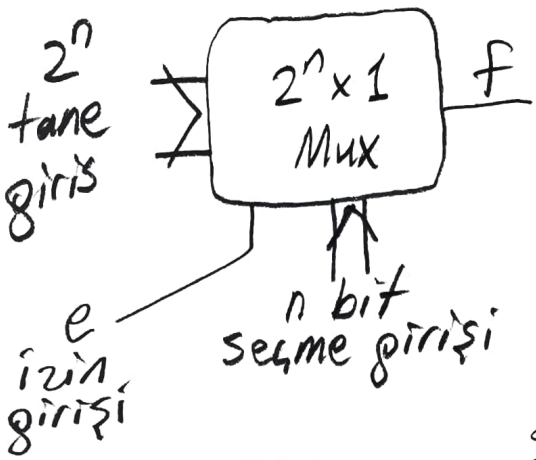
E	I_3	I_2	I_1	I_0	E_1	E_2
0	X	X	X	X	0	0
1	0	0	0	1	0	0
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	1	0	0	0	1	1



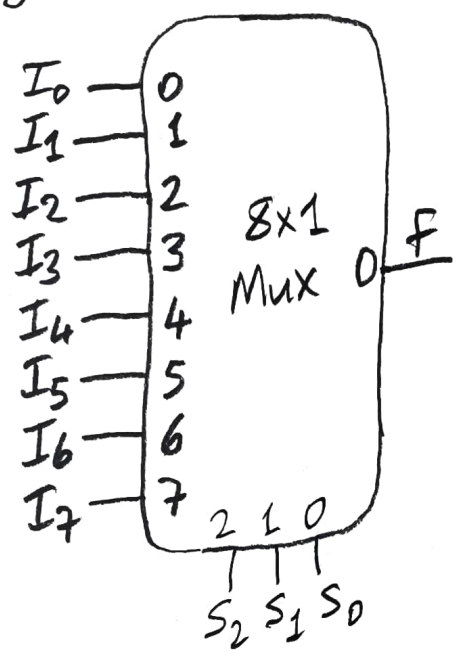


I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	E_2	E_1	E_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

Multiplexers (Veri Seçiciler)

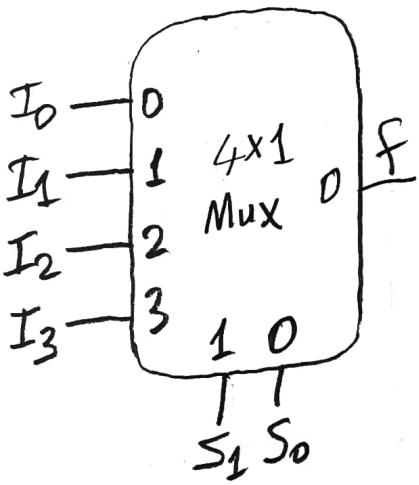


2^n tane veri girişi, n tane seçme girişi ve 1 tane çıkış vardır. n bitlik seçme girişinin durumuna göre 2^n tane veri girişinden biri çıkışa aktarılır.



S_2	S_1	S_0	f
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

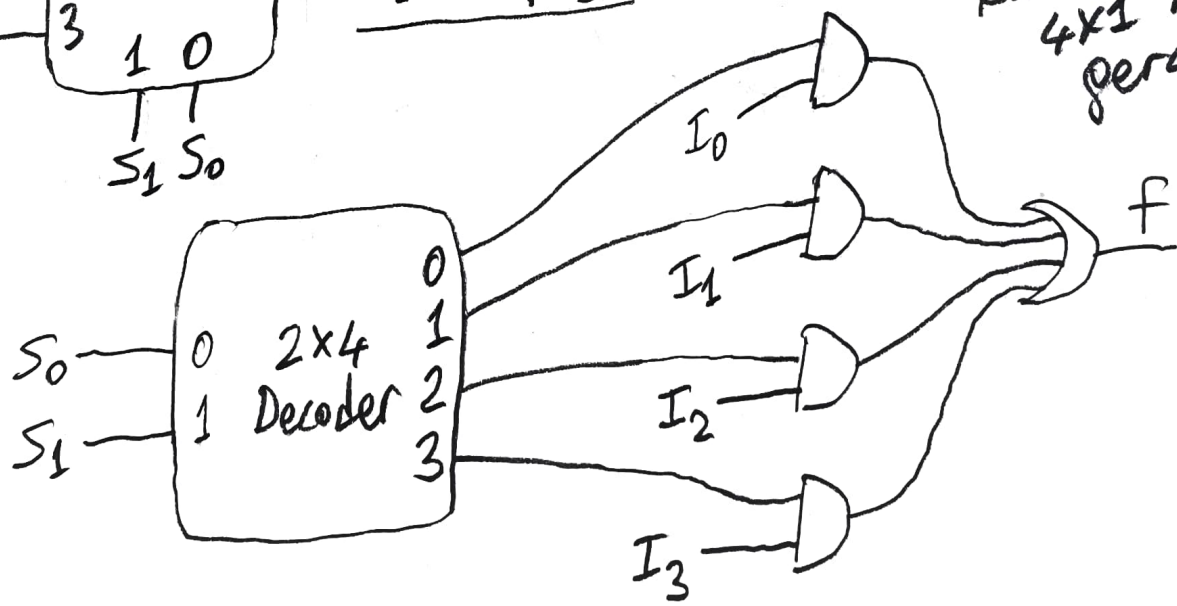
$$f = S_2'S_1'S_0'I_0 + S_2'S_1'S_0I_1 + S_2'S_1S_0'I_2 + S_2'S_1S_0I_3 + S_2S_1'S_0'I_4 + S_2S_1'S_0I_5 + S_2S_1S_0'I_6 + S_2S_1S_0I_7$$



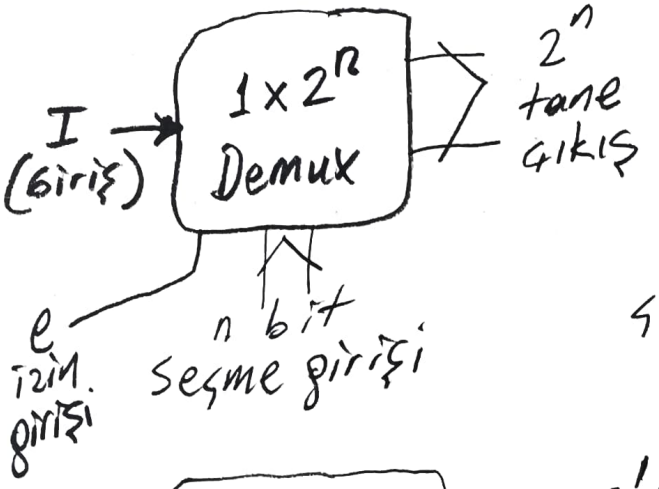
S_1	S_0	f
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$f = S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$$

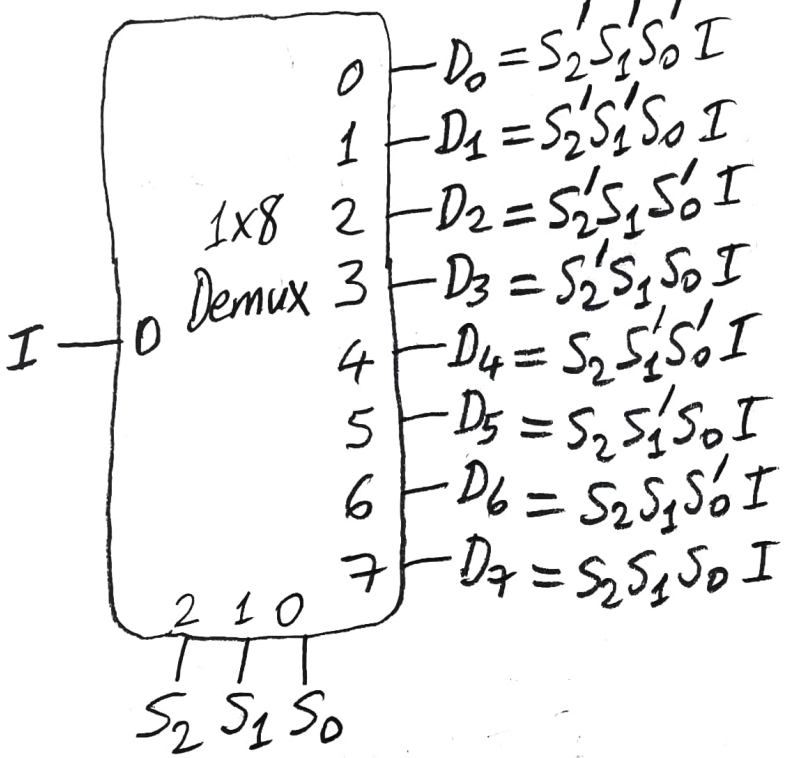
2x4 decoder kullanarak 4x1 mux gerçekleme



Demultiplexers (Veri Yayıcılar)

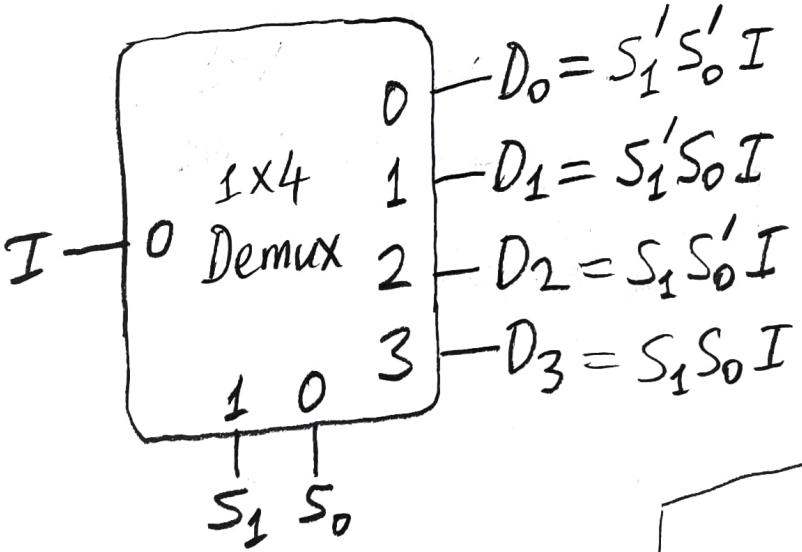


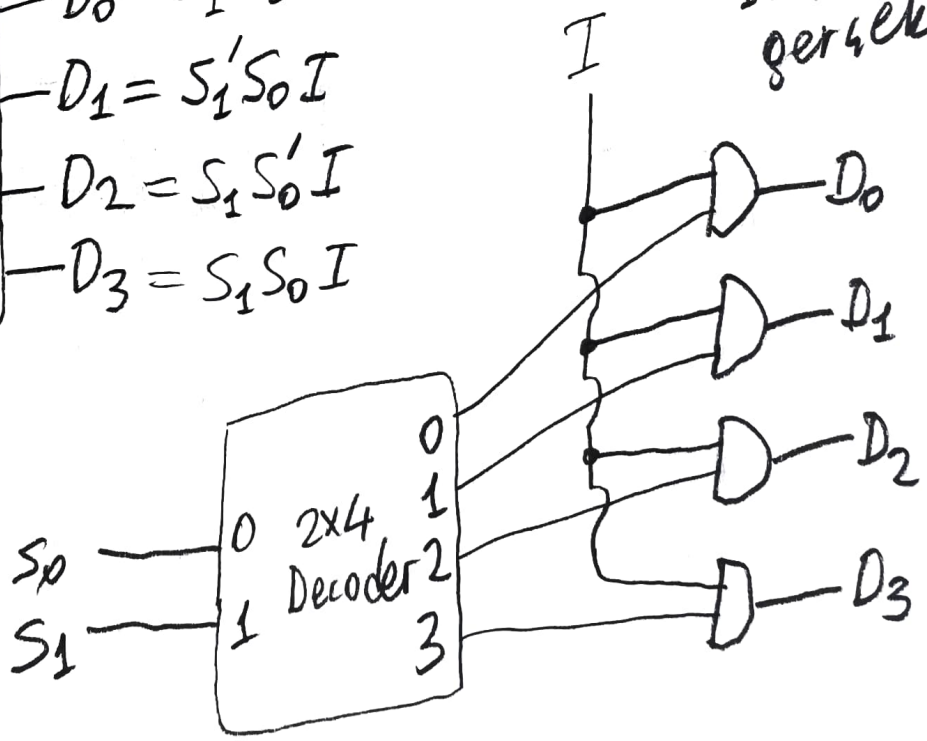
n bitlik seçme girişinin durumuna göre giriş, 2^n tane veri çıkışından birine aktarılır. Diğer veri çıkışları 0'dır.



$S_2S_1S_0$	$D_7D_6D_5D_4D_3D_2D_1D_0$
000	0 0 0 0 0 0 0 I
001	0 0 0 0 0 0 I 0
010	0 0 0 0 0 I 0 0
011	0 0 0 0 I 0 0 0
100	0 0 0 I 0 0 0 0
101	0 0 I 0 0 0 0 0
110	0 I 0 0 0 0 0 0
111	I 0 0 0 0 0 0 0

2x4 Decoder kullanarak 1x4 Demux gerçekleme



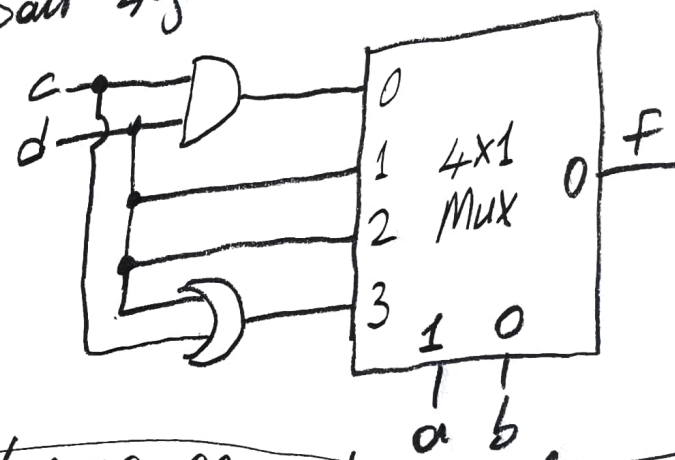


Bir sendikanın yönetim kurulunda 4 temsilci vardır. a temsilcisi 100, b temsilcisi 60, c temsilcisi 140, d temsilcisi 200 kişiyi temsil etmektedir. Her temsilcinin önünde bir düğme vardır. Olumlu oy kullanan temsilci önündeki düğmeye basmaktadır. Kararların alınmasında salt çoğunluk yeterlidir. Salt çoğunluk sağlanırsa lamba yanmaktadır. Bu işi yapan lojik devreyi 4x1 mux ve en az kapı elemanı kullanarak tasarlayınız. Mux'ın seçme girişleri $S_1 = a$, $S_2 = b$ olsun.

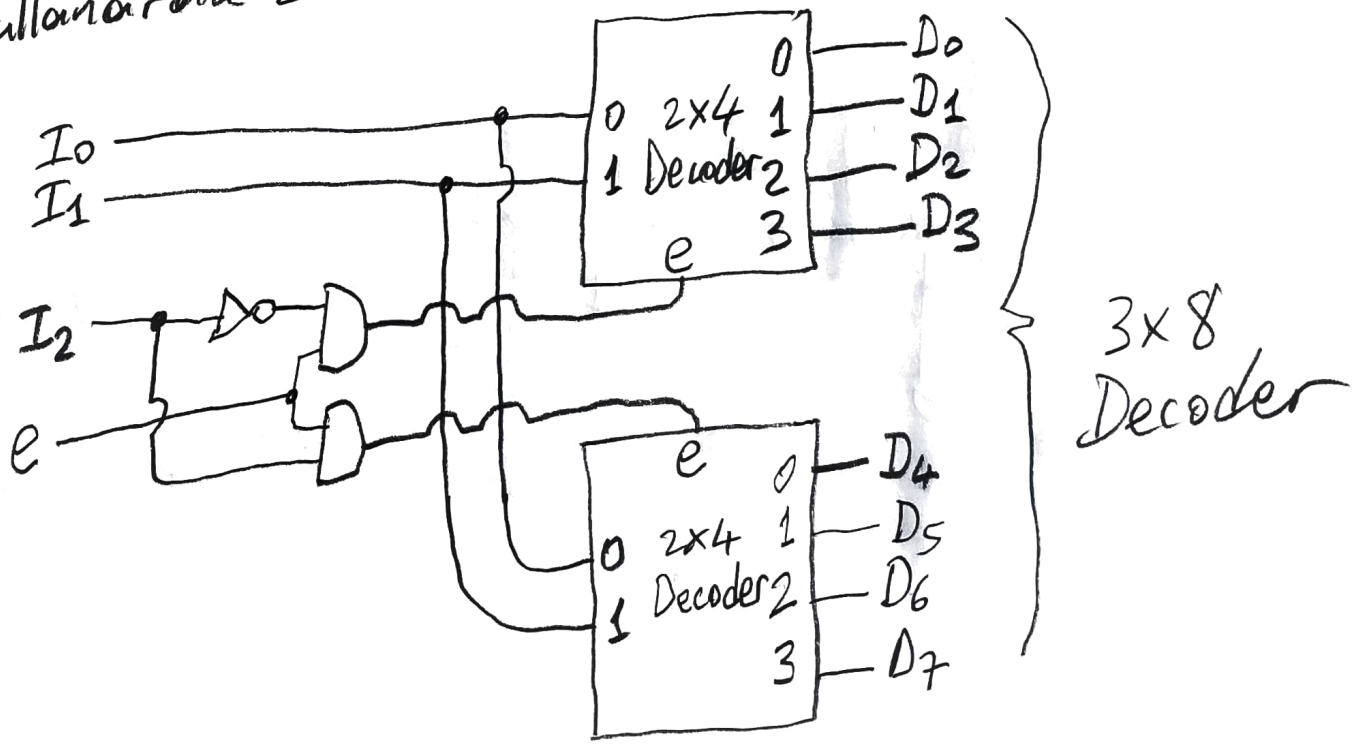
a	b	c	d	f
0	0	1	1	$f_0 = cd$
0	1	0	1	$f_1 = c'd + cd$
0	1	1	1	$= (c'+c)d = d$
1	0	0	1	$f_2 = c'd + cd$
1	0	1	1	$= (c'+c)d = d$
1	1	0	1	$f_3 = (c'd')'$
1	1	1	0	$= c + d$
1	1	1	1	

a	b	c	d	Toplam
100	60	140	200	500

Salt çoğunluk 251 kişi



İki adet izin girişli 2x4 Decoder ve en az kapı elemanı kullanarak bir adet izin girişli 3x8 Decoder gerçekleyiniz.

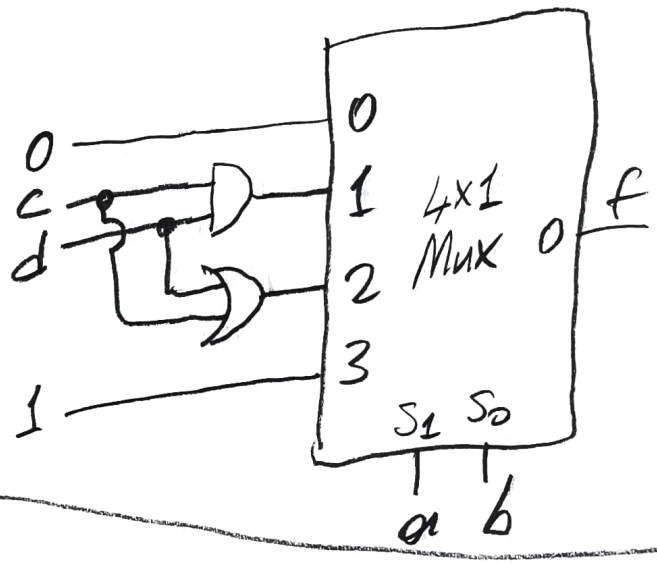


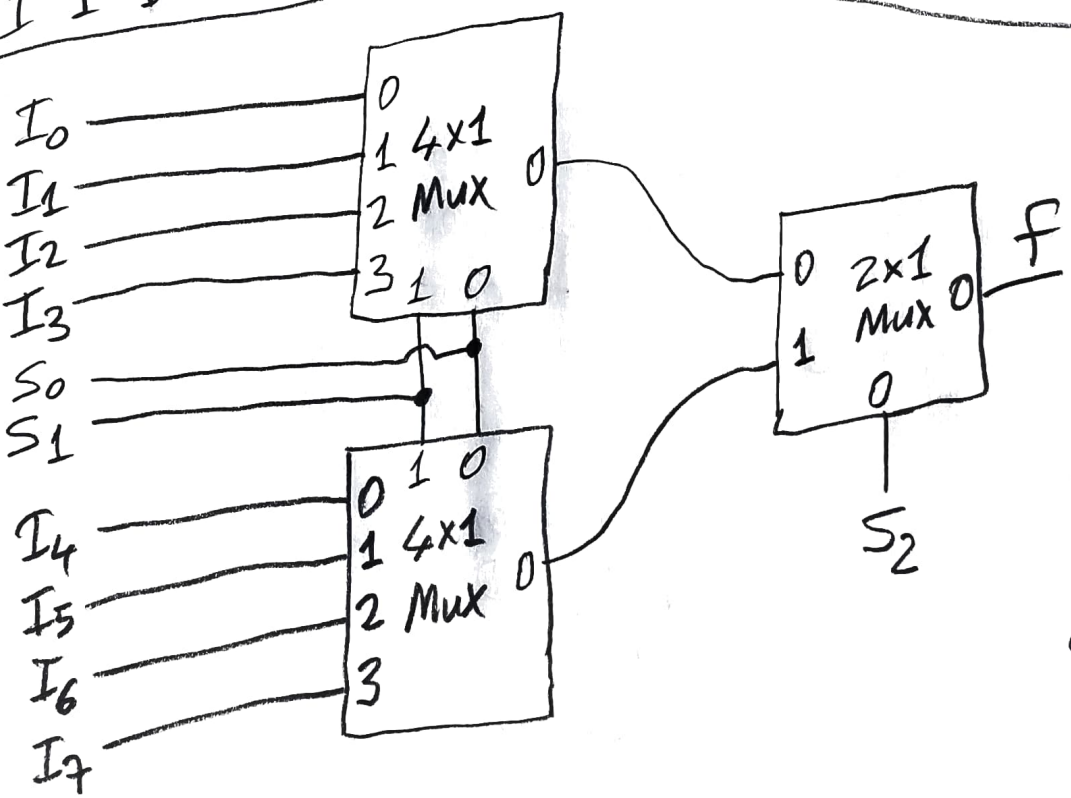
Bir sendikanın yönetim kurulunda 4 temsilci vardır. a temsilcisi 17, b temsilcisi 10, c temsilcisi 13 ve d temsilcisi 9 kişiyi temsil etmektedir. Her temsilcinin önünde bir düğme vardır. Olumlu oy kullanan temsilci önündeki düğmeye basmaktadır. Kararların alınmasında salt çoğunluk yeterlidir. Salt çoğunluk sağlanırsa düğme yanmaktadır. Bu işi yapan lojik devreyi 4x1 mux ve en az kapı elemanı kullanarak tasarlayınız. Mux seçme girişleri $S_1=a$, $S_0=b$ olsun

a b c d	Toplam
17 10 13 9	49

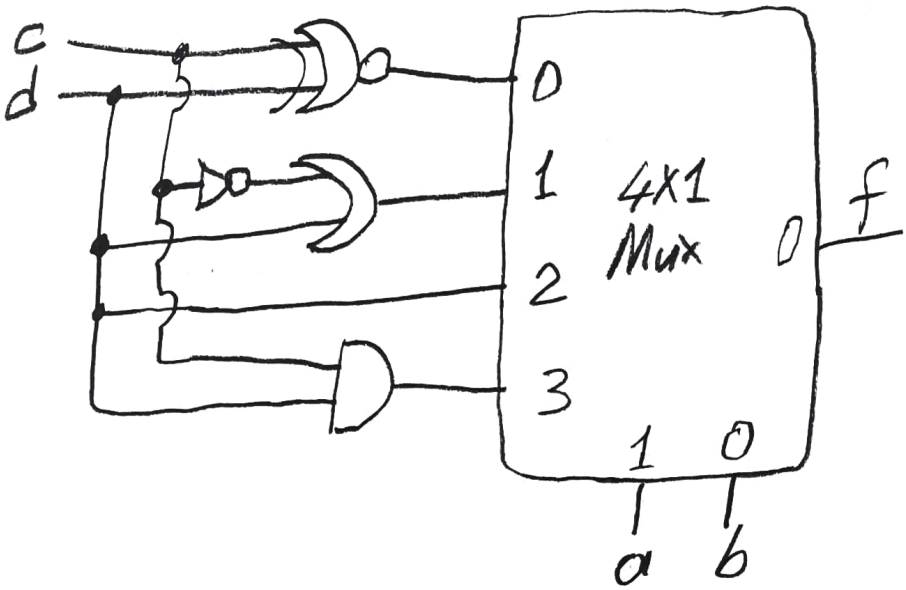
Salt çoğunluk 25 kişi

a b c d	f
0 1 1 1	$f_1=cd$
1 0 0 1	$f_2=(c'd')'$
1 0 1 0	$=c+d$
1 0 1 1	
1 1 0 0	$f_3=c'd'+c'd$
1 1 0 1	$+cd'+cd$
1 1 1 0	$=1$
1 1 1 1	



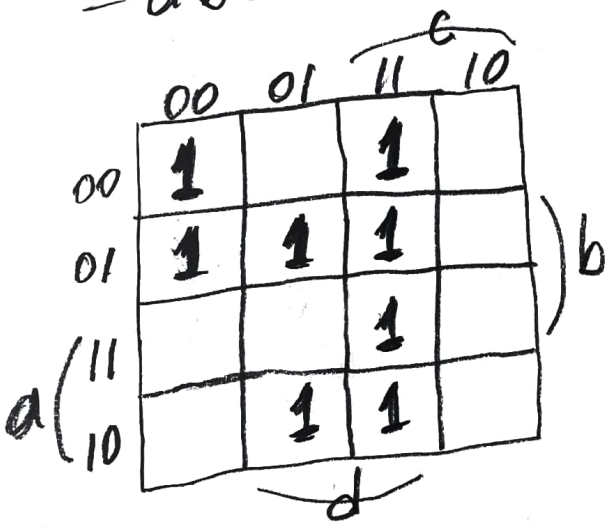


2 tane 4x1 Mux, 1 tane 2x1 Mux kullanarak 8x1 Mux Gerçekleme

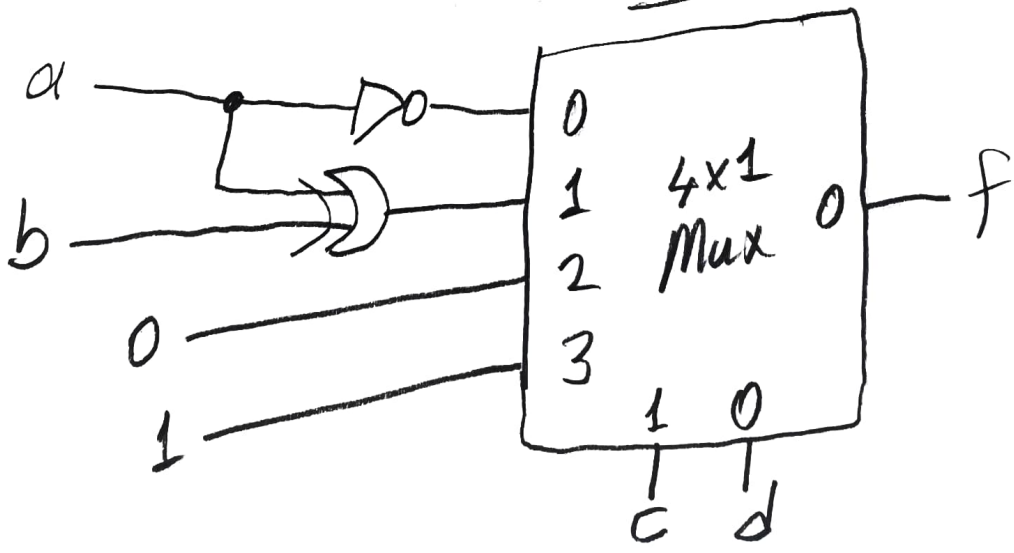


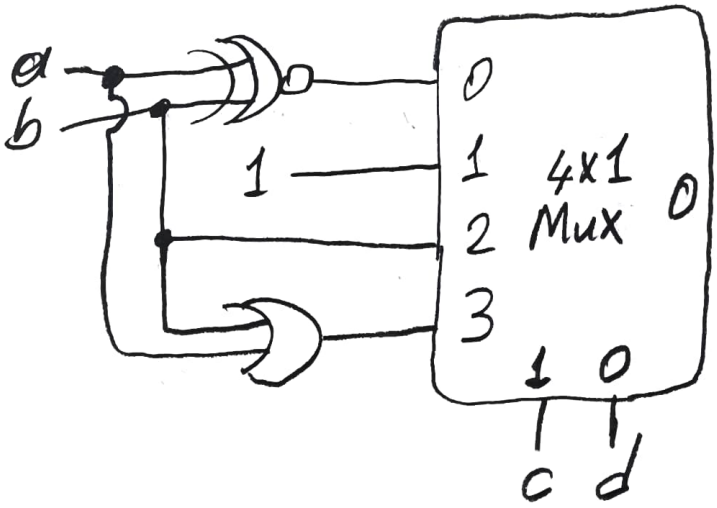
Yanda verilen 4x1 Mux'lı mantık devresini Mux'ın seçme girişlerini a, b yerine c, d olarak yeniden gerçekle.

$$f = a'b'(c \odot d) + a'b(c'+d) + ab'd + abcd$$
$$= a'b'(cd + c'd') + a'bc' + a'bd + ab'd + abcd$$
$$= a'b'cd + a'b'cd' + a'bc' + a'bd + ab'd + abcd$$



c d	a b	f
0 0	0 0	$f_0 = a'b' + a'b$
0 0	0 1	$= a'(b'+b) = a'$
0 1	0 1	$a'b$ } $f_1 = a \oplus b$
0 1	1 0	ab' }
1 1	0 0	$a'b'$ } $f_3 = 1$
1 1	0 1	$a'b$
1 1	1 0	ab'
1 1	1 1	ab





Yanda verilen mantık devresini 4x1 Mux'ın seçme girişlerini c,d yerine a,b alarak 4x1 Mux ve en az kapı elemanı kullanarak yeniden tasarla.

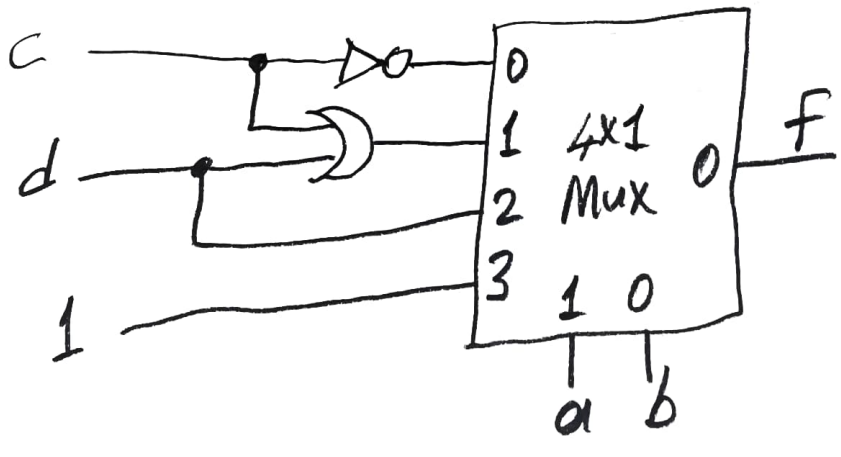
$$f = (a \odot b)c'd' + c'd + bcd' + (a+b)cd$$
$$= (ab + a'b')c'd' + c'd + bcd' + acd + bcd$$
$$= abc'd' + a'b'c'd' + c'd + bcd' + acd + bcd$$

	00	01	11	10
00	1	1		
01		1	1	1
11	1	1	1	1
10		1	1	

(c: 11, 10; b: 01, 11, 10; a: 11, 10; d: 01, 11)

a b	c d	f
0 0	0 0	$f_0 = c'd' + c'd = c'(d'+d) = c'$
0 0	0 1	
0 1	0 1	$f_1 = (c'd')' = c + d$
0 1	1 0	
0 1	1 1	
1 0	0 1	$f_2 = c'd + cd = (c'+c)d = d$
1 0	1 1	
1 1	0 0	$c'd'$
1 1	0 1	$c'd$
1 1	1 0	cd'
1 1	1 1	cd

$f_3 = 1$



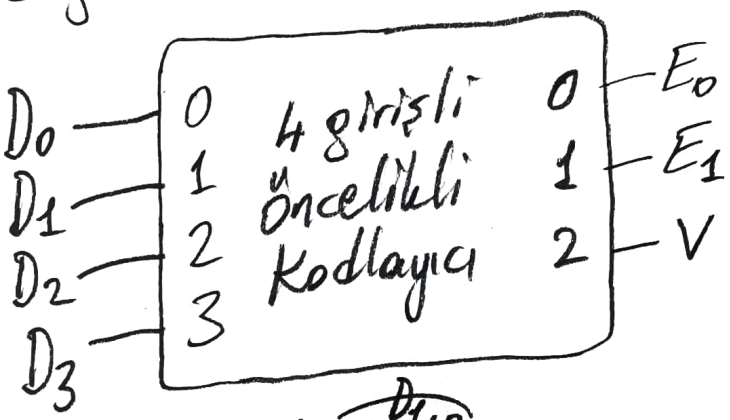
Priority Encoder (öncelikli Kodlayıcı)

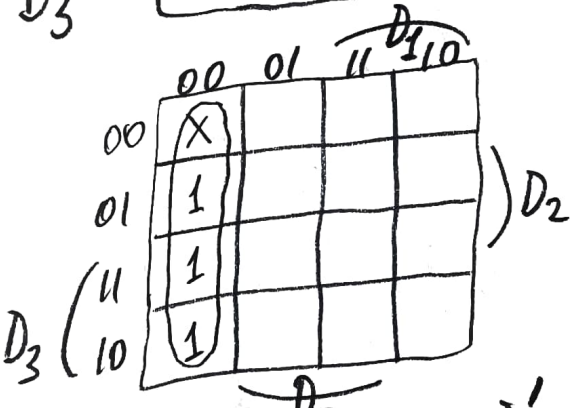
Girişler				Çıkışlar		
D_3	D_2	D_1	D_0	E_1	E_0	V
0	0	0	0	X	X	0
X	X	X	1	0	0	1
X	X	1	0	0	1	1
X	1	0	0	1	0	1
1	0	0	0	1	1	1

Doğruluk Tablosu

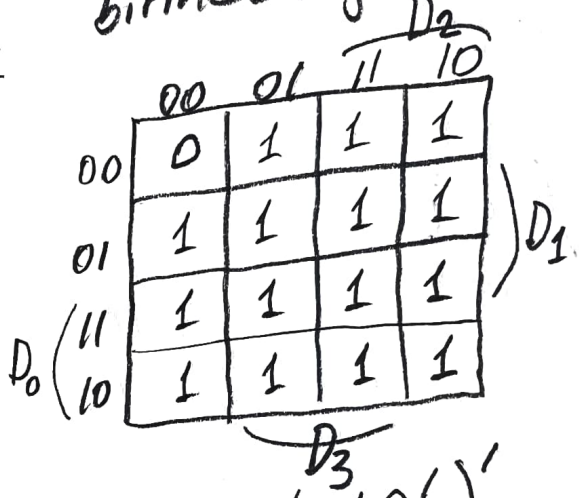
Mikroişlemcili cihazlara farklı cihazlar bağlanabilir. Her bir cihazın bir önceliği vardır. D_0 girişine bağlanan cihazın önceliği en yüksek, D_3 girişine bağlanan cihazın önceliği en düşüktür.

Hiçbir cihazdan sinyal gelmezse V=0, en az birinden gelirse V=1 olur.

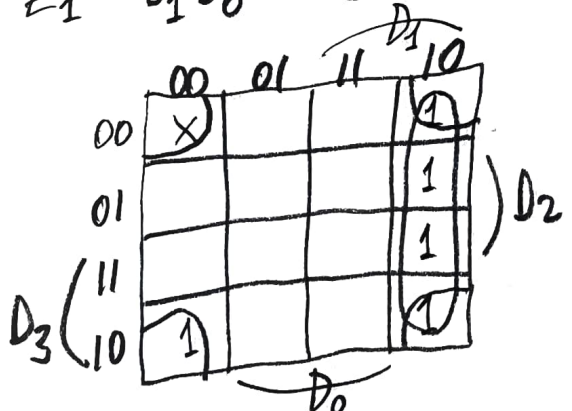




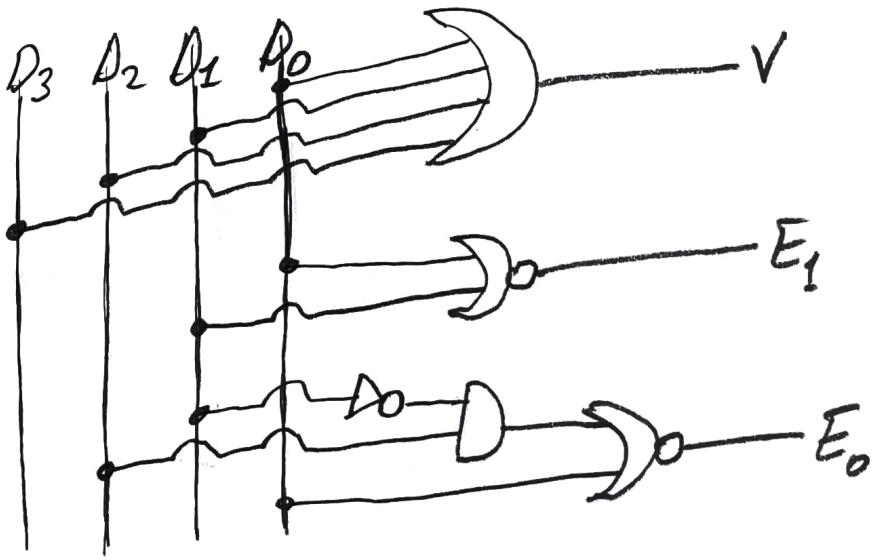
$$E_1 = D_1'D_0' = (D_0 + D_1)'$$



$$V = (D_3'D_2'D_1'D_0')'$$
$$= D_0 + D_1 + D_2 + D_3$$



$$E_0 = D_2'D_0' + D_1D_0'$$
$$= D_0'(D_2' + D_1) = (D_0 + D_1'D_2)'$$



D_3 D_2 D_1 D_0	E_1 E_0 V
0 0 0 0	X X 0
X X X 1	0 0 1
X X 1 0	0 1 1
X 1 0 0	1 0 1
1 0 0 0	1 1 1

İki tane 4 girişli öncelikli kodlayıcı ve en az kapı elemanı kullanarak bir tane 8 girişli öncelikli kodlayıcı tasarlayınız.

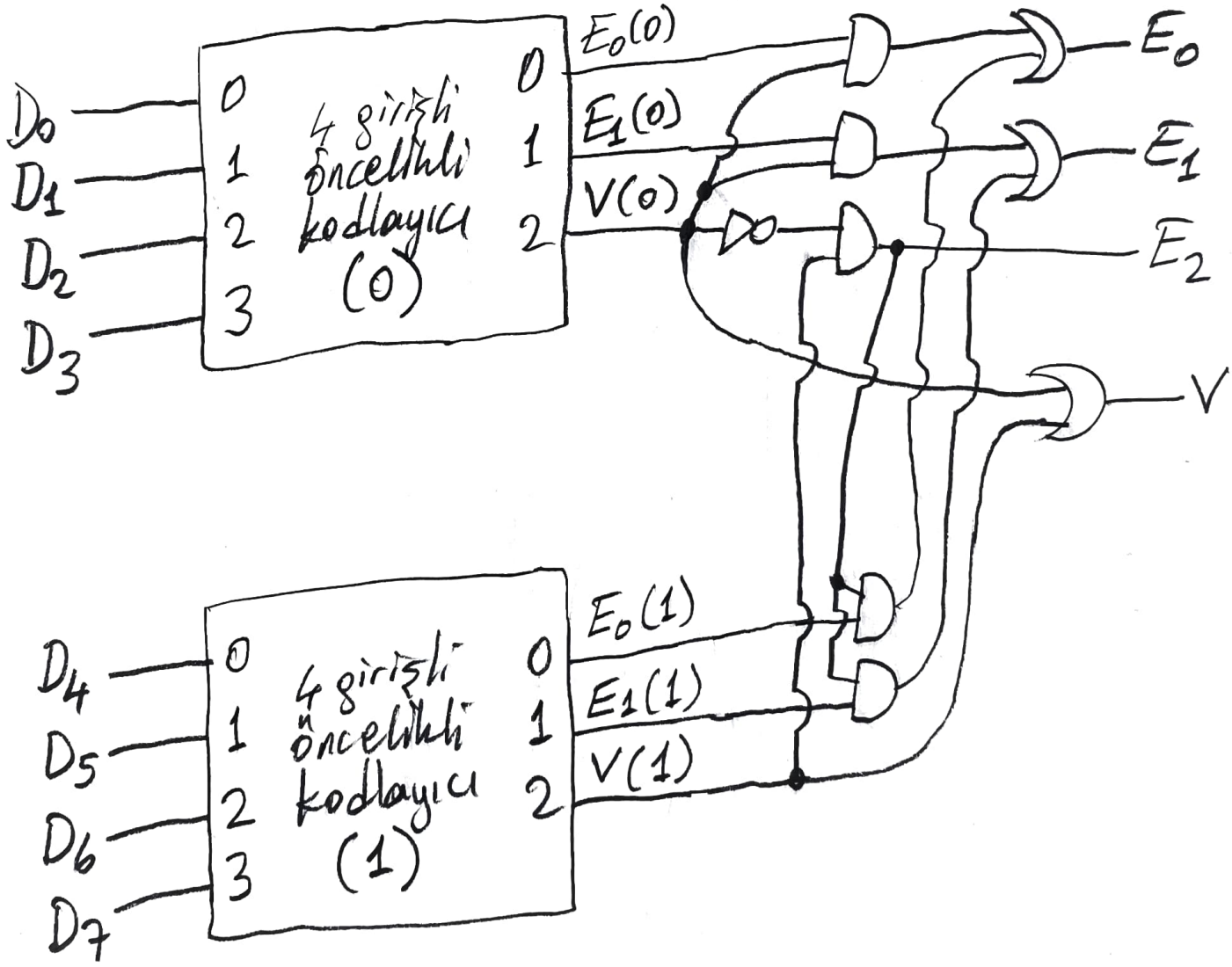
$D_7 \cdots D_0$	E_2 E_1 E_0 V
X X X X	0
0 0 0 0	1
0 0 0 1	1
0 0 1 0	1
0 0 1 1	1
0 1 0 0	1
0 1 0 1	1
0 1 1 0	1
0 1 1 1	1
1 0 0 0	1
1 0 0 1	1
1 0 1 0	1
1 0 1 1	1
1 1 0 0	1
1 1 0 1	1
1 1 1 0	1
1 1 1 1	1

$$E_0 = V(0)\,E_0(0) + V'(0)\,V(1)\,E_0(1)$$

$$E_1 = V(0)\,E_1(0) + V'(0)\,V(1)\,E_1(1)$$

$$E_2 = V'(0)\,V(1)$$

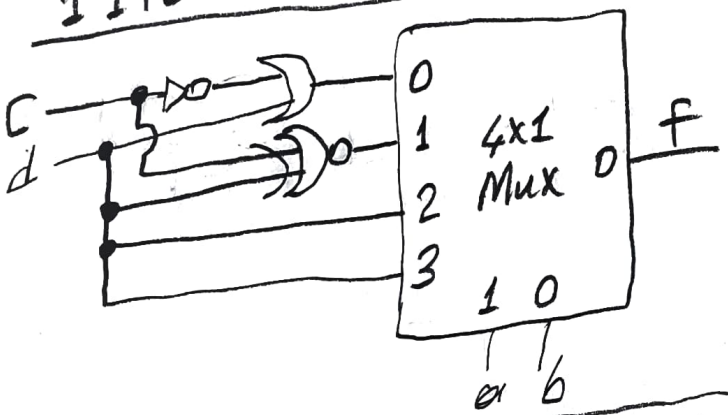
$$V = V(0) + V(1)$$



$f(a,b,c,d) = \Sigma(0,1,3,4,7,9,11,13,15)$ ifadesi veriliyor.

a) Seçme girişlerine a, b verilirse 4x1 mux ile gerçekle

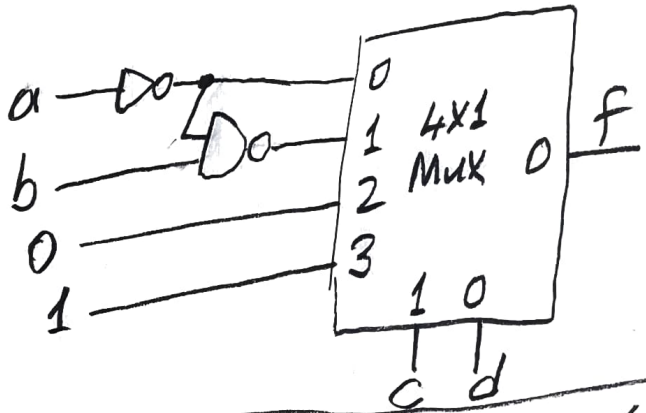
a b	c d	f
0 0	0 0	$f_0 = (cd')$
0 0	0 1	$= c' + d$
0 0	1 1	
0 1	0 0	$f_1 = c'd' + cd$
0 1	1 1	$= c \odot d$
1 0	0 1	$f_2 = c'd + cd$
1 0	1 1	$= (c'+c)d = d$
1 1	0 1	$f_3 = c'd + cd$
1 1	1 1	$= (c'+c)d = d$



b) Seçme girişlerine c, d verilirse 4x1 mux ile gerçekle.

c d	a b	f
0 0	0 0	$f_0 = a'b' + a'b$
0 0	0 1	$= a'(b'+b) = a'$
0 1	0 0	$f_1 = (a'b)'$
0 1	1 0	$= a + b'$
0 1	1 1	
1 1	0 0	$a'b'$
1 1	0 1	$a'b$
1 1	1 0	ab'
1 1	1 1	ab

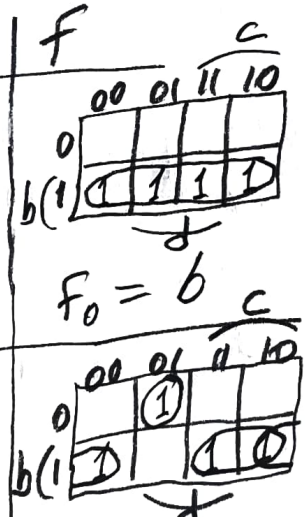
$f_3 = 1$

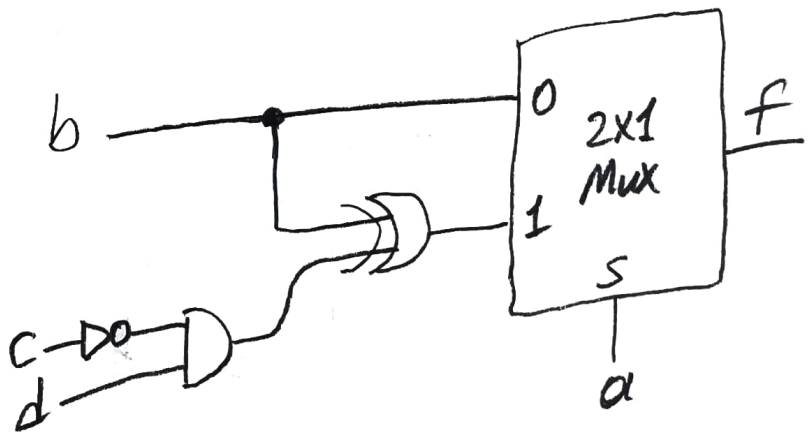


$f(a,b,c,d) = \Pi(0,1,2,3,8,10,11,13)$ 2x1 mux ile gerçekle

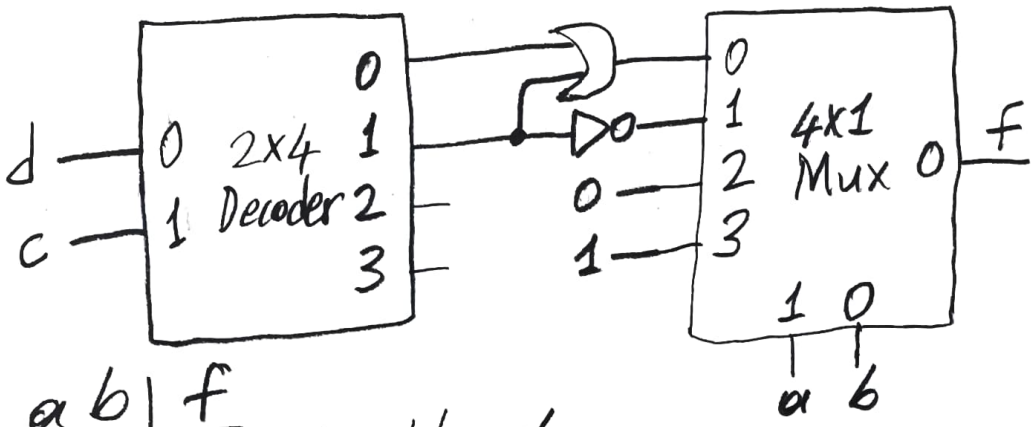
$f = \Sigma(4,5,6,7,9,12,14,15)$

a	b c d	f
0	1 0 0	$f_0 = b$
0	1 0 1	
0	1 1 0	
0	1 1 1	
1	0 0 1	$f_1 = bc + bd' + b'c'd$
1	1 0 0	$= b(c+d') + b'(c'd)$
1	1 1 0	$= b(c'd)' + b'(c'd) = b \oplus (c'd)$
1	1 1 1	



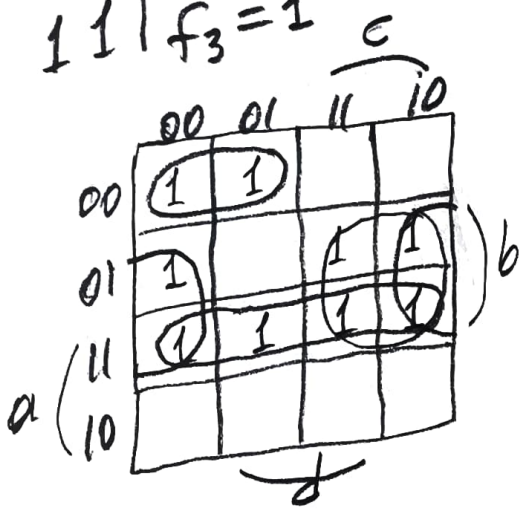


Yanda verilen mantık devresini en az kapı elemanı kullanarak yeniden şekle.

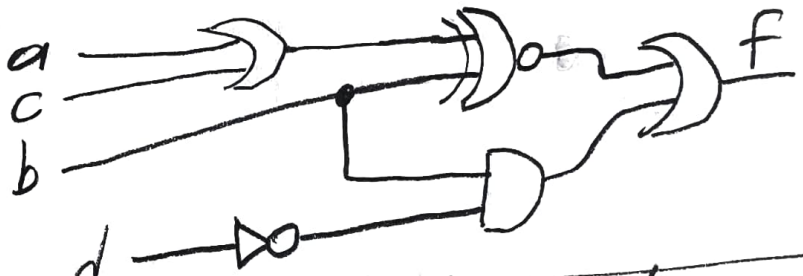


a b	f
0 0	$f_0 = c'd' + c'd = c'$
0 1	$f_1 = (c'd)' = c + d'$
1 0	$f_2 = 0$
1 1	$f_3 = 1$

$$f = a'b'c' + a'b(c+d') + ab$$
$$= a'b'c' + a'bc + a'bd' + ab$$



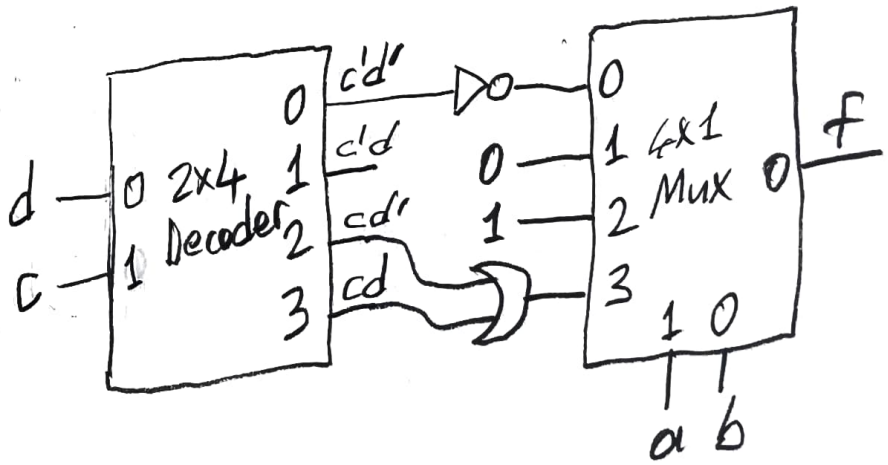
$$f = ab + bc + bd' + a'b'c'$$
$$= b(a+c) + bd' + b'(a+c)'$$
$$= b \odot (a+c) + bd'$$



$f(a,b,c,d) = \sum(1,2,3,8,9,10,11,14,15)$ veriliyor.
2x4 Decoder, 4x1 Mux ve en az kapı kullanarak tasarla.

a b	c d	f
0 0	0 1	$f_0 = (c'd')'$
0 0	1 0	
0 0	1 1	
1 0	0 0	$c'd'$
1 0	0 1	$c'd$
1 0	1 0	cd'
1 0	1 1	cd
1 1	1 0	$f_3 = cd' + cd$
1 1	1 1	

$f_2 = 1$



$f(a,b,c,d) = \Sigma(0,1,3,6,8,9,11,12,13,15)$ veriliyor.

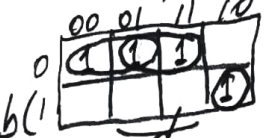
a) 2x1 Mux ve en az kapı kullanarak gerçekle.

b) 4x1 Mux ve en az kapı kullanarak gerçekle.

c) 8x1 Mux ve en az kapı kullanarak gerçekle.

a)

a	b	c	d	f
0	0	0	0	
0	0	0	1	
0	0	1	1	
0	1	1	0	
1	0	0	0	
1	0	0	1	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	1	

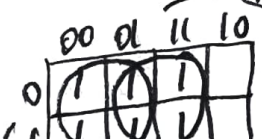


$f_0 = b'c' + b'd + bcd'$

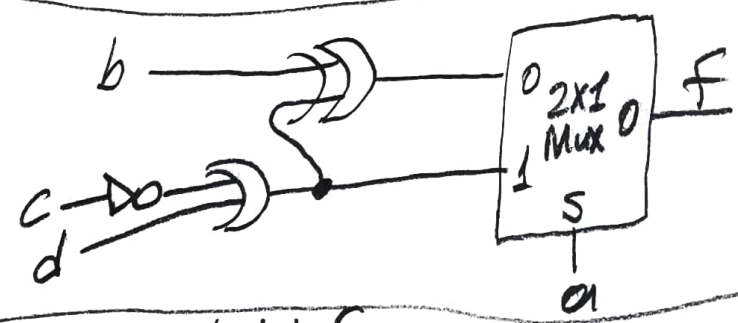
$= b'(c'+d) + b(cd')$

$= b'(c'+d) + b(c'+d)'$

$= b \oplus (c'+d)$

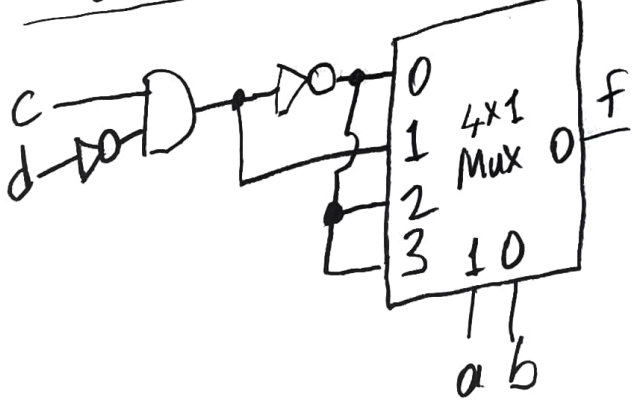


$f_1 = c'+d$



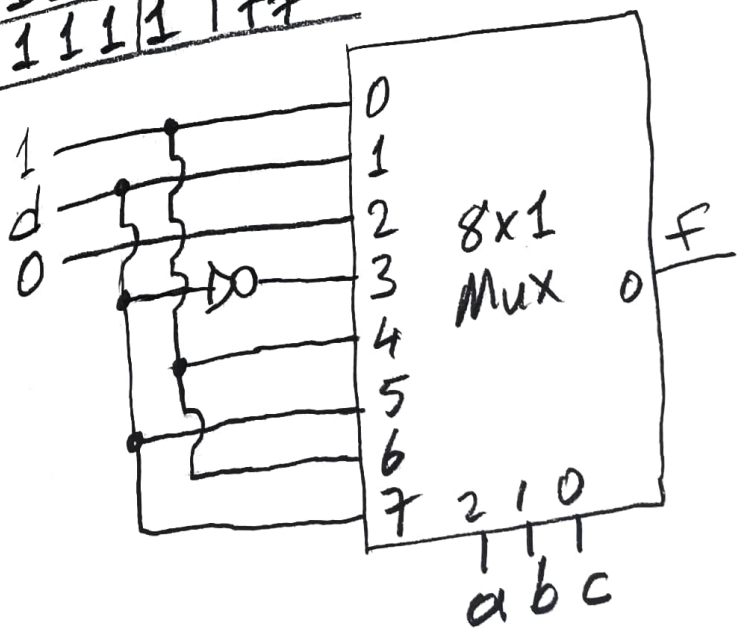
b)

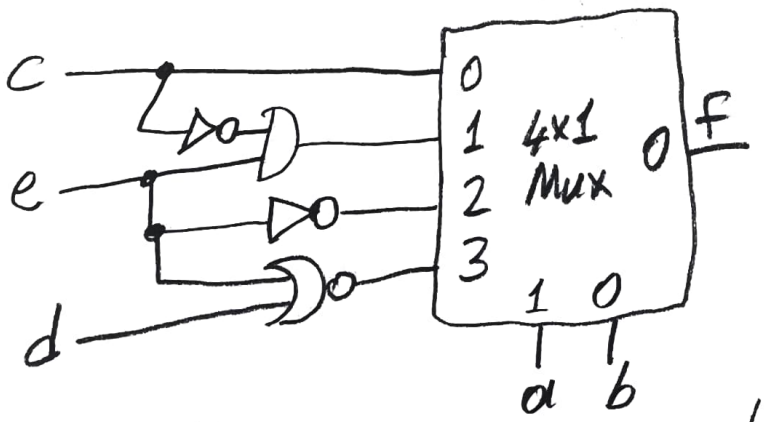
a	b	c	d	f
0	0	0	0	$f_0 = (cd')'$
0	0	0	1	
0	0	1	1	
0	1	1	0	$f_1 = cd'$
1	0	0	0	$f_2 = (cd')'$
1	0	0	1	
1	0	1	1	
1	1	0	0	$f_3 = (cd')'$
1	1	0	1	
1	1	1	1	



c)

a	b	c	d	f
0	0	0	0	$f_0 = d'+d = 1$
0	0	0	1	
0	0	1	1	$f_1 = d$
0	1	1	0	$f_3 = d'$
1	0	0	0	$f_4 = d'+d = 1$
1	0	0	1	
1	0	1	1	$f_5 = d$
1	1	0	0	$f_6 = d'+d = 1$
1	1	0	1	
1	1	1	1	$f_7 = d$





Yanda verilen mantık devresini $f(a,b,c,d,e) = \Sigma(?)$ formunda ifade et.

a b	f
0 0	$f_0 = c$
0 1	$f_1 = c'e$
1 0	$f_2 = e'$
1 1	$f_3 = (e+d)' = d'e'$

a b c d e	f
0 0 1 X X	4,5,6,7
0 1 0 X 1	9,11
1 0 X X 0	16,18,20,22
1 1 X 0 0	24,28

$$f(a,b,c,d,e) = \Sigma(4,5,6,7,9,11,16,18,20,22,24,28)$$

$f = a \oplus d \oplus c + d \odot e \oplus b + a \oplus e \odot c \oplus d$ ifadesi ile verilen boole fonksiyonunu 4x1 Mux ve en az kapı elemanı kullanarak tasarla. 4x1 Mux'ın seçme girişleri d, e olsun.

d e	f
0 0	$f_0 = a \oplus c + b' + a \odot c = b' + 1 = 1$
0 1	$f_1 = a \oplus c + b + a \oplus c = b + a \oplus c$
1 0	$f_2 = a \odot c + b + a \oplus c = b + 1 = 1$
1 1	$f_3 = a \odot c + b' + a \odot c = b' + a \odot c = (b \cdot (a \oplus c))'$