

Precision OpAmp Design

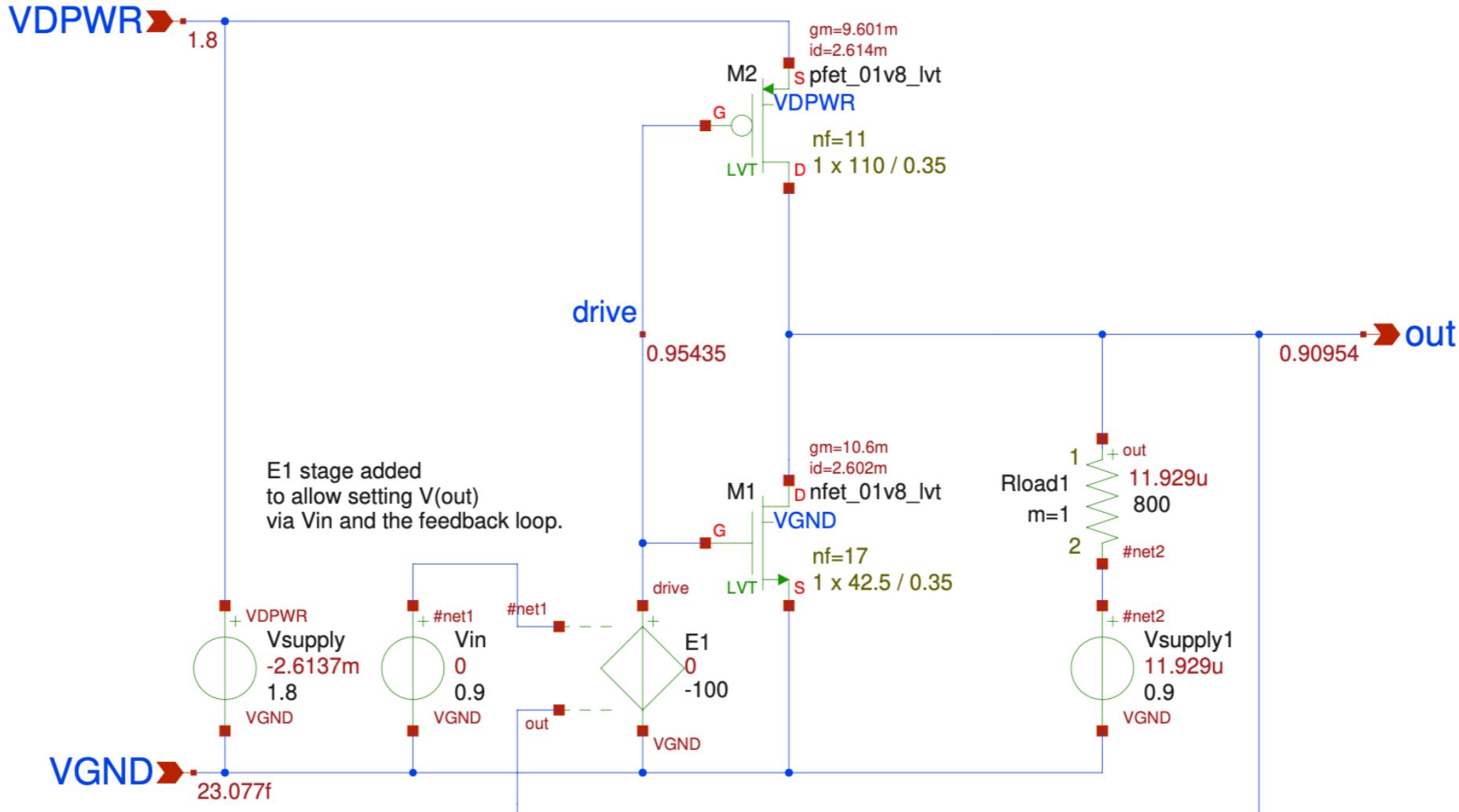
- a tutorial -

Rod Burt, Aug 22, 2024

design goals for this example

- $V_{supply} = 1.8V$ nominal, 1.7V to 1.9V
- V_{out} range = 0.1V to ($V_{supply} - 0.1$)
- $I_{out} > 1mA$
- $C_{load} = 50pf$ or $1nf$ with series $R = 100\Omega$
- $GBW = 10MHz$
- Slew Rate = 5V/us
- V_{in} range = 0.1 to ($V_{supply} - 0.6V$)
- $e_n = 10nV/\sqrt{Hz}$ @ 1MHz, $2uV/\sqrt{Hz}$ @ 1Hz
- Temperature = 27°C nominal, -40°C to 125°C

output stage



Start with the output stage;

We set the loading conditions for each stage by designing from the output back to the input.

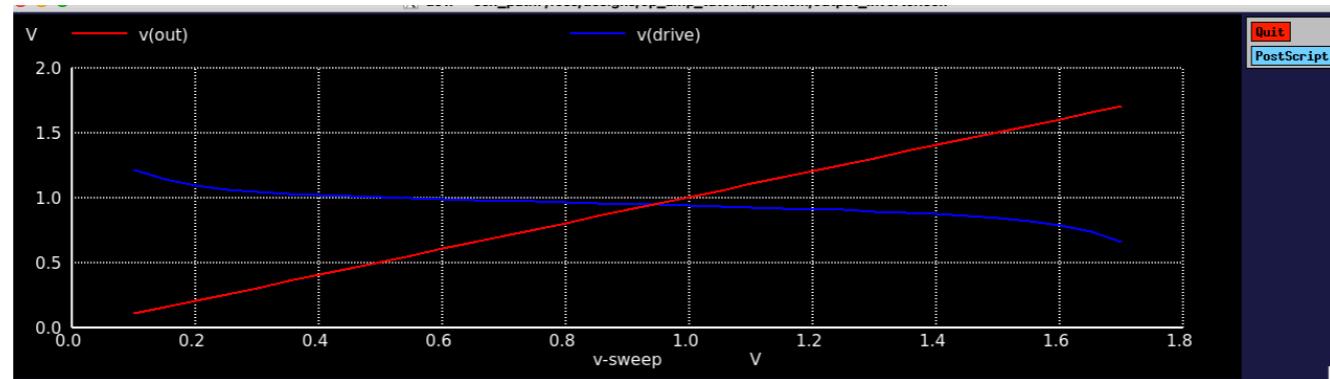
A rail to rail output stage can be as simple as an inverter.

For $I_{out} > 1\text{mA}$ at the rails the device sizes are made large to reduce v_{dsat} .

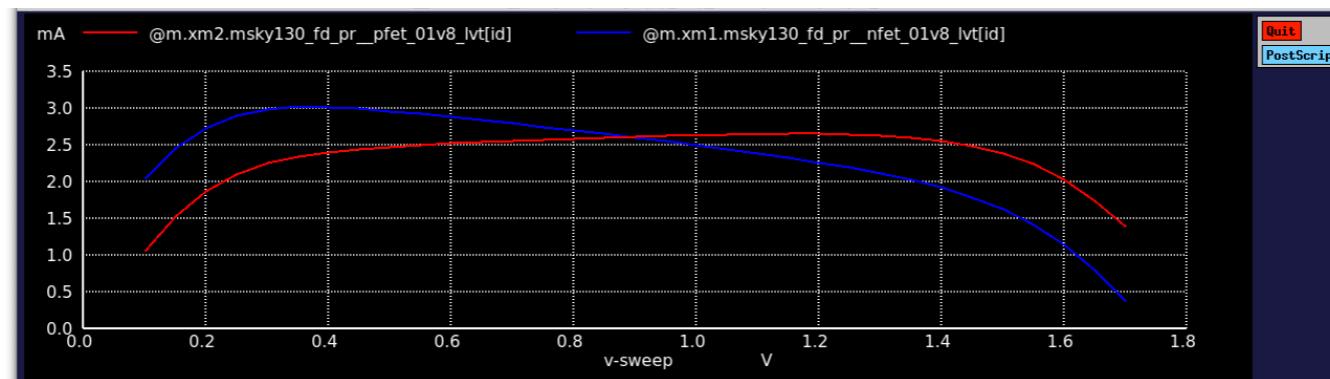
For stability with Cloud $\frac{1}{(gm_1 + gm_2)}$ should be $\approx 100\Omega$.

This results in Id quiescent = 2.6mA. This is too much!

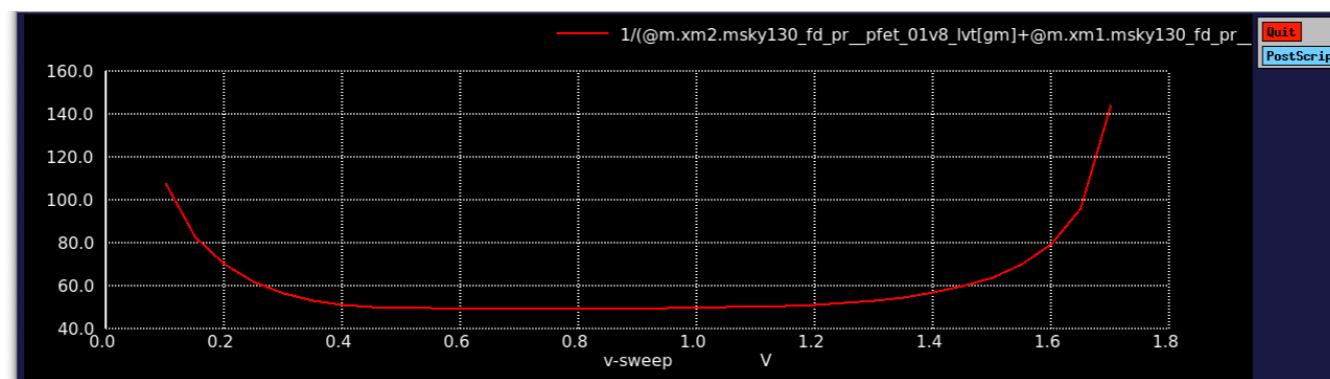
output stage - simulations



$v(\text{out})$ and $v(\text{drive})$

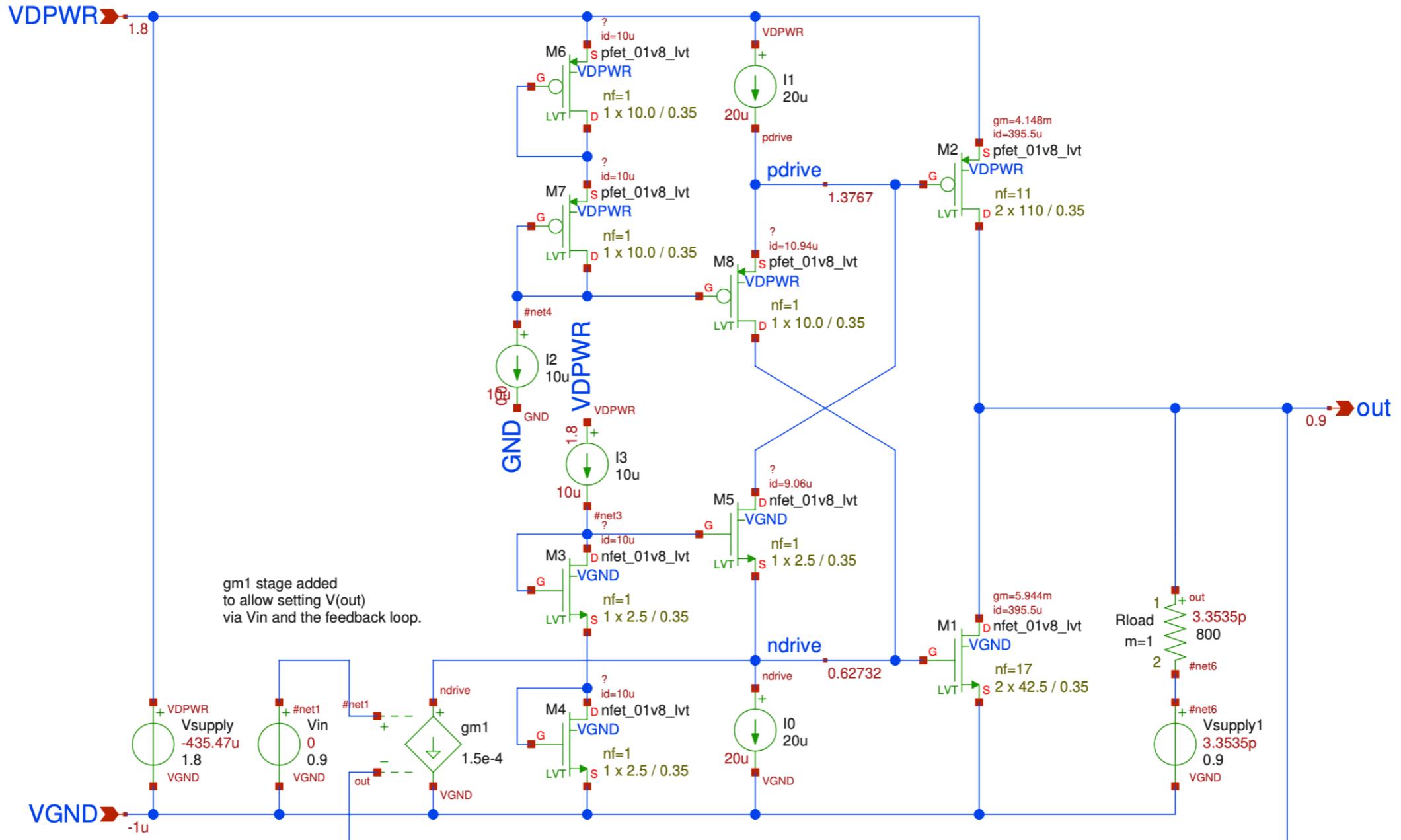


id_1 and id_2



$$\frac{1}{(gm_1 + gm_2)}$$

class AB output stage

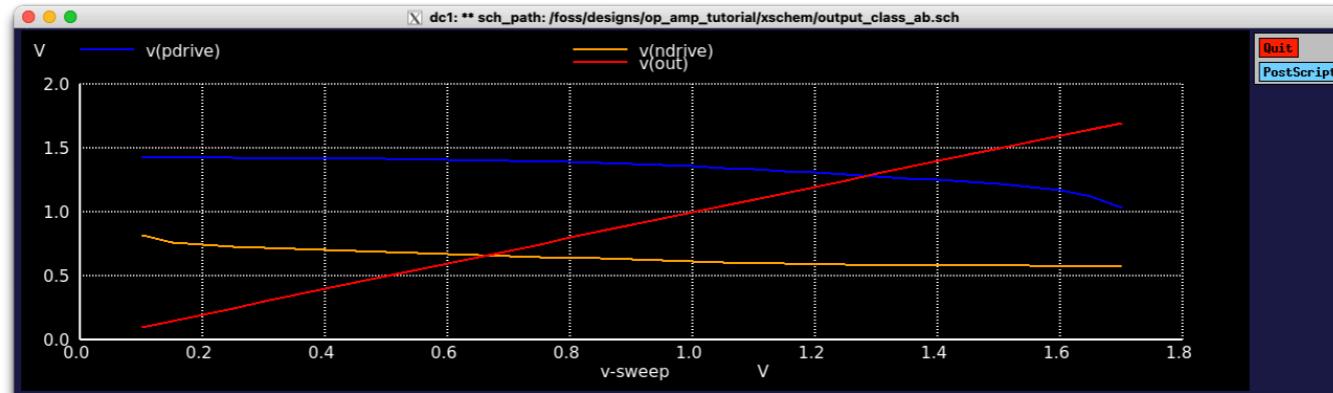


Add class AB biasing control to fix problems of using a basic inverter stage.

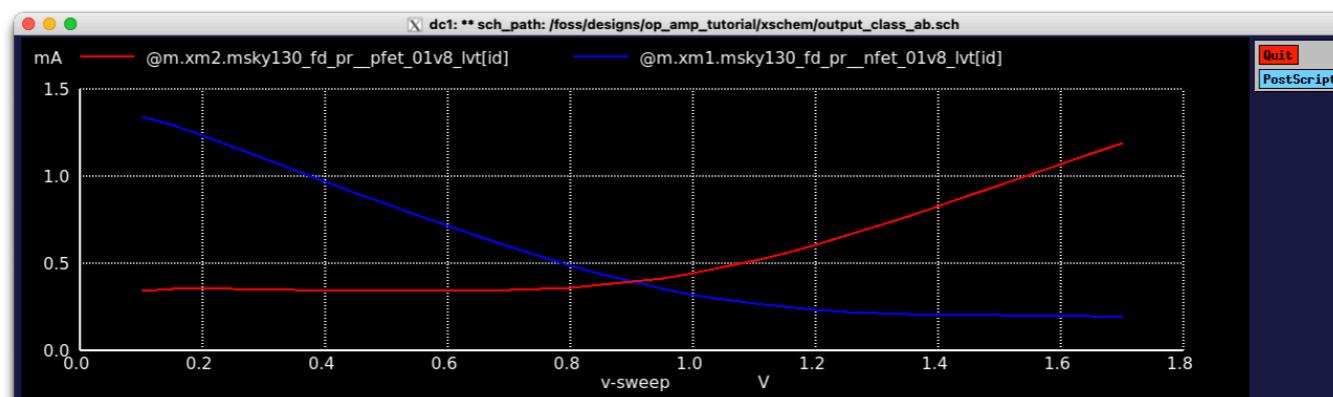
$$\frac{1}{gm1 + gm2} \approx 100\Omega$$

Id quiescent reduced to 395uA.

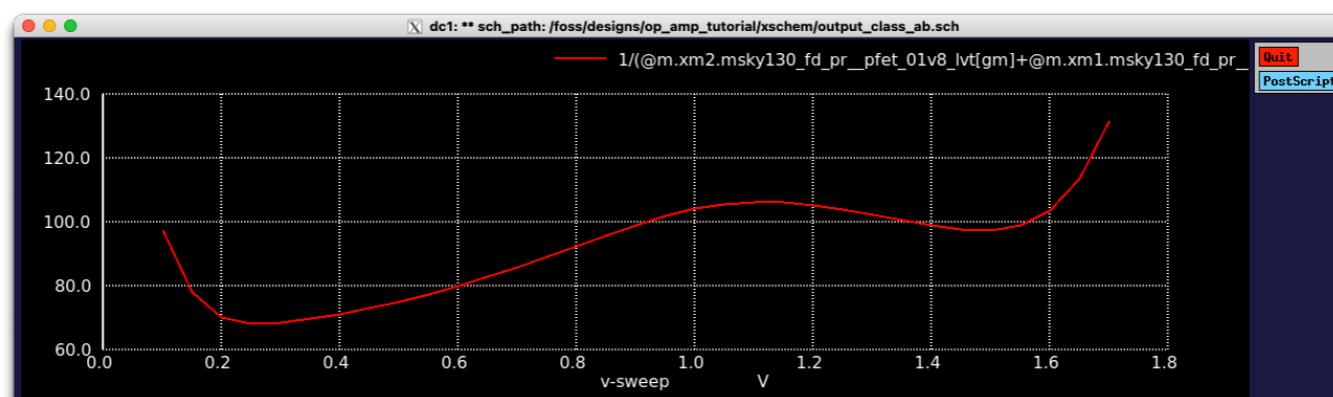
class AB output stage - simulations



$v(\text{out})$, $v(\text{pdrive})$, and $v(\text{ndrive})$

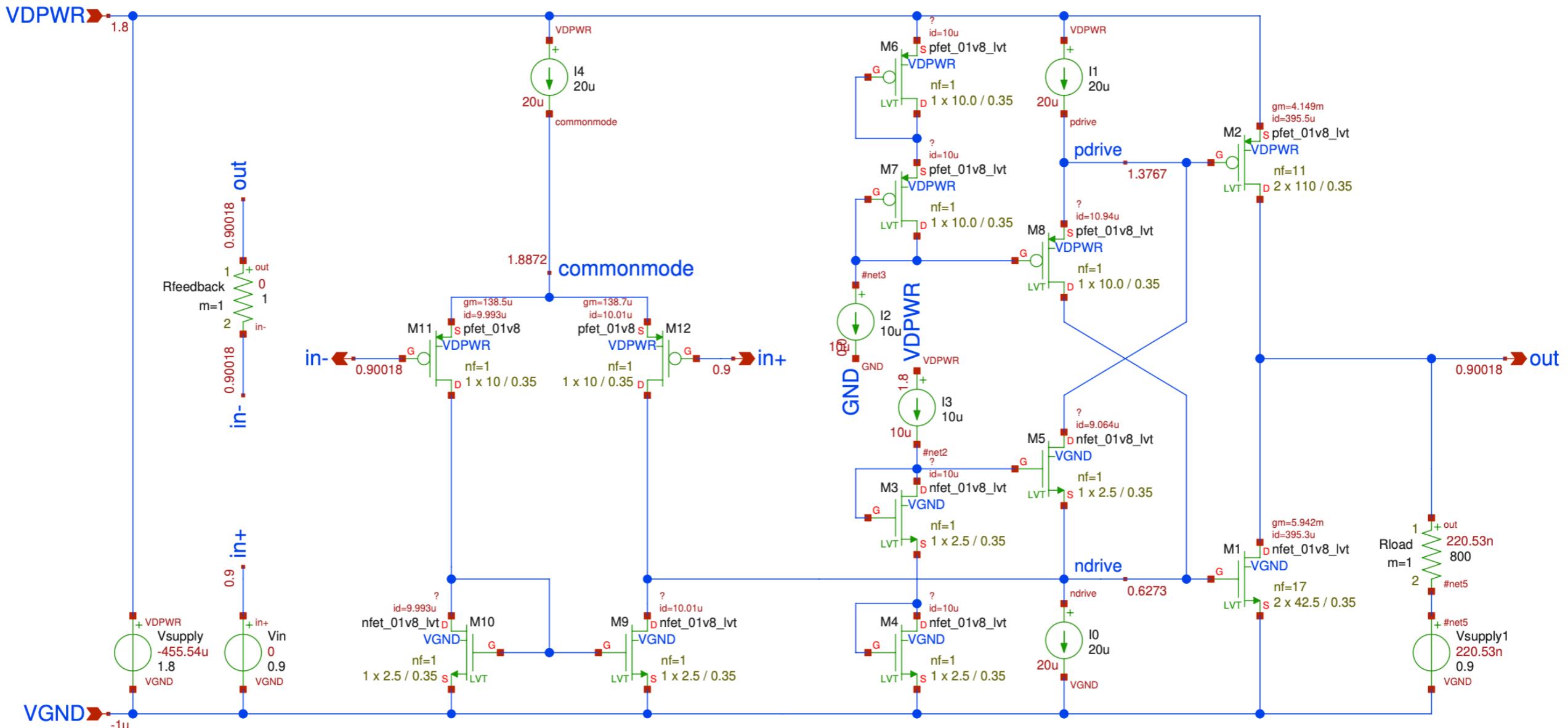


id1 and id2



$$\frac{1}{(gm_1 + gm_2)}$$

2 stage PMOS OpAmp



Add a PMOS level shifting diff pair and we have a simple 2 stage design.

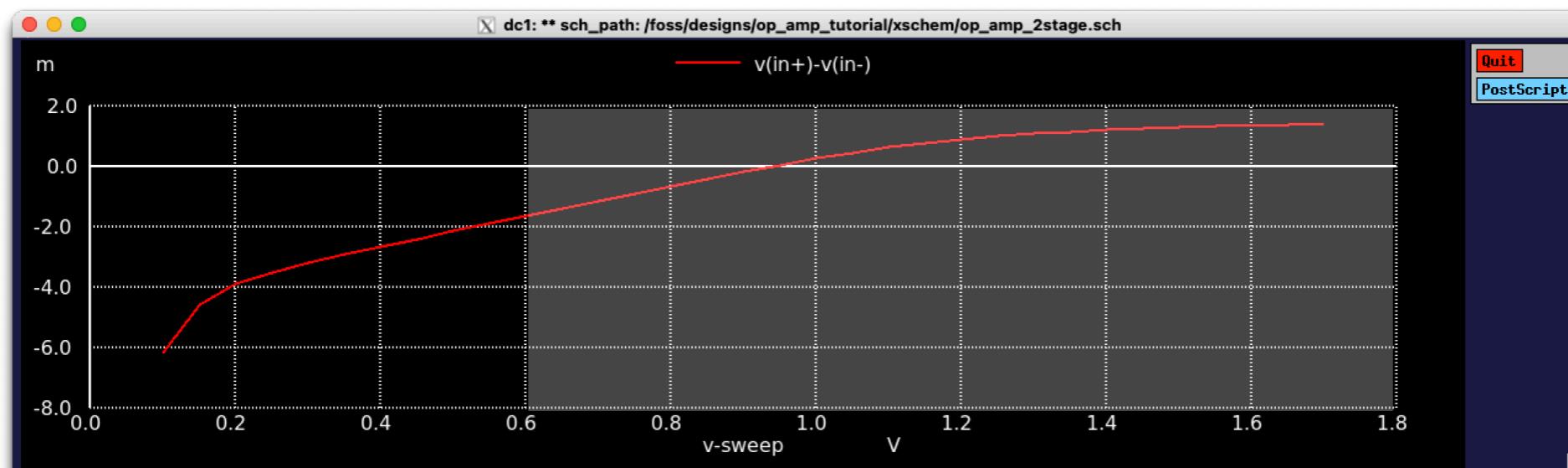
2 stage PMOS OpAMP - preliminary simulations



$v(\text{out})$, $v(\text{VDPWR})$, and $v(\text{common mode})$

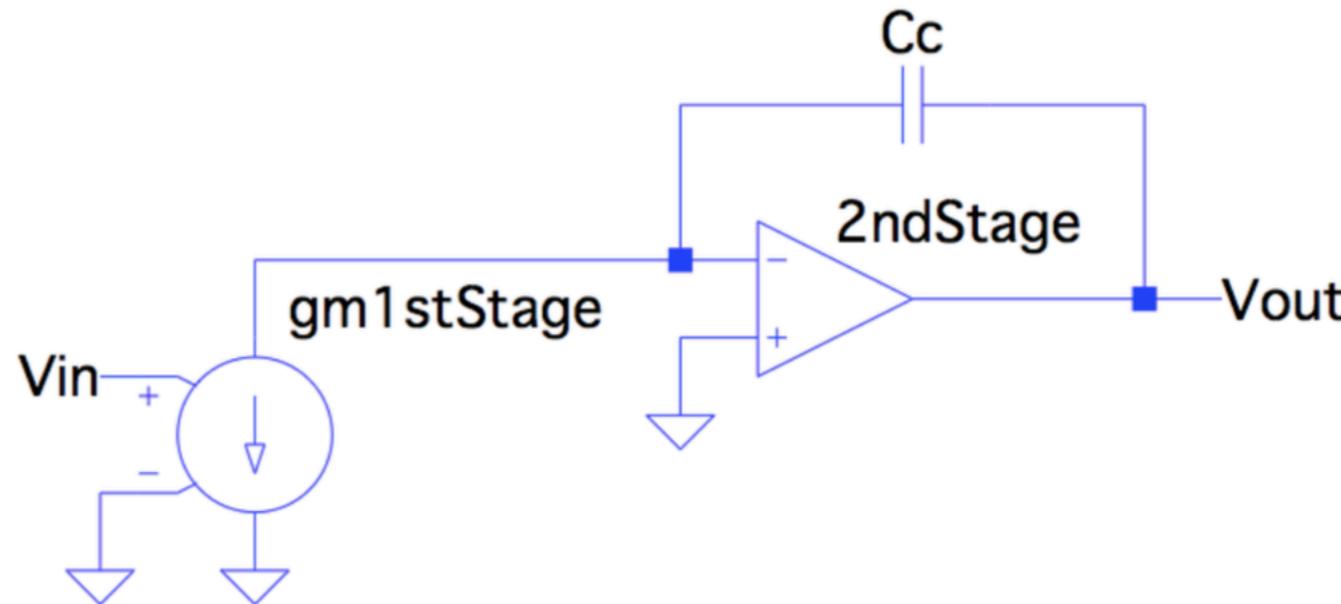
Ideal current source I4 is allowed to swing above the rail in simulation, but the common mode voltage will limit the input to $\approx 0.6\text{v}$ in the final circuit.

We will work on this later.



input error voltage vs output swing, $R_{\text{load}} = 800\Omega$ to mid supply

2 stage PMOS OpAmp - frequency compensation



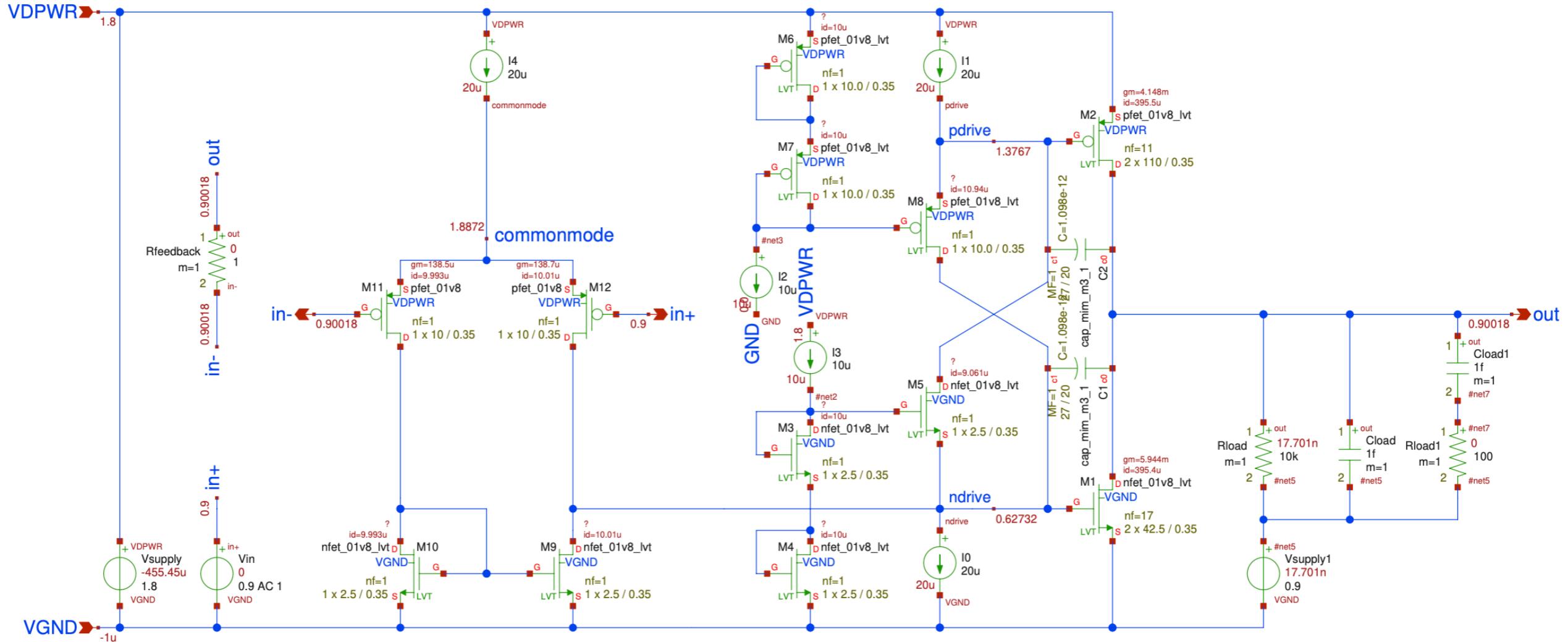
A simple 2 stage model helps us calculate frequency compensation values:

$$\frac{V_{out}}{V_{in}} = 1 = 2\pi GBW \frac{C_c}{g_m}$$

$$C_c = \frac{g_m}{2\pi GBW}$$

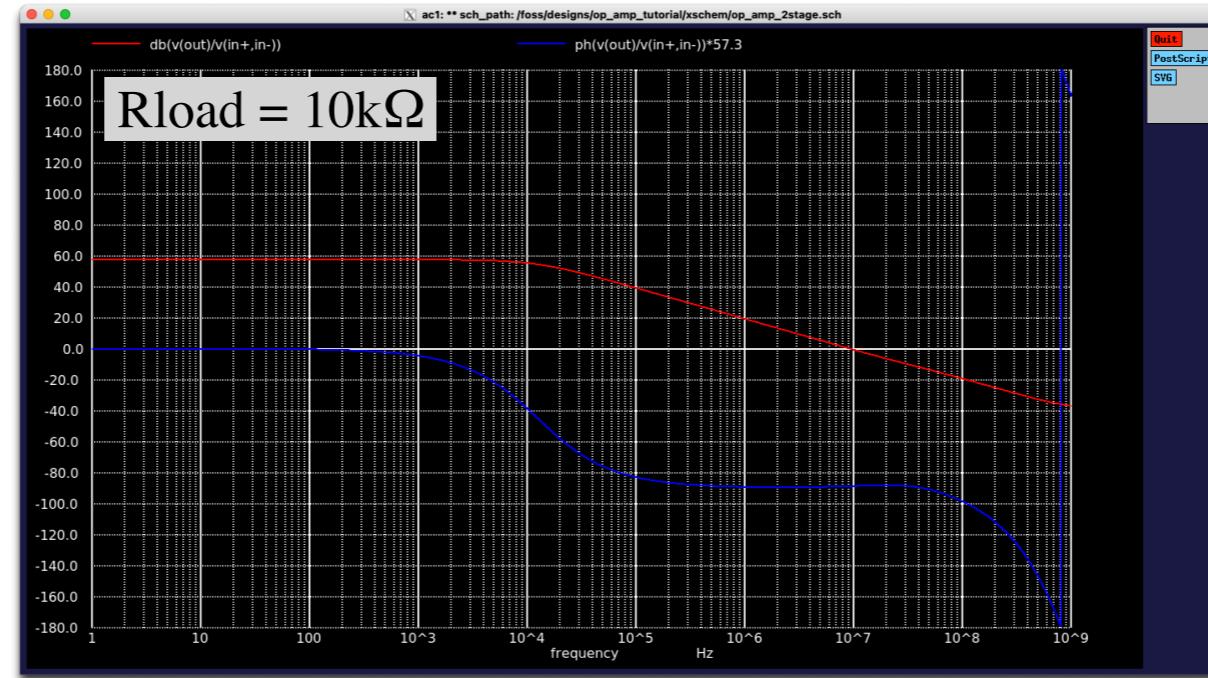
Our design with $g_m = 139\mu\text{S}$ and $\text{GBW} = 10\text{MHz}$ requires $C_c = 2.2\text{pF}$. We split the total C_c between the PMOS (1.1pF) and NMOS (1.1pF) output devices.

2 stage PMOS OpAmp w/ frequency compensation

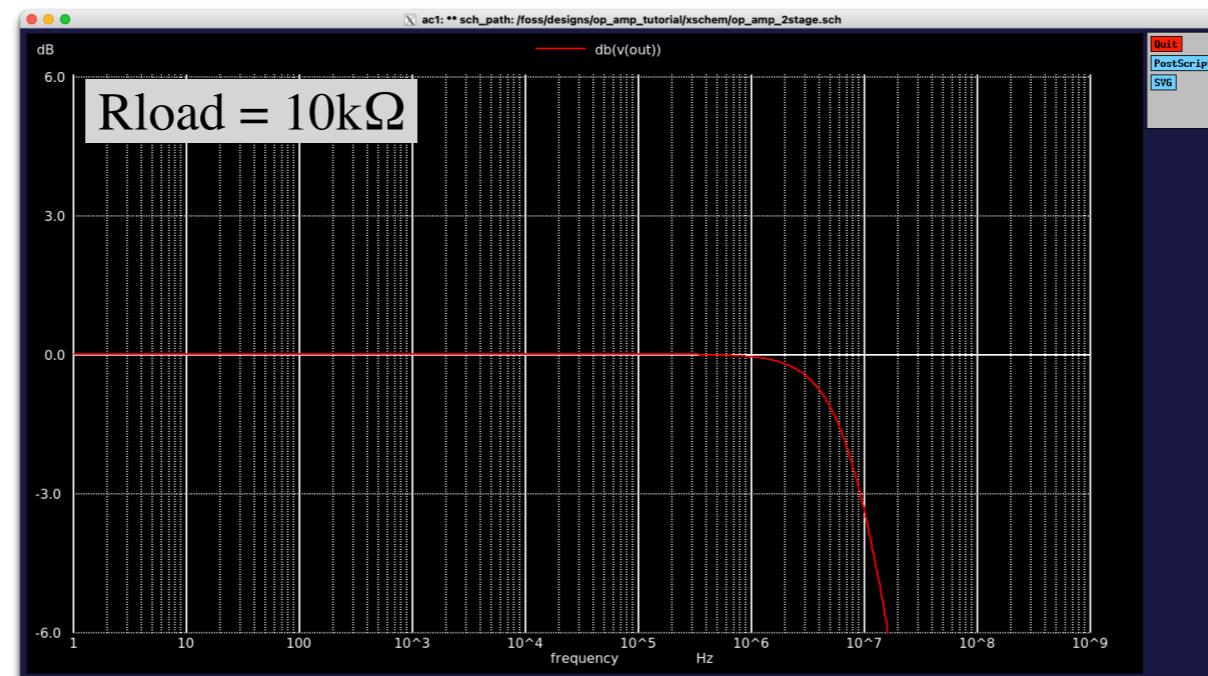


For our design $gm = 139\mu\text{A}$ and $\text{GBW} = 10\text{MHz}$ requires $C_c = 2.2\text{pF}$. We split the total C_c between the PMOS (1.1pF) and NMOS (1.1pF) output devices.

2 stage PMOS OpAMP - ac

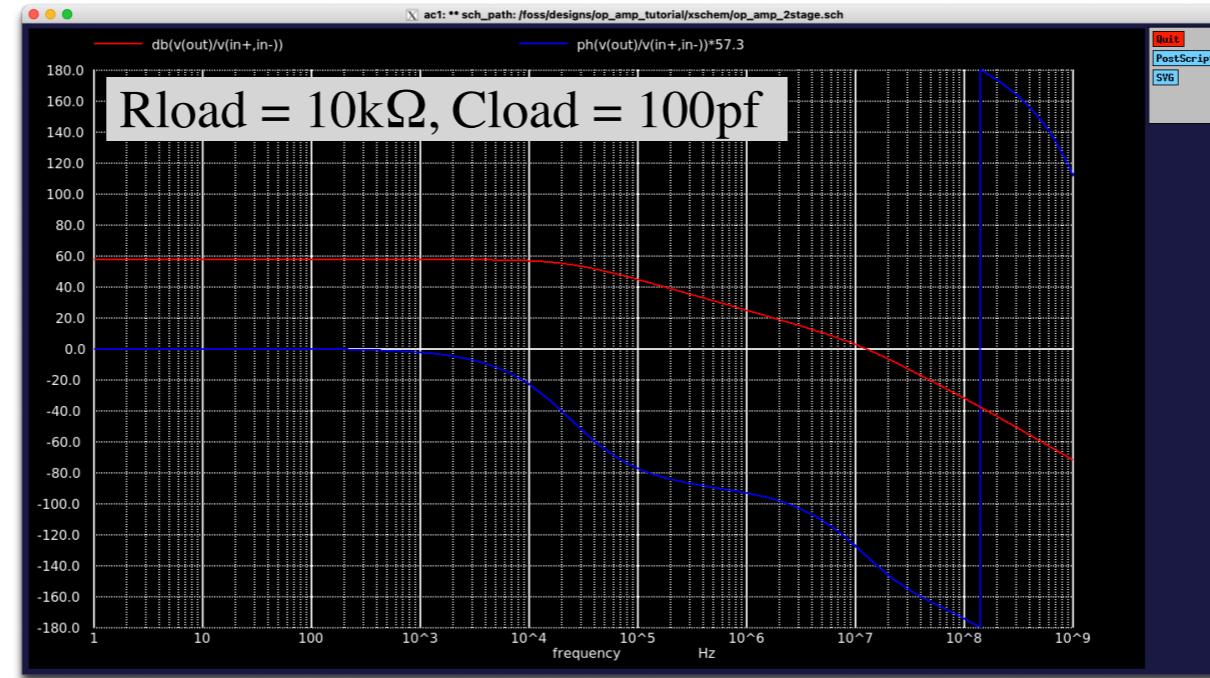


open loop gain $\approx 60\text{dB}$, GBW = 10MHz, phase margin = 90°

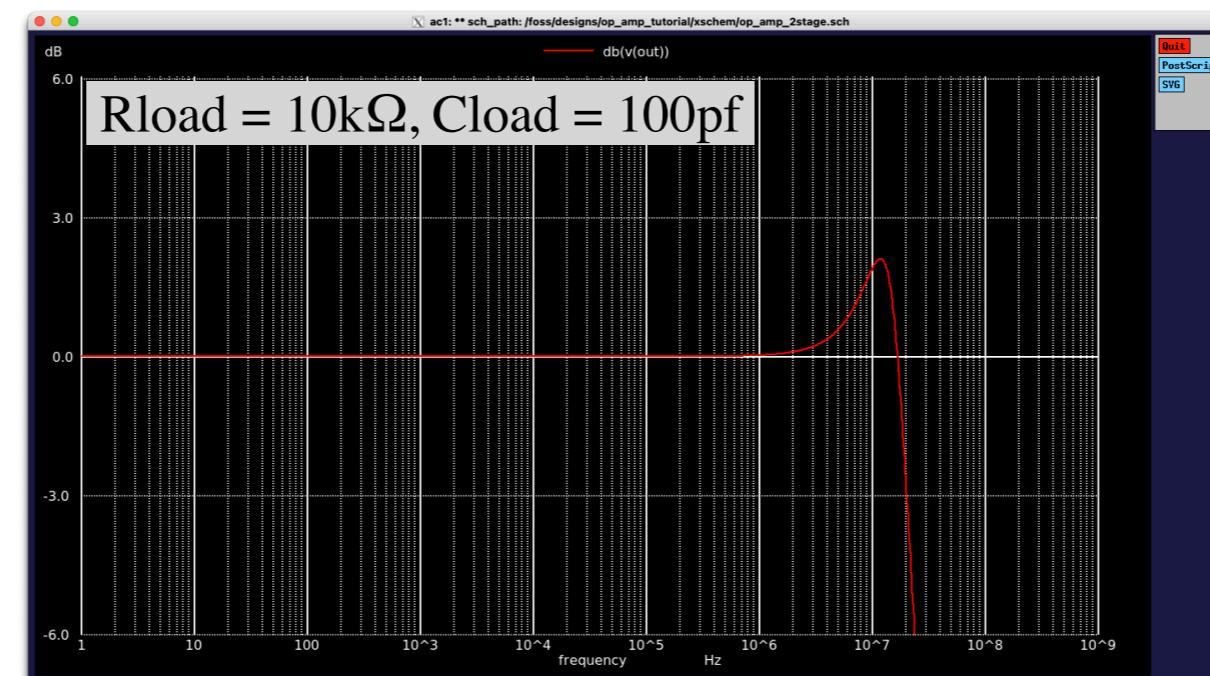


unity gain follower, -3dB @ 10MHz, no gain peaking

2 stage PMOS OpAmp - ac

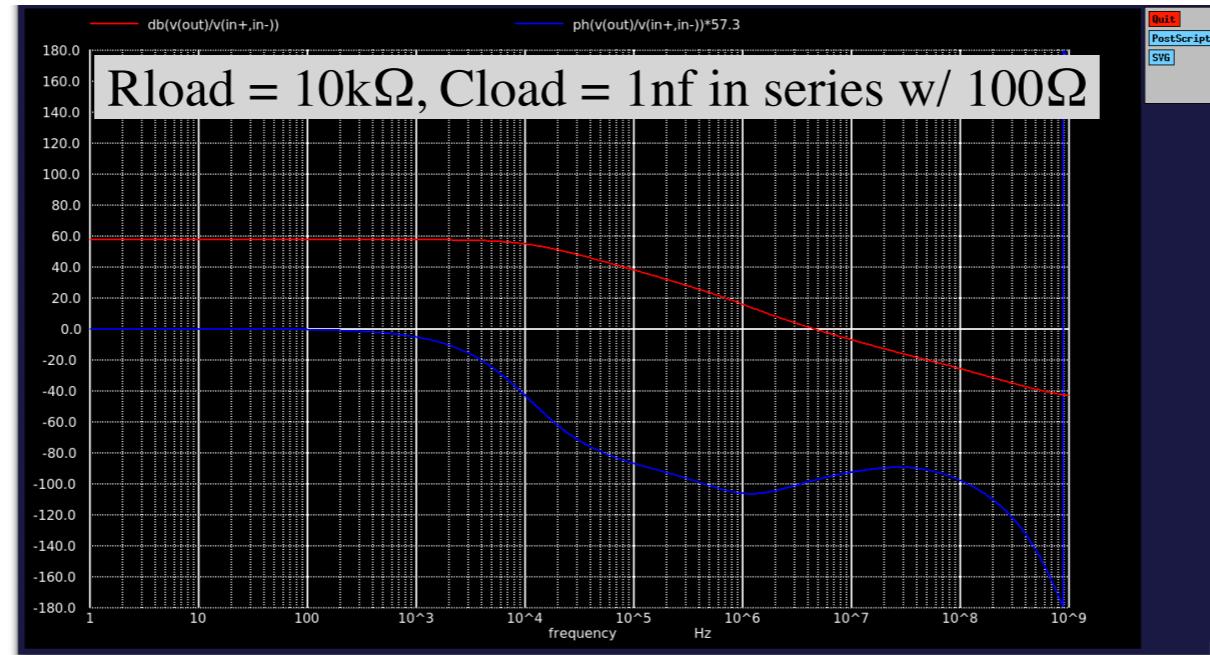


open loop gain $\approx 60\text{dB}$, GBW = 10MHz, phase margin = 50°

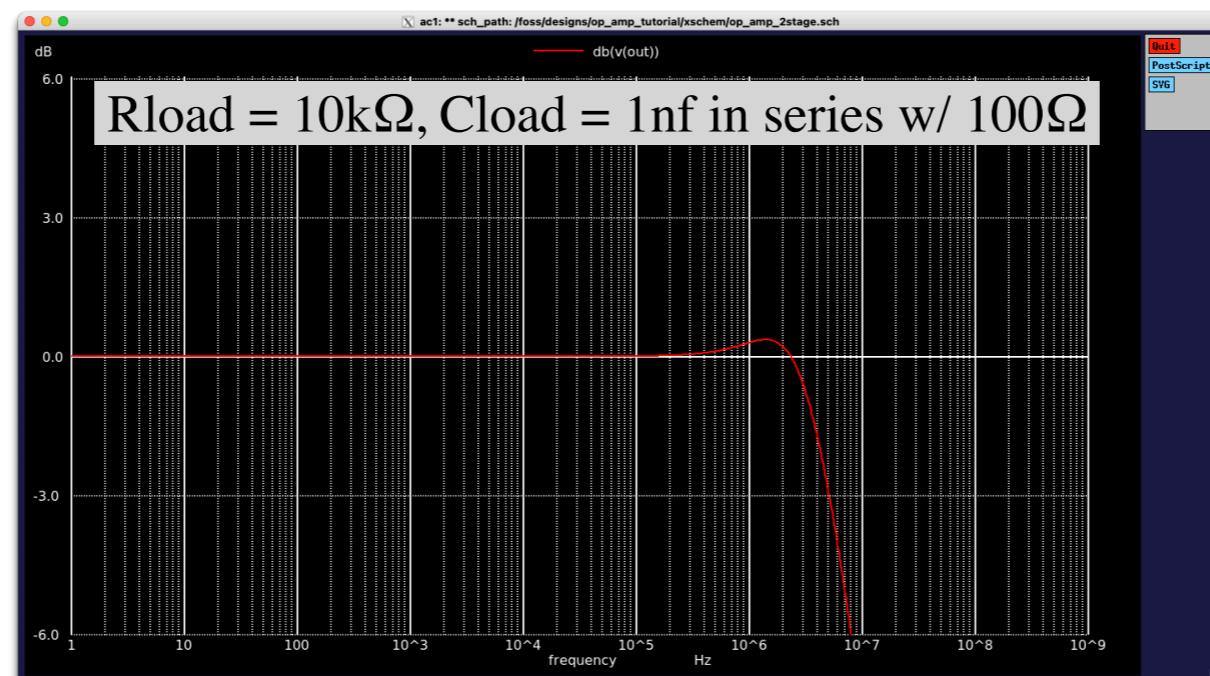


unity gain follower, -3dB @ 10MHz, gain peaking = 2dB

2 stage PMOS OpAmp - ac

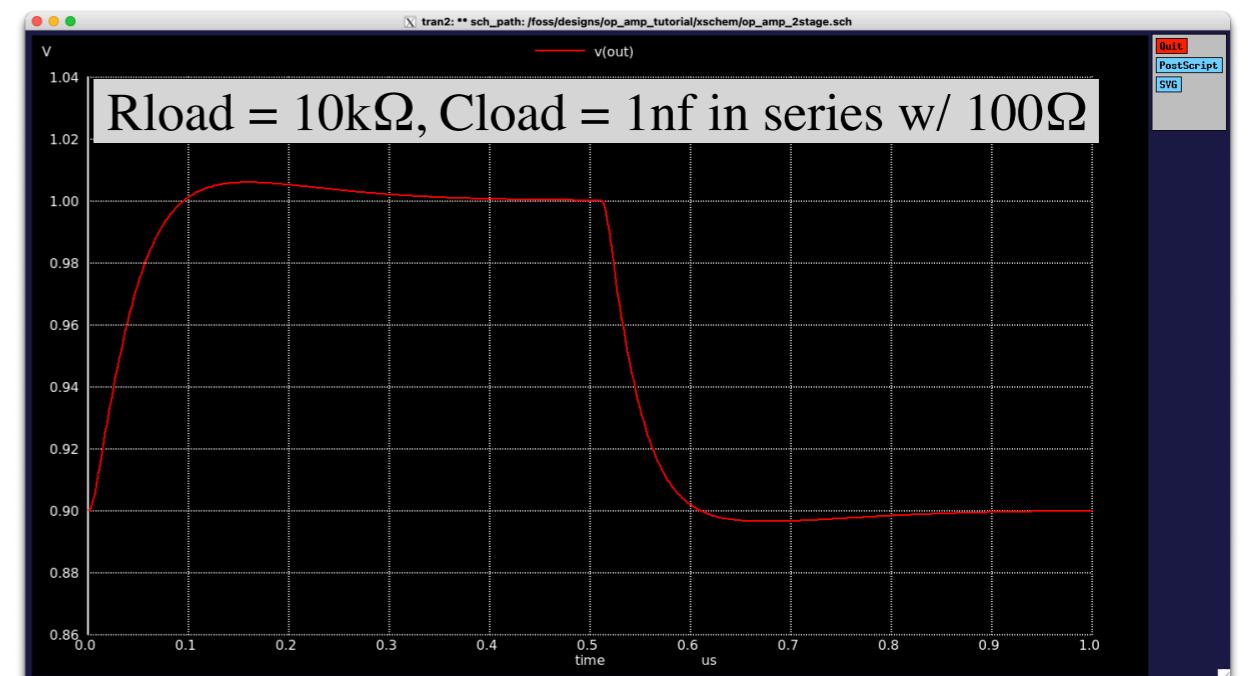
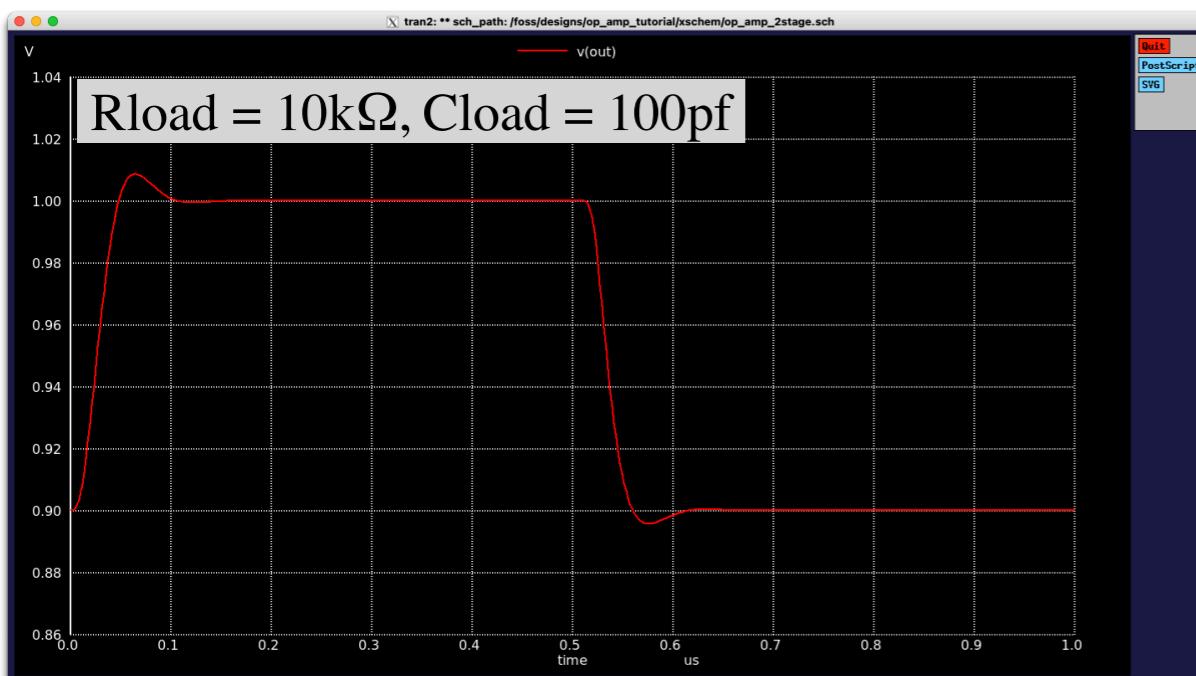
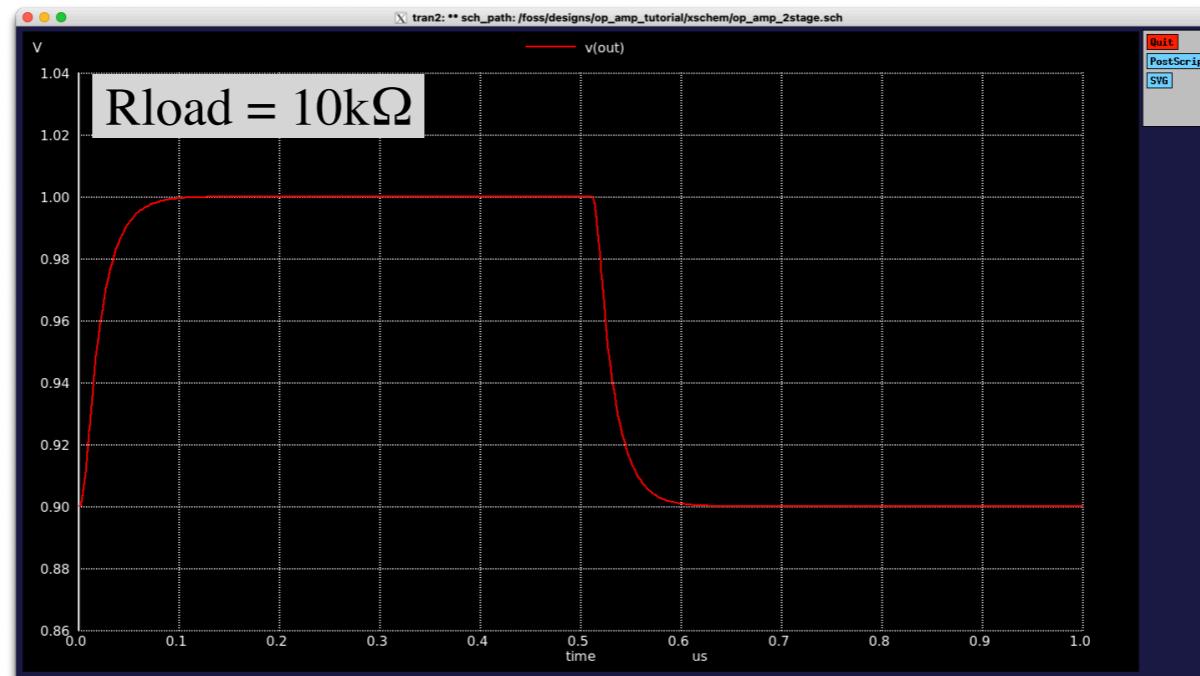


open loop gain $\approx 60\text{dB}$, GBW = 10MHz, phase margin = 80°

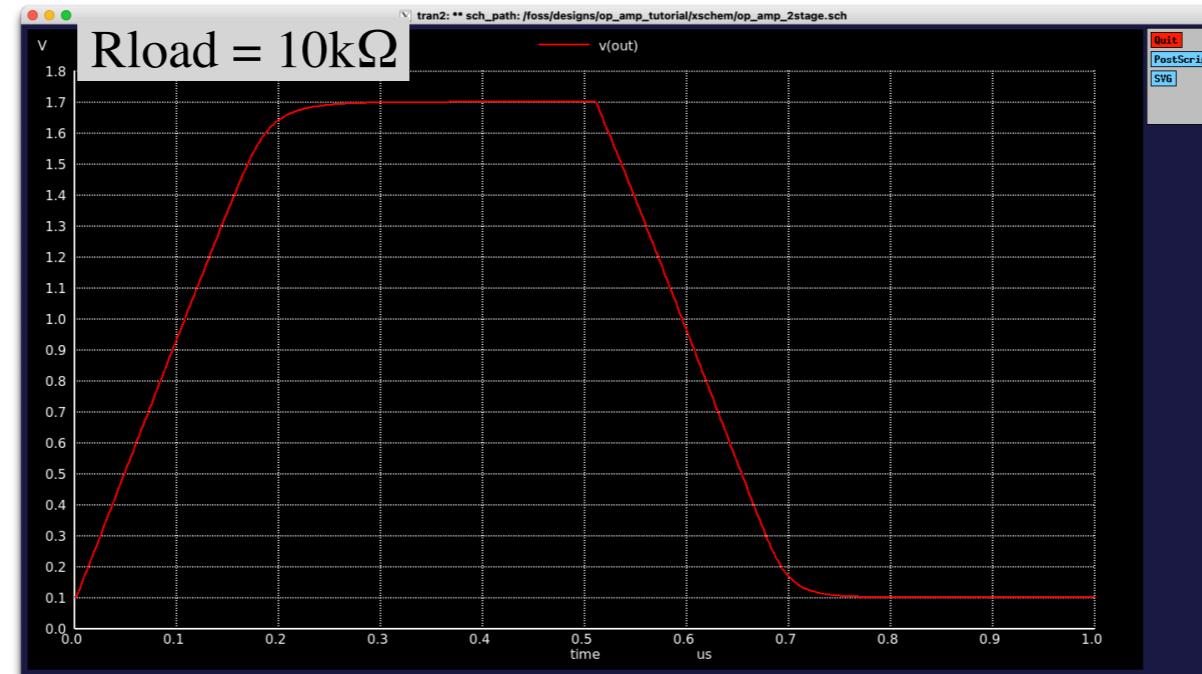


unity gain follower, $-3\text{dB} @ 5\text{MHz}$, gain peaking = 0.4dB

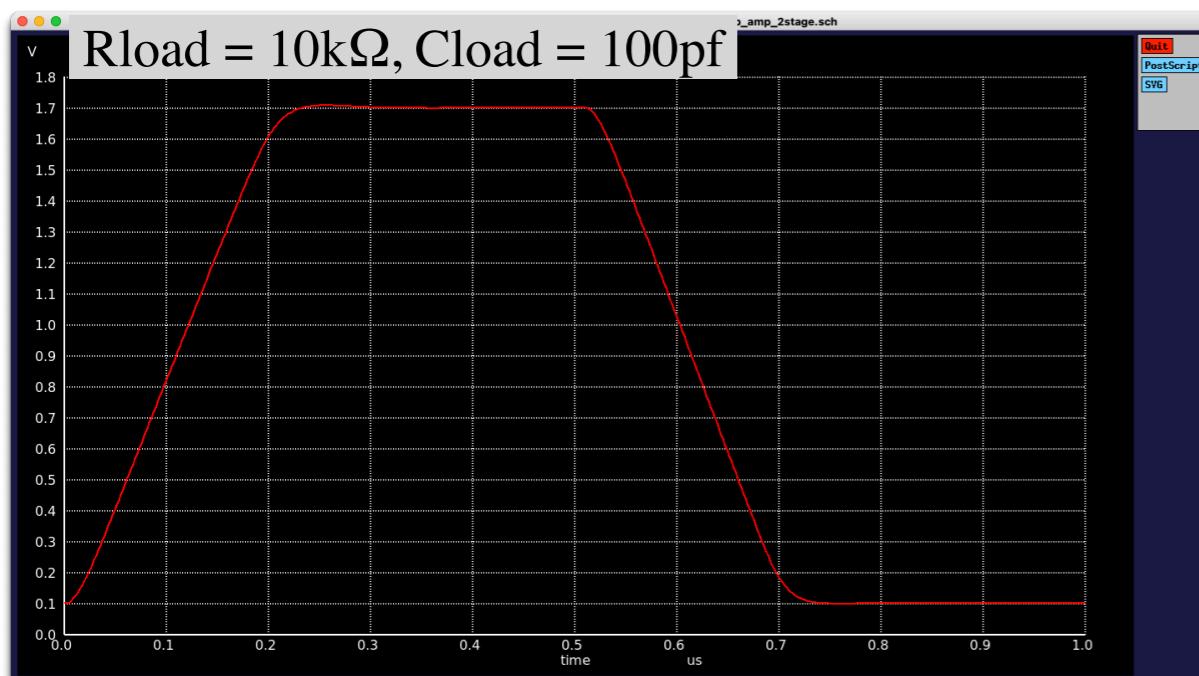
2 stage PMOS OpAmp - small signal step response



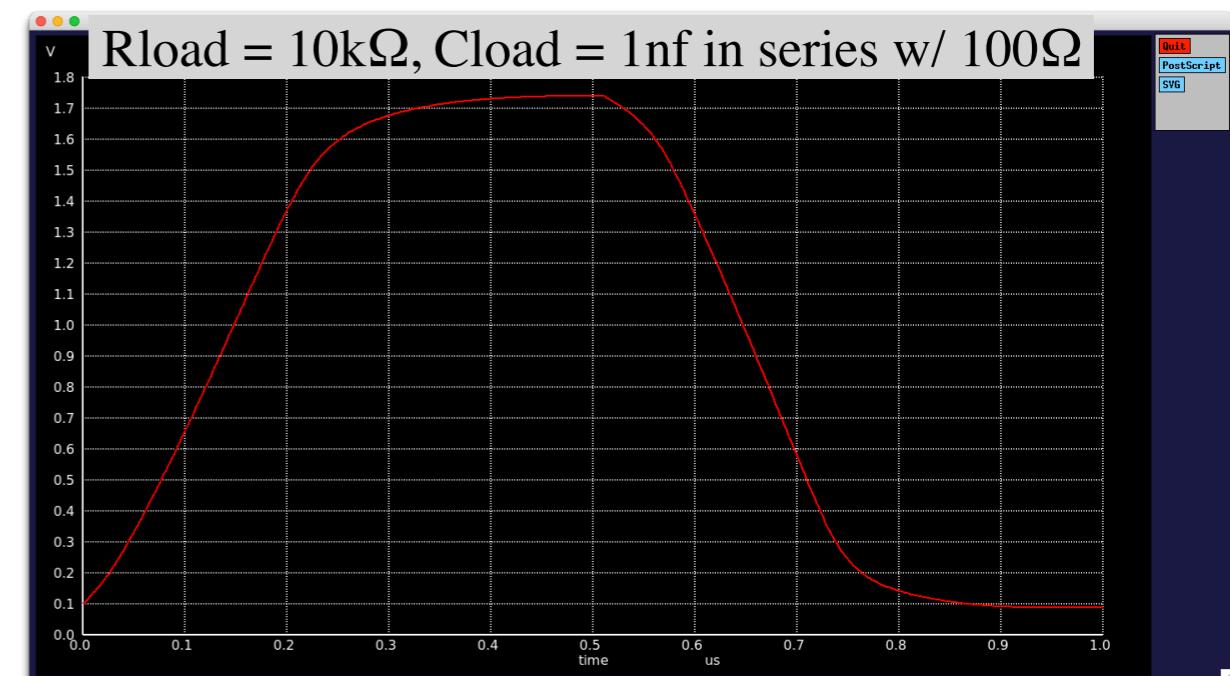
2 stage PMOS OpAmp - large signal step response



slew rate > 5V/us



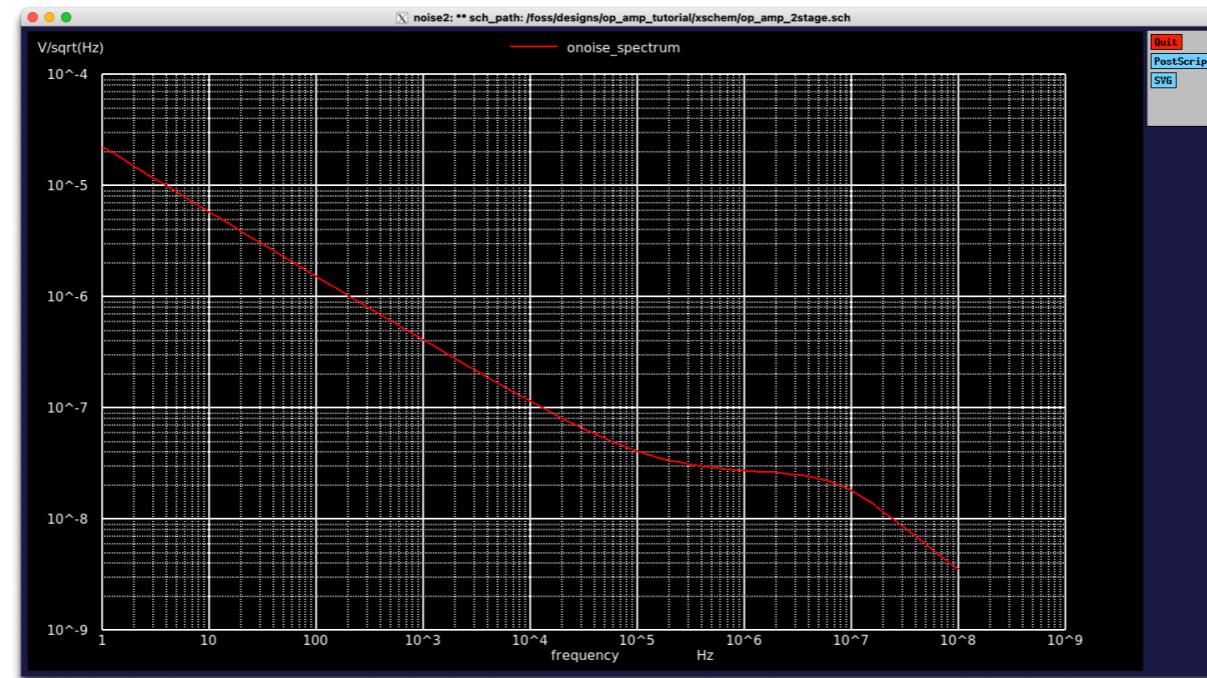
slew rate > 5V/us



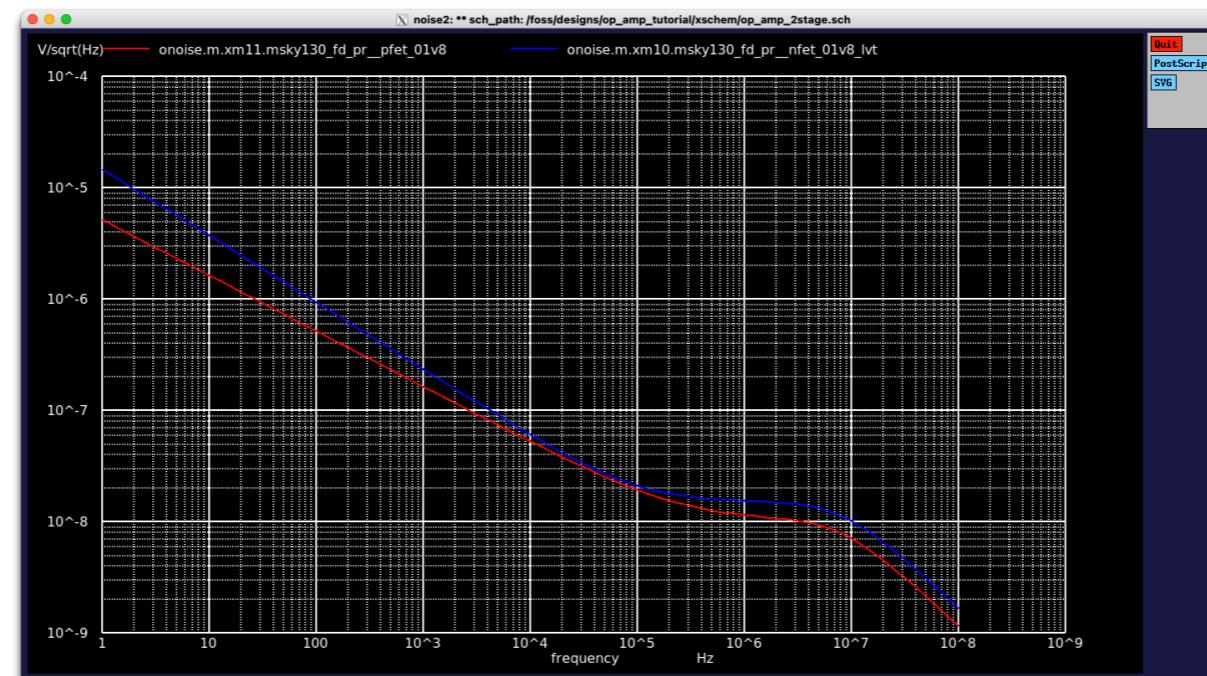
slew rate > 5V/us

note: I_{out} slew current to charge C_{load} is $\gg +/ - 1\text{mA}$ limits

2 stage PMOS OpAmp - noise



output noise in follower configuration (en), **too high!**



dominated by NMOS loads instead of PMOS input devices

2 stage PMOS OpAmp - summary

Limited input range.

DC open loop gain is low.

Noise is high and dominated by NMOS loads.

Offsets will also be high with small devices used in input stage.

Simulations over Process Voltage Temperature:

Low gain with $V_{out} = 100\text{mv}$ @ corner = fs and temp = 125°

Options for improvement:

- 1) Optimize devices, this could help a little.
- 2) Add another input stage, experience has shown that this will help a lot.

We will pick option #2 and evolve this into a 3 stage design.

3 stage PMOS OpAmp

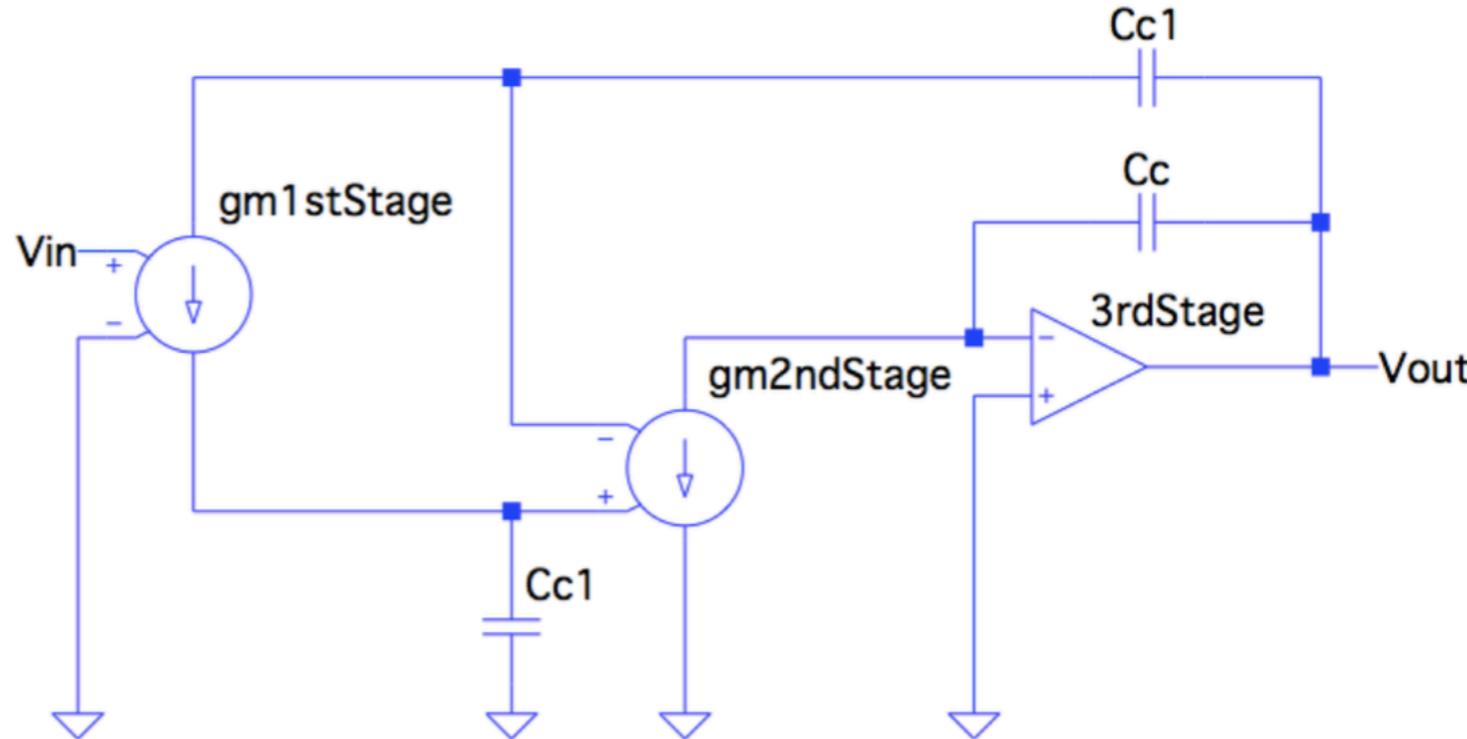
Let's create a precision OpAmp by adding another stage, **a new 1st stage.**

The new 1st stage needs higher stage current and larger input devices to meet the broadband noise requirements of $en = 10\text{nV}/\sqrt{\text{Hz}}$.

The NMOS loads should have lower gm 's compared to input PMOS devices to reduce their noise and offset reflected back to the input.

Both the inputs and loads should have much higher $W*L$ to reduce flicker noise and offset errors.

3 stage PMOS OpAmp - frequency compensation



A simple 3 stage model with a differential 1st stage helps us calculate frequency compensation values:

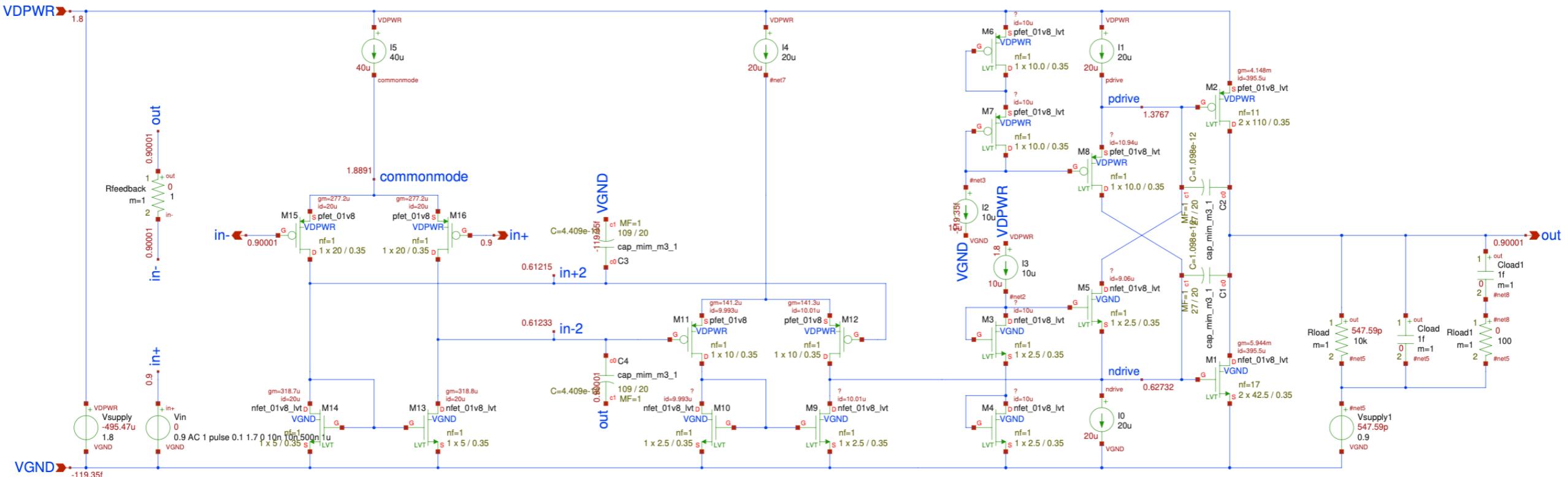
$$\frac{V_{out}}{V_{in}} = 1 = 2\pi GBW \frac{Cc1}{gm}$$

$$Cc1 = \frac{gm}{2\pi GBW}$$

This simple model ignores the roll off of the internal 2 stage OpAmp formed by gm2ndStage and Cc.

Our new 1st stage design with $gm = 277\mu\text{A}$ and $GBW = 10\text{MHz}$ requires $Cc1 = 4.4\text{pF}$.

3 stage PMOS OpAmp



For our design $gm = 277\mu\text{A}$ and $\text{GBW} = 10\text{MHz}$ requires $C_{c1} = 4.4\text{pF}$.

3 stage PMOS OpAMP - ac

DC open loop gain is improved.

GBW = 10MHz

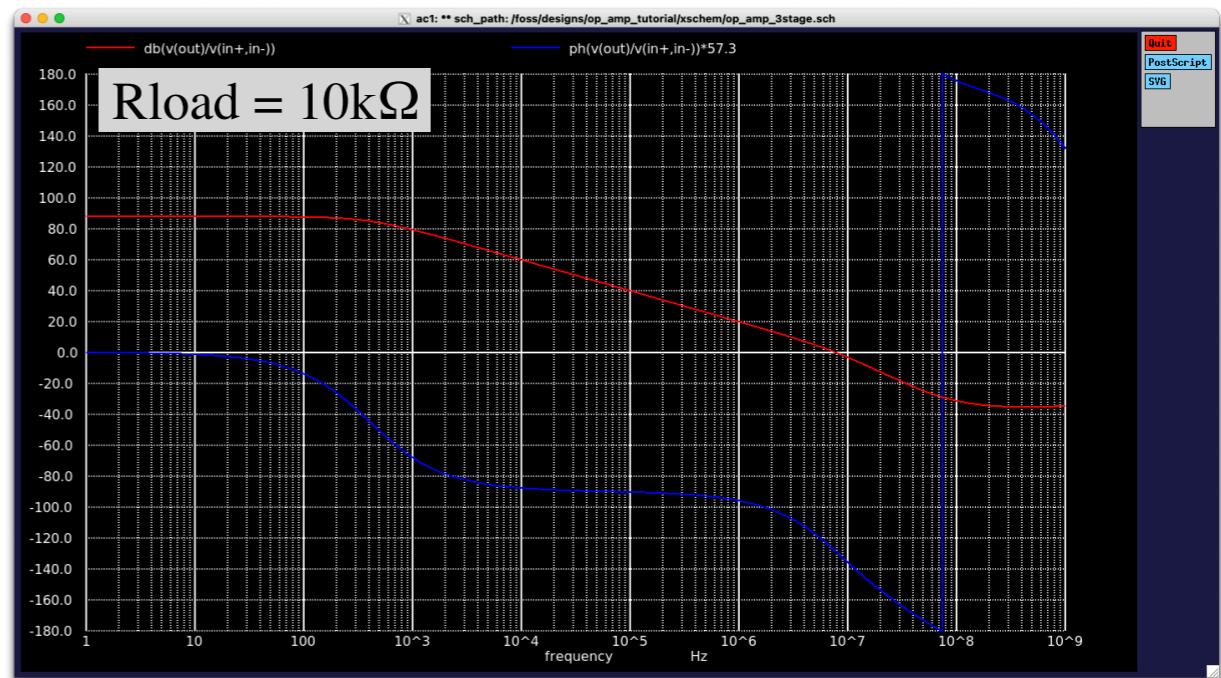
unity gain crossover = 8MHz

phase margin = 50°

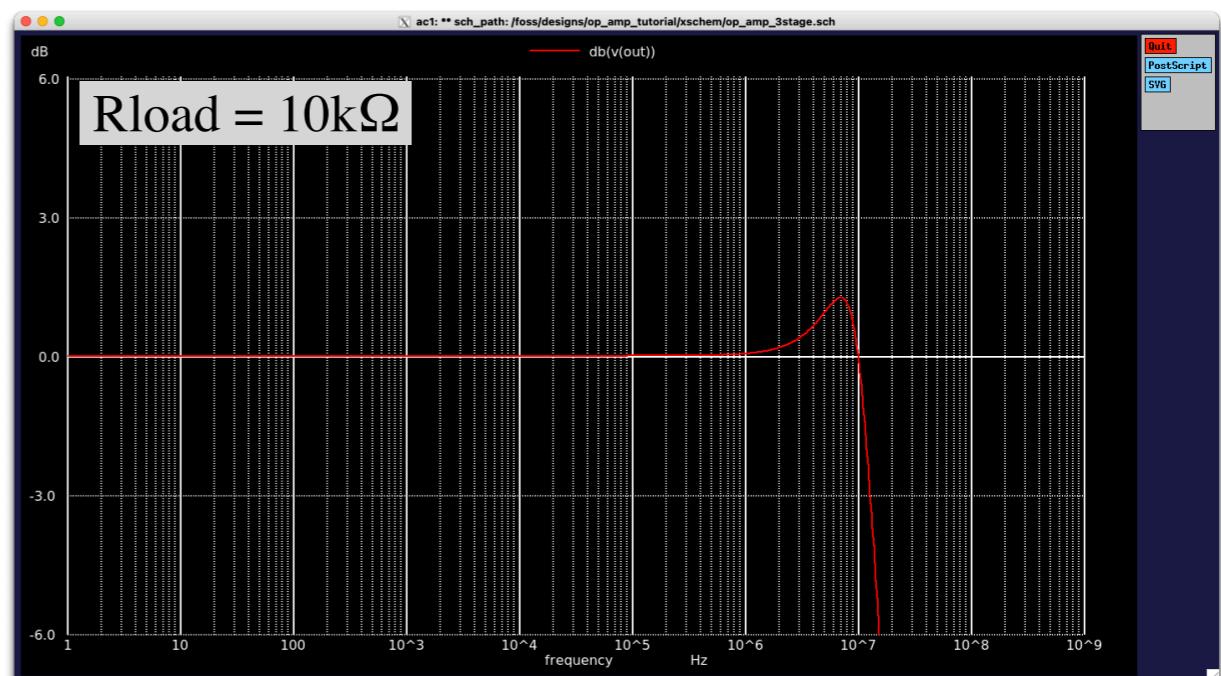
gain peaking = 1dB

The 2 stage amplifier runs out of loop gain at 10MHz creating another pole in the overall response!

Need to change the compensation of the 2 stage amplifier for a GBW = 20MHz, 1 octave beyond the overall GBW. Change C1 and C2 to 0.55pf.



open loop gain ≈ 86dB, GBW = 10MHz, phase margin = 50°



unity gain follower, -3dB @ 10MHz, gain peaking = 1dB

3 stage PMOS OpAMP - ac

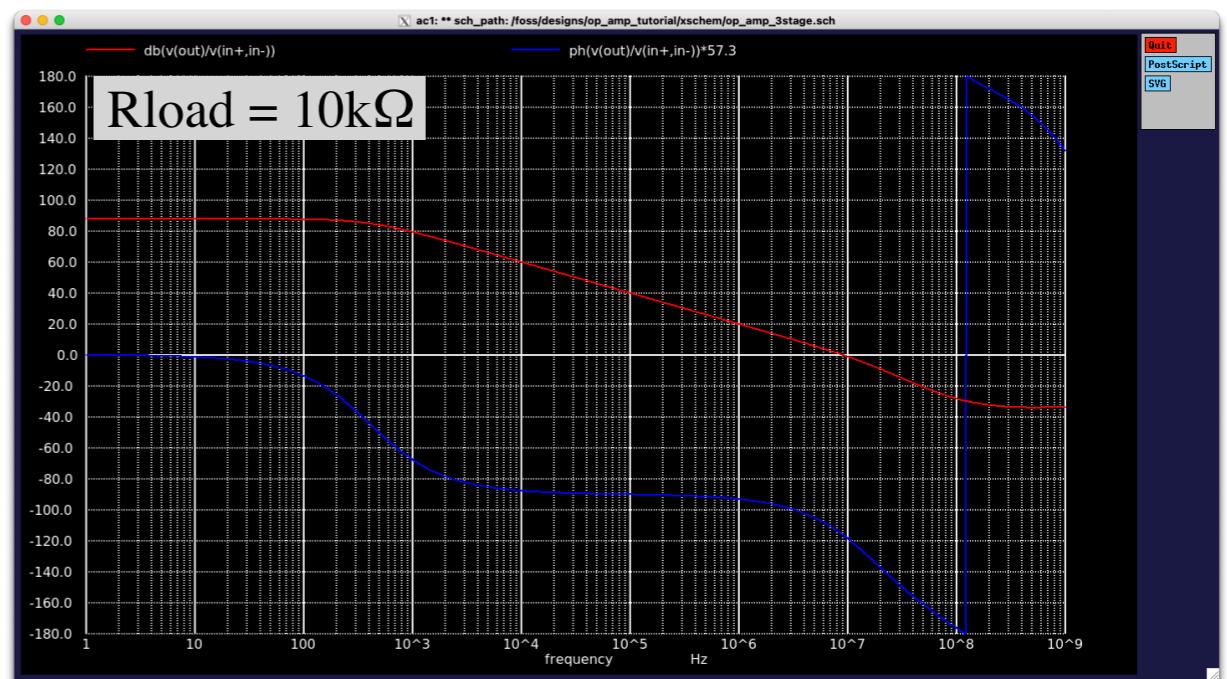
With C1 and C2 changed to 0.55pf.

GBW = 10MHz

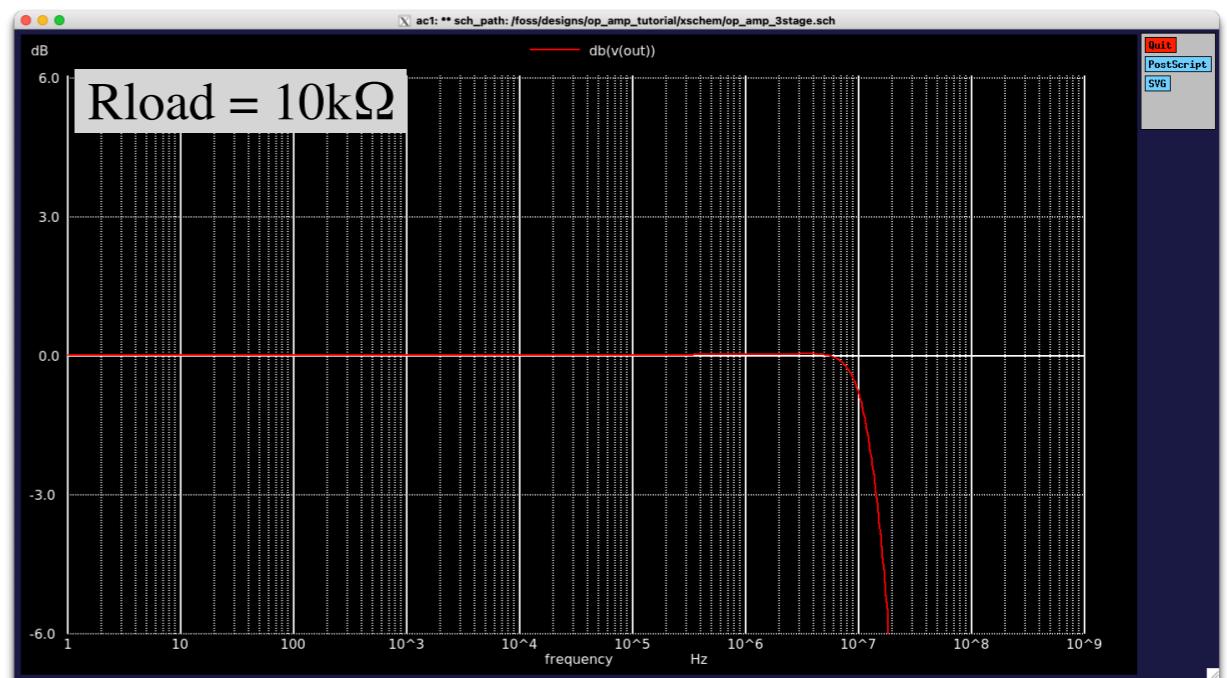
unity gain crossover = 9MHz

phase margin = 60°

no gain peaking



open loop gain ≈ 86 dB, GBW = 10MHz, phase margin = 60°

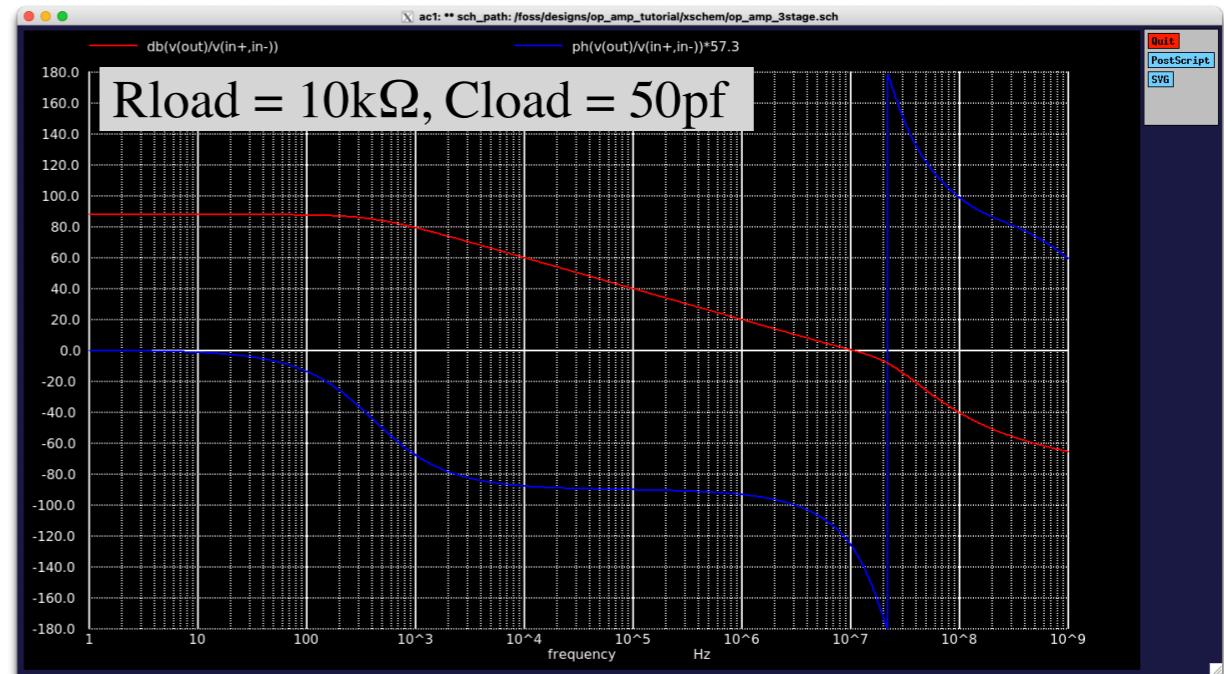


unity gain follower, -3dB @ 10MHz, no gain peaking

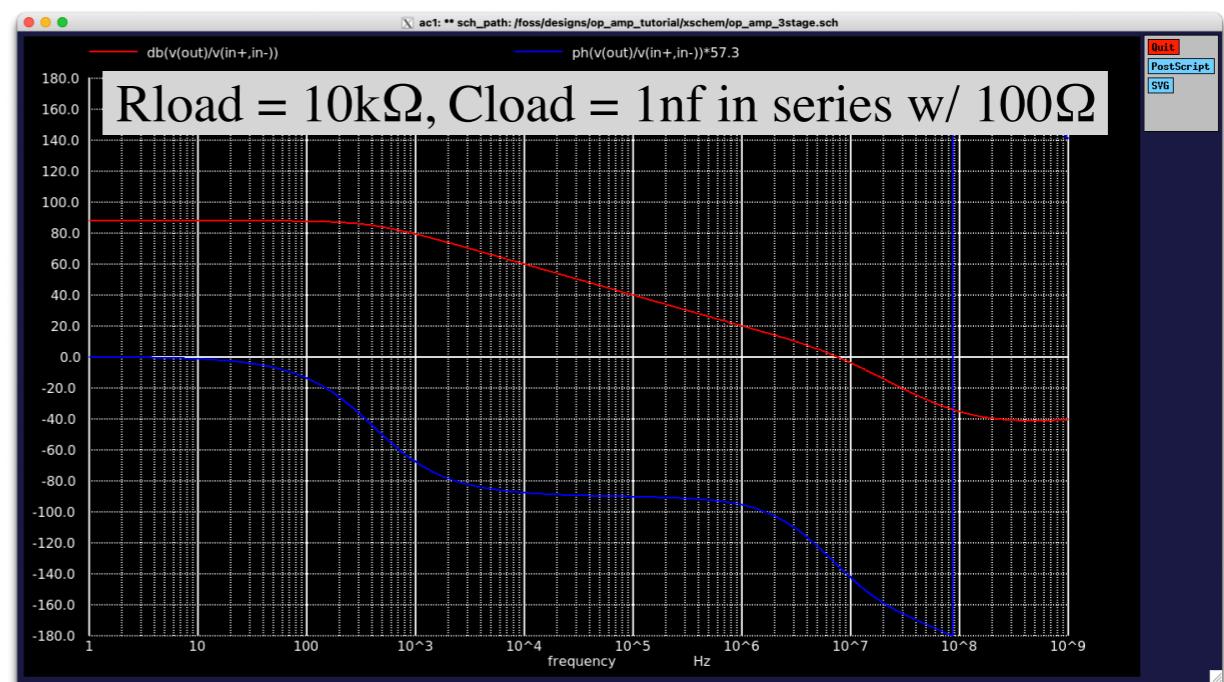
3 stage PMOS OpAMP - ac

With **C1** and **C2** changed to **0.55pf**.

Check 2 stage amplifier's new frequency compensation stability with load.

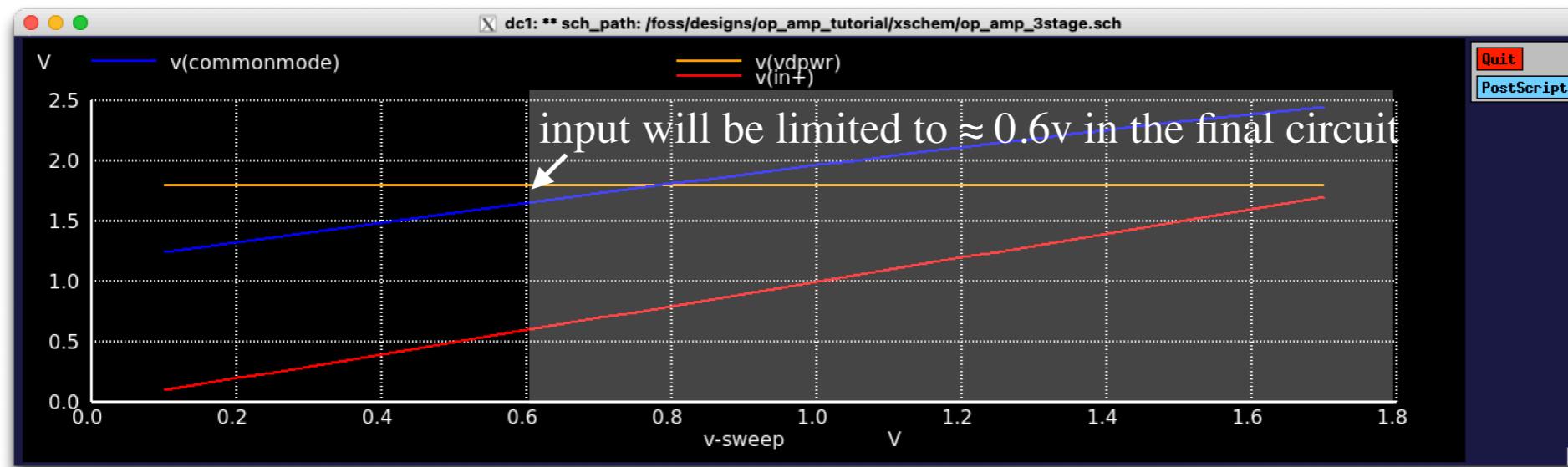


unity gain crossover = 10MHz, phase margin = 50°



unity gain crossover = 8MHz, phase margin = 50°

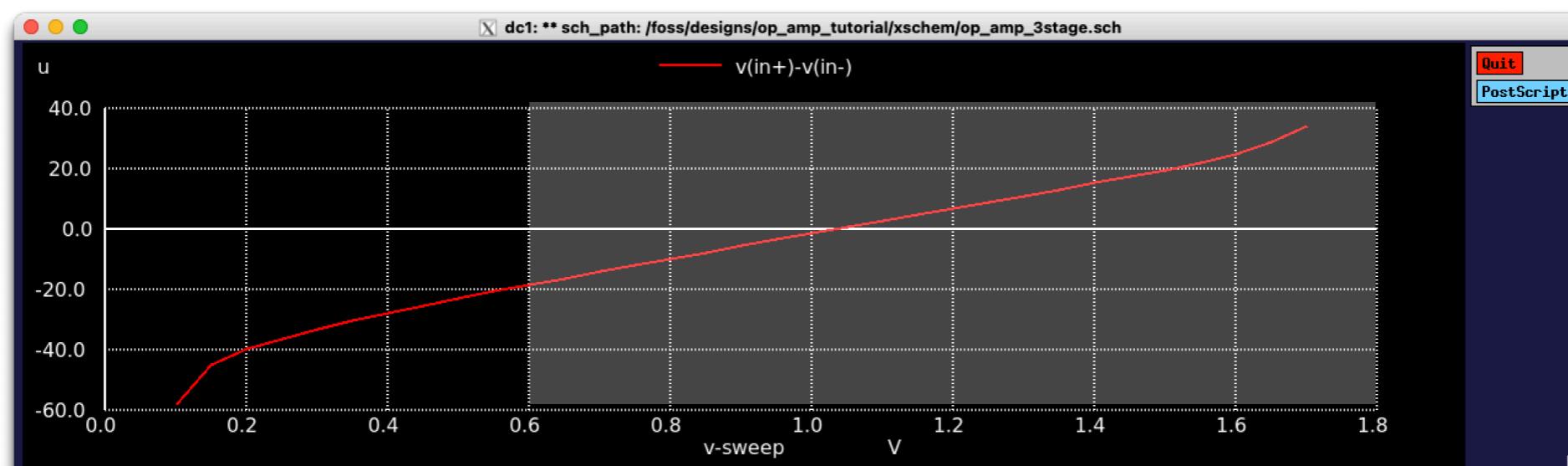
3 stage PMOS OpAMP - common mode range



v(out), v(VDPWR), and v(common mode)

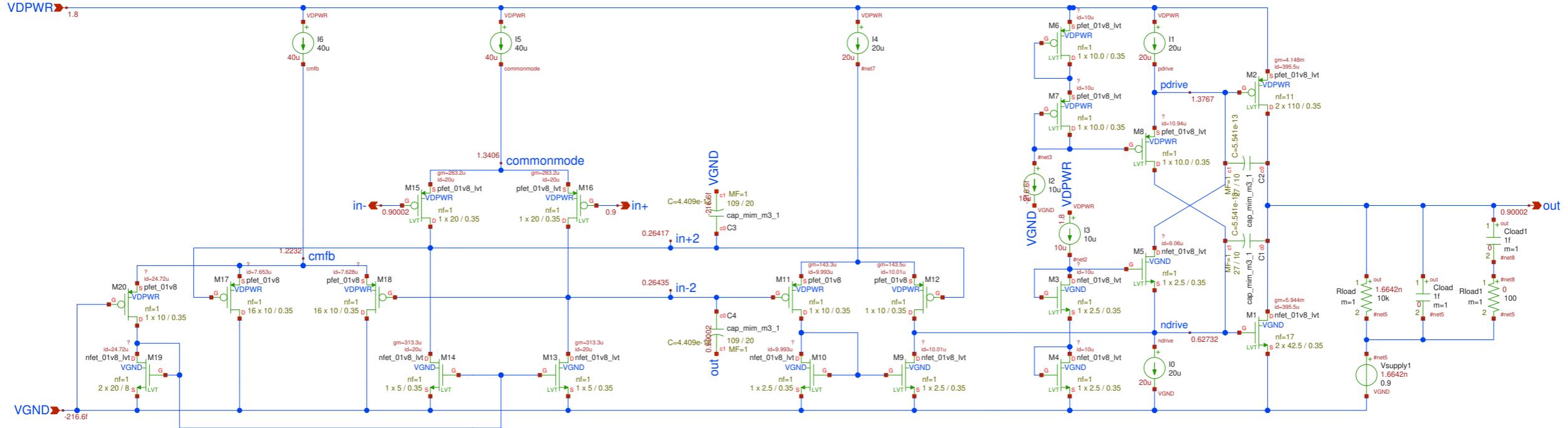
Ideal current source I5 is allowed to swing above the rail in simulation, but the common mode voltage will limit the input to $\approx 0.6v$ in the final circuit.

The input stage needs to be modified to improve this!



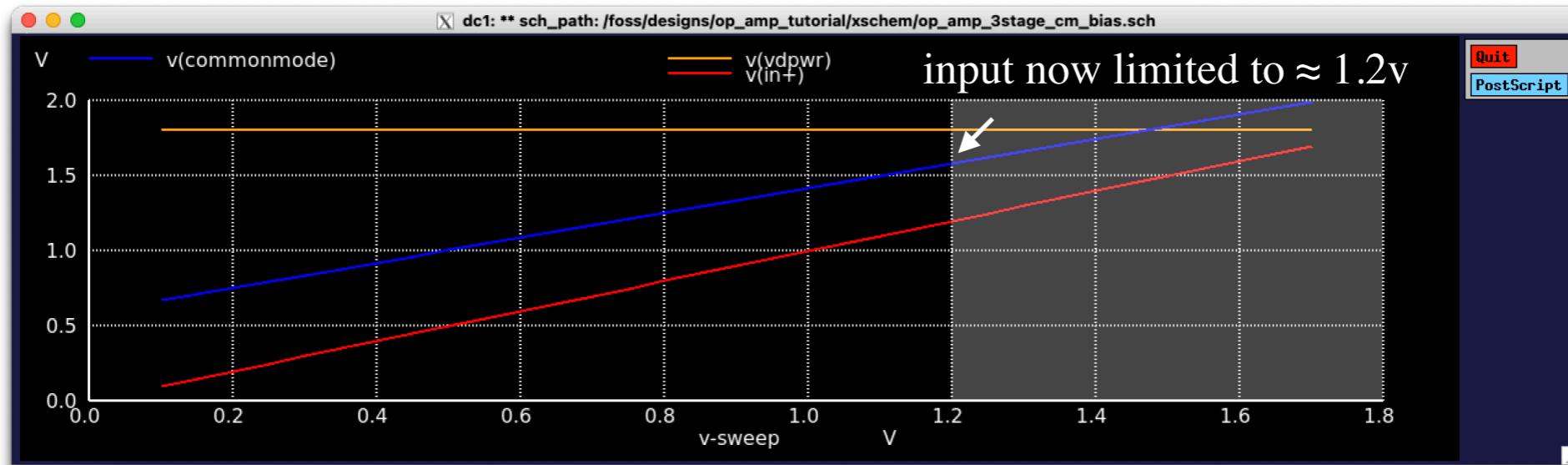
input error voltage vs output swing, Rload = 10k Ω to mid supply

3 stage PMOS OpAmp with improved common mode range



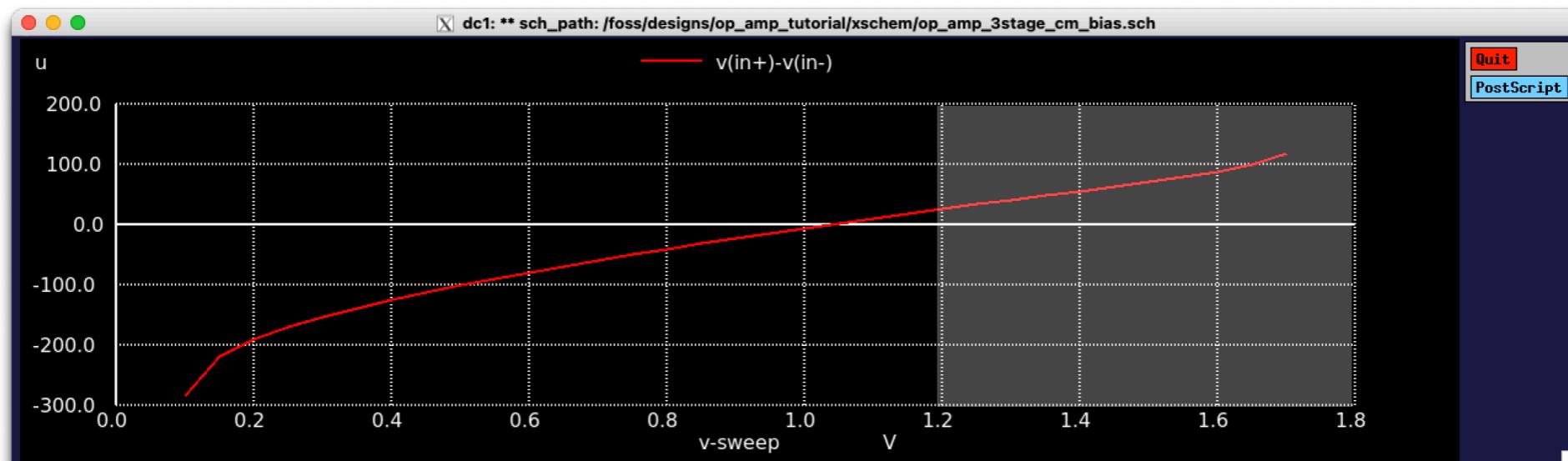
Input PMOS devices M15 and M16 are changed to low threshold devices for improved range to the positive rail. However, this creates a vdsat issue at the negative rail. Common mode feedback (CMFB) is added to bias NMOS input loads M13 and M14 to fix the vdsat issue. The CMFB loop is formed by devices M17, M18, M19, and M20.

3 stage PMOS OpAMP with improved common mode range



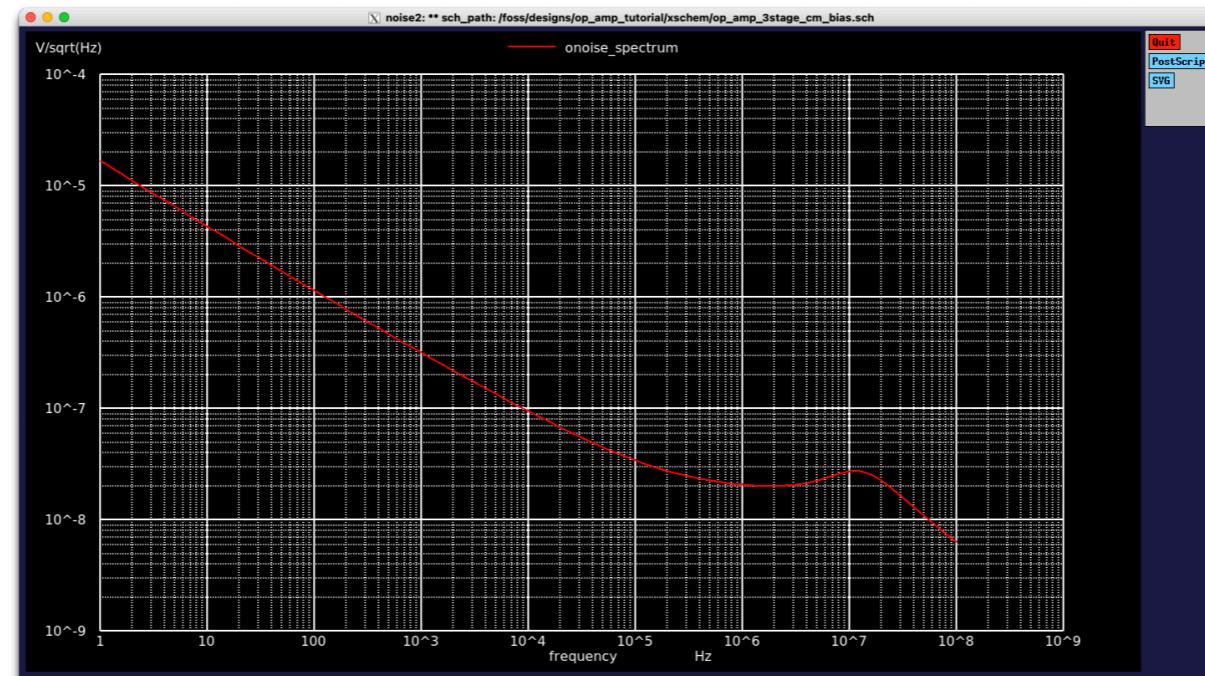
$v(\text{out})$, $v(\text{VDPWR})$, and $v(\text{common mode})$

Ideal current source I5 is allowed to swing above the rail in simulation,
but the common mode voltage will limit the input to $\approx 1.2\text{v}$ in the final circuit.

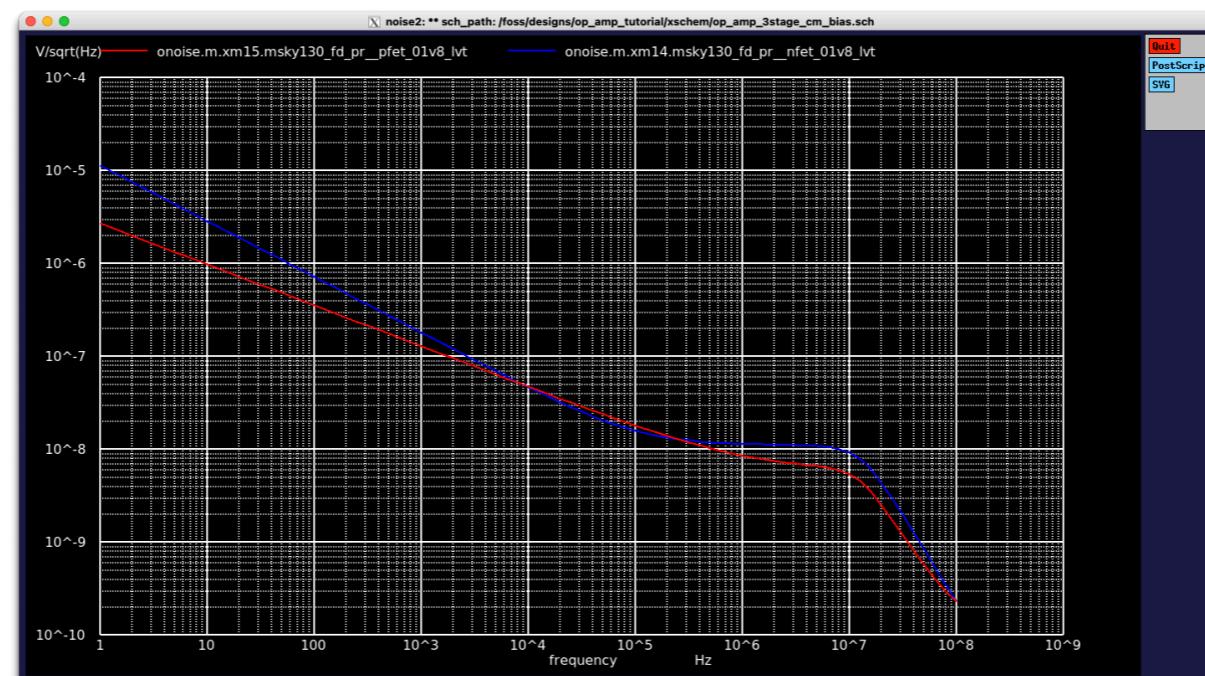


input error voltage vs output swing, $R_{\text{load}} = 10\text{k}\Omega$ to mid supply

3 stage PMOS OpAmp - noise

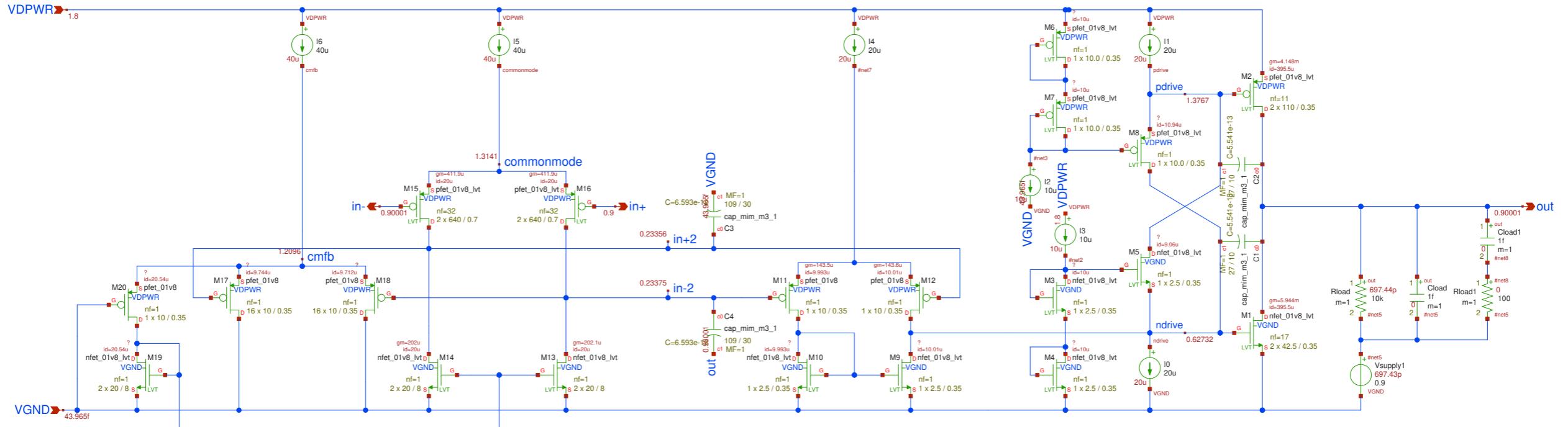


output noise in follower configuration (en), **too high!**



dominated by NMOS loads instead of PMOS input devices

3 stage PMOS OpAmp - final version

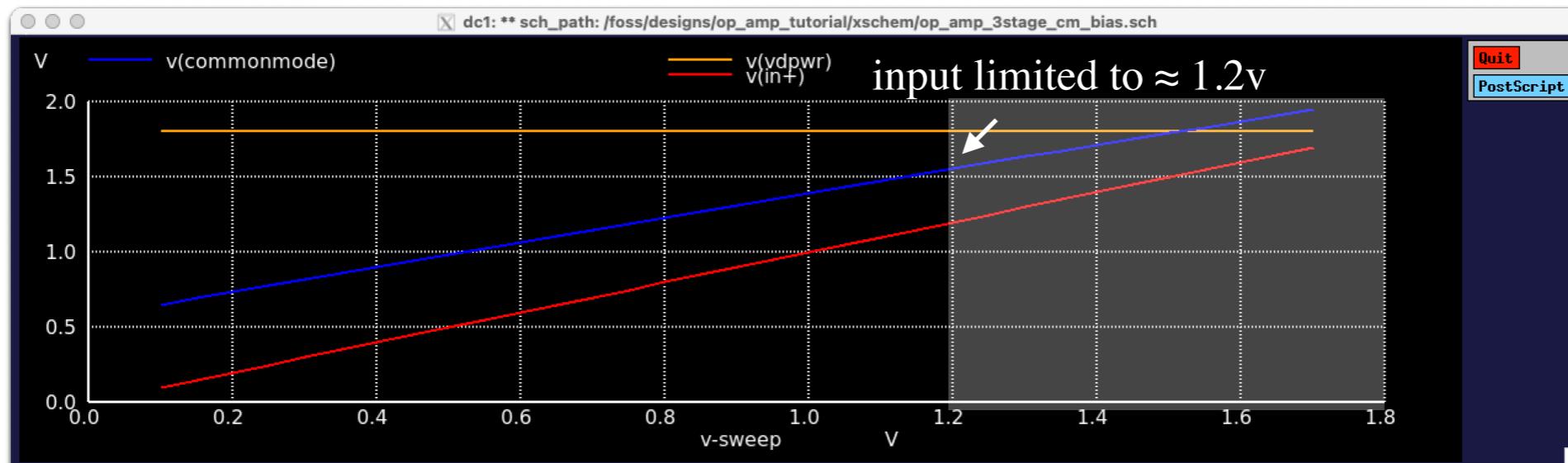


Optimized input:

M15 and M16 W/L's are increased for higher gm to reduce broadband noise. The contribution of M13 and M14 noise and offsets are also reduced due to ratio of gm's. C3 and C4 are increased to reflect gm change.

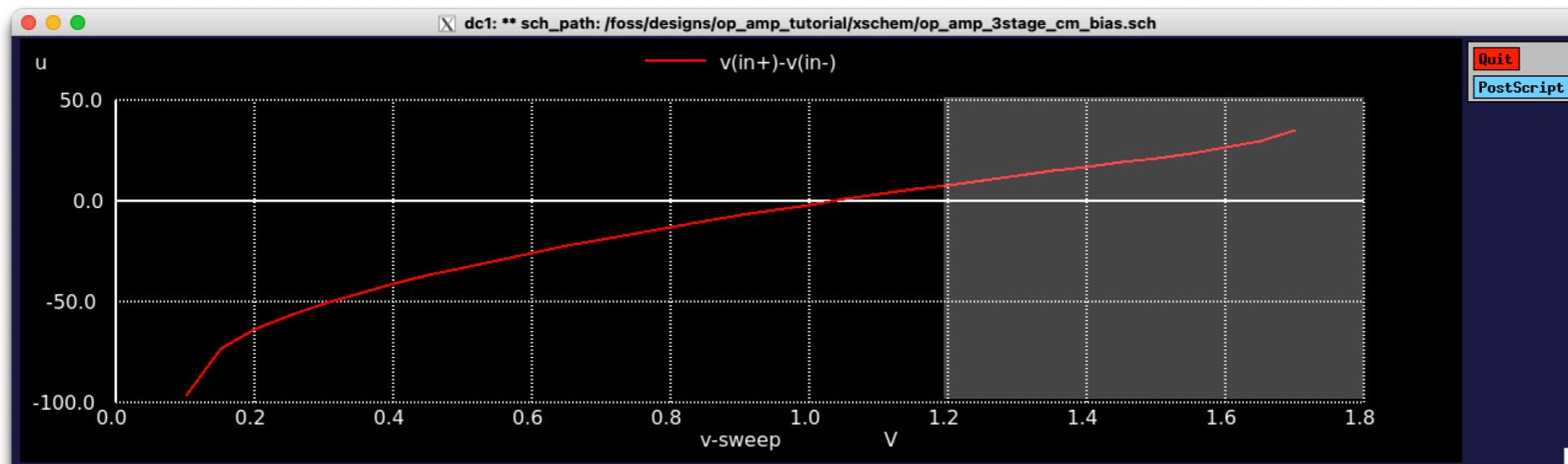
M15, M16, M13, and M14 W*L's are increased to reduce flicker noise and offsets. The increase of L's also increases DC open loop gain.

3 stage PMOS OpAMP - final sims



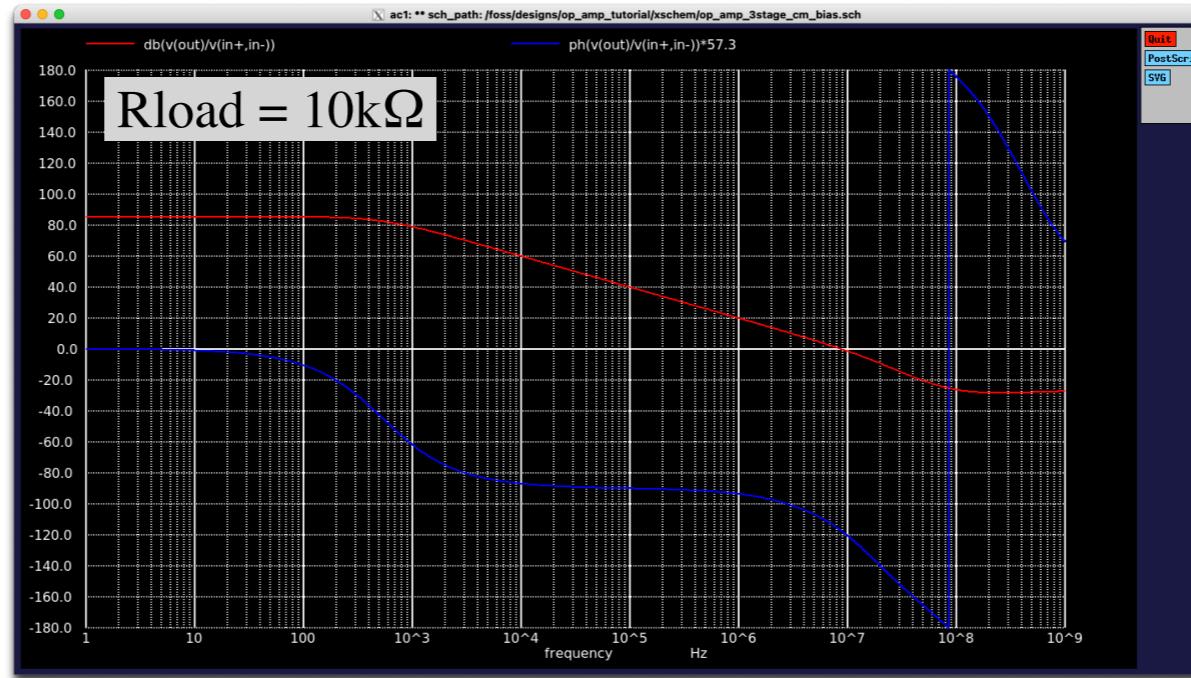
$v(\text{out})$, $v(\text{VDPWR})$, and $v(\text{common mode})$

Ideal current source I5 is allowed to swing above the rail in simulation,
but the common mode voltage will limit the input to $\approx 1.2\text{V}$ in the final circuit.

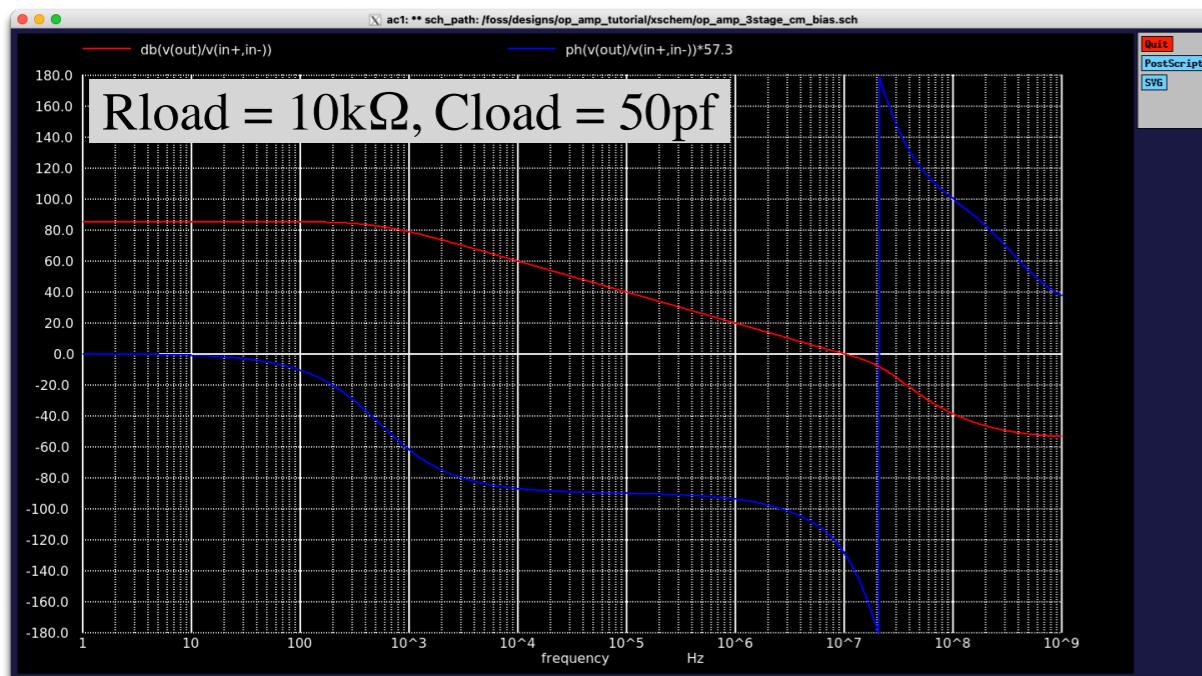


input error voltage vs output swing, $R_{\text{load}} = 10\text{k}\Omega$ to mid supply

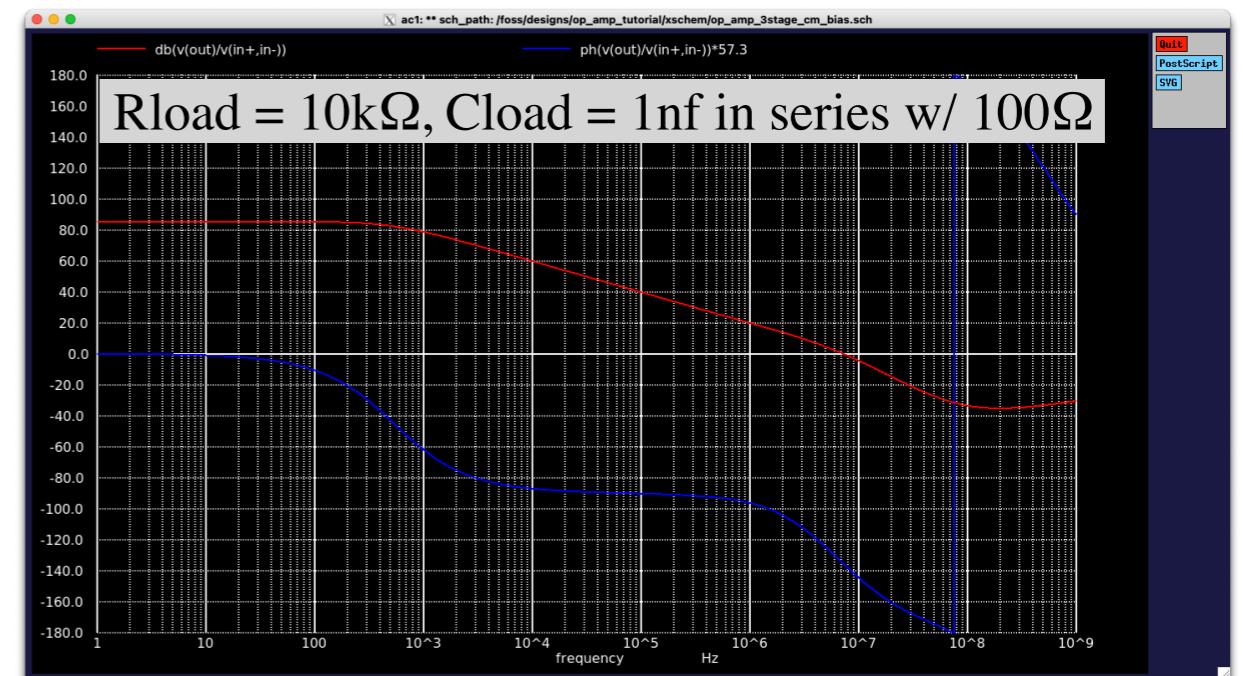
3 stage PMOS OpAMP - final sims - ac



open loop gain $\approx 85\text{dB}$, GBW = 10MHz, phase margin = 60°

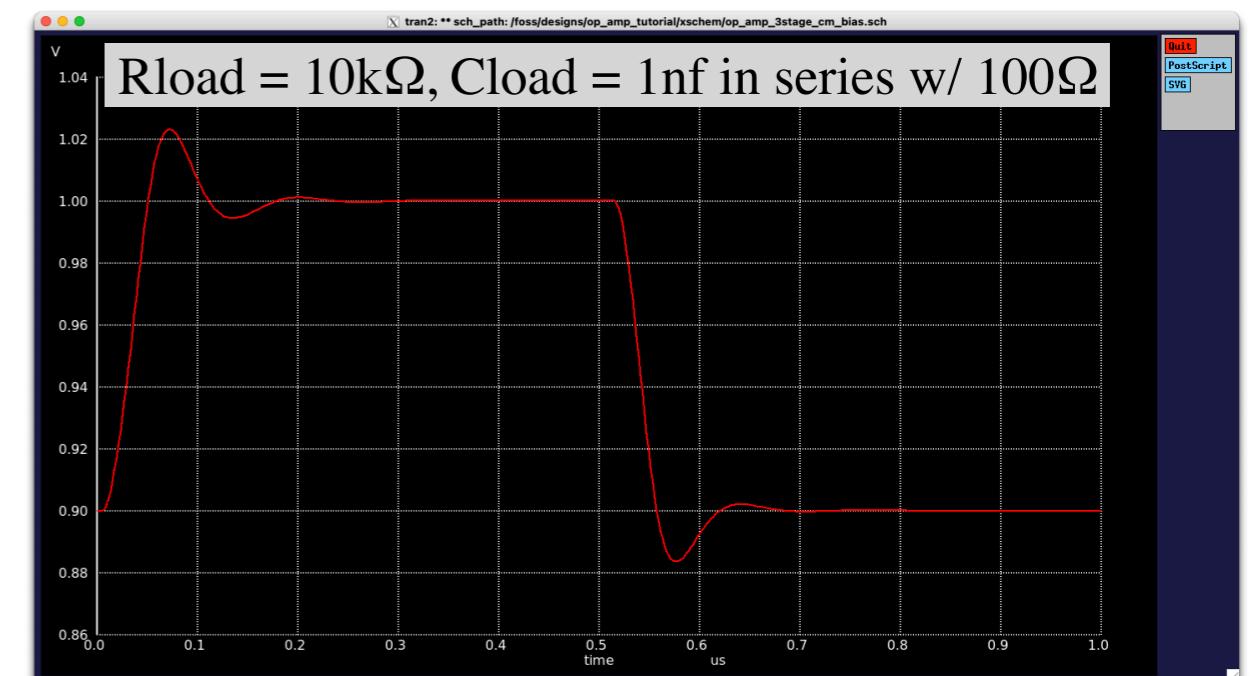
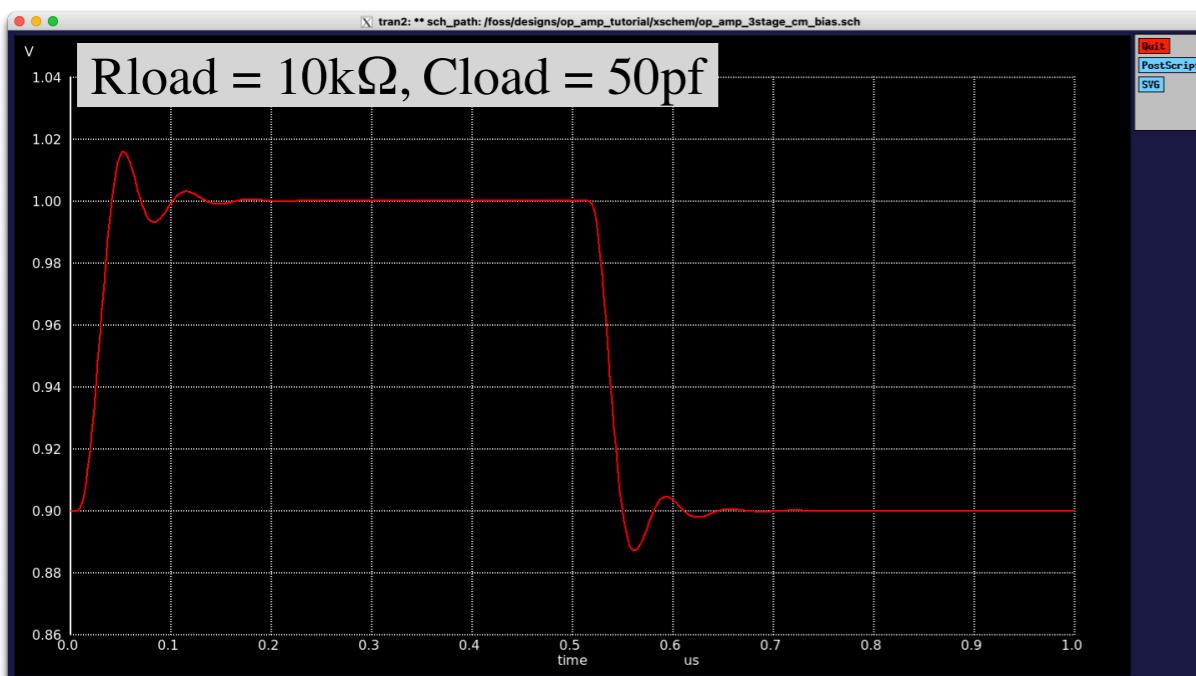
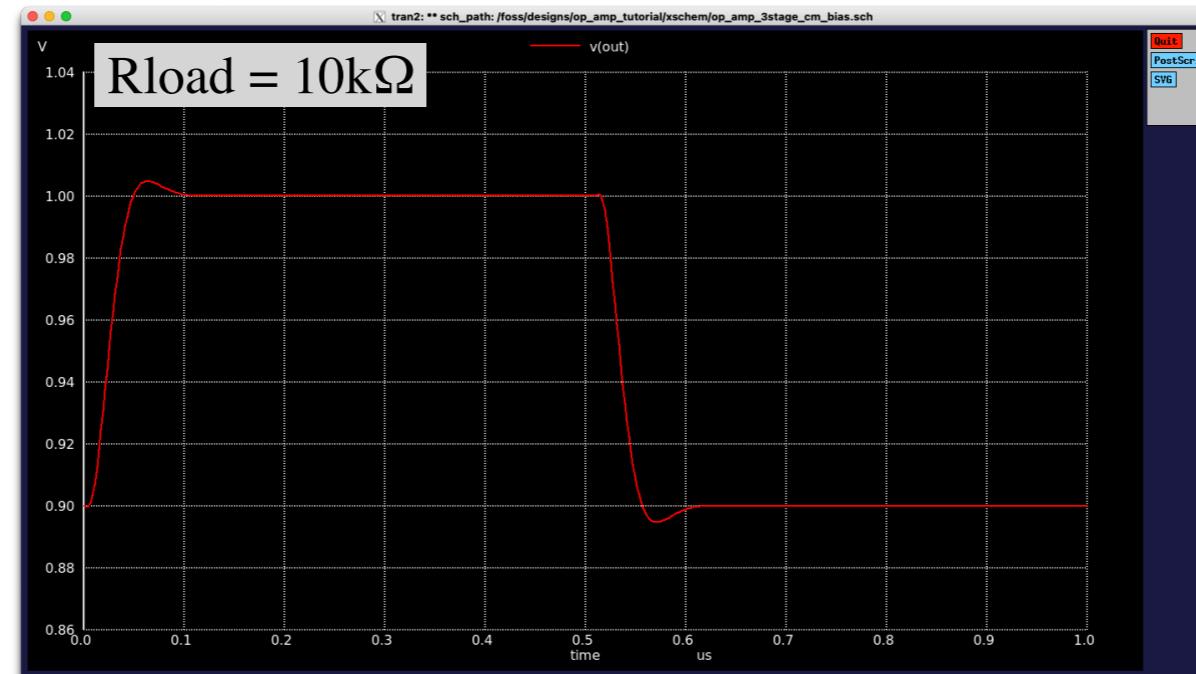


phase margin = 50°

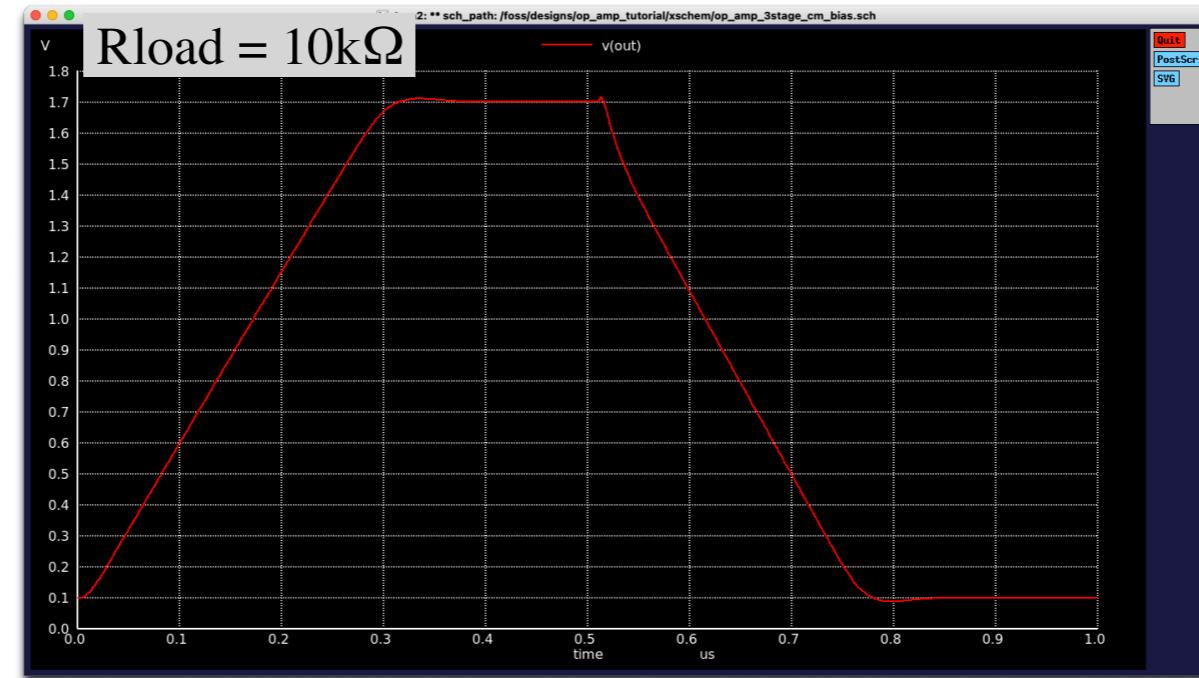


phase margin = 40°

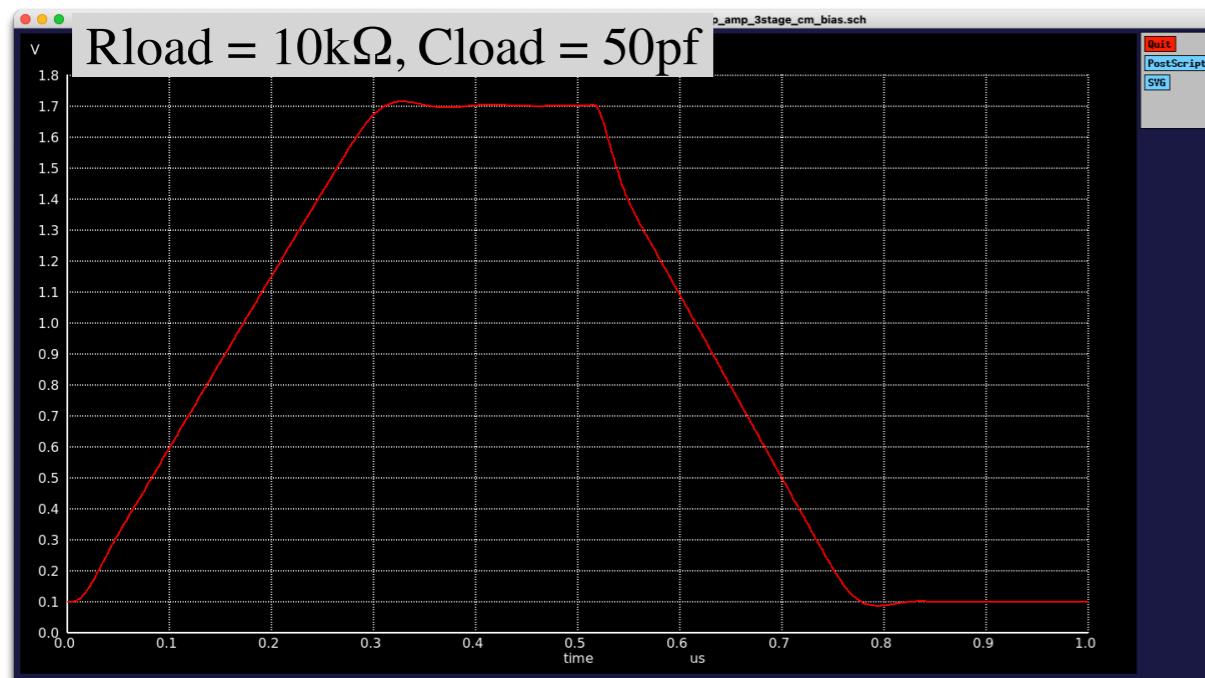
3 stage PMOS OpAmp - final sims -small signal step response



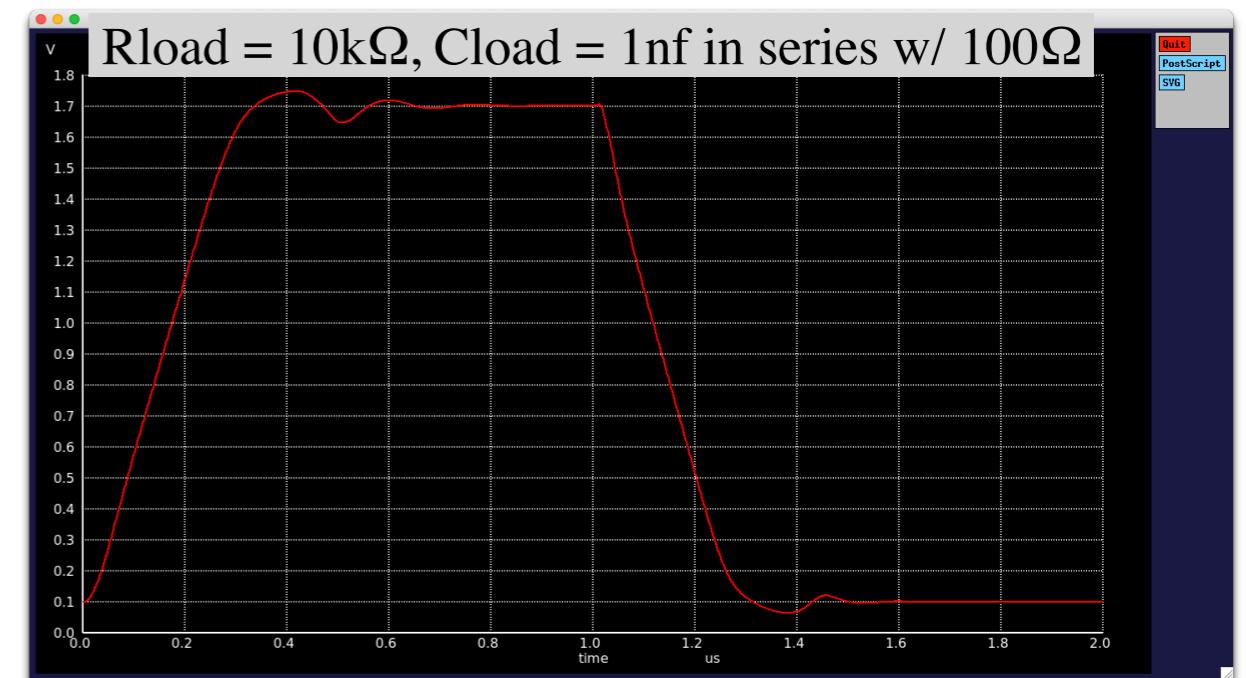
3 stage PMOS OpAmp - final sims - large signal step response



slew rate > 5V/us



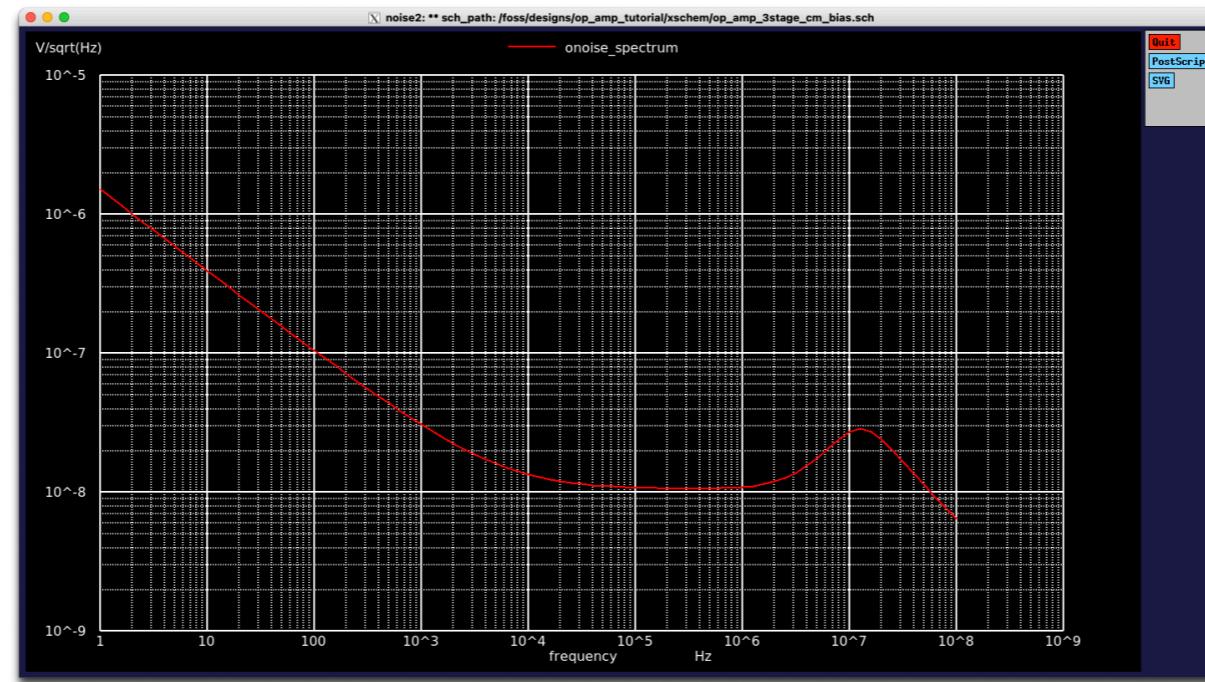
slew rate > 5V/us



slew rate > 5V/us

note: I_{out} slew current to charge C_{load} is $\gg +/ - 1\text{mA}$ limits

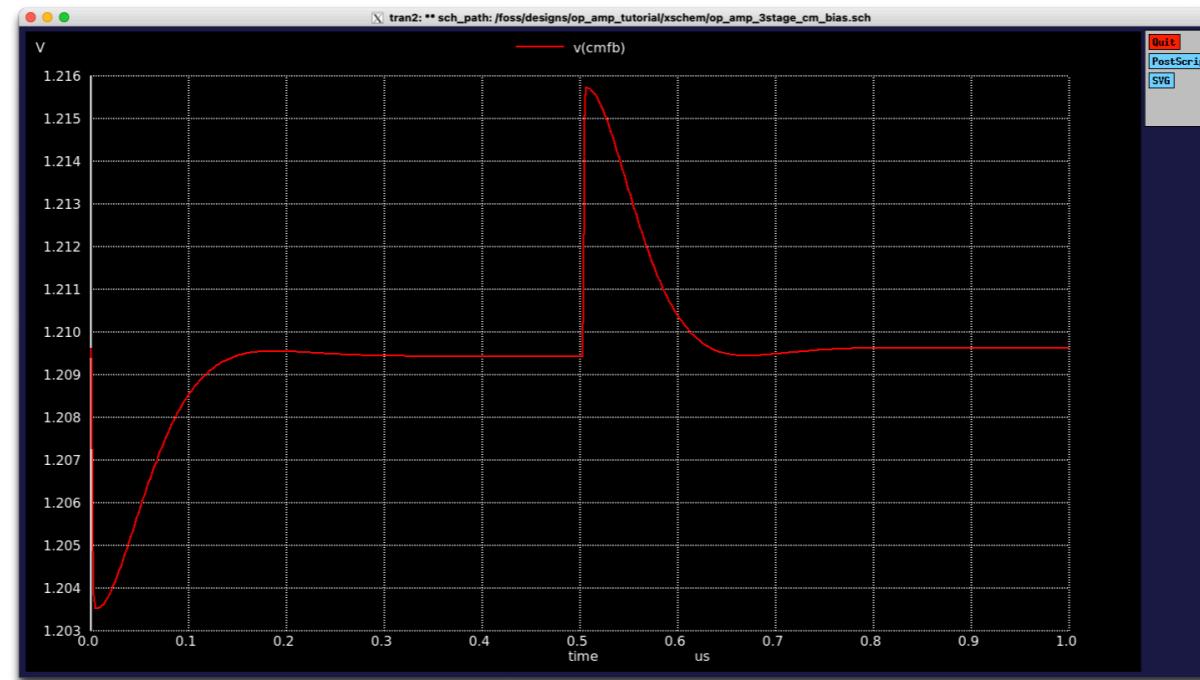
3 stage PMOS OpAmp - final sims - noise



output noise in follower configuration, $en = 10\text{nV}/\sqrt{\text{Hz}} @ 1\text{MHz}, 2\mu\text{V}/\sqrt{\text{Hz}} @ 1\text{Hz}$

3 stage PMOS OpAmp - final sims

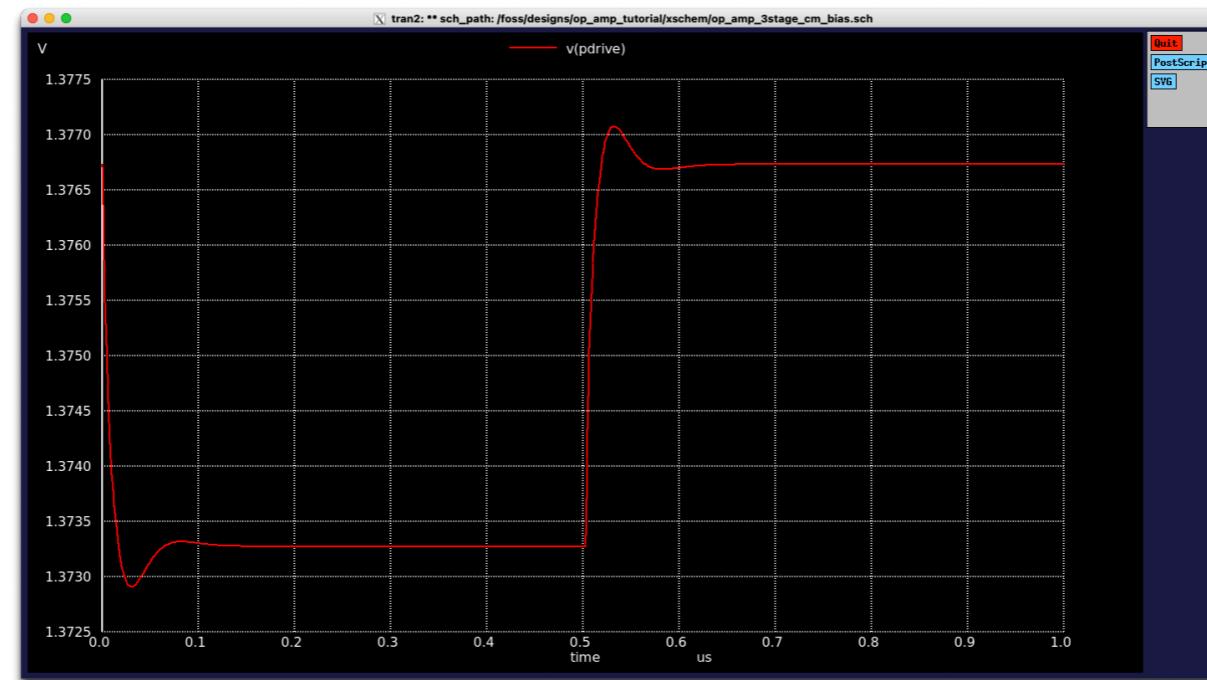
internal cmfb loop stability



response to current pulse checking the stability of the internal cmfb loop looks good

3 stage PMOS OpAmp - final sims

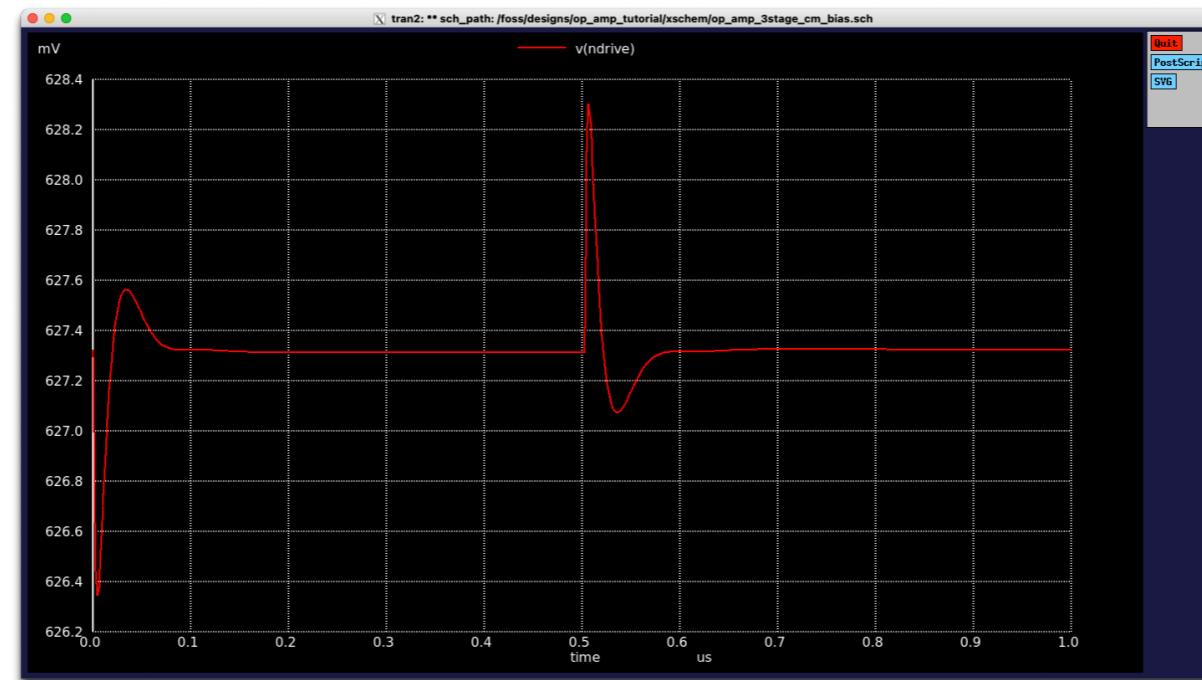
internal pdrive loop stability



response to current pulse checking the stability of the internal pdrive loop looks good

3 stage PMOS OpAmp - final sims

internal ndrive loop stability



response to current pulse checking the stability of the internal ndrive loop looks good

design goal results

- $V_{supply} = 1.8V$ nominal, 1.7V to 1.9V ✓
- V_{out} range = 0.1V to ($V_{supply} - 0.1$) ✓
- $I_{out} > 1mA$ ✓
- $C_{load} = 50pf$ or $1nf$ with series $R = 100\Omega$ ✓
- $GBW = 10MHz$ ✓
- Slew Rate = 5V/us ✓
- V_{in} range = 0.1 to ($V_{supply} - 0.6V$) ✓
- $e_n = 10nV/\sqrt{Hz}$ @ 1MHz, $2uV/\sqrt{Hz}$ @ 1Hz ✓
- Temperature = 27°C nominal, -40°C to 125°C ✓