

3 stage PMOS OpAmp

- design review -

design goals

- $V_{supply} = 1.8V$ nominal, 1.7V to 1.9V
- V_{out} range = 0.1V to ($V_{supply} - 0.1$)
- $I_{out} > 1mA$
- $C_{load} = 50pf$ or $1nf$ with series $R = 100\Omega$
- $GBW = 10MHz$
- Slew Rate = 5V/us
- V_{in} range = 0.1 to ($V_{supply} - 0.6V$)
- $e_n = 10nV/\sqrt{Hz}$ @ 1MHz, $2uV/\sqrt{Hz}$ @ 1Hz
- Temperature = 27°C nominal, -40°C to 125°C

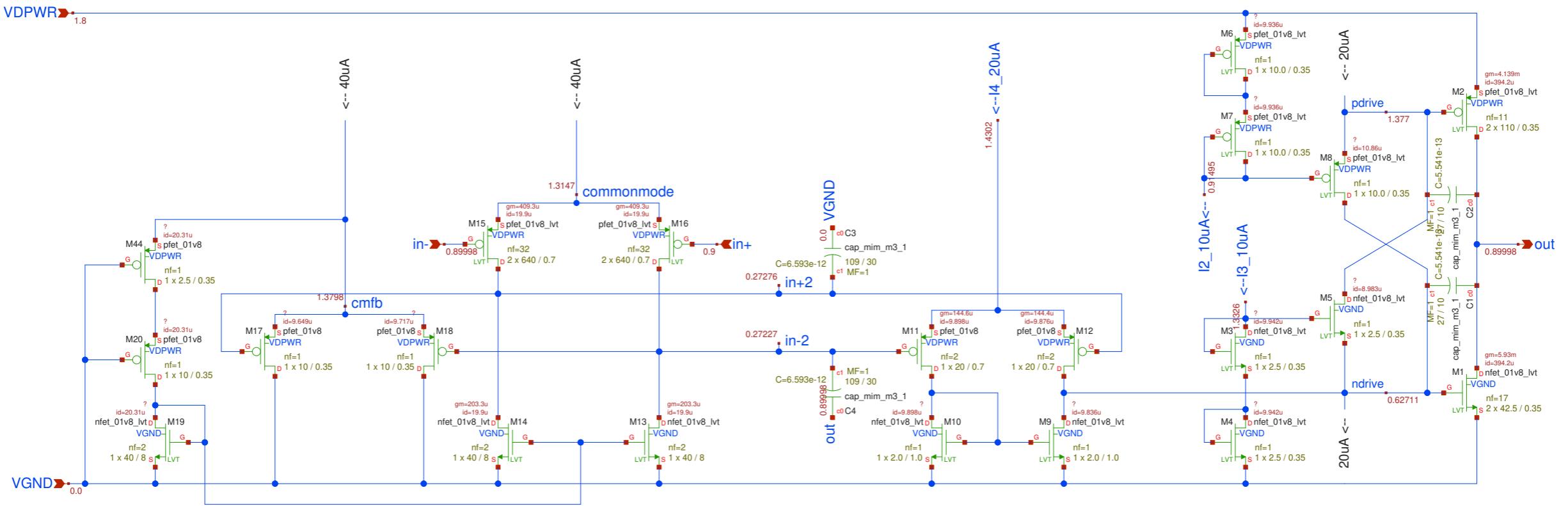
design methodology

Refer to the following documents located in the /docs folder for more detailed coverage of the design methodology used:

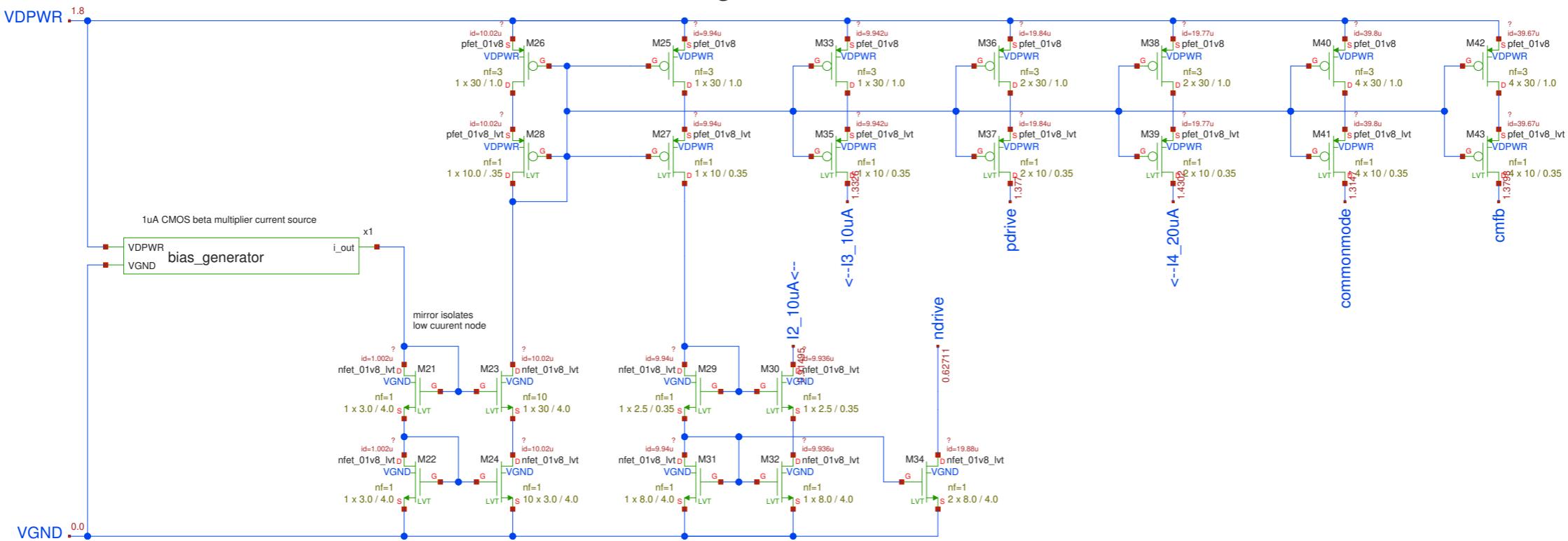
Precision_OpAmp_Design_tutorial.pdf

bias_generator_design_review.pdf

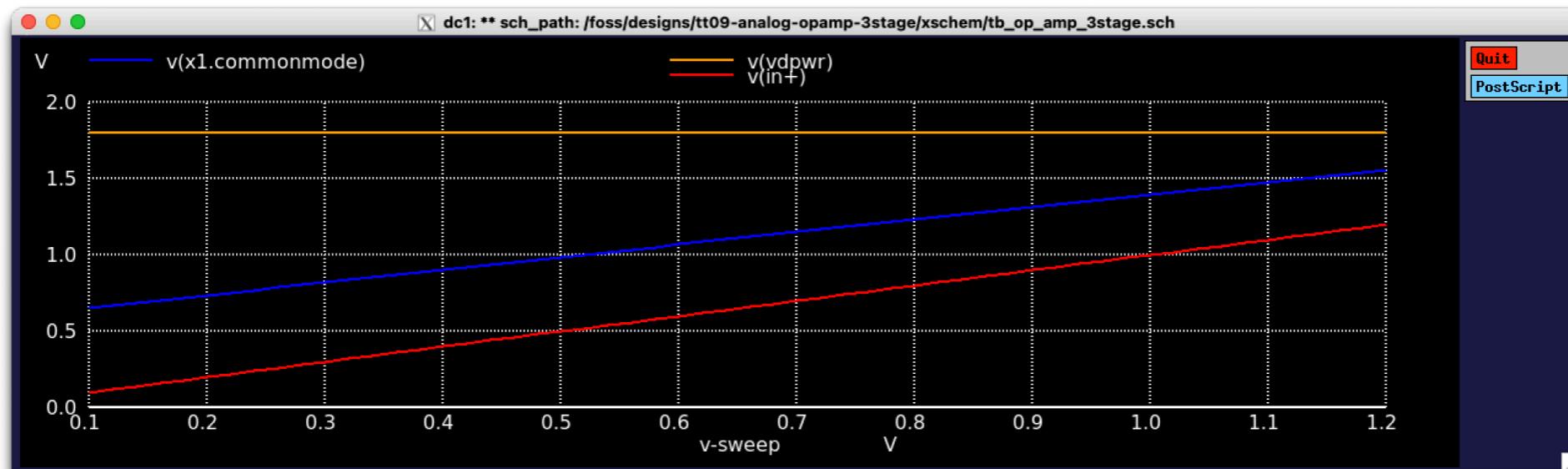
3 stage PMOS OpAMP



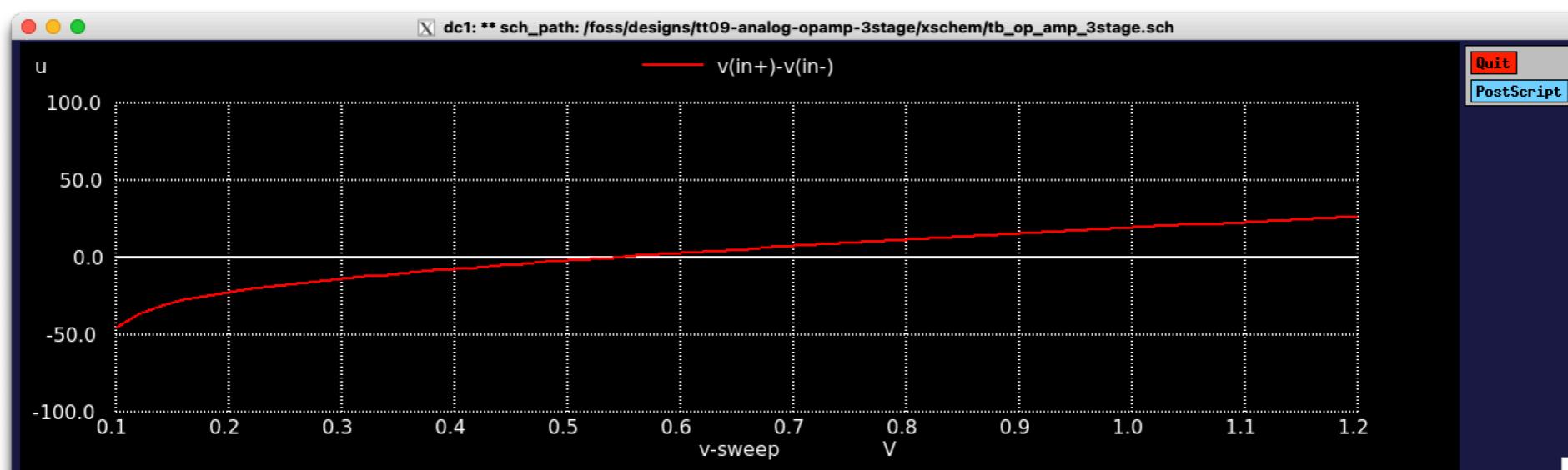
bias generator



3 stage PMOS OpAMP - sims

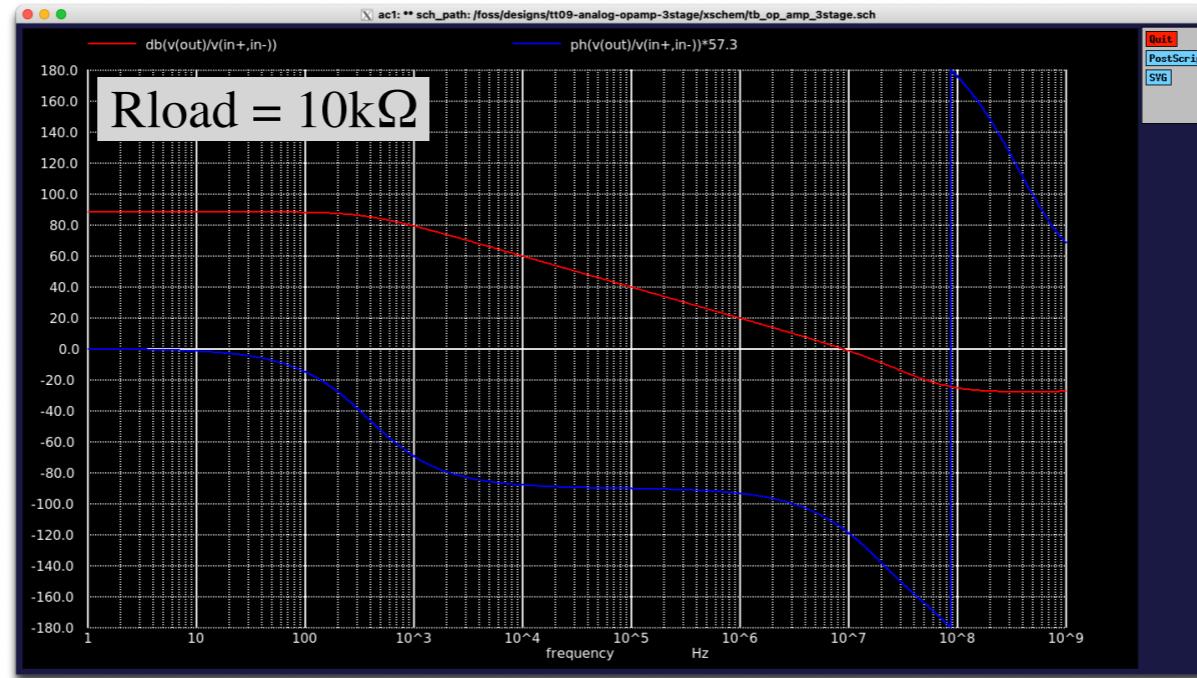


v(in+), v(VDPWR), and v(common mode)

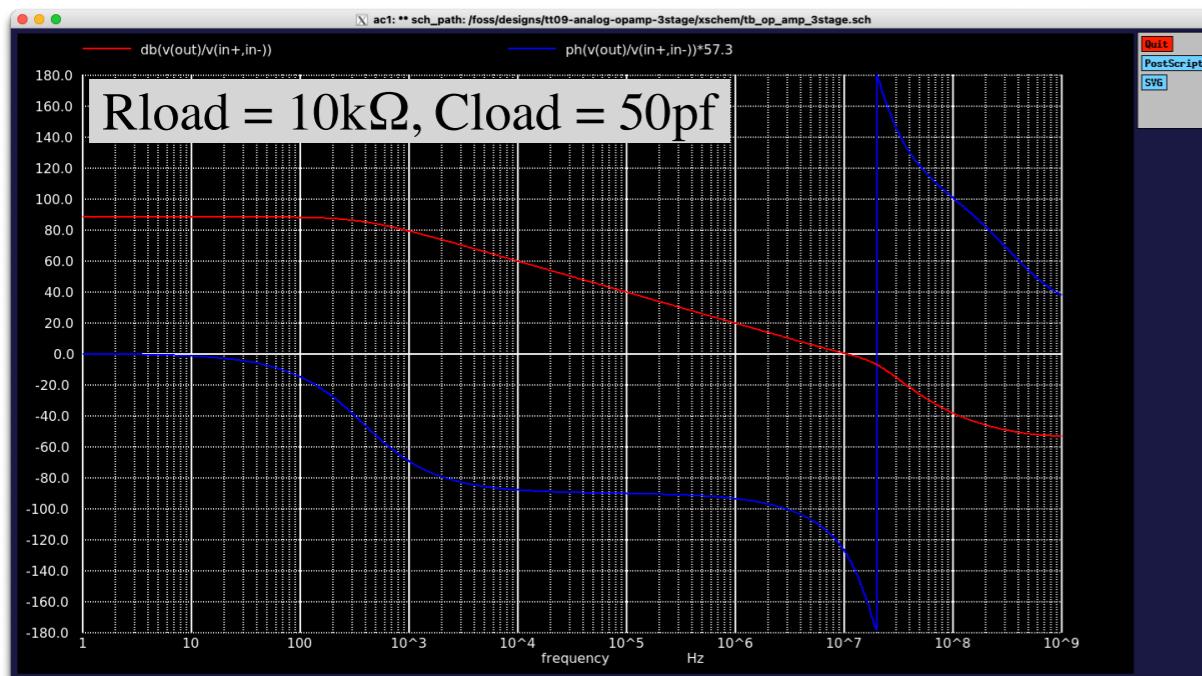


input error voltage vs output swing, Rload = 10kΩ to mid supply

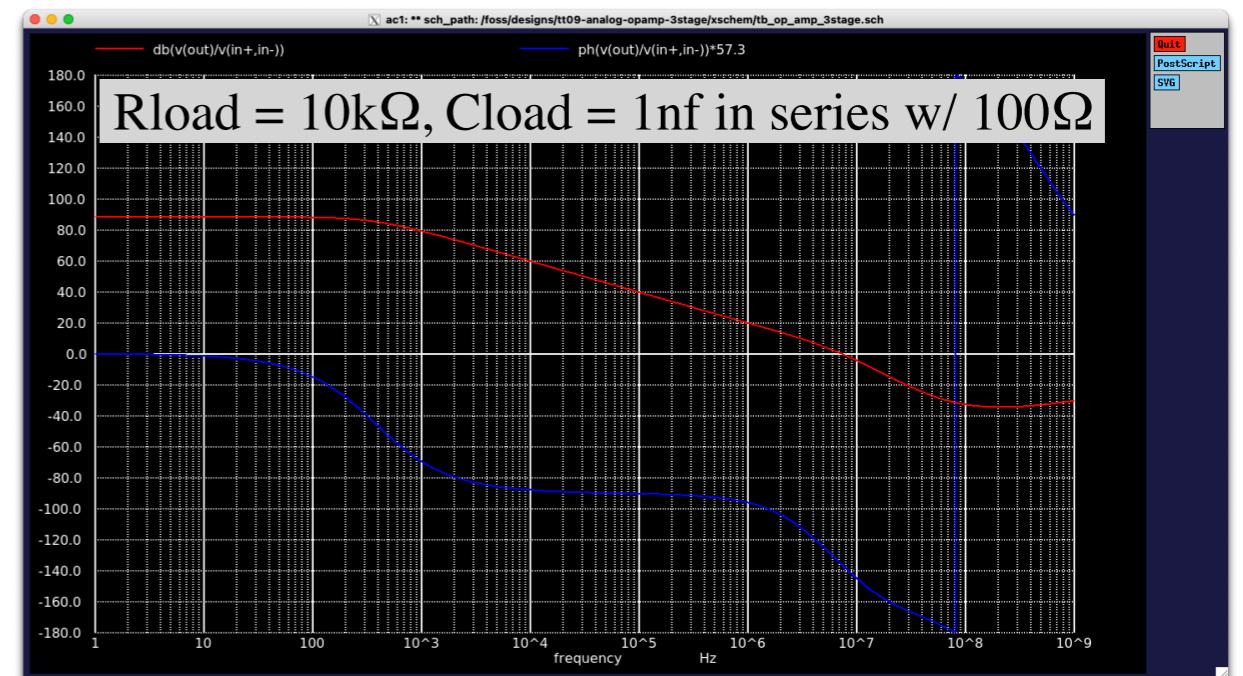
3 stage PMOS OpAMP - sims - ac



open loop gain $\approx 86\text{dB}$, GBW = 10MHz, phase margin = 60°

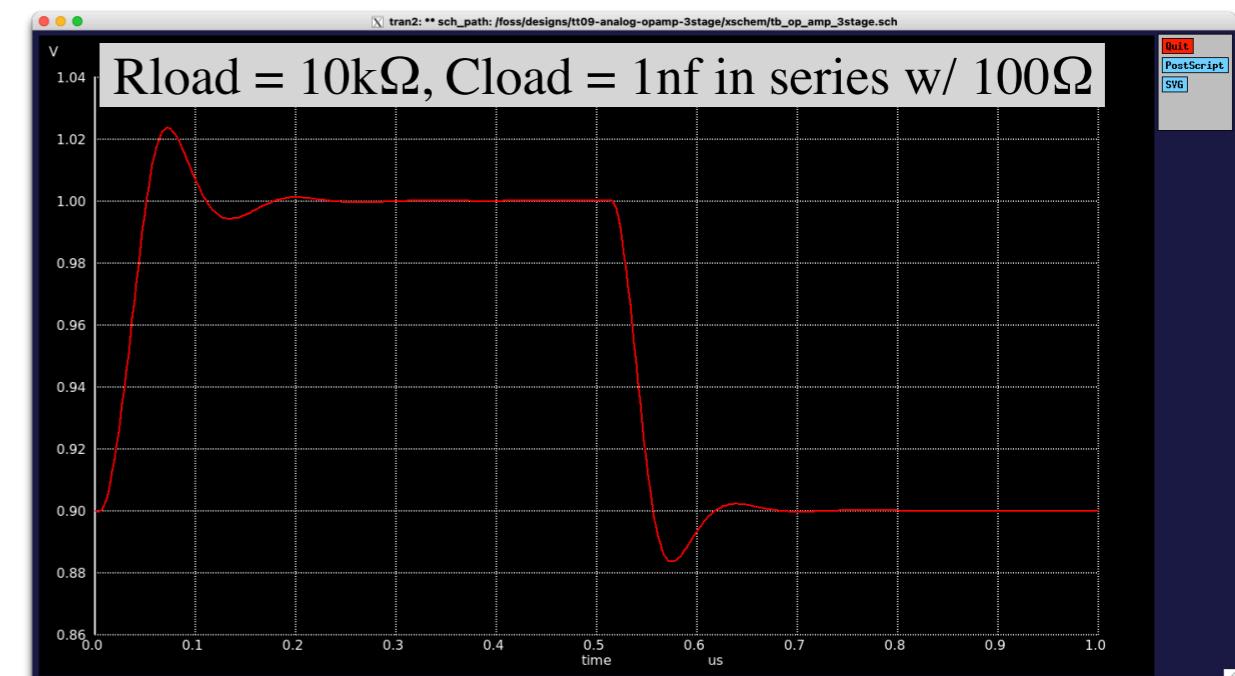
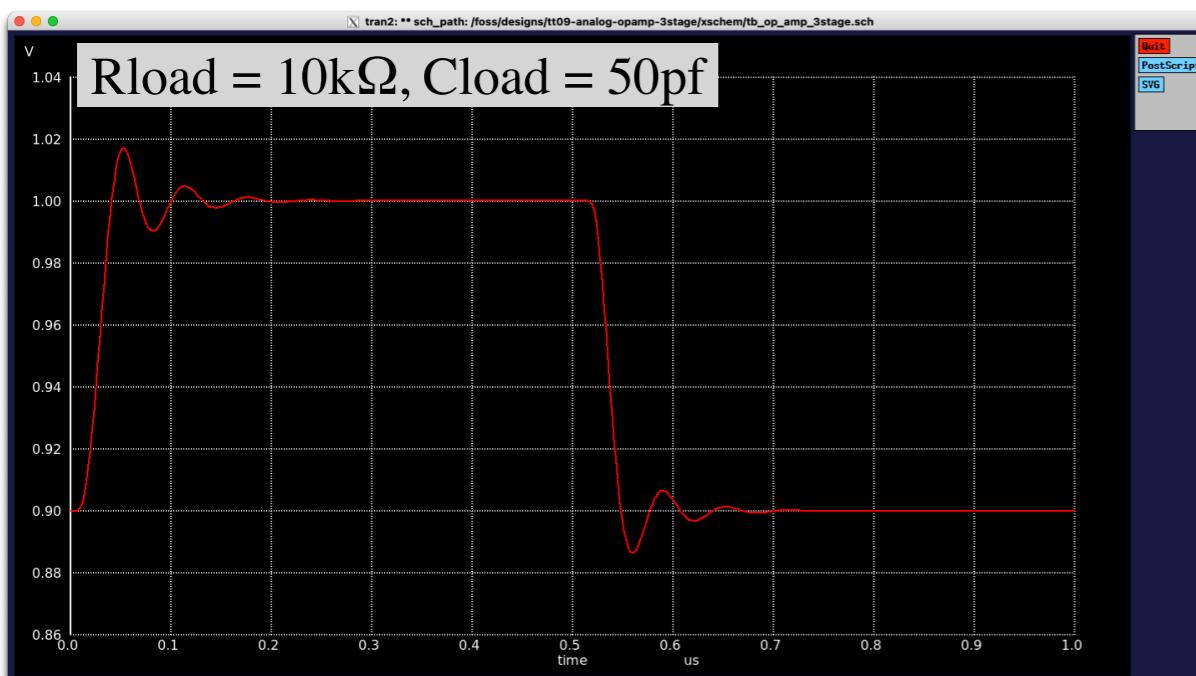
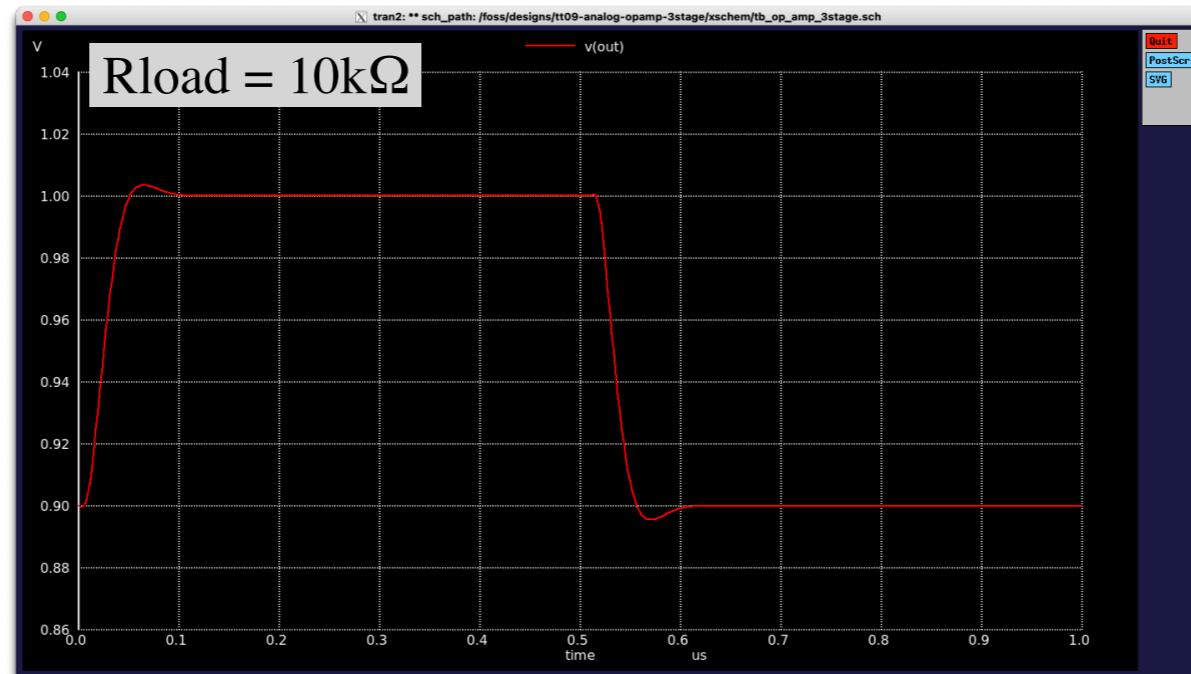


phase margin = 50°

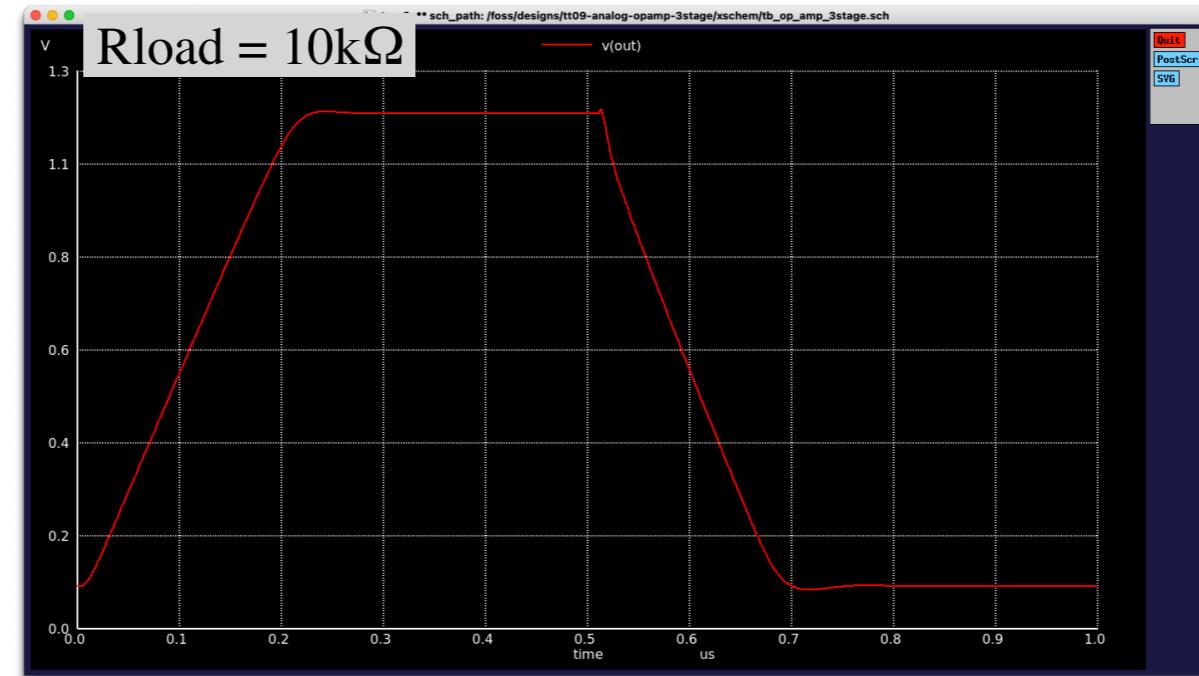


phase margin = 40°

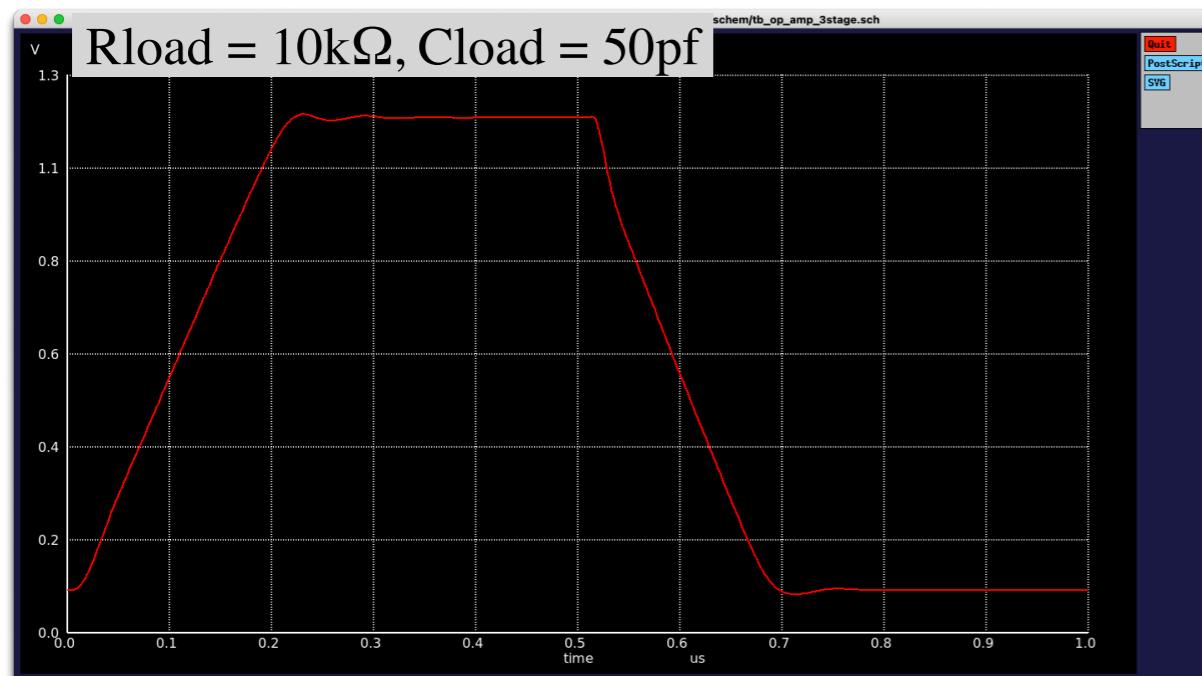
3 stage PMOS OpAmp - sims -small signal step response



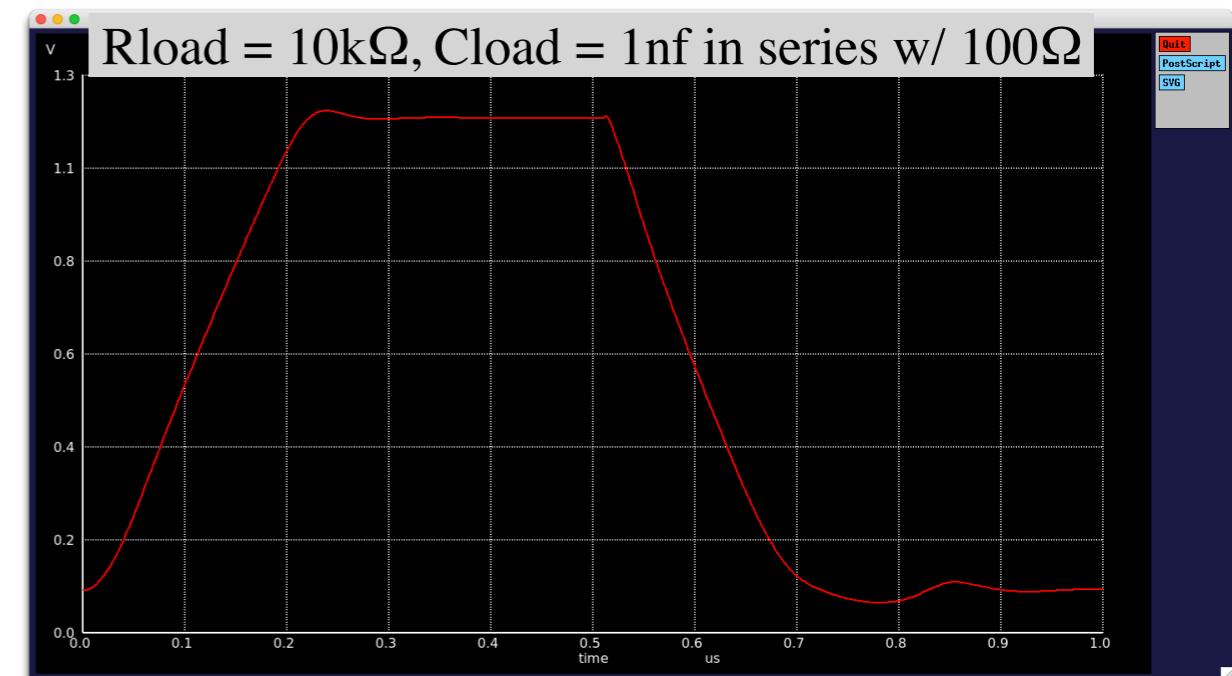
3 stage PMOS OpAmp - sims - large signal step response



slew rate > 5V/us



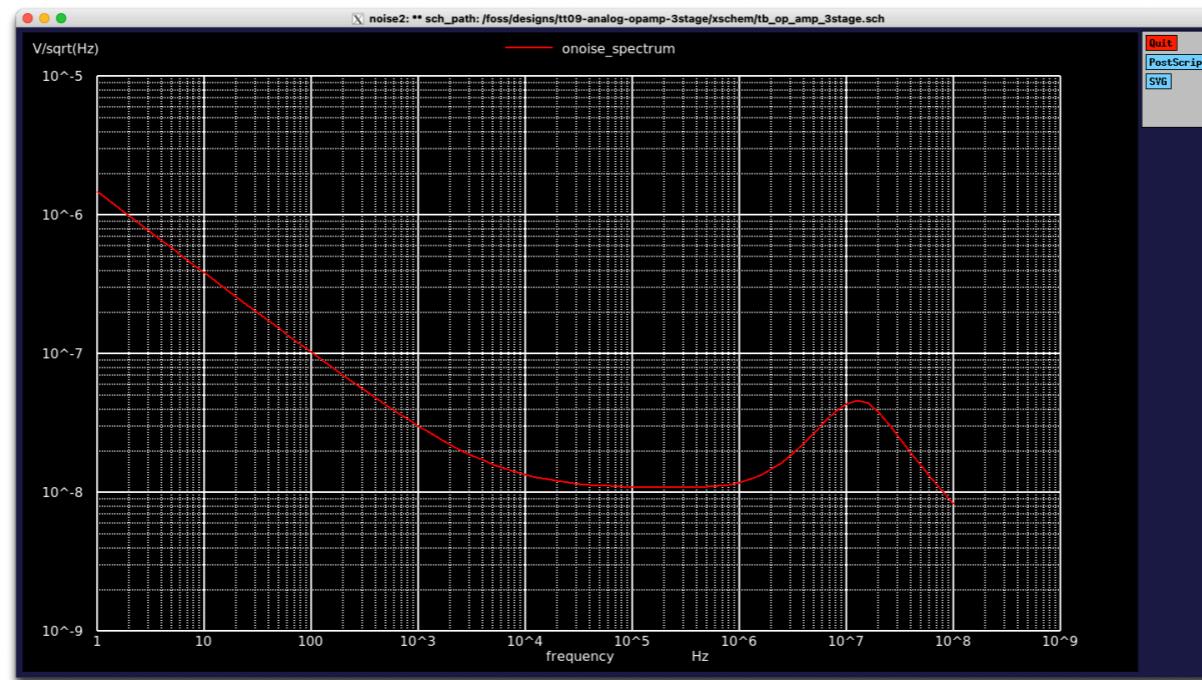
slew rate > 5V/us



slew rate > 5V/us

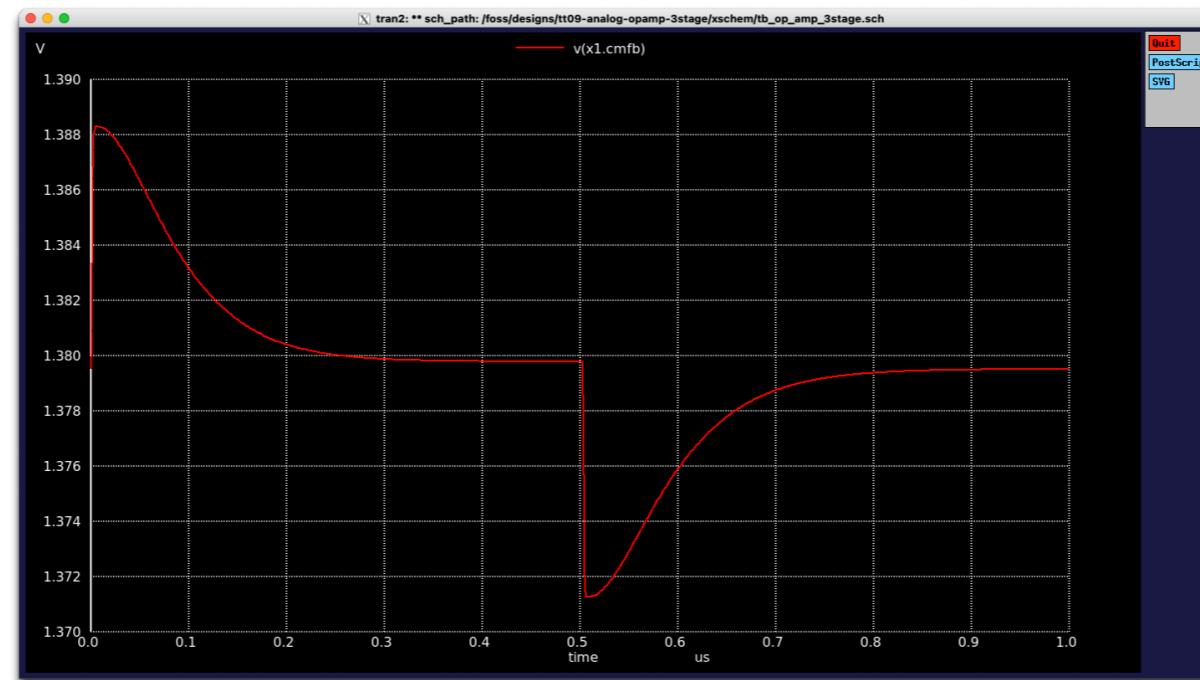
note: Iout slew current to charge Cload is >> +/-1mA limits

3 stage PMOS OpAmp - sims - noise



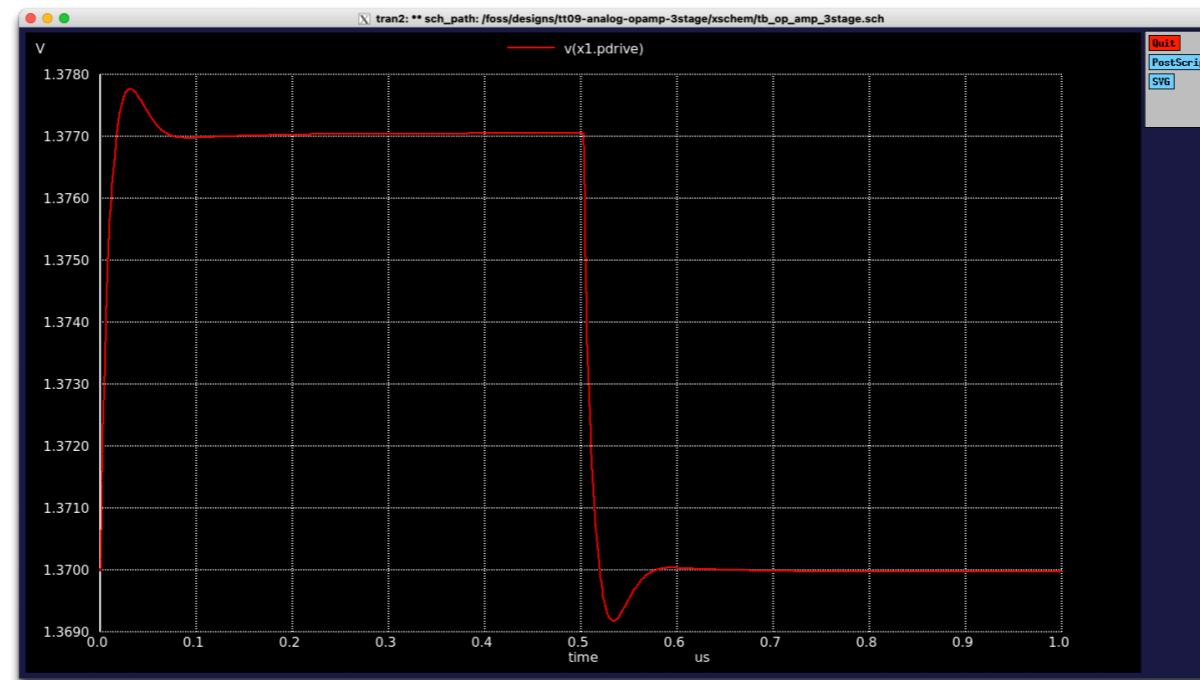
output noise in follower configuration, $en = 10\text{nV}/\sqrt{\text{Hz}}$ @ 1MHz, $2\mu\text{V}/\sqrt{\text{Hz}}$ @ 1Hz

3 stage PMOS OpAmp - sims internal cmfb loop stability



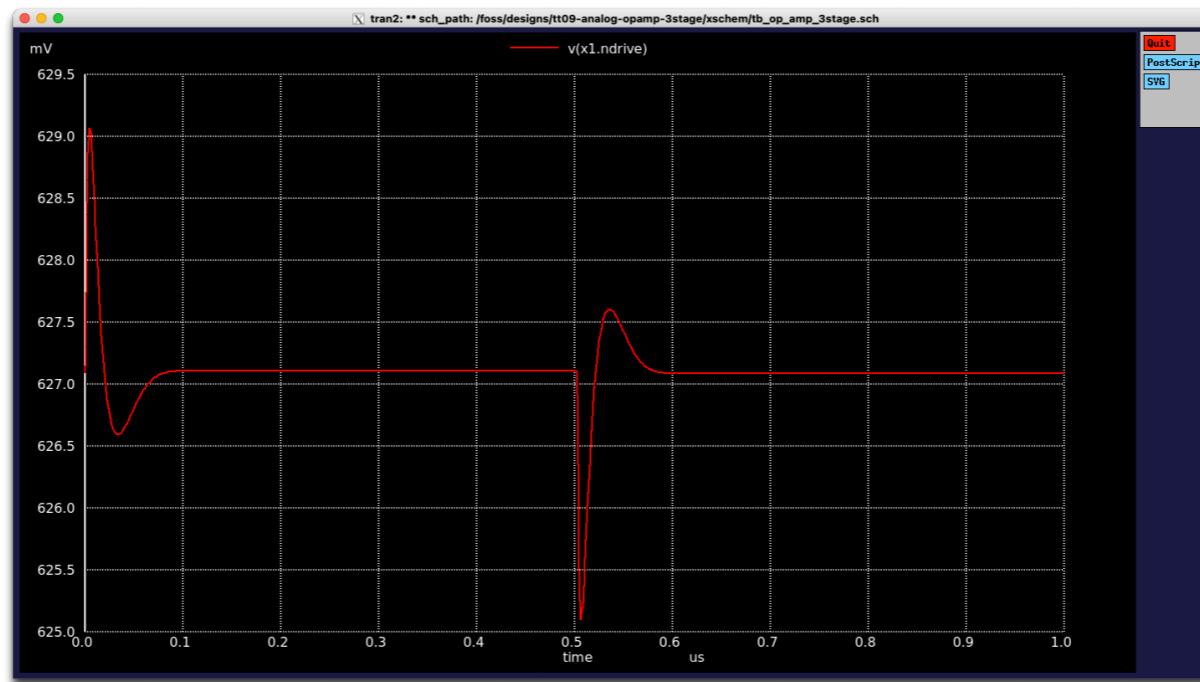
response to current pulse checking the stability of the internal cmfb loop looks good

3 stage PMOS OpAmp - sims internal pdrive loop stability



response to current pulse checking the stability of the internal pdrive loop looks good

3 stage PMOS OpAmp - sims internal ndrive loop stability



response to current pulse checking the stability of the internal ndrive loop looks good

layout considerations

- device matching

Match both W's and L's and create critical ratios with device multipliers.

Insure that everything the gate sees to the edge of it's well is the same.

Current flow from the source to the drain should be in the same direction.

Use a cross quad layout technique for input devices (M15 and M16) and input loads (M14 and M13). This will minimize sensitivities to stress and thermal gradients.

- merging devices

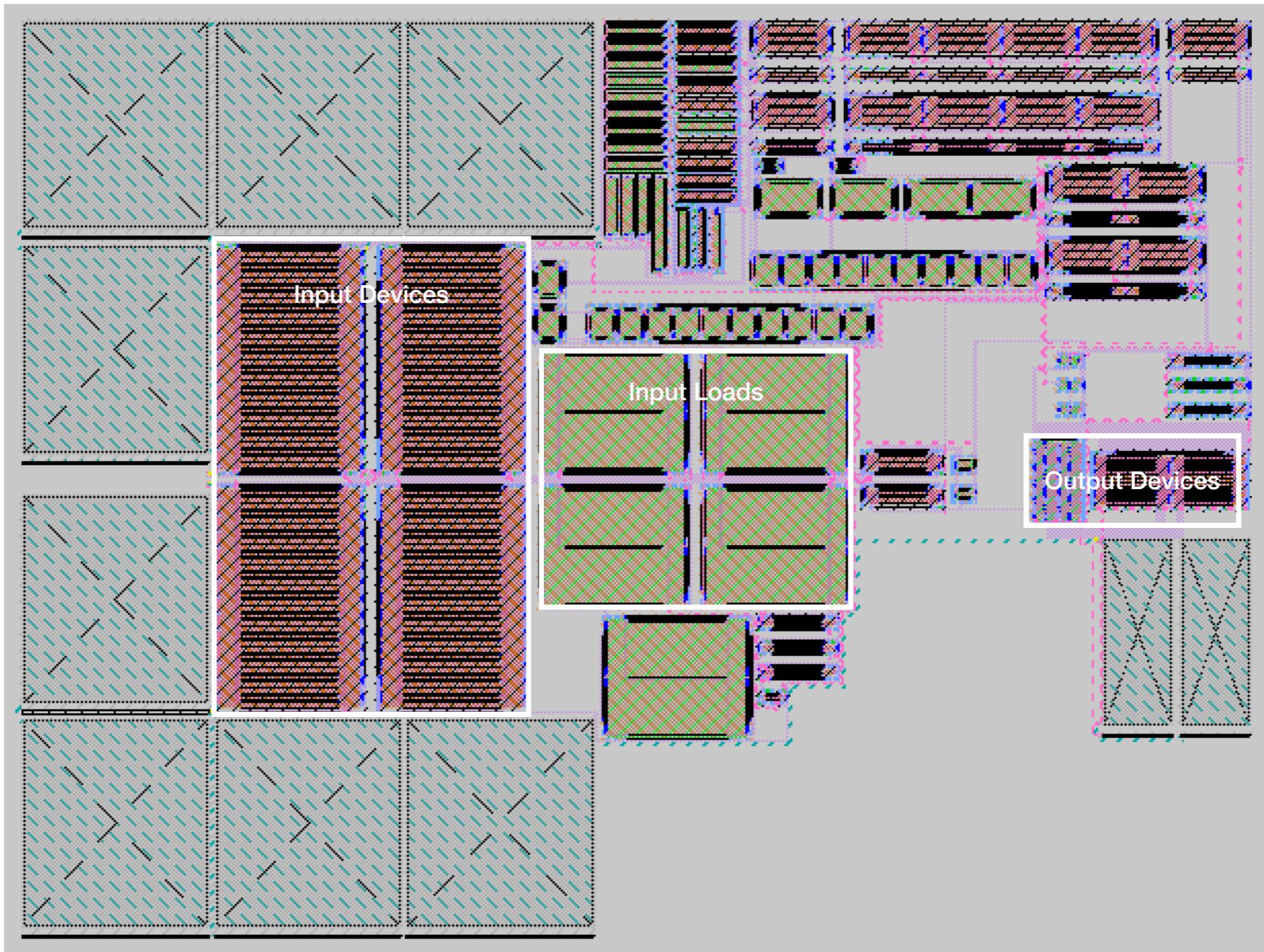
Parametrized layout cells on the sky130A PDK allows merging of wells.

- critical chip floor plan

Output and input devices should be laid out on a thermal center line as far away from each other a practical to minimize thermal feedback.

Inputs should be away from the edge of the chip to minimize stress effects from the edge of the chip or effects from surrounding cells. Laying out the large compensation capacitors (C3 and C4) between the edge of the chip and the inputs is a good way to do this.

layout



layout area $\approx 179\text{um} \times 134\text{um}$

design goal results

- PVT variations
 - Process corners ss, sf, ff, and fs ✓
 - supply Voltage from 1.7V to 1.9V ✓
 - Temperature from -40°C to 125°C ✓

note : Vin range at 125°C is reduced to 0.2 to (Vsupply - 0.6V) due to process corners ff and fs. Vin range at 85°C is not changed.

- Vout range = 0.1V to (Vsupply - 0.1) ✓
- Iout > 1mA ✓
- Cload = 50pf or 1nf with series R = 100Ω ✓
- GBW = 10MHz ✓
- Slew Rate = 5V/us ✓
- Vin range = 0.1 to (Vsupply - 0.6V) ✓
- en = 10nV/√Hz @ 1MHz, 2uV/√Hz @ 1Hz ✓
- device mismatch still needs to be simulated with monti-carlo